

1 General description

The FS23 is a family of automotive Safety SBC devices with multiple power supplies, designed to support general purpose body applications requiring low power modes and CANFD and LIN communication.

This family of devices supports a wide range of applications, offering choice in output voltage settings, physical interfaces and integrated system level features to address low power and noise sensitive applications with Automotive Safety Integrity Levels up to FS2320-ASILB.

The FS23 integrates an EMC optimized switch mode regulator (HVBUCK), which can be replaced by an LDO voltage regulator (HVLDO1), to supply a microcontroller and two other LDO voltage regulators (HVLDO2, HVLDO3) to supply communication devices and others. The HVBUCK is an high performance switching regulator capable to switch from pulse frequency modulation (PFM) mode to pulse width modulation (PWM) mode via I2C or SPI command to optimize noise management. The LDOs are connected to VSUP.

The FS23 is developed in compliance with the ISO26262:2018 standard, and it includes enhanced safety features, with fail-safe outputs, becoming part of a full safety-oriented system, covering FS2320-ASILB safety integrity level.

2 Features and benefits

- One high voltage buck with low power mode support
- Two linear regulators with low power mode support
- CAN FD and LIN transceivers
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Selectable wake-up sources to bring the system back from low power modes
- Two wake-up inputs and four configurable GPIO pins
- Four high side drivers, with PWM and cyclic sense capabilities
- SPI communication interface
- Safety mechanisms to reach ASIL B level
- Internal voltage monitoring, Watchdog, FCCU monitoring
- Analog built-in self-test on demand
- Three safety outputs (RSTB, FSOB, LIMP0)



3 Applications

- Body control module
- HVAC
- Lighting
- Steering column lock
- Seat module
- Roof module
- Door control module
- Car access

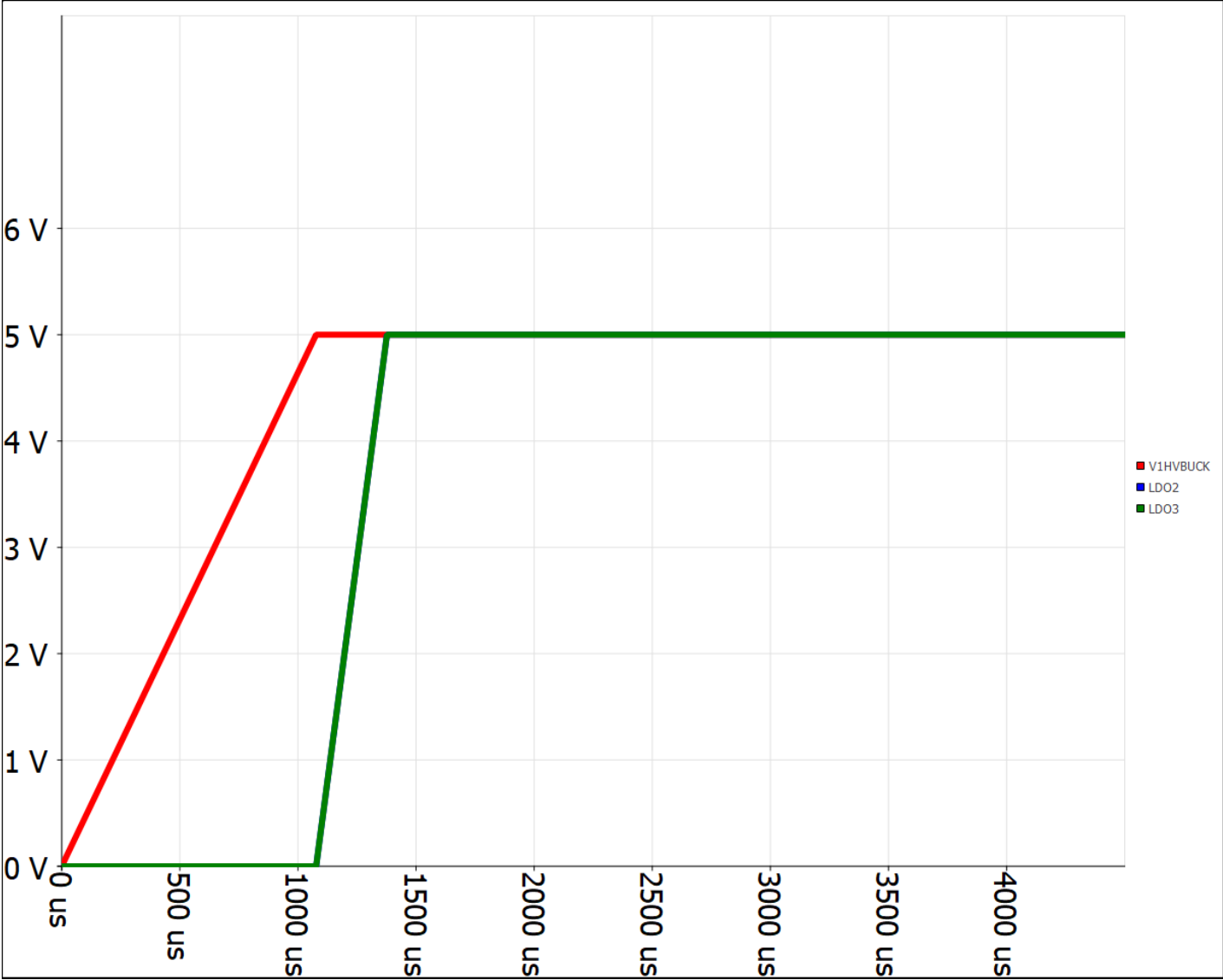
4 Ordering information

Table 1. Ordering information

Type number ^[1]	Package		
	Name	Description	Version
MFS2320BMBB1EP	H-PQFN-48	QFN48-EP plastic thermally enhanced,wettable flanks. 48 terminals; 0.5 mm pitch; 7 mm x 7 mm x 0.85 mm body	SOT619-27

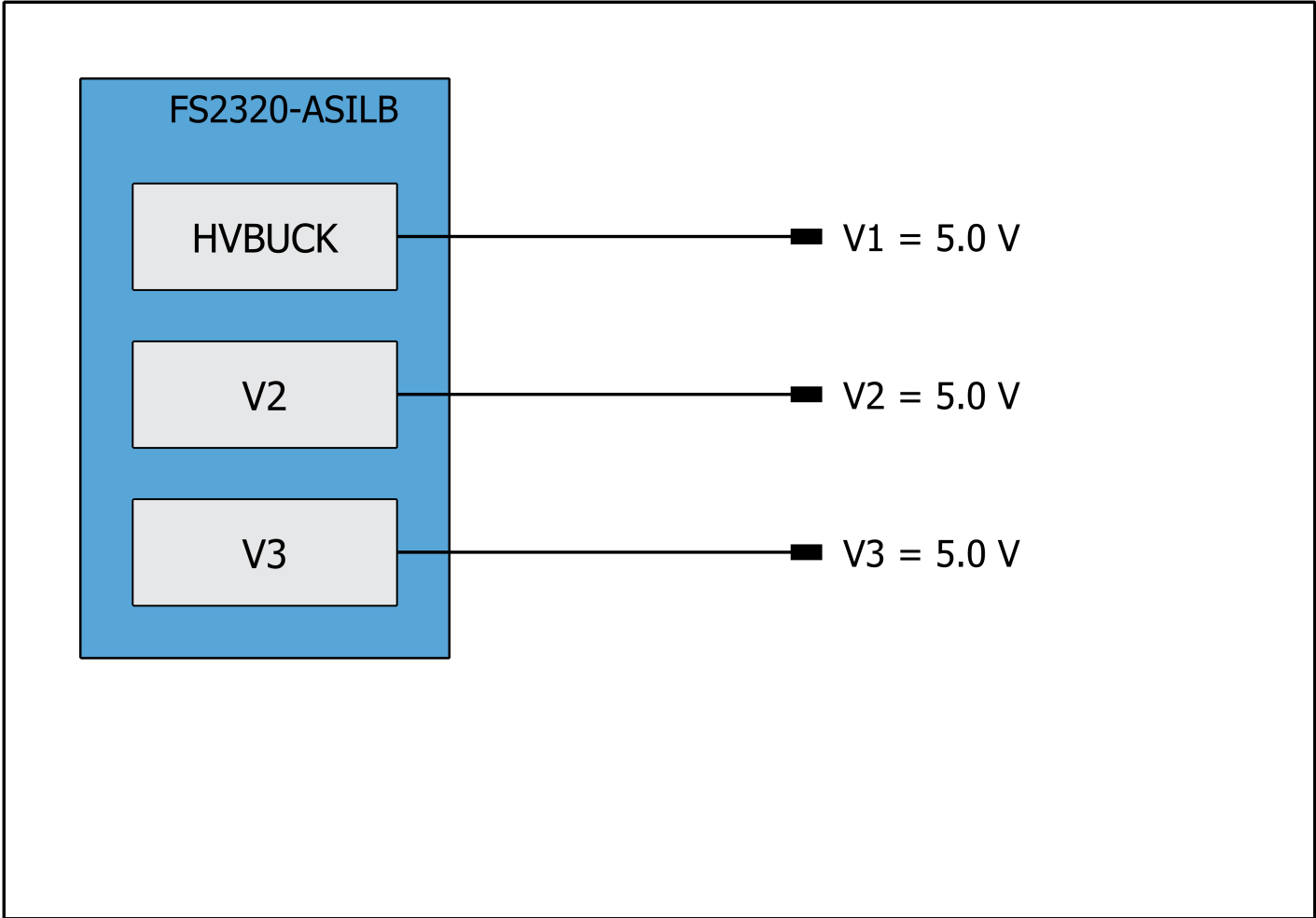
[1] To order parts in tape and reel, add the R2 suffix to the part number.

5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

6 Hardware configuration diagram



Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

7 OTP configuration

See FS2300 datasheet for parametric details. The OTP configuration summary for BB1 sequence ID is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System configuration	Enable HS24	HSD2 and HSD4 are enabled
	Enable HS13	HSD1 and HSD3 are enabled
	Enable LDT	LDT is disabled
	Enable LIN	LIN is disabled
	Enable CAN	CAN is enabled
	Enable Key OFF-ON	Key OFF - Key ON function is disabled
	Bypass Slots	Disabled
	SPI Enable	SPI pins are enabled
	I2C Address	Not Used
Clock configuration	Enable Clock Modulation	Modulation is enabled
	Clock Modulation Configuration	Pseudo random modulation is selected
WAKEs configuration	WAKE1 Pull Down	WAKE1 internal pull down is enabled and pull up is disabled
	WAKE2 Pull Down	WAKE2 internal pull down is disabled and pull up is enabled
LVIOs configuration	Power Sequence Slot For LVIO3	LVIO3 polarity is changed in slot 0
	Enable HS Of LVIO3	LVIO3 HS is disabled
	Enable LS Of LVIO3	LVIO3 LS is disabled
	Pull Down On LVIO3	LVIO3 internal pull down is enabled and pull up is disabled

Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

	Config LVIO3 Pin Default State	LVIO3 default state is low (LS ON or LS OFF with ext PD)
	Power Sequence Slot For LVIO4	LVIO4 polarity is changed in slot 0
	Enable HS Of LVIO4	LVIO4 HS is disabled
	Enable LS Of LVIO4	LVIO4 LS is disabled
	Pull Down On LVIO4	LVIO4 internal pull down is enabled and pull up is disabled
	Config LVIO4 Pin Default State	LVIO4 default state is low (LS ON or LS OFF with ext PD)
	Pull Down On LVI5	LVI5 internal pull down is disabled and pull up is enabled
HVIOs configuration	Power Sequence Slot For HVIO1	HVIO1 polarity is changed in slot 0
	Pull Down On HVIO1	HVIO1 internal pull down is disabled and pull up is enabled
	Configure HVIO1	HVIO1 default state is low (asserted)
	HVIO1 Enable	HVIO1 is configured as an input
	Power Sequence Slot For HVIO2	HVIO2 polarity is changed in slot 0
	Pull Down On HVIO2	HVIO2 internal pull down is disabled and pull up is enabled
	Configure HVIO2	HVIO2 default state is low (asserted)
	HVIO2 Enable	HVIO2 is configured as an input
IO function selection	HVIO1 Function Selection	HVO1 is connected to alternate function
	HVIO2 Function Selection	HVO2 is connected to alternate function

Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

	LVO3 Function Selection	LVO3 is connected to alternate function
	LVO4 Function Selection	LVO4 is connected to alternate function
	HS1 Function Selection	HS1 is connected to HS1 driver
	HS3 Function Selection	HS3 is connected to HS3 driver

Table 3. Regulators

Functional block	Feature	OTP selection
V1 HVBUCK configuration	V1 HVBUCK Power-up Slot	Slot 0
	V1HVBUCK Soft Start Ramp	Soft start is 1077 us
	V1HVBUCK Behaviour In Case Of TSD	The device transition to FailSafe state (M30) in case of TSD
	V1 BUCK Regulator Voltage In Normal Mode	5.0 V
	V1 BUCK Regulator Voltage In LPON Mode	5.0 V
	BUCK Switching Frequency	Switching frequency is 2.25 MHz
	BUCK Compensation Resistor	975 kOhm
	BUCK Compensation Capacitor	33.5 pF
	BUCK Slope Compensation	3362 mV/μs
	BUCK HS Slew Rate When ON	HS rising slew rate is 5 ns
	BUCK HS Slew Rate When OFF	HS falling slew rate is 5 ns
	BUCK Average Over Current Detection Threshold In PWM Mode	Average overcurrent threshold is 600 mA
	BUCK Over Current Threshold In PWM Mode	Overcurrent (peak) threshold is 800 mA
	BUCK Over Current Threshold In PFM Mode	Overcurrent (peak) threshold is 600 mA

Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

	BUCK TON Time In PFM	TON time in PFM is 386 ns
	BUCK TOFF Time In PFM	TOFF time in PFM is 250 ns
	BUCK DVS Ramp Rate	5.625 mV/us
	Vbos Switch Always Enabled	Always enabled
	VBOS To V1 Switch In LPON Mode	VBOS to V1 switch is closed in LPON mode
	Enable OL Monitoring Protection	OL protection is disabled
V2 configuration	LDO2 Power-up Slot	Slot 1
	Enable Request Of LDO2	Enabled
	LDO2 Behaviour In Case Of TSD	The V2 is disabled in case of TSD
	V2 LDO Overcurrent Threshold	V2 LDO OC = 150 mA
	V2 LDO Regulator Voltage	V2 = 5.0 V
V3 configuration	LDO3 Power-up Slot	Slot 1
	LDO3 Behaviour In Case Of TSD	The device transition to FailSafe state (M30) in case of TSD
	V3 LDO Overcurrent Threshold	V3 LDO OC = 150 mA
	V3 LDO Regulator Voltage	V3 = 5.0 V

Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

Table 4. Functional Safety

Functional block	Feature	OTP selection
System configuration	LIMP0 Enable	LIMP0 is disabled
	FS0B Enable	FS0B is enabled
	FCCU Enable	FCCU monitoring is enabled
	ABIST Enable	ABIST checks are enabled
	Configure First Fault	Do Not GoTo FS at first fault
	Disable The RSTB 8s Timer	RSTB 8s timer is enabled
	RSTB Pulse Duration	10 ms
	Lock The Watchdog	Watchdog Functional
	Configure FS State Duration	FS state duration is 100 ms
	Configure FS State Exit	GoTo LPOFF after FS state
	V1 Overvoltage Detection	The device transition to FailSafe state (M30) in case of OV
	V2 Overvoltage Detection	The V2 is disabled in case of OV
	V3 Overvoltage Detection	The V3 is disabled in case of OV
LIMP configuration	LIMP1 Polarity	PWM frequency = 1.25 Hz with 50 % duty cycle (Default high)
	LIMP2 Polarity	PWM frequency = 100 Hz (Default high)
V0MON_RES configuration	V0MON Enable	Disabled
	V0MON Voltage Configuration	1.0 V
	V0MON Undervoltage Threshold	91.5 %

Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

	V0MON Overvoltage Threshold	110 %
	V0MON Undervoltage Deglitcher Time	40 us
	V0MON Overvoltage Deglitcher Time	45 us
	Configure V0 UV Impact On RSTB	VMON_EXT UV does not assert RSTB
	Configure V0 OV Impact On RSTB	VMON_EXT OV does not assert RSTB
V1MON_DAC configuration	V1MON Enable	Enabled
	V1MON Voltage Configuration	V1MON = 5.0 V
	V1MON Undervoltage Threshold	61 %
	V1MON Overvoltage Threshold	110 %
	V1MON Undervoltage Deglitcher Time	25 us
	V1MON Overvoltage Deglitcher Time	25 us
	Configure V1 UV Impact On RSTB	V1 UV asserts RSTB
	Configure V1 OV Impact On RSTB	V1 OV asserts RSTB
V2MON_DAC configuration	V2MON Enable	Enabled
	V2MON Voltage Configuration	V2MON = 5.0 V
	V2MON Undervoltage Threshold	91.5 %
	V2MON Overvoltage Threshold	110 %
	V2MON Undervoltage Deglitcher Time	25 us
	V2MON Overvoltage Deglitcher Time	25 us
	Configure V2 UV Impact On RSTB	V2 UV does not assert RSTB

Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

V3MON_DAC configuration	V3MON Enable	Enabled
	V3MON Voltage Configuration	V3MON = 5.0 V
	V3MON Undervoltage Threshold	61 %
	V3MON Overvoltage Threshold	110 %
	V3MON Undervoltage Deglitcher Time	25 us
	V3MON Overvoltage Deglitcher Time	25 us
	Configure V3 UV Impact On RSTB	V3 UV does not assert RSTB
	Configure V3 OV Impact On RSTB	V3 OV does not assert RSTB

Table 5. Program ID

Functional block	Feature	OTP selection
Program ID	Program ID High	B
	Program ID Low	1

Configuration report for FS2320-ASILB OTP program ID: BB1 rev A

8 Legal information

8.1 Definitions

Draft - The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Limited warranty and liability - Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use - NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications - Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem

which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values - Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale - NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license - Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications - This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control - This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations - A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

8.2 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

NXP - is a trademark of NXP B.V.

Contents

1 General description 1

2 Features and benefits 1

3 Applications 2

4 Ordering information 2

5 Power up sequence summary 3

6 Hardware configuration diagram 4

7 OTP configuration 5

8 Legal information 12

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2024 . All rights reserved.

For more information, please visit: <http://www.nxp.com>
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1/22/2024
Document identifier: R_MFS2320BMBB1EP