

### 1 General description

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The FS23 is a family of automotive Safety SBC devices with multiple power supplies, designed to support general purpose body applications requiring low power modes and CANFD and LIN communication.

This family of devices supports a wide range of applications, offering choice in output voltage settings, physical interfaces and integrated system level features to address low power and noise sensitive applications with Automotive Safety Integrity Levels up to FS2300-QM.

The FS23 integrates an EMC optimized switch mode regulator (HVBUCK), which can be replaced by an LDO voltage regulator (HVLDO1), to supply a microcontroller and two other LDO voltage regulators (HVLDO2, HVLDO3) to supply communication devices and others. The HVBUCK is an high performance switching regulator capable to switch from pulse frequency modulation (PFM) mode to pulse width modulation (PWM) mode via I2C or SPI command to optimize noise management. The LDOs are connected to VSUP.

The FS23 is developed in compliance with the ISO26262:2018 standard, and it includes enhanced safety features, with fail-safe outputs, becoming part of a full safety-oriented system, covering FS2300-QM safety integrity level.

### 2 Features and benefits

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- Three linear regulators with low power mode support
- CAN FD and LIN transceivers
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Selectable wake-up sources to bring the system back from low power modes
- Two wake-up inputs and four configurable GPIO pins
- Four high side drivers, with PWM and cyclic sense capabilities
- SPI communication interface
- Internal voltage monitoring, Watchdog
- Two safety outputs (RSTB, LIMP0)



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### 3 Applications

- Body control module
- HVAC
- Lighting
- Steering column lock
- Seat module
- Roof module
- Door control module
- Car access

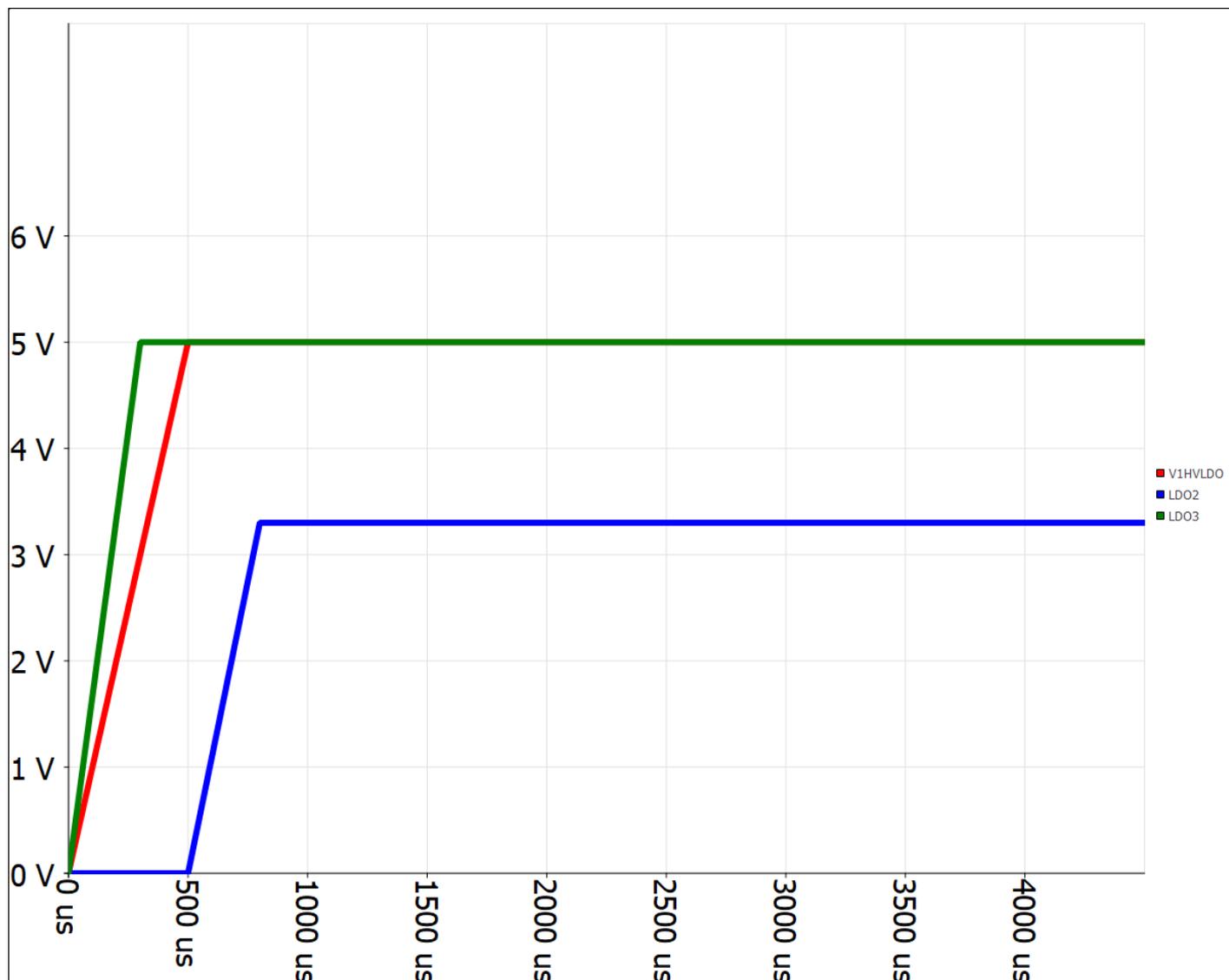
### 4 Ordering information

Table 1. Ordering information

Type number <sup>[1]</sup>	Package		
	Name	Description	Version
MFS2303BMMA4EP	H-PQFN-48	QFN48-EP plastic thermally enhanced, wettable flanks. 48 terminals; 0.5 mm pitch; 7 mm x 7 mm x 0.85 mm body	SOT619-27

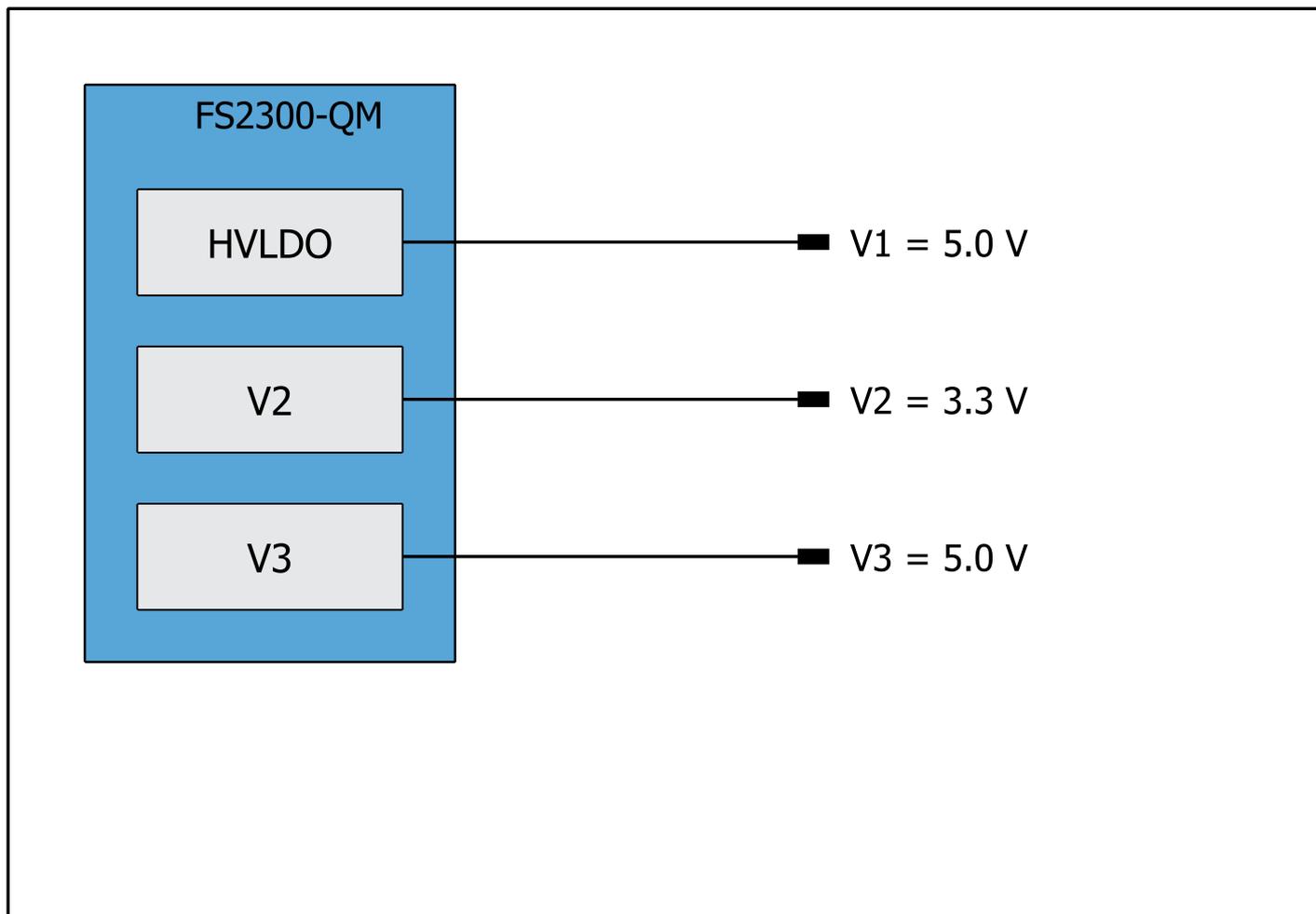
[1] To order parts in tape and reel, add the R2 suffix to the part number.

## 5 Power-up sequence summary



The signals depicted above are enable signals for each regulator. They don't represent the actual ramp voltage.

## 6 Hardware configuration diagram



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## 7 OTP configuration

See FS2300 datasheet for parametric details. The OTP configuration summary for MA4 sequence ID is provided in Tables below.

Table 2. Device OTP configuration

Functional block	Feature	OTP selection
System configuration	Enable V1 PNP	V1 PNP mode is disabled
	Enable HS24	HSD2 and HSD4 are enabled
	Enable HS13	HSD1 and HSD3 are enabled
	Enable LDT	LDT is enabled
	Enable LIN	LIN is enabled
	Enable CAN	CAN is enabled
	Enable Key OFF-ON	Key OFF - Key ON function is disabled
	Bypass Slots	Disabled
	SPI Enable	SPI pins are enabled
	I2C Address	Not Used
WAKES configuration	WAKE1 Pull Down	WAKE1 internal pull down is enabled and pull up is disabled
	WAKE2 Pull Down	WAKE2 internal pull down and pull up are configured as cell repeater
LVIOs configuration	Power Sequence Slot For LVIO3	LVIO3 polarity is changed in slot 0
	Enable HS Of LVIO3	LVIO3 HS is disabled
	Enable LS Of LVIO3	LVIO3 LS is disabled
	Pull Down On LVIO3	LVIO3 internal pull down is enabled and pull up is disabled

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	Config LVIO3 Pin Default State	LVIO3 default state is low (LS ON or LS OFF with ext PD)
	Power Sequence Slot For LVIO4	LVIO4 is not released in a slot (En by SPI/I2C)
	Enable HS Of LVIO4	LVIO4 HS is enabled
	Enable LS Of LVIO4	LVIO4 LS is enabled
	Pull Down On LVIO4	LVIO4 internal pull down and pull up are disabled
	Config LVIO4 Pin Default State	LVIO4 default state is low (LS ON or LS OFF with ext PD)
	Pull Down On LVI5	LVI5 internal pull down is disabled and pull up is enabled
HVIOs configuration	Power Sequence Slot For HVIO1	HVIO1 polarity is changed in slot 0
	Pull Down On HVIO1	HVIO1 internal pull down and pull up are disabled
	Configure HVIO1	HVIO1 default state is high (HIZ)
	HVIO1 Enable	HVIO1 is configured as an output
	Power Sequence Slot For HVIO2	HVIO2 polarity is changed in slot 0
	Pull Down On HVIO2	HVIO2 internal pull down and pull up are disabled
	Configure HVIO2	HVIO2 default state is high (HIZ)
	HVIO2 Enable	HVIO2 is configured as an output
IO function selection	HVIO1 Function Selection	HVO1 is connected to LIMP1 function
	HVIO2 Function Selection	HVO2 is connected to LIMP2 function
	LVO3 Function Selection	LVO3 is connected to alternate function
	LVO4 Function Selection	LVO4 is connected to alternate function

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	HS1 Function Selection	HS1 is connected to HS1 driver
	HS3 Function Selection	HS3 is connected to HS3 driver

Table 3. Regulators

Functional block	Feature	OTP selection
V1 HVLDO configuration	V1 HVLDO Power-up Slot	Slot 0
	V1 HVLDO Behaviour In Case Of TSD	The device transition to FailSafe state (M30) in case of TSD
	V1 LDO Overcurrent Threshold	V1 LDO OC = 150 mA
	V1 LDO Regulator Voltage	V1 = 5.0 V
V2 configuration	LDO2 Power-up Slot	Slot 1
	Enable Request Of LDO2	Enabled
	LDO2 Behaviour In Case Of TSD	The device transition to FailSafe state (M30) in case of TSD
	V2 LDO Overcurrent Threshold	V2 LDO OC = 150 mA
	V2 LDO Regulator Voltage	V2 = 3.3 V
V3 configuration	LDO3 Power-up Slot	Slot 0
	LDO3 Behaviour In Case Of TSD	The device transition to FailSafe state (M30) in case of TSD
	V3 LDO Overcurrent Threshold	V3 LDO OC = 150 mA
	V3 LDO Regulator Voltage	V3 = 5.0 V

Table 4. Functional Safety

Functional block	Feature	OTP selection
System configuration	LIMP0 Enable	LIMP0 is enabled
	Configure First Fault	Do Not GoTo FS at first fault

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	Disable The RSTB 8s Timer	RSTB 8s timer is disabled
	RSTB Pulse Duration	10 ms
	Lock The Watchdog	Watchdog Functional
	Configure FS State Duration	FS state duration is 100 ms
	Configure FS State Exit	Automatic restart after FS state
	Disable INIT Registers CRC Protection	CRC is enabled
	V1 Overvoltage Detection	The device transition to FailSafe state (M30) in case of OV
	V2 Overvoltage Detection	The device transition to FailSafe state (M30) in case of OV
	V3 Overvoltage Detection	The device transition to FailSafe state (M30) in case of OV
LIMP configuration	LIMP1 Polarity	PWM frequency = 1.25 Hz with 50 % duty cycle (Default high)
	LIMP2 Polarity	PWM frequency = 100 Hz (Default high)
V0MON_RES configuration	V0MON Enable	Disabled
	V0MON Voltage Configuration	1.0 V
	V0MON Undervoltage Threshold	64 %
	V0MON Overvoltage Threshold	102.5 %
	V0MON Undervoltage Deglitcher Time	5 us
	V0MON Overvoltage Deglitcher Time	25 us
	Configure V0 UV Impact On RSTB	VMON_EXT UV does not assert RSTB
	Configure V0 OV Impact On RSTB	VMON_EXT OV does not assert RSTB
V1MON_DAC configuration	V1MON Enable	Enabled
	V1MON Voltage Configuration	V1MON = 5.0 V

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	V1MON Undervoltage Threshold	61 %
	V1MON Overvoltage Threshold	110 %
	V1MON Undervoltage Deglitcher Time	25 us
	V1MON Overvoltage Deglitcher Time	25 us
	Configure V1 UV Impact On RSTB	V1 UV asserts RSTB
	Configure V1 OV Impact On RSTB	V1 OV asserts RSTB
V2MON_DAC configuration	V2MON Enable	Enabled
	V2MON Voltage Configuration	V2MON = 3.3 V
	V2MON Undervoltage Threshold	91.5 %
	V2MON Overvoltage Threshold	110 %
	V2MON Undervoltage Deglitcher Time	25 us
	V2MON Overvoltage Deglitcher Time	25 us
	Configure V2 UV Impact On RSTB	V2 UV does not assert RSTB
	Configure V2 OV Impact On RSTB	V2 OV does not assert RSTB
V3MON_DAC configuration	V3MON Enable	Enabled
	V3MON Voltage Configuration	V3MON = 5.0 V
	V3MON Undervoltage Threshold	91.5 %
	V3MON Overvoltage Threshold	110 %
	V3MON Undervoltage Deglitcher Time	25 us
	V3MON Overvoltage Deglitcher Time	25 us
	Configure V3 UV Impact On RSTB	V3 UV does not assert RSTB
	Configure V3 OV Impact On RSTB	V3 OV does not assert RSTB

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Table 5. Program ID

Functional block	Feature	OTP selection
Program ID	Program ID High	A
	Program ID Low	4

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For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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