

Hands-On Exercise (PWM_ADC_SYN)

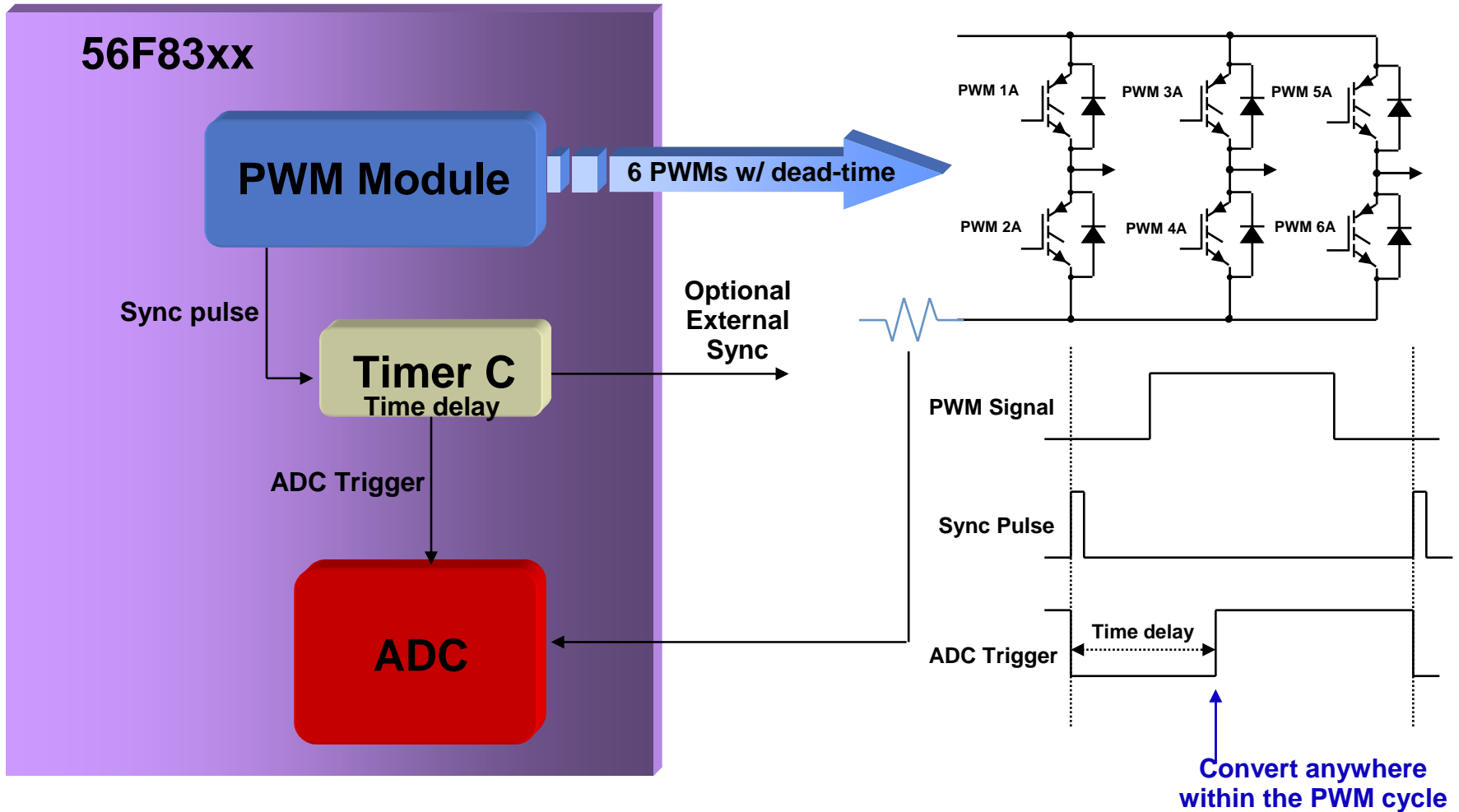
Hands-On Training



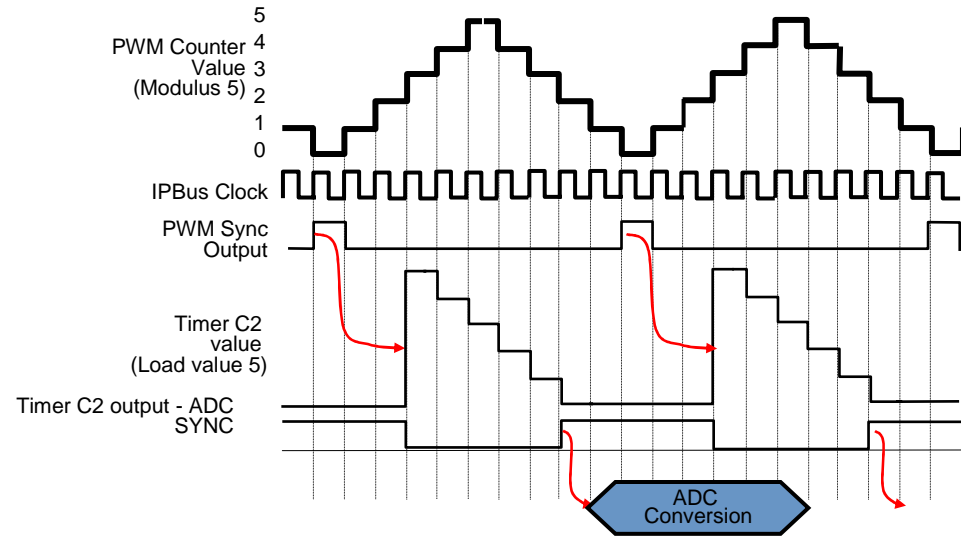
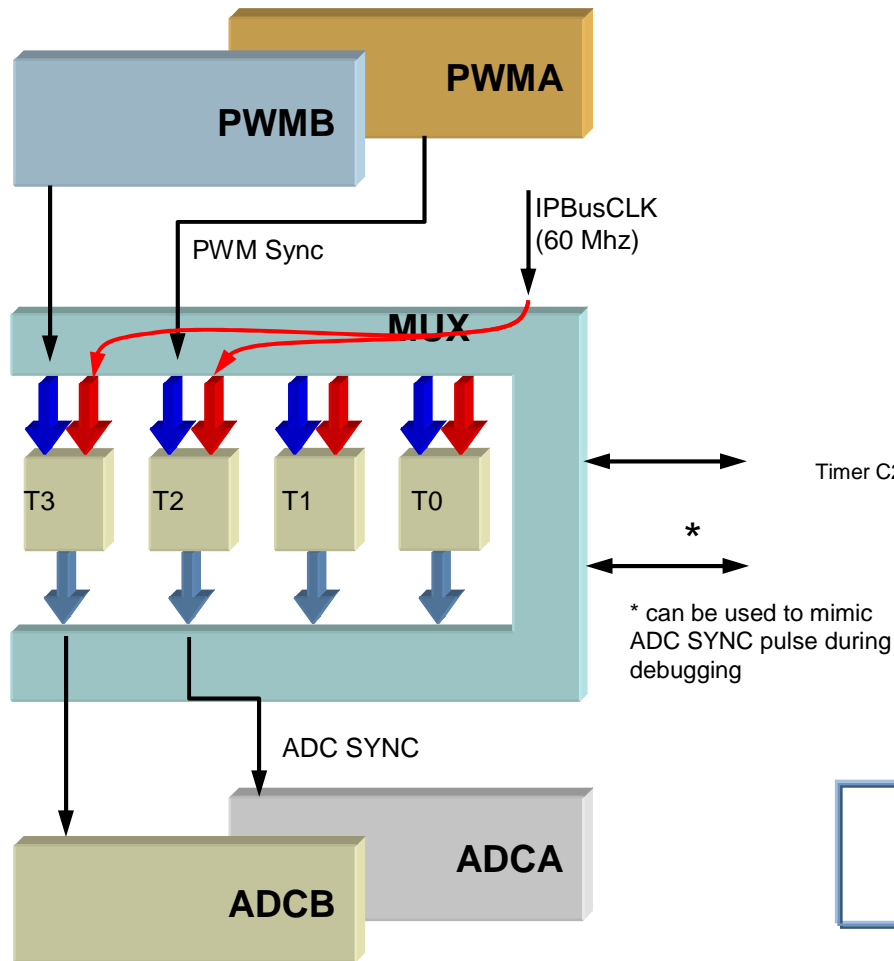
Approach

- ❖ **Use Processor Expert Beans to implement Target System application**
 - ✓ **Use 56F83xx PWM0 with Internal TimerC Channel 2 to trigger ADCA (Channel 0) .**
 - ✓ **Download and Execute on 56F83xx EVM**

ADC Synchronization from the PWM Module

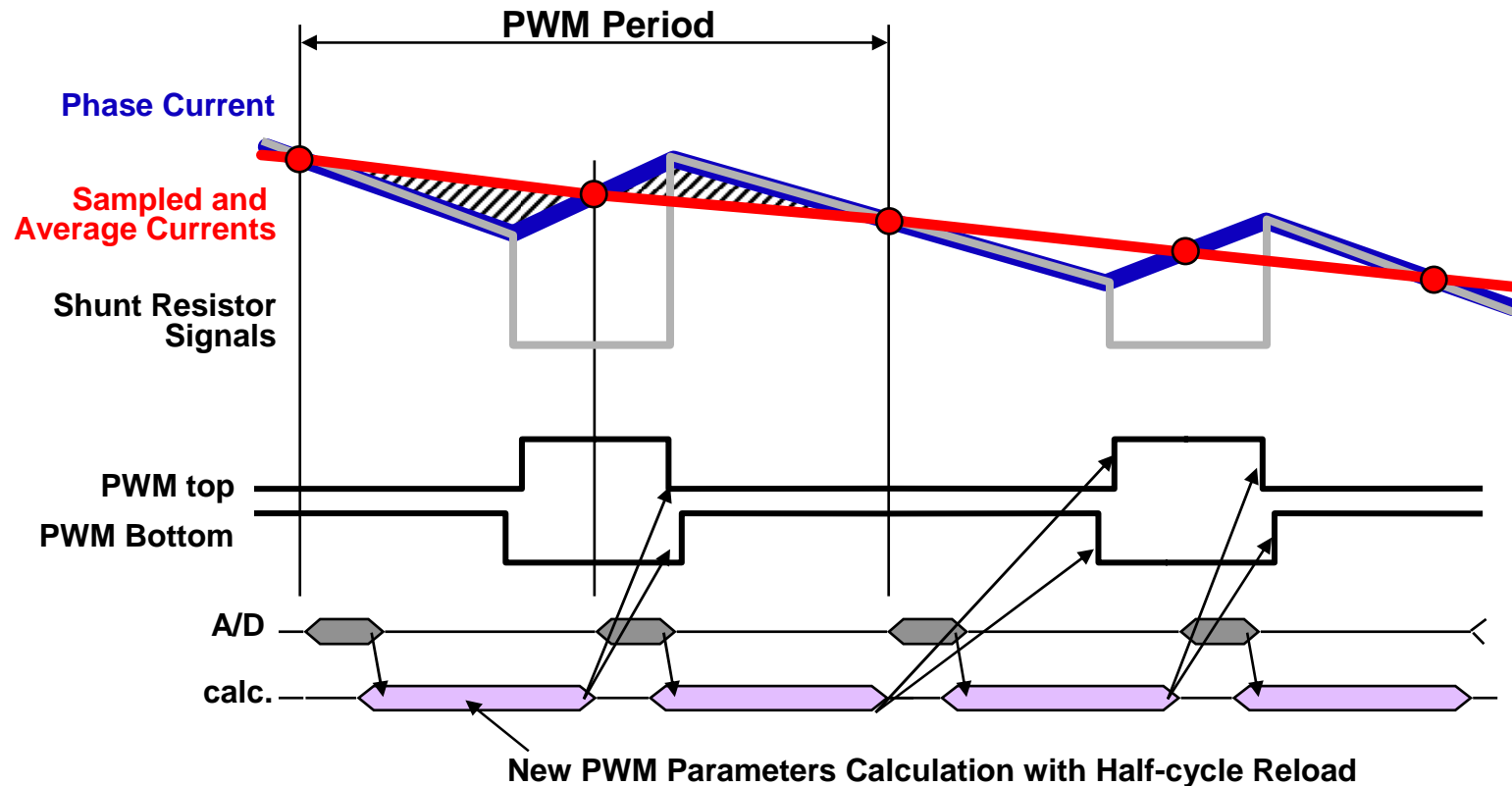


ADC-PWM Synchronization for 56F83XX



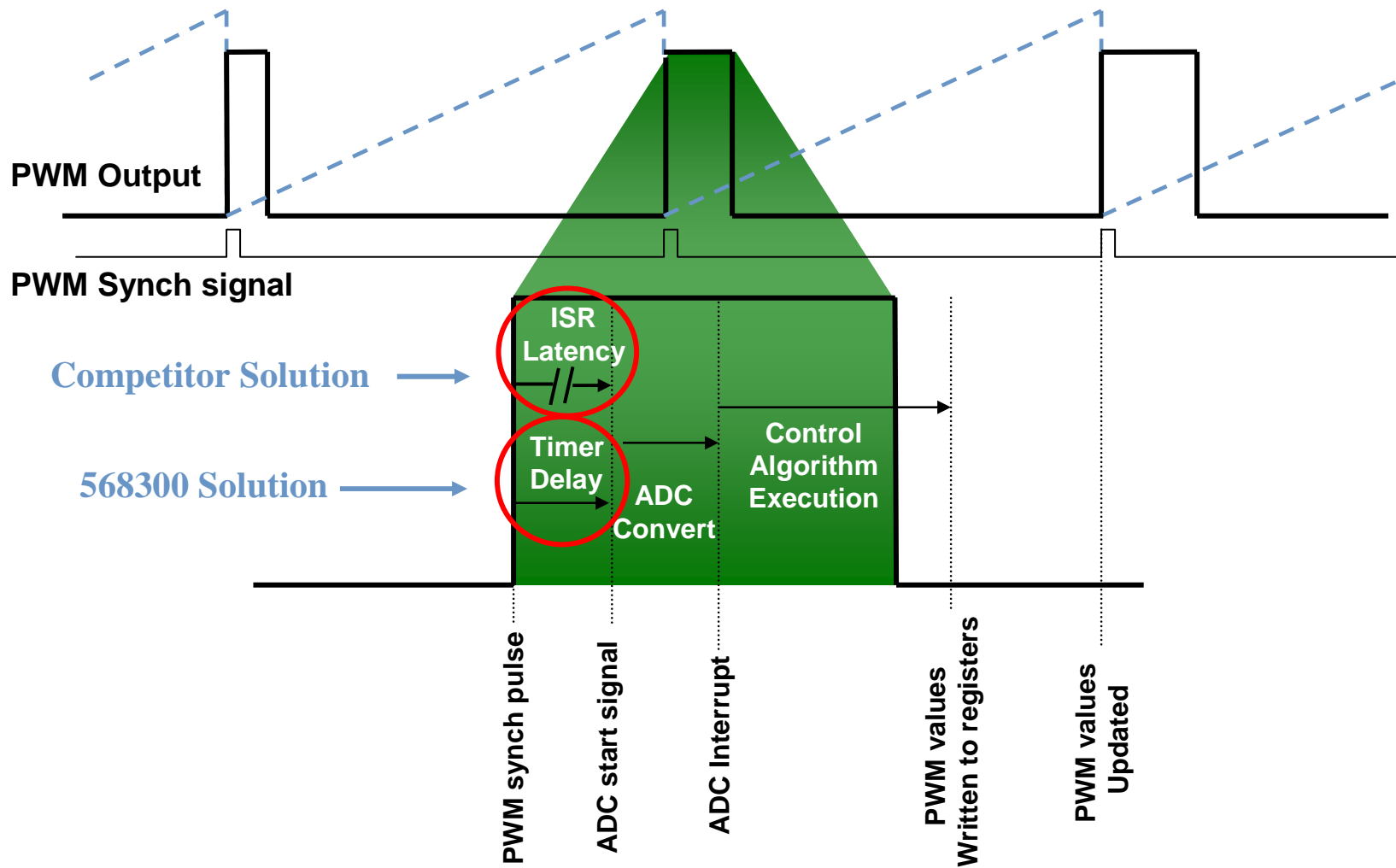
PWM, QUADTimer and ADC can communicate internally with no CPU support

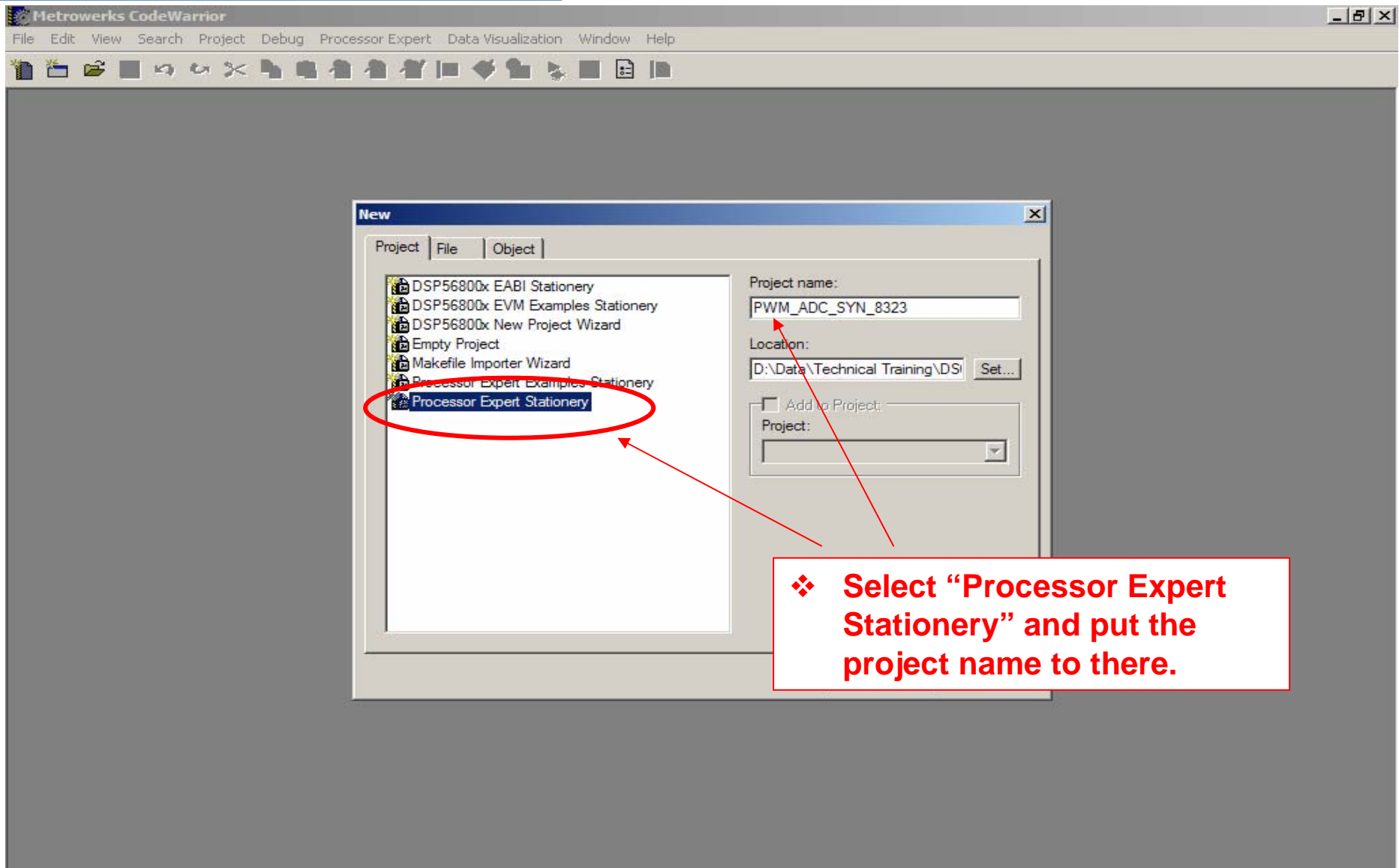
A/D Converters - PWM Synchronization Benefits

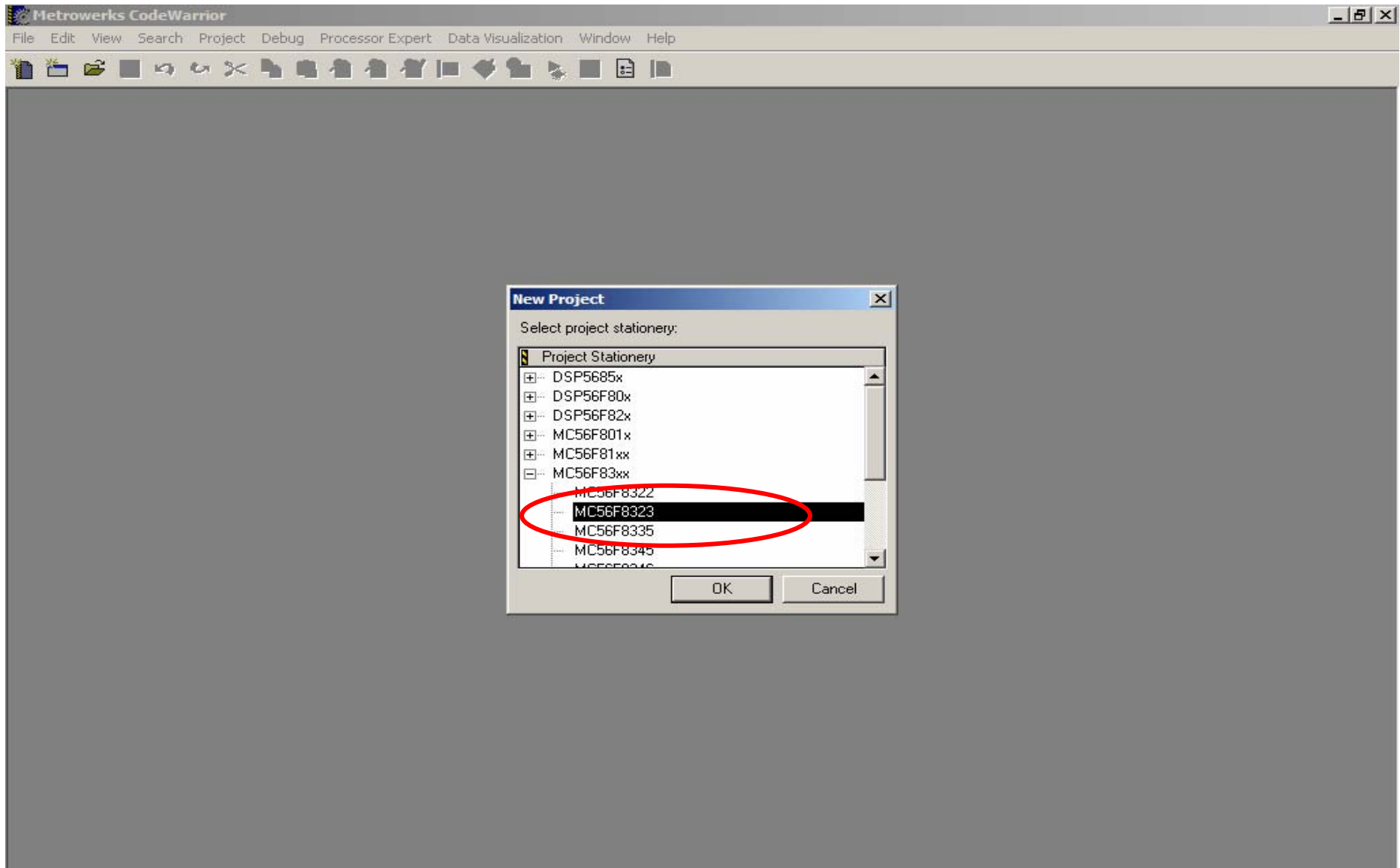


- ✓ ADC Sampling helps to filtering the measured current - antialiasing.
- ✓ Noise free ADC sampling when the power switch is not acting
- ✓ ADC sample is taken when shunt resistor signal (information) is available

ADC Synchronization with the PWM







DDFAE Training

The screenshot shows the Metrowerks CodeWarrior IDE interface. The main window displays a project named 'PWM_ADC_SYN_8323.mcp'. The 'Target CPU [Cpu:56F8323]' window shows a 3D model of the 56F8323 microcontroller. The 'Bean Selector' window is open, showing a tree view of components. The 'ADC' component is selected and circled in red. A red callout box points to the ADC component with the text: '❖ Select and double click ADC inside "CPU Internal Peripherals - Converter Beans"'. The 'Bean Selector' window has tabs for 'Categories', 'On-Chip Prphrls', 'Alphabet', 'Keywords', and 'Quick help >'. The tree view shows the following structure:

- [-] CPU
 - [-] CPU External Devices
 - [-] CPU Internal Peripherals
 - [-] Communication
 - [-] Converter
 - [-] ADC (Selected)
 - [-] Interrupts
 - [-] Measurement
 - [-] Memory
 - [-] Peripheral Initialization Beans
 - [-] Port I/O
 - [-] Timer
 - [-] SW

Filter: all/CPU Licensed

Confirm

Do you want to enable the bean in all configurations?
Select "No" if you want to use the bean in current configuration only.

Do not ask again

Bean Inspector AD1:ADC

Bean	Items	Visibility	Help
Bean name	AD1		
A/D converter	ADCA	ADCA	
Sharing	Disabled		
Interrupt service/event	Enabled		
A/D interrupt	INT_ADCA	INT_ADC	
A/D interrupt priority	medium pri	1	
Interrupt preserve registers	yes		
Interrupt	INT_ADCA	INT_ADC	
Interrupt priority	medium pri	1	
Interrupt preserve registers	yes		
A/D channels	1		
Channel0			
A/D channel (pin)	ANA0	ANA0	
A/D channel (pin) signal			
Mode select	Single End		
Queue	Enabled		
Mode	Sequential		
A/D samples	8		
Sample0	Enabled		
Channel	0		
High limit	32760		
Low limit	0		
Offset	0		
Zero crossing	Disabled		
Sample1	Disabled		
Sample2	Disabled		
Sample3	Disabled		
Sample4	Disabled		

Errors: 1, warnings: 0, hints: 0

AD1
ERROR: Error in the bean setting. More details provide...

The screenshot shows the DDFAE configuration interface for the PWM_ADC_SYN_8323.mcp project. The left pane shows a tree view with 'Beans' expanded to 'AD1-ADC'. The right pane shows the configuration table for the AD1 bean.

Property	Value	Comment
Bean name	AD1	
A/D converter	ADCA	ADCA
Sharing	Disabled	
Interrupt service/event	Enabled	
A/D interrupt	INT_ADCA_Complete	INT_ADCA_Complete
A/D interrupt priority	medium priority	1
Interrupt preserve registers	yes	
Interrupt	INT_ADCA_ZC_LE	INT_ADCA_ZC_LE
Interrupt priority	medium priority	1
Interrupt preserve registers	yes	
A/D channels	1	
Channel0		
A/D channel (pin)	ANA0	ANA0
A/D channel (pin) signal		
Mode select	Single Ended	
Queue	Enabled	
Mode	Sequential	
A/D samples	8	
Sample0	Enabled	
Sample1	Disabled	
Sample2	Disabled	
Sample3	Disabled	
Sample4	Disabled	
Sample5	Disabled	
Sample6	Disabled	
Sample7	Disabled	
A/D prescaler	ADCA_ADCR2	ADCA_ADCR2
A/D resolution	Autoselect	12 bits
Conversion time	1.700 μ s	high: 1.700 μ s
Internal trigger	Disabled	
Trigger source		Bean is not selected
Sync from PWM	no	
Volt. ref. recovery time	100	
Power up delay		

❖ 1.7usec

❖ Select Enable internal trigger.

❖ Select "Yes" for Sync from PWM

Property	Value	Unit/Detail
Bean name	AD1	
A/D converter	ADCA	ADCA
Sharing	Disabled	
Interrupt service/event	Enabled	
A/D interrupt	INT_ADCA_Complete	INT_ADCA_Complete
A/D interrupt priority	medium priority	1
Interrupt preserve registers	yes	
Interrupt	INT_ADCA_ZC_LE	INT_ADCA_ZC_LE
Interrupt priority	medium priority	1
Interrupt preserve registers	yes	
A/D channels	1	
Channel0		
A/D channel (pin)		
A/D channel (pin) signal		
Mode select		
Queue		
Mode		
A/D samples	8	
Sample0	Enabled	
Sample1	Disabled	
Sample2	Disabled	
Sample3	Disabled	
Sample4	Disabled	
Sample5	Disabled	
Sample6	Disabled	
Sample7	Disabled	
A/D prescaler	ADCA_ADCR2	ADCA_ADCR2
A/D resolution	Autoselect	12 bits
Conversion time	1.700 μs	high: 1.700 μs
Internal trigger	Enabled	
Trigger source		Bean is not selected
Sync from PWM	yes	
PWM source		Bean is not selected
Volt. ref. recovery time	100	

DDFAE Training

Processor Expert helps you to select or create a shared bean ...

The bean "ADC" uses shared bean for item "Trigger source".
Currently you have no appropriate bean in your project, you can add new one just now.

- Add new shared bean from template: TriggerTimer
- Add new shared bean: Init_TMR

Hint: It's recommended to add new shared bean from templates, because templates usually contain predefined settings.

OK Cancel Help

Sample2	Disabled	
Sample3	Disabled	
Sample4	Disabled	
Sample5	Disabled	
Sample6	Disabled	
Sample7	Disabled	
A/D prescaler	ADCA_ADCR2	ADCA_ADCR2
A/D resolution	Autoselect	12 bits
Conversion time	1.700 µs	high: 1.700 µs
Internal trigger	Enabled	
Trigger source		Bean is not selected
Sync from PWM	yes	
PWM source		Bean is not selected
Volt. ref. recovery time	100	

❖ Kick Trigger Source and select “Add new shared bean from template TriggerTimer”.

Confirm

Do you want to enable the bean in all configurations?
Select "No" if you want to use the bean in current configuration only.

Do not ask again

❖ Kick "yes"

Bean name	TMR1	Device	TMRA0
Settings			
Clock settings			
Primary source	prescaler (IP BUS clock / 128)		
Secondary source	counter 0 input pin		
Operation mode			
Count mode	count repeatedly		
Count length	count till compare, then reinitialize		
Input capture mode			
OutputMode	toggle OFLAG output on successful comp		
Compare load control 1			
Compare load control 2			
Pins: 0			
Interrupts			
Timer Channel			
Interrupt	INT_TMRA0	INT_TMRA0	
Timer compare interrupt	Disab		
Timer overflow interrupt	Disab		
Input edge interrupt	Disab		
Timer compare 1 interrupt	Disab		
Timer compare 2 interrupt	Disab		
Interrupt priority	mediu		

The screenshot displays the DDFAE configuration environment. On the left, a project tree shows the configuration for 'sdm pROM-xRAM'. The main window shows the configuration for the 'TMR1' timer bean, which is associated with the 'TMRA0' device.

Property	Value
Bean name	TMR1
Device	TMRA0
Settings	
Clock settings	
Primary source	
Primary source	prescaler (IP BUS clock / 128)
Secondary source	
Secondary source	counter 0 input pin
Operation mode	
Count once	count repeatedly
Count length	count till compare, then reinitialize
Count direction	up
Master mode	Disabled
External OFLAG force	Disabled
Forced OFLAG value	Disabled
Force OFLAG output	Disabled
Output enable	no
Output polarity	true
Input polarity	true
Co-channel initialization	Disabled
Input capture mode	Disabled
OutputMode	toggle OFLAG output on successful comp
Compare load control 1	Disabled
Compare load control 2	Disabled
Pins	0
Interrupts	
Timer Channel	
Interrupt	INT_TMRA0
Timer compare interrupt	Disabled
Timer overflow interrupt	Disabled
Input edge interrupt	Disabled
Timer compare 1 interrupt	Disabled
Timer compare 2 interrupt	Disabled
Interrupt priority	medium priority

The screenshot shows the DDFAE software interface with the following components:

- Left Panel (Project Explorer):** Shows a project named "PWM_ADC_SYN_8323.mcp". Under "Beans", the bean "TMR1:ADC\TriggerTimer[Init_TMR]" is selected and highlighted.
- Right Panel (Properties View):** Shows the configuration for the selected bean. The "Device" is set to "TMRC2". A dropdown menu is open under "Settings", showing a list of timer channels: TMRA0, TMRA1, TMRA2, TMRA3, TMRC0, TMRC1, and **TMRC2** (which is highlighted with a red circle and a red arrow).
- Annotation:** A red box contains the text: "❖ Select Timer C channel 2 'TMRC2'".
- Properties Table:**

Property	Value	Value
Bean name	TMR1	
Device	TMRC2	TMRC2
Settings		
Clock settings		
Primary source		
Primary source		
Secondary source		
Secondary source		
Operation mode		
Count once		
Count length		Count till compare, then reinitialize
Count direction	up	
Master mode	Disabled	
External OFLAG force	Disabled	
Forced OFLAG value	Disabled	
Force OFLAG output	Disabled	
Output enable	no	
Output polarity	true	
Input polarity		
Co-channel initialization		
Input capture mode		
OutputMode		
Compare load control 1		
Compare load control 2		
Pins		
Interrupts		
Timer Channel		
Interrupt	INT_TMRC2	INT_TMRC2
Timer compare interrupt	Disabled	
Timer overflow interrupt	Disabled	
Input edge interrupt	Disabled	
Timer compare 1 interrupt	Disabled	
Timer compare 2 interrupt	Disabled	
Interrupt priority	medium priority	1

The screenshot shows the DDFAE configuration tool with the following components:

- Left Panel (Project Explorer):** Shows a project named "PWM_ADC_SYN_8323.mcp". Under "Beans", the "TMR1:ADC\TriggerTimer[Init_TMR]" bean is selected.
- Right Panel (Properties View):** Shows the configuration for the "TMR1" bean on the "TMRC2" device. The "Secondary source" dropdown menu is open, with "prescaler (IP BUS clock)" selected and circled in red. Other settings include:
 - Bean name: TMR1
 - Device: TMRC2
 - Primary source: prescaler (IP BUS clock)
 - Secondary source: prescaler (IP BUS clock)
 - Operation mode: Count once
 - Count length: (empty)
 - Count direction: (empty)
 - Master mode: (empty)
 - External OFLAG force: (empty)
 - Forced OFLAG value: (empty)
 - Force OFLAG output: (empty)
 - Output enable: (empty)
 - Output polarity: (empty)
 - Input polarity: (empty)
 - Co-channel initialization: Disabled
 - Input capture mode: Disabled
 - OutputMode: toggle OFLAG output on successful comp...
 - Compare load control 1: Disabled
 - Compare load control 2: Disabled
 - Pins: 0
 - Interrupts:
 - Timer Channel:
 - Interrupt: INT_TMRC2
 - Timer compare interrupt: Disabled
 - Timer overflow interrupt: Disabled
 - Input edge interrupt: Disabled
 - Timer compare 1 interrupt: Disabled
 - Timer compare 2 interrupt: Disabled
 - Interrupt priority: medium priority

The screenshot displays the DDFAE configuration environment for a project named 'PWM_ADC_SYN_8323.mcp'. The left-hand pane shows a hierarchical tree of configurations, including 'sdm pROM-xRAM', 'Operating System', 'CPUs', 'Beans', and 'User Modules'. The 'Beans' section is expanded, and 'TMR1:ADC\TriggerTimer[Init_TMR]' is selected.

The right-hand pane shows the 'Properties' view for the selected bean. The 'Settings' section is expanded, and the 'Secondary source' dropdown menu is open, showing a list of options: 'counter 0 input pin', 'counter 1 input pin', 'counter 2 input pin', and 'counter 3 input pin'. The 'counter 2 input pin' option is highlighted and circled in red.

Other visible settings include:

- Bean name:** TMR1
- Device:** TMRC2
- Primary source:** prescaler (IP BUS clock)
- Operation mode:** Count once
- Count length:** (value not specified)
- Count direction:** up
- Master mode:** Disabled
- External OFLAG force:** Disabled
- Forced OFLAG value:** Disabled
- Force OFLAG output:** Disabled
- Output enable:** no
- Output polarity:** true
- Input polarity:** true
- Co-channel initialization:** Disabled
- Input capture mode:** Disabled
- OutputMode:** toggle OFLAG output on successful comp...
- Compare load control 1:** Disabled
- Compare load control 2:** Disabled
- Pins:** 0
- Interrupts:**
 - Timer Channel:**
 - Interrupt:** INT_TMRC2
 - Timer compare interrupt:** Disabled
 - Timer overflow interrupt:** Disabled
 - Input edge interrupt:** Disabled
 - Timer compare 1 interrupt:** Disabled
 - Timer compare 2 interrupt:** Disabled
 - Interrupt priority:** medium priority

The screenshot displays the DDFAE configuration tool for a PWM_ADC_SYN_8323.mcp project. The left pane shows a project tree with 'Beans' expanded to 'TMR1:ADC\TriggerTimer[Init_TMR]'. The right pane shows the configuration for this bean, with the 'Operation mode' dropdown menu open and 'Triggered count mode' selected. The configuration table is as follows:

Property	Value
Bean name	TMR1
Device	TMRC2
Settings	
Clock settings	
Primary source	prescaler (IP BUS clock)
Secondary source	counter 2 input pin
Operation mode	Triggered count mode
Count once	Stop mode
Count length	Count mode
Count direction	Edge count mode
Master mode	Gated count mode
External OFLAG force	Quadrature count mode
Forced OFLAG value	Signed count mode
Force OFLAG output	Triggered count mode
Output enable	Disabled
Output polarity	no
Input polarity	true
Co-channel initialization	Disabled
Input capture mode	Disabled
OutputMode	toggle OFLAG output on successful comp
Compare load control 1	Disabled
Compare load control 2	Disabled
Pins	0
Interrupts	
Timer Channel	
Interrupt	INT_TMRC2
Timer compare interrupt	Disabled
Timer overflow interrupt	Disabled
Input edge interrupt	Disabled
Timer compare 1 interrupt	Disabled
Timer compare 2 interrupt	Disabled
Interrupt priority	medium priority

The screenshot displays the IDE interface for configuring a timer bean. On the left, a project tree shows the configuration for 'sdm pROM-xRAM'. The main window shows the 'Properties' view for the 'TMR1' bean on the 'TMRC2' device. The 'Settings' section is expanded, showing various configuration options. The 'Output enable' property is set to 'yes' and is circled in red. Other properties include 'Primary source' (prescaler (IP BUS clock)), 'Secondary source' (counter 2 input pin), 'Operation mode' (Triggered count mode), and 'Interrupts' (INT_TMRC2).

Property	Value
Bean name	TMR1
Device	TMRC2
Settings	
Clock settings	
Primary source	
Primary source	prescaler (IP BUS clock)
Secondary source	
Secondary source	counter 2 input pin
Operation mode	Triggered count mode
Count once	count repeatedly
Count length	count till compare, then reinitialize
Count direction	up
Master mode	Disabled
External OFLAG force	Disabled
Forced OFLAG value	Disabled
Force OFLAG output	Disabled
Output enable	yes
Output polarity	true
Input polarity	true
Co-channel initialization	Disabled
Input capture mode	Disabled
OutputMode	asserted while counter is active
Compare load control 1	Disabled
Compare load control 2	Disabled
Pins	0
Interrupts	
Timer Channel	
Interrupt	INT_TMRC2
Timer compare interrupt	Disabled
Timer overflow interrupt	Disabled
Input edge interrupt	Disabled
Timer compare 1 interrupt	Disabled
Timer compare 2 interrupt	Disabled
Interrupt priority	medium priority

The screenshot displays the configuration of a TMR1 timer bean in the NXP IDE. The left pane shows the project structure, and the right pane shows the configuration table. The 'Input capture mode' row is highlighted, and a tooltip is displayed over it, listing several options for clearing the OFLAG output.

Bean name	TMR1
Device	TMRC2
Settings	
Clock settings	
Primary source	prescaler (IP BUS clock)
Secondary source	counter 2 input pin
Operation mode	
Count once	count repeatedly
Count length	count till compare, then reinitialize
Count direction	up
Master mode	Disabled
External OFLAG force	Disabled
Forced OFLAG value	Disabled
Force OFLAG output	Disabled
Output enable	yes
Output polarity	true
Input polarity	true
Co-channel initialization	Disabled
Input capture mode	Disabled
OutputMode	set on compare, cleared on secondary source input edge
Compare load control 1	asserted while counter is active
Compare load control 2	clear OFLAG output on successful compare
	set OFLAG output on successful compare
	toggle OFLAG output on successful compare
	toggle OFLAG output using alternating compare registers
	set on compare, cleared on secondary source input edge
	set on compare, cleared on counter rollover
	enable Gated Clock output while counter is active
Interrupts	
Timer Channel	
Interrupt	Disabled
Timer compare interrupt	Disabled
Timer overflow interrupt	Disabled
Input edge interrupt	Disabled
Timer compare 1 interrupt	Disabled
Timer compare 2 interrupt	Disabled
Interrupt priority	medium priority

The screenshot displays the configuration of a TMR1 bean in the IDE. The left pane shows the project structure, and the right pane shows the configuration table. The 'Compare load control 1' setting is highlighted with a red circle.

Property	Value
Bean name	TMR1
Device	TMRC2
Settings	
Clock settings	
Primary source	
Primary source	prescaler (IP BUS clock)
Secondary source	
Secondary source	counter 2 input pin
Operation mode	Triggered count mode
Count once	count repeatedly
Count length	count till compare, then reinitialize
Count direction	up
Master mode	Disabled
External OFLAG force	Disabled
Forced OFLAG value	Disabled
Force OFLAG output	Disabled
Output enable	yes
Output polarity	true
Input polarity	true
Co-channel initialization	Disabled
Input capture mode	Disabled
OutputMode	set on compare, cleared on secondary compare
Compare load control 1	Enabled
Load upon successful compare	with the value in TMRx_CMP1
Compare load control 2	Disabled
Pins	0
Interrupts	
Timer Channel	
Interrupt	INT_TMRC2
Timer compare interrupt	Disabled
Timer overflow interrupt	Disabled
Input edge interrupt	Disabled
Timer compare 1 interrupt	Disabled
Timer compare 2 interrupt	Disabled

The screenshot displays the configuration of the TMRC2 timer peripheral in the NXP IDE. The left pane shows the project structure, and the right pane shows the 'Properties' view for 'TMRC2'. The 'Registers' section is expanded, showing the following values:

Register Name	Value	Hex
Timer Compare register 1	10	D
Timer Compare register 2	0000	H
Timer Load register	0000	H
Timer Counter register	0000	H
Timer Comparator Load register 1	10	D
Timer Comparator Load register 2	0000	H

Two red circles highlight the values '10' for 'Timer Compare register 1' and '0000' for 'Timer Counter register'.

The screenshot displays the configuration interface for the TMRC2 timer peripheral. The left pane shows the project structure with 'TMR1:ADC\TriggerTimer[Init_TMR]' selected. The right pane shows the configuration details for 'TMRC2'.

Property	Value	Icon
Device	TMRC2	
Settings		
Clock settings		
Primary source	prescaler (IP BUS clock)	
Secondary source	counter 2 input pin	
Operation mode		
Count once	count repeatedly	<input type="radio"/>
Count length	count till compare, then reinitialize	<input type="radio"/>
Count direction	up	<input type="radio"/>
Master mode	Disabled	<input type="radio"/>
External OFLAG force	Disabled	<input type="radio"/>
Forced OFLAG value	Disabled	<input type="radio"/>
Force OFLAG output	Disabled	<input type="radio"/>
Output enable	yes	<input type="radio"/>
Output polarity	true	<input type="radio"/>
Input polarity	true	<input type="radio"/>
Co-channel initialization	Disabled	<input type="radio"/>
Input capture mode	Disabled	<input type="radio"/>
OutputMode	set on compare, cleared on secondary sou	<input type="radio"/>
Compare load control 1	Enabled	<input type="radio"/>
Load upon successful compare	with the value in TMRx_CMP1	<input type="radio"/>
Compare load control 2	Disabled	<input type="radio"/>
Pins	0	<input type="radio"/>
Interrupts		
Timer Channel		
Registers		
Timer Compare register 1	10	<input type="radio"/>
Timer Compare register 2	0000	<input type="radio"/>
Timer Load register	0000	<input type="radio"/>
Timer Counter register	0000	<input type="radio"/>
Timer Comparator Load register 1	10	<input type="radio"/>
Timer Comparator Load register 2	0000	<input type="radio"/>

❖ Double click AD1:ADC for PWM

❖ Select PWM source

Property	Value	Comment
Bean name	AD1	
A/D converter	ADCA	ADCA
Sharing	Disabled	
Interrupt service/event	Enabled	
A/D interrupt	INT_ADCA_Complete	INT_ADCA_Complete
A/D interrupt priority	medium priority	1
Interrupt preserve registers	yes	
Interrupt	INT_ADCA_ZC_LE	INT_ADCA_ZC_LE
Interrupt priority	medium priority	1
Interrupt preserve registers	yes	
A/D channels	1	
Channel0		
A/D channel (pin)	ANA0	ANA0
A/D channel (pin) signal		
Mode select	Single Ended	
Queue	Enabled	
Mode	Sequential	
A/D samples	8	
Sample0	Enabled	
Sample1	Disabled	
Sample2	Disabled	
Sample3	Disabled	
Sample4	Disabled	
Sample5	Disabled	
Sample6	Disabled	
Sample7	Disabled	
A/D prescaler	ADCA_ADCR2	ADCA_ADCR2
A/D resolution	Autoselect	12 bits
Conversion time	1.700 μs	high: 1.700 μs
Internal trigger	Enabled	
Trigger source	TMR1	
Sync from PWM	yes	
PWM source	...	Bean is not selected
Volt. ref. recovery time	100	

Processor Expert helps you to select or create a shared bean ...

The bean "ADC" uses shared bean for item "PWM source".
Currently you have no appropriate bean in your project, you can add new one just now.

- Add new shared bean: PWMMC
- Add new shared bean: Init_PWM

OK Cancel Help

Sample2	Disabled	
Sample3	Disabled	
Sample4	Disabled	
Sample5	Disabled	
Sample6	Disabled	
Sample7	Disabled	
A/D prescaler	ADCA_ADCR2	ADCA_ADCR2
A/D resolution	Autoselect	12 bits
Conversion time	1.700 µs	high: 1.700 µs
Internal trigger	Enabled	
Trigger source	TMR1	
Sync from PWM	yes	
PWM source		Bean is not selected
Volt. ref. recovery time	100	

BASIC ADVANCED EXPERT Bean Level: High Level Bean

DDFAE Training

The screenshot shows the DDFAE (Device Design Framework) interface. On the left is a project tree for 'Pwm_Adc_Syn_8323.mcp'. The main area displays the configuration for the 'PwM C1' bean. A 'Confirm' dialog box is open, asking: 'Do you want to enable the bean in all configurations? Select "No" if you want to use the bean in current configuration only.' The 'Yes' button is highlighted with a red circle.

Property	Value
Bean name	PwM C1
Device	PwM_A
Align	center-aligned mode
Mode of PWM Pair 0	complementary
Mode of PWM Pair 1	complementary
Mode of PWM Pair 2	complementary
Top-Side PWM Pair 0 Polarity	Positive
Top-Side PWM Pair 1 Polarity	Positive
Top-Side PWM Pair 2 Polarity	Positive
Bottom-Side PWM Pair 0 Polarity	Positive
Bottom-Side PWM Pair 1 Polarity	Positive
PwM prescaler	Auto selected prescaler
Reload	1
Half cycle reload	no
Hardware acceleration	Disabled
Dead-time	Unassigned timing
Correction	Disabled
Interrupt service/event	Disabled
Channel 0	
Channel	PwModA0
PWM pin	PwMA0_GPIOA0
PWM pin signal	
Duty	50 %
Pin PWM0 active	yes
Output software control	no

DDFAE Training

PWM_ADC_SYN_8323.mcp

sdm pROM-xRAM

Files | Link Order | Targets | Processor Expert

- Configurations
 - sdm pROM-xRAM
 - ldm pROM-xRAM
 - sdm xROM-xRAM
 - ldm xROM-xRAM
- Operating System
- CPU's
 - Cpu:56F8323
 - Cpu:56F8323
- Beans
 - AD1:ADC
 - TMR1:ADC\TriggerTimer[Init_TMR]
 - PwMCM1:PwMMC**
- User Modules
 - PWM_ADC_SYN_8323.c:main
 - Events.c:event
- Generated Modules
- External Modules
- Documentation
- PESL

Bean Items Visibility Help < > Peripheral Initialization >

Properties | Methods | Events | Comment

Bean name	PwMCM1	
Device	PWM_A	PWM_A
Align	center-aligned mode	
Mode of PWM Pair 0	independent	
Mode of PWM Pair 1	independent	
Mode of PWM Pair 2	independent	
Top-Side PWM Pair 0 Polarity	Positive	
Top-Side PWM Pair 1 Polarity	Positive	
Top-Side PWM Pair 2 Polarity	Positive	
Bottom-Side PWM Pair 0 Polarity	Positive	
Bottom-Side PWM Pair 1 Polarity	Positive	
Bottom-Side PWM Pair 2 Polarity	Positive	
Write Protect	no	
Output pads	Disabled	
Enable in Wait mode	no	
Enable in EnOnCE mode	no	
Frequency		... Unassigned timing
Output Frequency		
Same frequency in modes	no	
PWMA		
PWMA prescaler	Auto selected prescaler	1
Reload	1	
Half cycle reload	no	
Hardware acceleration	Disabled	
Dead-time		... Unassigned timing
Correction	Disabled	
Interrupt service/event	Disabled	
Channel 0		
Channel	PWModA0	PWModA0
PWM pin	PWMA0_GPIOA0	PWMA0_GPIOA0
PWM pin signal		
Duty	50 %	... Error in main timing (Frequency)
Pin PWM0 active	no	
Output software control	no	

BASIC | ADVANCED | EXPERT Bean Level: Low Level Bean

The screenshot shows the configuration of a PWM bean in the NXP IDE. The left pane displays a project tree with the following structure:

- Configurations
 - sdm pROM-xRAM
 - ldm pROM-xRAM
 - sdm xROM-xRAM
 - ldm xROM-xRAM
- Operating System
- CPU
 - Cpu:56F8323
 - Cpu:56F8323
- Beans
 - AD1:ADC
 - TMR1:ADC\triggerTimer[Init_TMR]
 - PwMCl:PwMMC** (selected)
- User Modules
 - PWM_ADC_SYN_8323.c:main
 - Events.c:event
- Generated Modules
- External Modules
- Documentation
- PESL

The right pane shows the properties of the selected bean, 'PwMCl'. The 'Output pads' property is highlighted with a red circle. The properties are as follows:

Property	Value
Bean name	PwMCl
Device	PwM_A
Align	center-aligned mode
Mode of PWM Pair 0	independent
Mode of PWM Pair 1	independent
Mode of PWM Pair 2	independent
Top-Side PWM Pair 0 Polarity	Positive
Top-Side PWM Pair 1 Polarity	Positive
Top-Side PWM Pair 2 Polarity	Positive
Bottom-Side PWM Pair 0 Polarity	Positive
Bottom-Side PWM Pair 1 Polarity	Positive
Bottom-Side PWM Pair 2 Polarity	Positive
Write Protect	no
Output pads	Enabled
Enable in Wait mode	no
Enable in EnOnCE mode	no
Frequency	Unassigned timing
Output Frequency	
Same frequency in modes	no
PWMA	
PWMA prescaler	Auto selected prescaler
Reload	1
Half cycle reload	no
Hardware acceleration	Disabled
Dead-time	Unassigned timing
Correction	Disabled
Interrupt service/event	Disabled
Channel 0	
Channel	PwModA0
PWM pin	PwMA0_GPIOA0
PWM pin signal	PwMA0_GPIOA0
Duty	50 %
Pin PWM0 active	no
Output software control	no

At the bottom of the right pane, there are tabs for 'BASIC', 'ADVANCED', and 'EXPERT', and a 'Bean Level: Low Level Bean' indicator.

❖ Kick “...” box to input PWM frequency.

Property	Value	Status
Bean name	PwM1	OK
Device	PWM_A	OK
Align	center-aligned mode	OK
Mode of PWM Pair 0	independent	OK
Mode of PWM Pair 1	independent	OK
Mode of PWM Pair 2	independent	OK
Top-Side PWM Pair 0 Polarity	Positive	OK
Top-Side PWM Pair 1 Polarity	Positive	OK
Top-Side PWM Pair 2 Polarity	Positive	OK
Bottom-Side PWM Pair 0 Polarity	Positive	OK
Bottom-Side PWM Pair 1 Polarity	Positive	OK
Bottom-Side PWM Pair 2 Polarity	Positive	OK
Write Protect	no	OK
Output pads	Enabled	OK
Enable in Wait mode	no	OK
Enable in EnOnCE mode	no	OK
Frequency	Unassigned timing	Warning
Output Frequency		OK
Same frequency in modes	no	OK
PWMA		
PWMA prescaler	Auto selected prescaler	OK
Reload	1	OK
Half cycle reload	no	OK
Hardware acceleration	Disabled	OK
Dead-time	Unassigned timing	Warning
Correction	Disabled	OK
Interrupt service/event	Disabled	OK
Channel 0		
Channel	PWModA0	OK
PWM pin	PWMA0_GPIOA0	OK
PWM pin signal		OK
Duty	50 %	Warning
Pin PWM0 active	no	OK
Output software control	no	OK

Timing - Frequency

Runtime setting type: **fixed value**

Requested value: **50** kHz Error allowed: **5** %

Speed mode Adjusted value: Prescaler: Error:

high	50 kHz	1	0%
low	disabled		
slow	disabled		

Possible settings:
 Closest values: 50kHz;
 Possible in all speed modes: 228.889Hz-457.764Hz, 457.778Hz-915.527Hz, 915.555Hz-1.831kHz, 1.831kHz-30MHz;

❖ Input 50khz

OK Cancel Help

Bean Level: Low Level Bean

❖ Kick “...” box to input dead time value.

Property	Value
Bean name	PwMCMC1
Device	PwM_A
Align	center-aligned mode
Mode of PWM Pair 0	independent
Mode of PWM Pair 1	independent
Mode of PWM Pair 2	independent
Top-Side PWM Pair 0 Polarity	Positive
Top-Side PWM Pair 1 Polarity	Positive
Top-Side PWM Pair 2 Polarity	Positive
Bottom-Side PWM Pair 0 Polarity	Positive
Bottom-Side PWM Pair 1 Polarity	Positive
Bottom-Side PWM Pair 2 Polarity	Positive
Write Protect	no
Output pads	Enabled
Enable in Wait mode	no
Enable in EnOnCE mode	no
Frequency	50 kHz
Output Frequency	25 kHz
Same frequency in modes	no
PwMA	
PwMA prescaler	Auto selected prescaler
Reload	1
Half cycle reload	no
Hardware acceleration	Disabled
Dead-time	Unassigned timing
Correction	Disabled
Interrupt service/event	Disabled
Channel 0	
Channel	PwModA0
PWM pin	PwMA0_GPIOA0
PWM pin signal	
Duty	50 %
Pin PWM0 active	no
Output software control	no

Timing - Dead-time

Runtime setting type: **fixed value**

Init. value

Requested value: **0** unit: μs Units: With value

Error allowed: **5** unit: %

Speed mode	Adjusted value:	Prescaler:	Error:
high	0 μs	0	0%
low	disabled		
slow	disabled		

Possible settings:

Closest values: 0 μs ;

Possible in all speed modes: 0 μs -17.067 μs by 0.017 μs , 17.100 μs -34.133 μs by 0.033 μs , 34.200 μs -68.267 μs by 0.067 μs , 68.400 μs -136.533 μs by 0.133 μs ;

❖ Input 0

Overclocked Intersection of speed modes

OK Cancel Help

BASIC ADVANCED EXPERT Bean Level: Low Level Bean

PWM_ADC_SYN_8323.mcp

sdm pROM-xRAM

Files | Link Order | Targets | Processor Expert

- Configurations
 - ✓ sdm pROM-xRAM
 - ✗ ldm pROM-xRAM
 - ✗ sdm xROM-xRAM
 - ✗ ldm xROM-xRAM
- Operating System
- CPU's
 - ✓ Cpu:56F8323
 - ✗ Cpu:56F8323
- Beans
 - ✓ AD1:ADC
 - ✓ TMR1:ADC\TriggerTimer[Init_TMR]
 - ✓ PwMCM1:PwMMC
- User Modules
 - ✓ PWM_ADC_SYN_8323.c:main
 - ✓ Events.c:event
- Generated Modules
- External Modules
- Documentation
- ✗ PESL

Bean Items Visibility Help < > Peripheral Initialization >

Properties | Methods | Events | Comment

✓ Bean name	PwMCM1	
✓ Device	PWM_A	PWM_A
✓ Align	center-aligned mode	
✓ Mode of PWM Pair 0	independent	
✓ Mode of PWM Pair 1	independent	
✓ Mode of PWM Pair 2	independent	
✓ Top-Side PWM Pair 0 Polarity	Positive	
✓ Top-Side PWM Pair 1 Polarity	Positive	
✓ Top-Side PWM Pair 2 Polarity	Positive	
✓ Bottom-Side PWM Pair 0 Polarity	Positive	
✓ Bottom-Side PWM Pair 1 Polarity	Positive	
✓ Bottom-Side PWM Pair 2 Polarity	Positive	
✓ Write Protect	no	
✓ Output pads	Enabled	
✓ Enable in Wait mode	no	
✓ Enable in EnOnCE mode	no	
✓ Frequency	50 kHz	... high: 50 kHz
✓ Output Frequency	25 kHz	
✓ Same frequency in modes	no	
PWMA		
PWMA prescaler	Auto selected prescaler	1
✓ Reload	1	
✓ Half cycle reload	no	
Hardware acceleration	Disabled	
✓ Dead-time	0 μ s	... high: 0 μ s
Correction	Disabled	
Interrupt service/event	Disabled	
Channel 0		
✓ Channel	PWModA0	PWModA0
✓ PWM pin	PWMA0_GPIOA0	PWMA0_GPIOA0
✓ PWM pin signal		
✓ Duty	50 %	... high: 10 μ s
✓ Pin PWM0 active	no	
✓ Output software control	no	

BASIC | ADVANCED | EXPERT Bean Level: Low Level Bean

❖ Disable Channel1-5

❖ Disable all Fault inputs

Property	Value	Icon
Reload	1	
Half cycle reload	no	
Hardware acceleration	Disabled	
Dead-time	0 μ s	high: 0 μ s
Correction	Disabled	
Interrupt service/event	Disabled	
Channel 0	PwModA0	PwModA0
Channel	PwMA0_GPIOA0	PwMA0_GPIOA0
PWM pin	PwMA0_GPIOA0	
PWM pin signal		
Duty	50 %	high: 10 μ s
Pin PWM0 active	no	
Output software control	no	
Mask channel	no	
Mask fault 0	yes	
Mask fault 1	yes	
Mask fault 2	yes	
Channel 1	Disabled	
Channel 2	Disabled	
Channel 3	Disabled	
Channel 4	Disabled	
Channel 5	Disabled	
Fault protection	controlled by this bean	
Fault 0	Disabled	
Fault 1	Disabled	
Fault 2	Disabled	
Initialization		
Enabled in init. code	yes	
Events enabled in init.	yes	
CPU clock/speed selection		
High speed mode	This bean enabled	This bean is enabled
Low speed mode	This bean disabled	This bean is disabled
Slow speed mode	This bean disabled	This bean is disabled

DDFAE Training

The screenshot shows the Metrowerks CodeWarrior IDE interface. A red circle highlights the 'Generate Code' option in the context menu for the project 'PWM_ADC_SYN_8323.mcp'. The main window displays the configuration for the 'PWM_ADC_SYN_8323.mcp' project, showing various settings for channels, fault protection, and initialization.

Property	Value	Control
1	no	
Disabled	0 μs	... high: 0 μs
Disabled	Disabled	
PwModA0	PwModA0	
PwMA0_GPIOA0	PwMA0_GPIOA0	
Pwm pin signal	50 %	... high: 10μs
Pin PWM0 active	no	
Output software control	no	
Mask channel	no	
Mask fault 0	yes	
Mask fault 1	yes	
Mask fault 2	yes	
Channel 1	Disabled	
Channel 2	Disabled	
Channel 3	Disabled	
Channel 4	Disabled	
Channel 5	Disabled	
Fault protection	controlled by this bean	
Fault 0	Disabled	
Fault 1	Disabled	
Fault 2	Disabled	
Initialization		
Enabled in init. code	yes	
Events enabled in init.	yes	
CPU clock/speed selection		
High speed mode	This bean enabled	This bean is enabled
Low speed mode	This bean disabled	This bean is disabled
Slow speed mode	This bean disabled	This bean is disabled

DDFAE Training

The screenshot displays the IDE interface for configuring a PWM bean. On the left, the project tree shows the following structure:

- Configurations
 - sdm pROM-xRAM
 - ldm pROM-xRAM
 - sdm xROM-xRAM
 - ldm xROM-xRAM
- Operating System
- CPU's
 - Cpu:56F8323
 - Cpu:56F8323
- Beans
 - AD1:ADC
 - TMR1:ADC\TriggerTimer[Init_TMR]
 - PwMCM1:PwMMC
- User Modules
 - PWM_ADC_SYN_8323.c:main
 - Events.c:event
- Generated Modules
- External Modules
- Documentation
- PESL

The right pane shows the 'Properties' view for the 'sdm pROM-xRAM' bean. The 'Code Generation' dialog box is open, displaying the following information:

- Project: PWM_ADC_SYN_8323
- Module: PwMCM1
- Current line: 96 / Total lines: 430
- Errors: 0 / Warnings: 0 / Hints: 0
- Cancel button

The 'Properties' view is set to 'ADVANCED' and 'Bean Level: Low Level Bean'. The following table summarizes the visible properties:

Property	Value	Icon
Reload	1	
Half cycle reload	no	
Hardware acceleration	Disabled	
Dead-time	0 μ s	... high: 0 μ s
Correction	Disabled	
Interrupt service/event	Disabled	
Channel 0	PwModA0	PwModA0
Channel	PwMA0 GPIOA0	PwMA0_GPIOA0
PWM pin	PwMA0 GPIOA0	
...	high: 10 μ s	
Fault protection	controlled by this bean	
Fault 0	Disabled	
Fault 1	Disabled	
Fault 2	Disabled	
Initialization		
Enabled in init. code	yes	
Events enabled in init.	yes	
CPU clock/speed selection		
High speed mode	This bean enabled	This bean is enabled
Low speed mode	This bean disabled	This bean is disabled
Slow speed mode	This bean disabled	This bean is disabled

The screenshot displays the Processor Expert IDE interface. On the left, the 'Configurations' tree shows a project named 'sdm pROM-xRAM' with several sub-configurations. The 'User Modules' section is expanded, showing 'PWM_ADC_SYN_8323.c:main' selected. The main editor window on the right shows the source code for 'PWM_ADC_SYN_8323.c'. The code includes a header section with project details and copyright information, followed by preprocessor directives for including 'Cpu.h' and 'Events.h'.

```

/* *****
**      Filename   : PWM_ADC_SYN_8323.C
**      Project    : PWM_ADC_SYN_8323
**      Processor  : 56F8323
**      Version    : Driver 01.09
**      Compiler   : Metrowerks DSP C Compiler
**      Date/Time  : 10/24/2005, 5:09 PM
**      Abstract   :
**                  Main module.
**                  Here is to be placed user's code.
**      Settings   :
**      Contents   :
**                  No public methods
**
**      (c) Copyright UNIS, spol. s r.o. 1997-2004
**      UNIS, spol. s r.o.
**      Jundrovska 33
**      624 00 Brno
**      Czech Republic
**      http       : www.processorexpert.com
**      mail      : info@processorexpert.com
** ******/
/* MODULE PWM_ADC_SYN_8323 */

/* Including used modules for compiling procedure */
#include "Cpu.h"
#include "Events.h"

```

❖ Add the code for ADC conversion timing test

```

/* Include shared modules, which are used for whole project */
#include "PE_Types.h"
#include "PE_Error.h"
#include "PE_Const.h"
#include "IO_Map.h"

void main(void)
{
    /*** Processor Expert internal initialization. DON'T REMOVE THIS CODE!!!
    PE_low_level_init();
    /*** End of Processor Expert internal initialization.
    /*** Write your code here **/
    GPIO_C_DDR=3; // config Port C bit 0,1 as output
    GPIO_C_PER&=~3;
    GPIO_C_DR=1; // init Port C bit 0,1

    if(AD1_EnableIntTrigger()!=ERR_OK)
    {
        asm(debughalt);
    }
    for(;;) {}

}

/* END PWM_ADC_SYN_8323 */
** *****
**
** This file was created by UNIS Processor Expert 2.96 [03.65]
** for the Freescale 56800 series of microcontrollers.
** *****
**
    
```

❖ Put ADC PE bean EnableIntTrigger by Drag-n-Drop method.

The screenshot shows the Processor Expert IDE interface. On the left, the project tree for 'PWM_ADC_SYN_8323.mcp' is visible. Under 'User Modules', 'Events.c.event' is selected. A red box with the text '❖ Open Event.c event' has an arrow pointing to this file. On the right, the 'Events.c' file is open, displaying C code for an event module. The code includes headers, defines an event 'AD1_OnEnd', and provides a function signature 'void AD1_OnEnd(void)'. A red arrow points from the 'Events.c.event' file in the tree to the function definition in the code editor.

```

/* MODULE Events */

#include "Cpu.h"
#include "Events.h"

/*
** -----
**      Event      :  AD1_OnEnd (module Events)
**      From bean   :  AD1 [ADC]
**      Description :
**                  This event is called after the measurement (which
**                  consists of <1 or more conversions>) is/are finished.
**      Parameters  :  None
**      Returns     :  Nothing
** -----
*/
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt
                        /* is set to 'yes' (#pragma interrupt saveall is
void AD1_OnEnd(void)
{
    /* Write your code here ... */
}

/* END Events */

/*
** #####
**
** This file was created by UNIS Processor Expert 2.96 [03.65]
** for the Freescale 56800 series of microcontrollers.
** #####
**
*/

```


❖ Add Global variables

❖ Add GPIO pin for timing test

❖ Put ADC PE bean GetValue16 by Drag-n-Drop method.

```

**      Description :
**      This event is called after an interrupt
**      consists of <1 or more
**      Parameters : None
**      Returns : Nothing
**      -----
*/
unsigned int AdcSample;
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt
                        /* is set to 'yes' (#pragma interrupt saveall is

void AD1_OnEnd(void)
{
/* Write your code here ... */
unsigned int i=0x8;
if(AD1_GetValue16(&AdcSample)!=ERR_OK)
{
asm(debughlt);
}
//GPIO_C_DR^=0x0002;
GPIO_C_DR|=0x0001;
while(i-->0)
{
asm { nop; }
}
GPIO_C_DR&=~0x0001;
}

/* END Events */

/*
** #####
**
**      This file was created by UNIS Processor Expert 2.96 [03.65]
**      for the Freescale 56800 series of microcontrollers.
** #####
**
*/

```

The screenshot shows a development environment with two main panes. The left pane displays a project tree for 'PWM_ADC_SYN_8323.mcp'. The right pane shows the source code for 'Events.c'. A red circle highlights the 'Debug' button in the top toolbar, and a red arrow points from it to a red box containing the text 'Click debug'.

Project Tree (Left Pane):

- Configurations
 - sdm pROM-xRAM
 - ldm pROM-xRAM
 - sdm xROM-xRAM
 - ldm xROM-xRAM
- Operating System
- CPU's
 - Cpu:56F8323
 - Cpu:56F8323
- Beans
 - AD1:ADC
 - TMR1:ADC\TriggerTimer[Init_TMR]
 - PwMCM1:PwMMC
- User Modules
 - PWM_ADC_SYN_8323.c:main
 - Events.c:event
- Generated Modules
- External Modules
- Documentation
- PESL

Code Editor (Right Pane):

```

**      consists of <1 or more conversions>) is/are finished.
**      Parameters   : None
**      Returns      : Nothing
** -----
*/
unsigned int AdcSample;
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt
                        /* is set to 'yes' (#pragma interrupt saveall is

void AD1_OnEnd(void)
{
    /* Write your code here ... */
    unsigned int i=0x8;
    if(AD1_GetValue16(&AdcSample)!=ERR_OK)
    {
        asm(debughlt);
    }
    //GPIO_C_DR^=0x0003;
    GPIO_C_DR|=0x0001;
    while(i-->0)
    {
        asm { nsp; }
    }
    GPIO_C_DR&=~0x0001;
}

/* END Events */

/*
** #####
** This file was created by UNIS E
** for the Freescale 56800 series
** #####
** */
    
```

Line 42 Col 1

BASIC ADVANCED EXPERT

The screenshot shows the UNIS Processor Expert IDE. On the left, the project tree for PWM_ADC_SYN_8323.mcp is visible, showing configurations, operating system, CPUs, beans, and user modules. The 'Events.c' file is selected under 'User Modules'. The main editor window displays the code for 'Events.c' with the following content:

```

**      consists of <1 or more conversions>) is/are finished.
**      Parameters   : None
**      Returns      : Nothing
**      -----
*/
unsigned int AdcSample;
#pragma interrupt called /* Comment this line if the appropriate 'Interrupt
                        /* is set to 'yes' (#pragma interrupt saveall is

void AD1_OnEnd(void)
{
    /* Write your code here ... */
    unsigned int i=0x8;
    if(AD1_GetValue16(&AdcSample)!=ERR_OK)
    {
        GPIO_C_DR&=~0x0001;
    }
}

/* END Events */

/*
** #####
**      This file was created by UNIS Processor Expert 2.96 [03.65]
**      for the Freescale 56800 series of microcontrollers.
** #####
*/

```

A 'Downloading...' dialog box is overlaid on the code editor, showing 'Downloading 1588 bytes...' and a 'Cancel' button.

The screenshot displays the IDE interface for a project named **PWM_ADC_SYN_8323.mcp**. The left sidebar shows a tree view of project components:

- Configurations:
 - sdm pROM-xRAM (checked)
 - ldm pROM-xRAM (unchecked)
 - sdm xROM-xRAM (unchecked)
 - ldm xROM-xRAM (unchecked)
- Operating System
- CPUs:
 - Cpu:56F8323 (checked)
 - Cpu:56F8323 (unchecked)
- Beans:
 - AD1:ADC (checked)
 - TMR1:ADC\TriggerTimer[Init_TMR] (checked)
 - PwMCM1:PwMCMC (checked)
- User Modules:
 - PWM_ADC_SYN_8323.c:main (checked)
 - Events.c:event (checked)
- Generated Modules
- External Modules
- Documentation
- PESL (unchecked)

The main window shows the **sdm_pROM_xRAM.elf (Thread 0x0)** running. The **Variables: Live** table is empty, displaying *No local variables*.

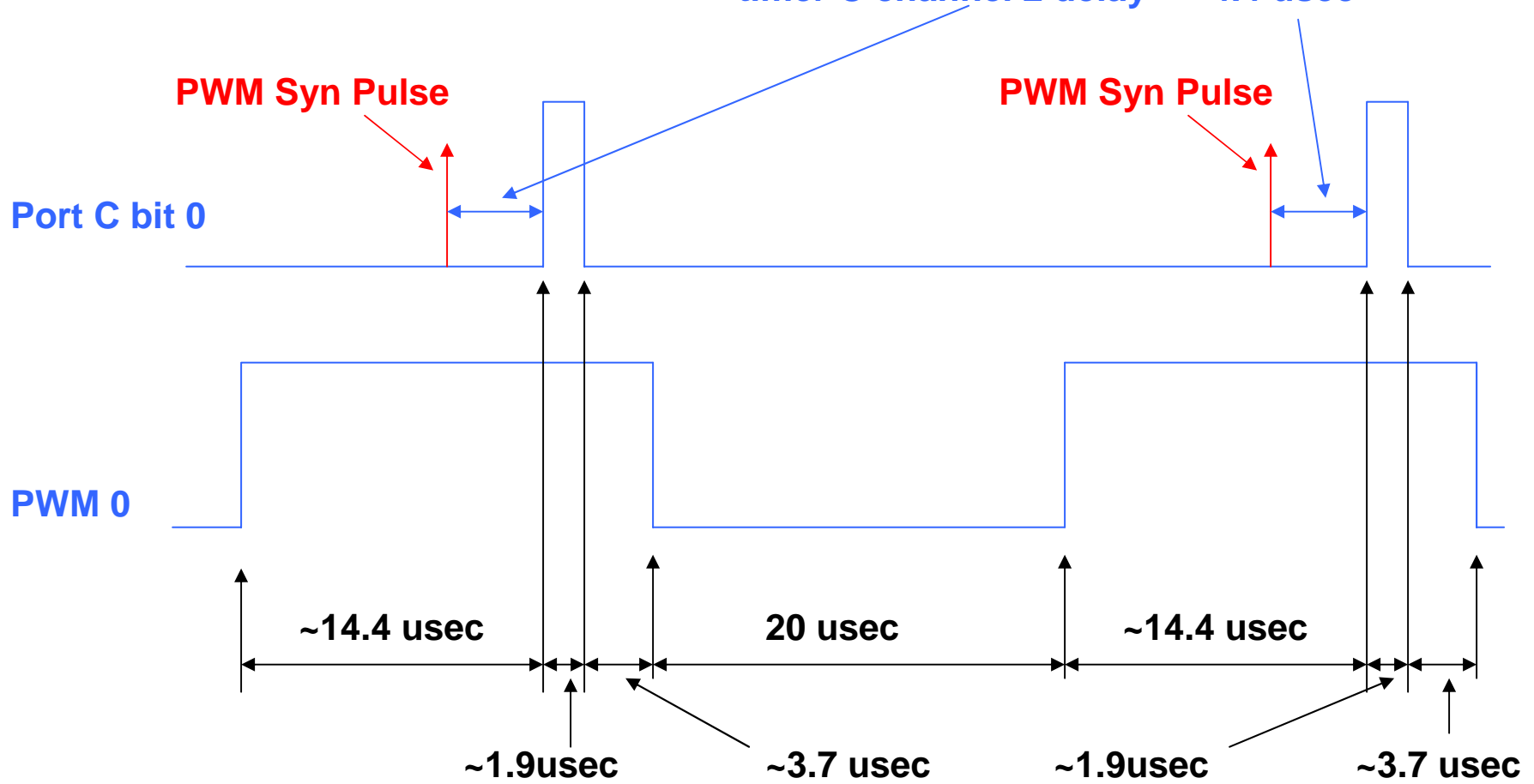
The **Source** window shows the following text:

```
Program "sdm_pROM_xRAM.elf" is executing.
Choose Break from the Debug menu to stop it.
```

The status bar at the bottom indicates **Line 1 Col 1 Source**. The IDE has tabs for **BASIC**, **ADVANCED**, and **EXPERT**.

Result 1:

In this example (PWM-Center Aligned mode):
 ADC conversion time +
 timer C channel 2 delay \approx 4.4 usec



The screenshot shows the configuration of a PWM bean named 'PwMC1'. The 'Align' property is currently set to 'center-aligned mode', but the 'edge-aligned mode' option is highlighted with a red circle and a red arrow. A callout box with a red border and a red diamond icon contains the text '❖ Change to Edge Aligned'.

Property	Value
Bean name	PwMC1
Device	PWM_A
Align	edge-aligned mode
Mode of PWM Pair 0	center-aligned mode
Mode of PWM Pair 1	edge-aligned mode
Mode of PWM Pair 2	independent
Top-Side PWM Pair 0 Polarity	Positive
Top-Side PWM Pair 1 Polarity	Positive
Top-Side PWM Pair 2 Polarity	Positive
Bottom-Side PWM Pair 0 Polarity	Positive
Bottom-Side PWM Pair 1 Polarity	Positive
Bottom-Side PWM Pair 2 Polarity	Positive
Write Protect	no
Output pads	Enabled
Enable in Wait mode	no
Enable in EnOnCE mode	no
Frequency	50 kHz
Output Frequency	50 kHz
Same frequency in modes	no
PWMA	
PWMA prescaler	Auto selected prescaler
Reload	1
Half cycle reload	no
Hardware acceleration	Disabled
Dead-time	0 μs
Correction	Disabled
Interrupt service/event	Disabled
Channel 0	
Channel	PWModA0
PWM pin	PWMA0_GPIOA0
PWM pin signal	
Duty	50 %
Pin PWM0 active	no
Output software control	no

DDFAE Training

The screenshot shows the IDE interface for configuring a PWM bean. On the left, a project tree shows the configuration for 'sdm pROM-xRAM'. The main area displays the 'Properties' tab for the 'PwM_C1' bean. The configuration includes various parameters such as 'Align', 'Mode of PWM Pair', 'Polarity', 'Frequency', and 'Output pads'. A red circle highlights the 'Debug' button in the top toolbar, and a red arrow points from it to a red box containing the text 'Click debug'.

Property	Value
Bean name	PwM_C1
Device	PwM_A
Align	edge-aligned mode
Mode of PWM Pair 0	independent
Mode of PWM Pair 1	independent
Mode of PWM Pair 2	independent
Top-Side PWM Pair 0 Polarity	Positive
Top-Side PWM Pair 1 Polarity	Positive
Top-Side PWM Pair 2 Polarity	Positive
Bottom-Side PWM Pair 0 Polarity	Positive
Bottom-Side PWM Pair 1 Polarity	Positive
Bottom-Side PWM Pair 2 Polarity	Positive
Write Protect	no
Output pads	Enabled
Enable in Wait mode	no
Enable in EnOnCE mode	no
Frequency	50 kHz
Output Frequency	50 kHz
Same frequency in modes	no
PwMA	
PwMA prescaler	Auto selected prescaler
Reload	1
Half cycle reload	no
Hardware acceleration	Disabled
Dead-time	0 μs
Correction	Disabled
Interrupt service/event	Disabled
Channel 0	
Channel	PwModA0
PWM pin	PwMA0_GPIOA0
PWM pin signal	
Duty	50 %
Pin PWM0 active	no
Output software control	no

DDFAE Training

PWM_AD1 Please wait.

sdm pROM-xRAM

Files | Link Order | Targets | Processor Expert

- Configurations
 - ✓ sdm pROM-xRAM
 - ✗ ldm pROM-xRAM
 - ✗ sdm xROM-xRAM
 - ✗ ldm xROM-xRAM
- Operating System
- CPU's
 - ✓ Cpu:56F8323
 - ✗ Cpu:56F8323
- Beans
 - ✓ AD1:ADC
 - ✓ TMR1:ADC\TriggerTimer[Init_TMR]
 - ✓ PwMCM1:PwMMC
- User Modules
 - ✓ PWM_ADC_SYN_8323.c:main
 - ✓ Events.c:event
- Generated Modules
- External Modules
- Documentation
- ✗ PESL

Bean Items Visibility Help < > Peripheral Initialization >

Properties | Methods | Events | Comment

✓ Bean name	PwMCM1
✓ Device	PWM_A
✓ Align	edge-aligned mode
✓ Mode of PWM Pair 0	independent
✓ Mode of PWM Pair 1	independent
✓ Mode of PWM Pair 2	independent
✓ Top-Side PWM Pair 0 Polarity	Positive
✓ Top-Side PWM Pair 1 Polarity	Positive
✓ Top-Side PWM Pair 2 Polarity	Positive

Code Generation

Project: PWM_ADC_SYN_8323

Module:

Preparing for code gener. Total lines: 1

Errors: 0 Warnings: 0 Hints: 0

X Cancel

✓ Half cycle reload	no
⊕ Hardware acceleration	Disabled
✓ Dead-time	0 μs
⊕ Correction	Disabled
⊕ Interrupt service/event	Disabled
⊖ Channel 0	
✓ Channel	PWModA0
✓ PWM pin	PWMA0_GPIOA0
✓ PWM pin signal	
✓ Duty	50 %
✓ Pin PWM0 active	no
✓ Output software control	no

BASIC | ADVANCED | EXPERT Bean Level: Low Level Bean

The screenshot displays the DDFAE interface for configuring a PWM bean. The left pane shows a project tree with 'PwmM1.PwmM1' selected under 'Beans'. The main pane shows the 'Properties' tab for the 'PwmM1' bean, which is a 'Pwm_A' device. The configuration table is as follows:

Property	Value
Bean name	PwmM1
Device	Pwm_A
Align	edge-aligned mode
Mode of PWM Pair 0	independent
Mode of PWM Pair 1	independent
Mode of PWM Pair 2	independent
Top-Side PWM Pair 0 Polarity	Positive
Top-Side PWM Pair 1 Polarity	Positive
Top-Side PWM Pair 2 Polarity	Positive
Bottom-Side PWM Pair 0 Polarity	Positive
Bottom-Side PWM Pair 1 Polarity	Positive
Bottom-Side PWM Pair 2 Polarity	Positive
Write Protect	no
Output pads	Enabled
Enable in Wait mode	no
Enable in EnOnCE mode	no
Frequency	50 kHz
Output Frequency	50 kHz
Correction	Disabled
Interrupt service/event	Disabled
Channel 0	
Channel	PwModA0
PWM pin	PwMA0_GPIOA0
PWM pin signal	
Duty	50 %
Pin PWM0 active	no
Output software control	no

An overlay window titled 'Building PWM_ADC_SYN_8323.mcp' shows the build progress:

File	Task	File Count	Line Count
Totals:			12551

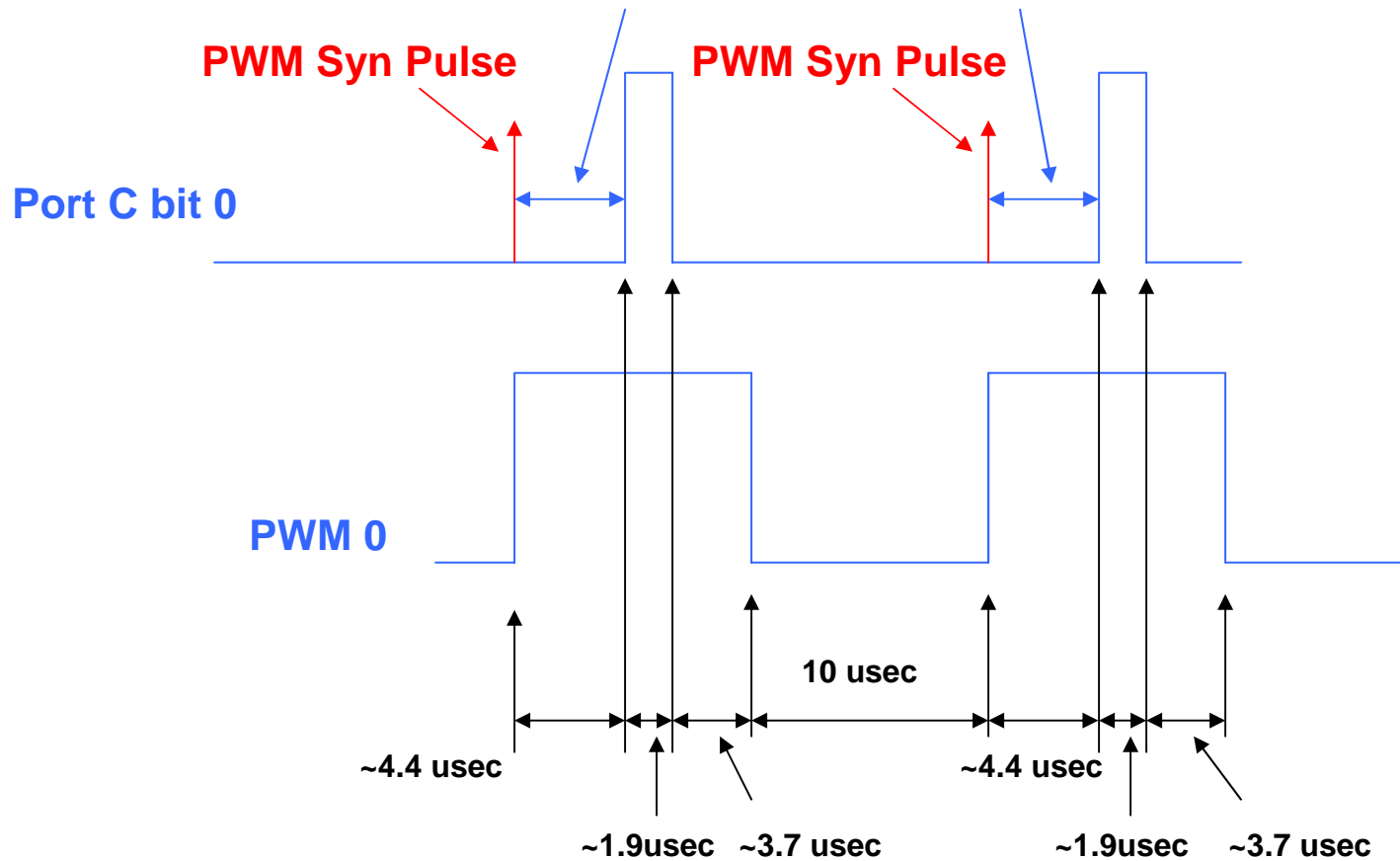
At the bottom, the 'BASIC' tab is selected, and the 'Bean Level' is set to 'Low Level Bean'.

The screenshot shows the IDE interface for the project `PWM_ADC_SYN_8323.mcp`. On the left, a tree view shows the project structure, including configurations, CPUs, beans, and user modules. The `PwMCP1.PwMMC` bean is selected. The main window displays the `sdm_pROM_xRAM.elf (Thread 0x0)` bean's properties, methods, and events. The `Run` button is highlighted with a red circle. A red arrow points from this button to a callout box containing the text **❖ Click Run**. Below the main window, a source code window shows the message: `Program "sdm_pROM_xRAM.elf" is executing. Choose Break from the Debug menu to stop it.` At the bottom, a table displays the bean's configuration parameters:

Property	Value	Additional Info
Pwm pin signal	50 %	high: 10µs
Duty	50 %	
Pin PWM0 active	no	
Output software control	no	

Result 2 :

In this example (PWM- Edge Aligned mode):
 ADC conversion time +
 timer C channel 2 delay \approx 4.4 usec



Summary

Hands-On Training



Summary

- ❖ Understand the hardware and software support available for the 56800E Hybrid Controller product line.
- ❖ Demonstrated the ease of developing applications using CodeWarrior development tools with Processor Expert™ technology for PWM_ADC_SYN conversion.

56800E



Thank You!!!