M68360QUADS-040

User's Manual

ISSUE 1.0 - DRAFT

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1 - GENERAL INFORMATION

1.1 INTRODUCTION

This document describes the evaluation board for the MC68EC040 - MC68360 combination called the M68360QUADS-040. This board is constructed with an MC68EC040 as the master processor and a MC68360 (QUICC) as a slave in MC68EC040 companion mode. The purpose of this board is to evaluate the performance of the above combination, rather than serve as a development system. .

1.2 RELATED DOCUMENTATION

- MC68360 User's Manual.
- MC68EC040 User's Manual.
- MC68LC040 User's Manual.
- ADI board specification.

1.3 ABBREVIATIONS USED IN THE DOCUMENT

- QUADS - Application Development System for the QUICC device.
- ADI - Application Development Interface.
- UART - Universal Asynchronous Receiver/Transmitter.
- SIMM - Single In-line Memory Module.
- AUI - Attachment Unit Interface.
- SPI - Serial Peripheral Interface
- NMI - Non Maskable Interrupt
- EEST - Enhanced Ethernet Serial Transceiver the MC68160
- SIA - Serial Interface Adapter, the Am7992
- TP - Twisted Pair
- nsec - nano second

1.4 SPECIFICATIONS

The M68360QUADS-040 specifications are given in TABLE 1-1. Paragraph 1.5 details the cooling requirements.

TABLE 1-1. M68360QUADS-040 Specifications

CHARACTERISTICS	SPECIFICATIONS
Power requirements (no other boards attached)	+5Vdc @ 3.5 A (typical), 5 A (maximum) +12Vdc - Determined by the Ethernet network[a]
Microprocessor	XC68EC/LC040FE33[b] @ 25 MHz

TABLE 1-1. M68360QUADS-040 Specifications

CHARACTERISTICS	SPECIFICATIONS
Addressing Total address range: on-board - Off-board - Flash Memory Dynamic RAM EEPROM	 256 MBytes[c] 4 GigaBytes 512 KByte, 32 bits wide expandable to 2 MBytes 1 MByte, 36 bits wide SIMM (32 bit data, 4 bit parity) option to use higher density SIMM, up to 8 MByte 256 Byte, serial EEPROM
Operating temperature	0°C - 30°C
Storage temperature	-25°C to 85°C
Relative humidity	5% to 90% (non-condensing)
Dimensions: Height Depth Thickness	 9.173 inches (233 mm) 6.3 inches (160 mm) 0.063 inches (1.6 mm)

a. The 12V supply is not used on the board, it is connected only to the Ethernet AUI connectors P3 & P5 to be supplied to the network. Therefore, the power consumption of that supply is independent of the M68360QUADS-040.
b. 33 MHz components are used to get better s.u. timing between the QUICC & the EC040.
c. Since A28 to A31 of the slave QUICC are used as Write-Enable signals, the on-board addressing space is reduced to 256 MBytes.

1.5 COOLING REQUIREMENTS

The M68360QUADS-040 is specified, designed, and tested to operate reliably with an ambient air temperature range from 0°C to 30°C. This, due to the overheating problems of the XC68EC040 as the 68EC040 **must** have a heat-sink attached to it for proper operation at room[1] temperature. Therefore, the ambient temperature of operation for the M68360QUADS-040 **should never exceed 30°C**.

1. If no heat sink is attached to the 68EC040, maximum ambient temperature allowed @ 25 Mhz is -4 °C !!!

1.6 FEATURES

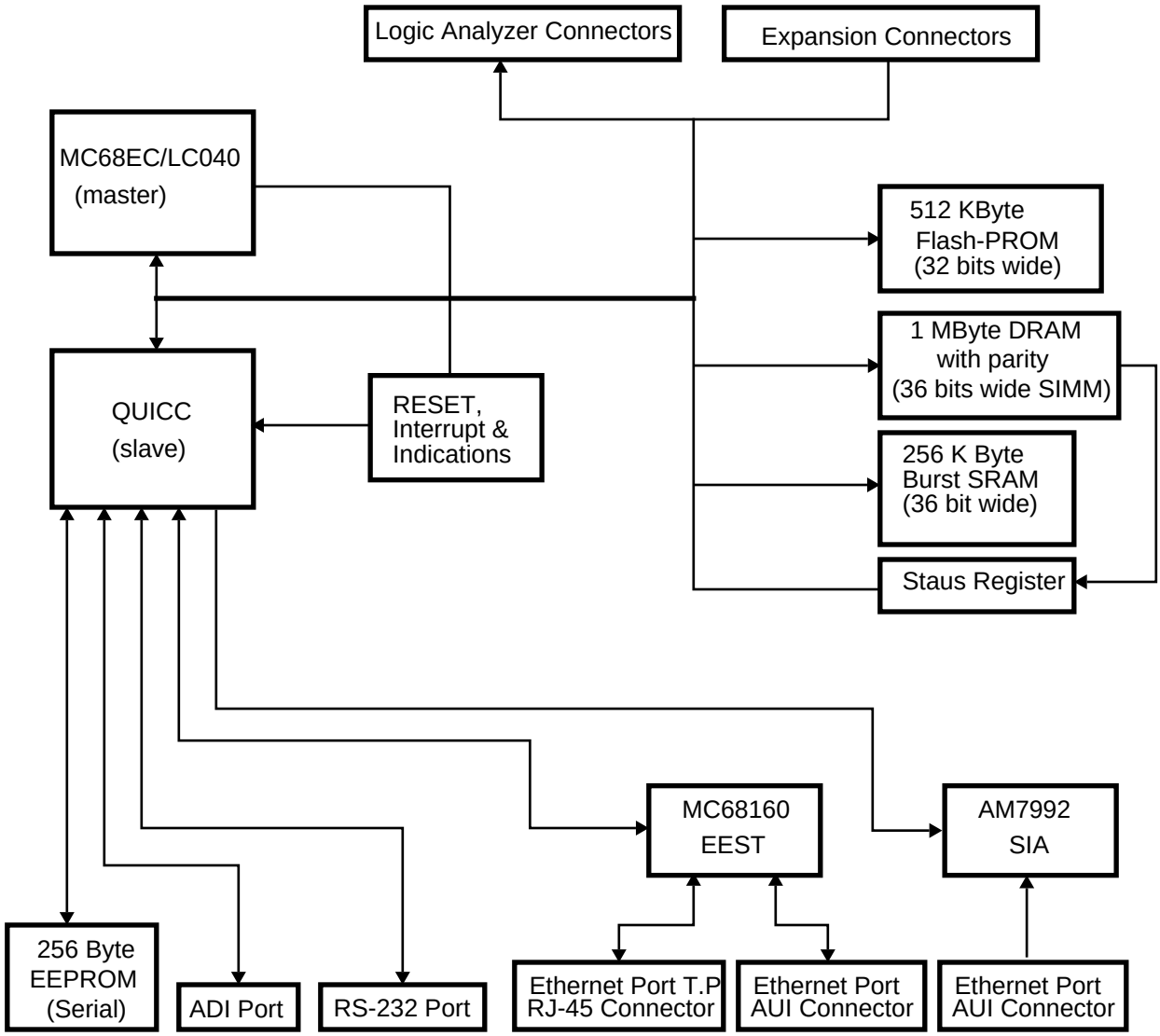
Following are the main features of the M68360QUADS-040:

- ❏ Master MC68EC040FE33 with 32-bit address bus, 32 bit data bus, instruction and data caches.
- ❏ Supports also MC68LC040.
- ❏ 1 Mbyte Dynamic RAM, 60 nsec access time, 36 bits wide (data and parity) SIMM, accessed with 3,2,2,2 clock cycles. Support for dram SIMMs upto 8 Mbyte with automatic size and speed detection.
- ❏ 512 Kbyte Flash PROM, On-board (5V) programmable, individual sector protection, 32 bits wide, 120 nsec access time, support is given up to 2 Mbyte.
- ❏ 128K byte synchronous bursting sram, 36 bits wide, 12 nsec access time. Accessed with 3,1,1,1 clock cycles. Option for additional 128K Byte identical bank.
- ❏ 256 byte serial EEPROM, accessed by the SPI port.
- ❏ Application Development Interface (ADI) port via 37 pin D-type connector.
- ❏ Serial RS-232 port for terminal or host computer connection via 9 pin Dtype connector.
- ❏ **Two** Ethernet ports:
    1. The first using Motorola's MC68160 (EEST) with both AUI and TP connectors.
    2. The second using AMD's Am7992 (SIA) with AUI connector.
- ❏ SCC2 (connected to the second Ethernet port) may be used for other purpose, by removing the SIA from its socket.
- ❏ Expansion and Logic Analyzer connectors for both slave QUICC and MC68EC040.
- ❏ Slave QUICC (core disabled in 68EC040 companion mode) providing the following functions:
    1. DRAM Controller
    2. Chip Select, TA~ and DSACK~ generator.
    3. Parallel port (ADI) controller.
    4. UART for terminal or host computer connection.

5. Dual-port Ethernet controller.

- ❏ VMEbus double-height board dimensions
- ❏ SOFT-RESET, HARD-RESET and ABORT switches.
- ❏ Status LEDs for power, EC040 run, DMA run, HALT and Ethernet signals.
- ❏ Single +5Vdc power supply.

1.7 HARDWARE BLOCK DIAGRAM



2 - Hardware Preparation and Installation

2.1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the M68360QUADS-040.

2.2 UNPACKING INSTRUCTIONS

NOTE

If the shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

CAUTION

AVOID TOUCHING AREAS OF INTEGRATED CIRCUITRY; STATIC DISCHARGE CAN DAMAGE CIRCUITS.

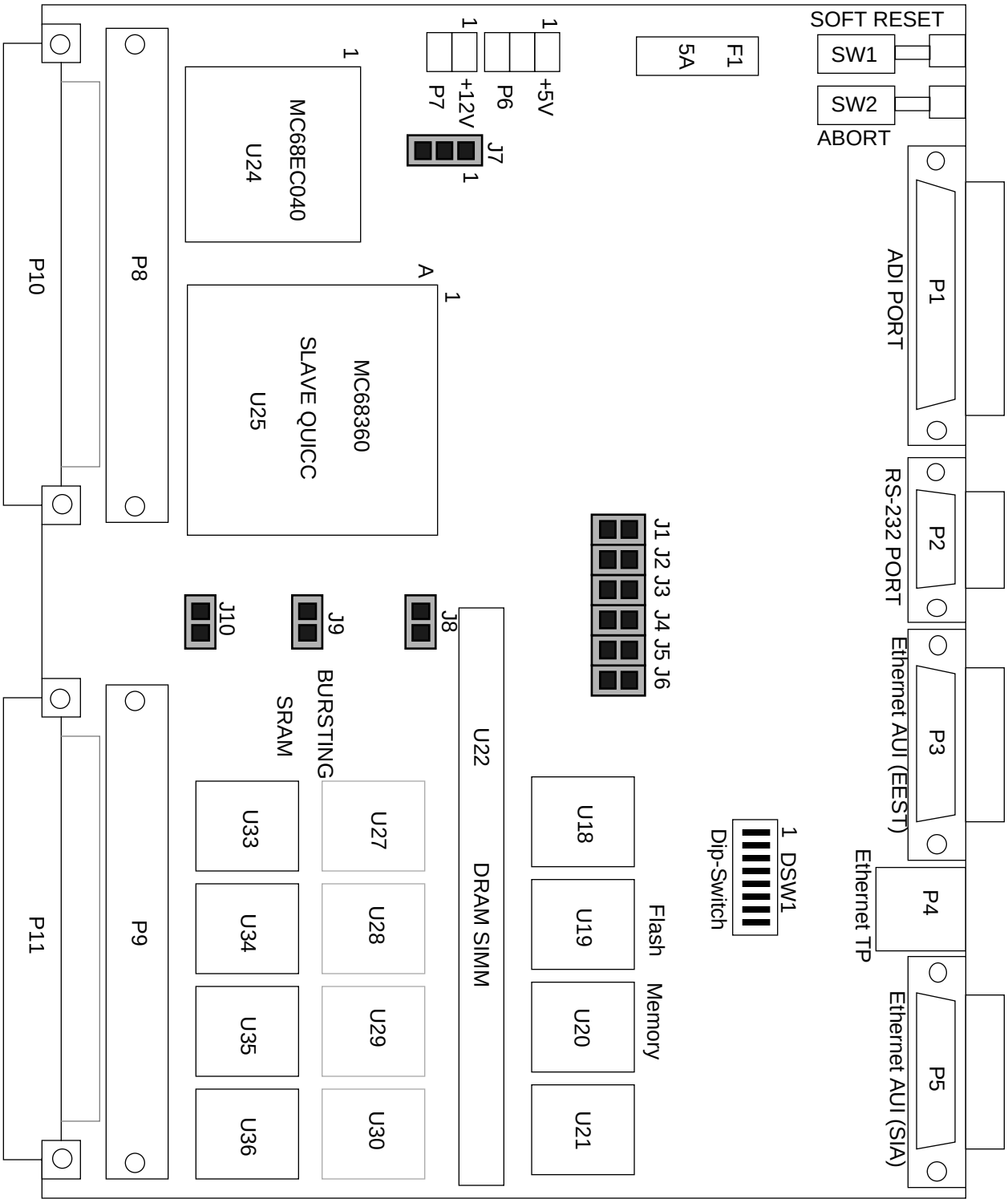
2.3 HARDWARE PREPARATION

To select the desired configuration and ensure proper operation of the M68360QUADS-040 board, changes of the Dip-Switch settings may be required before installation. The location of the switches, LEDs, Dip-Switches, and connectors is illustrated in FIGURE 2-1. The board has been factory tested and is shipped with Dip-Switch settings as described in the following paragraphs. Parameters can be changed for the following conditions:

- ADI port address
- Enable/Disable MC68EC040's caches (both Instruction and Data)
- Eanble / Disable MC68LC040's Memory Management Unit[1]
- Hardware BreakPoint logic operation
- Parity Error Interrupt generation
- Arbitration Configuration
- EEST Twisted Pair Interface configuration
- User Selectable Options

1. If a MC68**LC**040 device is installed.

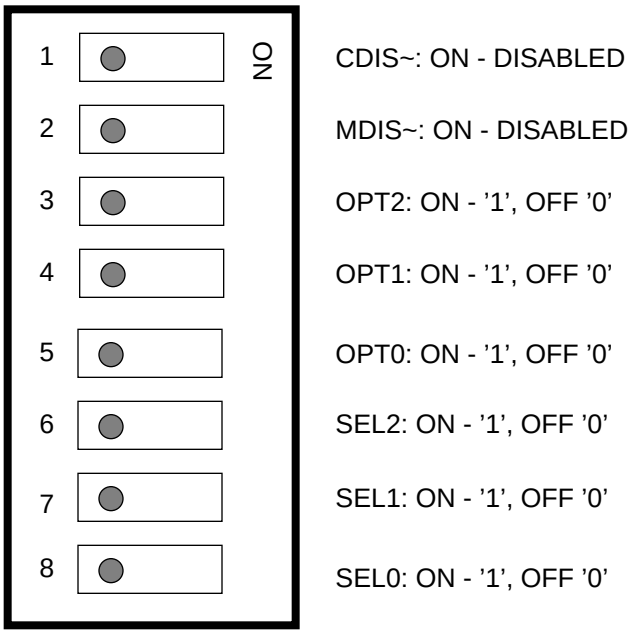
FIGURE 2-1 M68360QUADS Location diagram



2.3.1 ADI Port Address Selection

The M68360QUADS-040 can have eight possible slave addresses set for its ADI port, enabling up to eight M68360QUADS-040 boards to be connected to the same ADI board in the host computer. The selection of the slave address is done by setting switches 6, 7 & 8 in the Dip-Switch. Switch 6 stands for the most-significant bit of the address and switch 8 stands for the least-significant bit. If the switch is in the 'ON' state, it stands for logical '1'. In FIGURE 2-2 DSW1 is shown to be configured to address '0'.

FIGURE 2-2 Configuration Dip-Switch - DSW1



DSW1

Table 2-1 describes the switch settings for each slave address:

Table 2-1 ADI Address Selection

ADDRESS	Switch 6	Switch 7	Switch 8
0	OFF	OFF	OFF
1	OFF	OFF	ON
2	OFF	ON	OFF
3	OFF	ON	ON
4	ON	OFF	OFF
5	ON	OFF	ON
6	ON	ON	OFF
7	ON	ON	ON

2.3.2 Caches Enable / Disable

Switch #1 on DSW1 enables / disables the MC68EC040 caches. When it is in 'OFF' position (FACTORY SETUP) both caches may be enabled by software. When it is in 'ON' position, both instruction and data caches can not be enabled by software.

2.3.3 MMU Enable / Disable

Switch #2 on DSW1 enables / disables the Memory Management Unit, which exists only on a MC68LC040 processor. When a MC68EC040 is installed, this switch has no effect. When switch #2 is in 'OFF' position the MMU (if exists) is enabled, when in 'ON' position - the MMU (if exists) is disabled.

Hardware Break Point Logic Configuration

The Hardware BreakPoint Out signal (BKPTO~) of the QUICC may be used for 2 purposes:

1. Generating level 7 interrupt (NMI) to the EC040, serving its original purpose.
2. A caching shield logic, to avoid redundant caching of data into the data cache

The selection between the above is done via jumper J7. When pins 1 and 2 of J7 are connected, the breakpoint logic functions in its original goal. When pins 2 and 3 of J7 are connected, the breakpoint logic serves a data caching shield.

J7 is configured at factory to position 1-2.

2.3.4 Parity Error Interrupt Generation

When the QUICC's parity logic is operating, i.e., parity is generated and checked by the memory controller, it is possible to generate level 5 interrupt to the EC040 when parity error is encountered. When jumper J8 is connected, the QUICC's Parity Error line (PERR~) is connected to the QUICC's level 5 interrupt request line - IRQ5~ to generate level 5 interrupt upon parity error occurrence. When J8 is disconnected, no parity error interrupt is generated.

J8 is disconnected at factory.

2.3.5 Arbitration Configuration

To allow for external master to be connected off-board, the arbitration scheme must be changed.

Jumper J9 connects between the EC040 Bus Request Output (BR040~) and QUICC's Bus Request Input (BRQ~), while J10 connects between the QUICC's Bus Grant Output (BGQ~) and the EC040's Bus Grant Input (BG040~). When BOTH J9 and J10 are connected, arbitration is done by the QUICC's arbiter. When BOTH J9 and J10 are DISCONNECTED, an external arbiter may be introduced via the expansion connectors.

BOTH J9 & J10 are connected at factory.

2.3.6 EEST Configuration

The configuration of the MC68160 - EEST is determined by the position of jumpers J1 to J6. For the concise description of the role of each jumper see section 3.2.4 on page 17. The EEST is factory set to AUI interface, i.e., jumpers J1, J2 & J6 connected and J2 - J5 disconnected.

2.3.7 User Selectable Options

Since the state of switches #3 to #5 is readable to software via the board status-register, it is possible to use them for software configuration, modes' selection, etc. For further information on that subject see 4.11.5 on page 35.

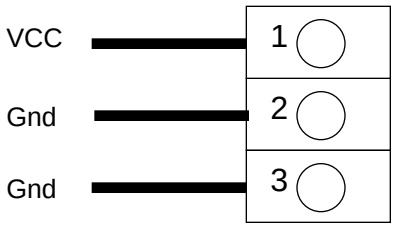
2.4 INSTALLATION INSTRUCTIONS

When the M68360QUADS-040 has been configured as desired by the user, it can be installed according to the required working environment as follows:

2.4.1 +5V Power Supply Connection

The M68360QUADS-040 requires +5 Vdc @ 5 A max, power supply for operation. Connect the +5V power supply to connector P11 as shown below:

FIGURE 2-3 P6: +5V Power Connector



P5 is a 3 terminal block power connector with power plug. The plug is designed to accept 14 to 22 AWG wires. It is recommended to use 14 to 18 AWG wires. To provide solid ground, two Gnd terminals are supplied. It is recommended to connect both Gnd wires to the common of the power supply, while VCC is connected with a single wire.

NOTE

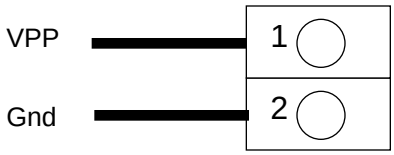
Since hardware applications can be connected to the M68360QUADS-040 using the expansion connectors P8 and P10, the additional power consumption should be taken into consideration when a power supply is connected to the M68360QUADS-040.

2.4.2 P7: +12V Power Supply Connection

The M68360QUADS-040 requires +12 Vdc @ 1 A max, power supply for the Ethernet AUI port. The M68360QUADS-040 can work properly without the +12V power supply, if the AUI port is not in use or if the AUI port is used with an AUI hub that does not require 12 V to be provided by the network termination equipment.

Connect the +12V power supply to connector P6 as shown below:

FIGURE 2-4 P6: +12V Power Connector



P6 is a 2 terminal block power connector with power plug. The plug is designed to accept 14 to 22 AWG wires. It is recommended to use 14 to 18 AWG wires.

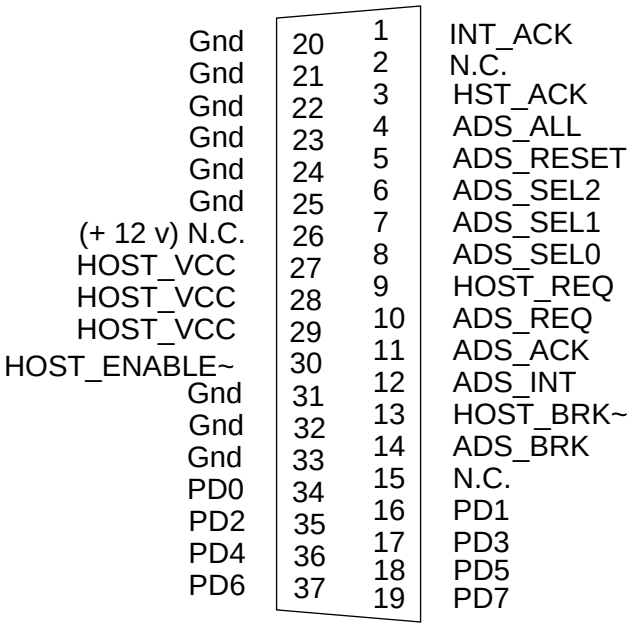
2.4.3 ADI Installation

For ADI installation on various host computers, refer to APPENDIX A - on page 51.

2.4.4 Host computer to M68360QUADS-040 Connection

The M68360QUADS-040 ADI interface connector, P1, is a 37 pin, male, D type connector. The connection between the M68360QUADS-040 and the host computer is by a 37 line flat cable, supplied with the ADI board. FIGURE 2-5 below shows the pin configuration of the connector.

FIGURE 2-5 P1 - ADI Port Connector

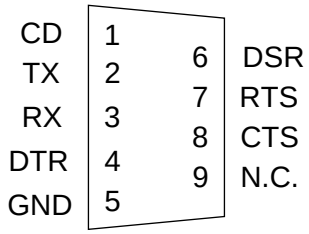


NOTE: Pin 26 on the ADI is connected to +12 v power supply, but it is not used in the M68360QUADS-040.

2.4.5 Terminal to M68360QUADS-040 RS-232 Connection

In the stand-alone operation mode, a VT100 compatible terminal should be connected to the RS-232 connector P2. The RS-232 connector is a 9 pin, female, D-type connector as shown in FIGURE 2-6.

FIGURE 2-6 P2 - RS-232 Serial Port Connector



NOTE: The RTS line (pin 7) is not connected in the M68360QUADS-040.

3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides necessary information to use the M68360QUADS-040 in host-controlled and stand-alone configurations. This includes controls and indicators, memory map details, and software initialization of the board.

3.2 CONTROLS AND INDICATORS

The M68360QUADS-040 has the following switches and indicators.

3.2.1 SOFT RESET Switch SW1

The SOFT RESET switch, SW1, resets all M68360QUADS-040 devices, and resets the EC040, and performs soft reset to the QUICC internal modules, maintaining QUICC's configuration (clocks & chip-selects) . The switch signal is debounced, and it is not possible to disable it by software.

3.2.2 ABORT Switch SW2

The ABORT switch is normally used to abort program execution by issuing a level 7 interrupt to the EC040 to return control to the QUICC040Bug. The ABORT switch signal is debounced and can not be disabled by software.

3.2.3 HARD RESET - Switches SW1 & SW2

When BOTH switches - SW1 and SW2 are depressed simultaneously, HARD reset is generated to both the EC040 and QUICC. When the QUICC is HARD reset, all its configuration is lost and has to be re-initialized.

3.2.4 EEST Configuration Jumpers J1 to J6

The following jumpers J1 to J6 are used to determine the EEST operation modes according to the description below:

3.2.4.1 TPEN Jumper - J1

The TPEN (Twisted Pair Enable) jumper, determines the interface type of the EEST ethernet port. When in position along with J2, the EEST port uses the AUI interface. When removed and J2 in position, the interface type is twisted pair.

WARNING

Whenever J2 is to be removed, J1 MUST be removed PRIOR to the removal of J2. Failure in doing so, might result in permanent damage to EEST device (U7).

3.2.4.2 APORT Jumper - J2

When the APORT (Automatic Port Selection Enable) jumper - J2 is in position, the interface type of the EEST device is selected manually via J1. When J2 is removed, the selection is done automatically according to the presence of link beats on the twisted pair receive input.

3.2.4.3 TPAPCE Jumper - J3

When the TPAPCE (Twisted Pair Automatic Polarity Correction Enable) jumper - J3 is removed, the EEST device corrects internally polarity faults and indicates them via the TPPLR led - LD6. When J3 is in position, automatic polarity correction is disabled.

3.2.4.4 TPSQEL Jumper - J4

When the TPSQEL (Twisted Pair Signal Quality Error Test Enable) jumper - J4 is in position, the collision detect circuitry test is enabled, i.e., simulated collision is generated to the EEST collision detect circuitry. The generated collision does not have any effect over the TP media. When J4 is removed, the above test is disabled.

3.2.4.5 TPFULDL Jumper - J5

When the TPFULDL (Twisted Pair Full Duplex Mode Select) jumper - J5 is in position, simultaneous receive and transmit are enabled for the TP port without collision indication. When J5 is removed, the above is disabled.

3.2.4.6 LOOP - Diagnostic Loopback Jumper - J6

When the LOOP jumper - J6 is removed, diagnostic loop-back mode is enabled for the EEST regardless of the interface type selected. In this mode, data is transmitted back into the receiver but not to the medium. When J6 is in position, the diagnostic loop-back mode is disabled.

3.2.5 Hardware Breakpoint Usage Jumper - J7

When J7 is connected between pins 1- 2, the hardware BreaKPoinT Out (BKPTO~) signal of the QUICC is connected to the interrupt logic. When breakpoint is reached, level 7 interrupt is generated to the EC040.

When J7 is connected between pins 2 - 3, BKPTO~ is connected to the Transfer cache Inhibit (TCI~) signal of the EC040. That way desired memory areas may be “shielded” and prevented from being cached. This allows for better utilization of the EC040 data cache, keeping one-time accessed data out of the data cache.

3.2.6 Parity Error Interrupt Jumper - J8

When J8 is positioned in place and parity is enabled, occurrence of parity error, causes a level 5 interrupt to the EC040 via the QUICC’s interrupt controller. When J8 is removed, parity error interrupts are disabled.

3.2.7 Bus Request Jumper - J9

When J9 is in position, the Bus Request (BR~) Output of the EC040 is connected to the Bus Request Input of the QUICC. This is the normal operating mode. When J9 is removed, the Bus Request Output of the EC040 is disconnected from the Bus Request Input of the QUICC, allowing for an external (off-board) arbiter to be located between them.

3.2.8 Bus Grant Jumper - J10

When J10 is in position the Bus Grant (BG~) Output of the QUICC is connected to the Bus Grant Input of the EC040. This is the normal operating mode. When J10 is removed, the Bus Grant Output of the QUICC is disconnected from the Bus Grant Input of the EC040, allowing for an external (off-board) arbiter to be located between them.

NOTE

For proper operation of the M68360QUADS-040, BOTH J9 and J10 must be In Position, unless an external arbiter is connected via the expansion connectors.

3.2.9 HALT Indicator - LD10

The red LED HALT indicator LD1 is lit whenever the EC040 enters the HALT state. For example, when the EC040 can not recover from an error, it frees the bus and enters the HALT state.

3.2.10 040RUN Indicator - LD8

The green LED 040RUN indicator is connected to the Transfer In Progress (TIP*) signal. It is lit if the TIP* signal is low (asserted) and it indicates the activity on the bus.

3.2.11 DMARUN Indicator - LD9

The yellow DMARUN indicator is connected to AS* signal of the slave QUICC, this to indicate bus activity of one of the QUICC's DMA channels.

3.2.12 Ethernet TX Indicator - LD3

The green LED Ethernet Transmit indicator blinks whenever the EEST is transmitting data through one of the Ethernet ports P3 or P4.

3.2.13 Ethernet RX Indicator - LD2

The green LED Ethernet Receive indicator blinks whenever the EEST is receiving data from one of the Ethernet ports P3 or P4.

3.2.14 Ethernet CLSN Indicator LD4

The red LED Ethernet Collision indicator CLSN, blinks whenever a collision is detected in the AUI P3 port or the TP P4 port, or a jabber condition is detected in TP mode.

3.2.15 Ethernet LIL Indicator - LD5

The yellow LED Ethernet Twisted Pair Link Integrity indicator - LIL, lights to indicate good link integrity on the TP P4 port. The LED is off when the link integrity fails, or when the AUI port is selected.

3.2.16 Ethernet PLR Indicator - LD6

The red LED Ethernet TP Polarity indicator - PLR, lights if the wires connected to the receiver input of TP P4 port are reversed. The LED is lit by the EEST, and remains on when the EEST has automatically corrected for the reversed wires.

3.2.17 Ethernet JABB Indicator - LD1

The red LED Ethernet TP Jabber indicator - JABB, lights whenever a jabber condition is detected on the TP P4 port.

3.2.18 POWER Indicator - LD7

The yellow POWER indicator, indicates the presence of the +5V supply at P5.

3.3 MEMORY MAP

At the beginning of each cycle, the chip-select generator of the slave QUICC determines the kind of memory cycle and which device is selected. Cycle types and address spaces are determined for EC040 cycles by the Transfer Modifier lines TM0 - TM2 and the Transfer Type lines TT0 - TT1 and by Function Codes FC0 - FC3 for QUICC's DMA cycles. The cycle types and the devices that respond are described in TABLE 3-1.

TABLE 3-1. EC040 Cycle Types and Responding Devices

TM(2:0)	TT(1:0)	Address Space	Responding Devices
000	00	Data cache Push	All
001	0X	User Data	All
010	00	User Program	All
011	00	MMU Table Search[a] Data	All

TABLE 3-1. EC040 Cycle Types and Responding Devices

TM(2:0)	TT(1:0)	Address Space	Responding Devices
100	00	MMU Table Search[b] Code	All
101	0X	Supervisor Data	All
110	00	Supervisor Program	All
111	00	Supervisor CPU	QUICC's MBAR register
111	11	Supervisor CPU	QUICC during interrupt acknowledge cycle.

a. For 68LC040 only, reserved otherwise
b. For 68LC040 only, reserved otherwise

3.3.1 Main Memory Map

The memory map of devices that respond to User Data, User Program, Supervisory Data, Supervisory Program, and DMA access is shown in TABLE 3-2.

TABLE 3-2 M68360QUADS-040 Main Memory Map

ADDESS RANGE	Accessed Device	Data Size	NOTES
00000000 - 001FFFFF	Flash PROM	32	2
00200000 - 003BFFFF	Empty Space		
003C0000 - 003CFFFF	Bursting SRAM - BANK 1[a]	32 + Parity	
003E0000 - 003EFFFF	Bursting SRAM - BANK 2	32 + Parity	
00400000 - 004FFFFF 00400000 - 005FFFFF 00400000 - 007FFFFF 00400000 - 00BFFFFF	DRAM SIMM MCM36256 DRAM SIMM MCM36512 DRAM SIMM MCM36100 DRAM SIMM MCM36200	32 + Parity	3
01210000 - 01211FFF	Slave QUICC Internal Memory	32	1
01230000 - 01231FFF	M68360QUADS-040 Status Register	16[b]	2

a. Not populated - optional.
b. Connected to D0 - D15

NOTES:

1. Refer to the MC68360 QUICC User's Manual for complete description of the QUICC internal memory.
2. The device appears repeatedly in multiples of its size. For example, the Status Register appears at memory locations 01230002, 01230006, 012300A etc...
3. The DRAM SIMM installed in the M68360QUADS-040 is MCM36256 256Kx36 bit. The user may replace the DRAM module with a higher density SIMM and increase the DRAM space up to 8 MBytes.

3.4 Programming the slave QUICC

The slave QUICC (core disabled) provides the following functions on the M68360QUADS-040:

1. DRAM Controller
2. Chip Select and DSACK~ generator.
3. Parallel port (ADI).
4. UART for terminal or host computer connection.
5. Dual Ethernet controller.
6. Interrupter
7. Serial EEPROM interface.
8. General Purpose I/O signals.

The slave QUICC internal registers must be programmed after hardware reset as described in the following paragraphs. The addresses and programming values are in hexadecimal base.

Please refer to the MC68360 QUICC User's Manual for more information.

3.4.1 Module Base Address Register

The slave QUICC's module base address register (MBAR) controls the location of its internal memory and registers and their access space. The slave QUICC MBAR resides at a fixed location in '0003FF00' in the CPU space.

The MBAR must be initialized to '00122001' to obtain the memory map as described in TABLE 3-2

3.4.2 Module Configuration Register

The module configuration register (MCR) controls the SIM60 configuration in the slave QUICC. The MCR is initialized to 60018C3F after reset.

3.4.3 CLKO Control Register

The CLKO control register (CLKOCR) controls the operation of the CLKO(1:2) pins. This register must be initialized to '03' after reset to enable CLKO2 and disable CLKO1.

3.4.4 PLL Control Register

The PLL control register (PLLCR) controls the operation of the PLL. There is no need to program the PLLCR after hard reset, because the configuration of the MODCK(0:1) pins on the QUADS determines its value. It is recommended to set the PLLWR bit to prevent accidental writing.

3.4.5 Port E Pin Assignment Register

Port E pins can be programmed by the port E pin assignment register (PEPAR). The PEPAR must be initialized to '37C0' to configure Port E of the slave QUICC as follows:

- The output of the slave QUICC interrupt request is on IOUT(0:2)~ pins.
- RAS1~ and RAS2~ double drive function is used to drive the DRAM.
- The A(31:28) pins of the slave QUICC are configured as write enables.
- The OE~/AMUX pin is configured as AMUX to drive the external multiplexers of the DRAM.
- The CAS(0:3)~ output function is used for the DRAM.
- CS7~ output function is enabled.
- AVECO~ function is chosen.

3.4.6 System Protection Control

The system protection register (SYPCR) controls the system monitors, the software watchdog, and the bus monitor timing. This register must be initialized to '34' to disable the software watchdog, disable the double

bus fault monitor and to enable the bus monitor function to respond after 1 K clock cycles in the slave QUICC.

3.4.7 Global Memory Register

The global memory register (GMR) contains selections for the memory controller of the slave QUICC. The GMR must be initialized according to the size and the access time of the DRAM SIMM installed on the M68360QUADS as follows:

- For 60, 70, 80 & 100 nsec DRAM type MCM36256 or MCM36100, the GMR must be initialized to '18A40000'.
- For 60, 70, 80 & 100 nsec DRAM type MCM36512 or MCM36200, the GMR must be initialized to '0CA40000'.

The GMR defines the following parameters:

- The DRAM refresh period is 15.36 µsec.
- The DRAM refresh cycle length 4 clocks long.
- The DRAM module port size is 32 bits.
- No extra wait between 040 dram accesses (4 phase precharge time)
- No extra wait between QUICC dram accesses (4 phase precharge time)
- Same length QUICC DRAM reads / writes
- Same length 040 SRAM reads / writes
- Parity is disabled.
- The CS~/RAS~ lines of the slave QUICC will not assert when accessing the CPU space.
- Internal address multiplexing for the DRAM is disabled.

3.4.8 Base Register 0 and Option Register 0

Base register 0 (BR0) and Option register 0 (OR0) control the operation of CS0~ pin of the slave QUICC, which serves as the Flash Prom chip-select.

BR0 is initialized to 00000001 to determine the following:

- Base address - 0.
- No burst support for EC040 access
- Parity disabled

3.4.9 Base Register 1 and Option Register 1

Base register 1 (BR1) and Option register 1 (OR1) control the operation of RAS1~ pin of the slave QUICC. This pin is connected to the RAS signal of the first bank in the DRAM module.

BR1 must be initialized to '00400021', regardless of the type and the access time of the DRAM to establish the following:

- Base address 400000.
- Burst support for EC040 access
- Parity disabled

OR1 must be initialized according to the type of the DRAM SIMM installed on the M68360QUADS-040 as follows:

- For MCM36256 or MCM36512 types:
  - For 100 nsec access time - 3FF00001
  - For 80 nsec or 70 nsec access time - 2FF00001
  - For 60 nsec access time 1FF00001
- For MCM36100 or MCM36200 types:
  - For 100 nsec access time - 3FC00001
  - For 80 nsec or 70 nsec access time - 2FC00001
  - For 60 nsec access time 1FC00001

NOTE

To ensure proper operation of the DRAM, its RAS signal should be asserted and negated 8 times after power-up. Therefore after power-up, each dram bank should be read 8 times to comply with the requirement above.

3.4.10 Base Register 2 and Option Register 2

Base register 2 (BR2) and Option register 2 (OR2) control the operation of RAS2~ pin of the slave QUICC. This pin is connected to the second[1] bank of the DRAM module.

BR2 must be initialized according to the type of DRAM SIMM installed on the M68360QUADS-040 as follows:

- For MCM36256 or MCM36100 types, BR2 is not initialized leaving RAS2 inactive.
- For MCM36512 type, BR2 must be initialized to 500021
- For MCM36200 type, BR2 must be initialized to 800021

OR2 initialization depends also of the DRAM SIMM type installed on the M68360QUADS-040 as to the following:

- For MCM36256 or MCM36512 types:
  - For 100 nsec access time - 3FF00001
  - For 80 nsec or 70 nsec access time - 2FF00001
  - For 60 nsec access time 1FF00001
- For MCM36100 or MCM36200 types:
  - For 100 nsec access time - 3FC00021
  - For 80 nsec or 70 nsec access time - 2FC00001
  - For 60 nsec access time 1FC00001

3.4.11 Base Register 3 and Option Register 3

Base register 3 (BR3) and Option register 3 (OR3) control the operation of CS3~ pin of the slave QUICC, which controls the first bank of the Bursting SRAM. BR3 must be initialized to '003C0021', and OR3 must be initialized to '1FFE0000' to obtain the memory map as described in TABLE 3-2.

3.4.12 Base Register 4 and Option Register 4

Base register 4 (BR4) and Option register 4 (OR4) control the operation of CS4~ pin of the slave QUICC, which controls the second bank of the Bursting SRAM. BR4 must be initialized to '003E0021', and OR4 must be initialized to '1FFE0000' to obtain the memory map as described in TABLE 3-2.

1. If available

3.4.13 Base Register 5 and Option Register 5

Base register 5 (BR5) and Option register 5 (OR5) control the operation of CS5~ pin of the slave QUICC, which is connected to the Status Register and to the level -7 interrupt logic. When CS5~ is asserted (for read-only) both the Status Register is read and all existing level - 7 status bits are cleared.

BR5 must be initialized to '01230003', and OR5 must be initialized to '0FFFF800' to obtain the memory map as described in TABLE 3-2.

3.4.14 Base Register 6 and Option Register 6

Since CS6~ is not being used on the M68360QUADS-040, BR6 and OR6 are not initialized by the debugger. CS6~ is available for user's applications via the expansion connector - P11.

3.4.15 Base Register 7 and Option Register 7

Since CS7~ is not being used on the M68360QUADS-040, BR7 and OR7 are not initialized by the debugger. CS7~ is available for user's applications via the expansion connector - P11.

3.4.16 Port A Open Drain Register

Port A of the slave QUICC is 16 pins port, and each pin may be configured as general purpose I/O pin or as dedicated peripheral interface pin. The port A open drain register (PAODR) configures the drivers of port A pins as open-drain or as active drivers. The PAODR must be initialized to '0000' to select the active drivers configuration.

3.4.17 Port A Data Register

The Port A data register (PADAT) can be read to check the data at the pin. If a port pin is configured as general purpose output pin, the value in the PADAT for that pin is driven onto the pin.

On the M68360QUADS-040, port A is used for serial channels as well as for ADI parallel port. PADAT must be initialized to '3F00' before configuring the other port registers.

3.4.18 Port A Data Direction Register

The port A data direction register (PADIR) has different functions according to the configuration of the port pins. If a pin is a general purpose I/O pin, the value in the PADIR for that pin defines the direction of the pin. If a pin is a dedicated peripheral interface pin, the value in the PADIR for that pin may select one of two dedicated functions of the pin. PADIR must be initialized to 'F000'.

3.4.19 Port A Pin Assignment Register

The port A pin assignment register (PAPAR) configures the function of the port pins. If the value in the PAPAR for a pin is '0', the pin is general purpose I/O, otherwise the pin is a dedicated peripheral interface pin. The PAPAR must be initialized to '0F3F'.

3.4.20 Port B Open Drain Register

Port B of the slave QUICC is a 18 bit port, and each pin may be configured as general purpose I/O pin or as dedicated peripheral interface pin. The port B open drain register (PBODR) configures the drivers of port B pins as open-drain or as active drivers. The PBODR must be initialized to '0000' to select the active drivers configuration.

3.4.21 Port B Data Register

Port B data register (PBDAT) can be read to check the data at the pin. If a port pin is configured as general purpose output pin, the value in the PBDAT for that pin is driven onto the pin. It is recommended to initialize PBDAT to '3FFFF' before configuring the other port registers.

3.4.22 Port B Data Direction Register

The port B data direction register (PBDIR) has different functions according to the configuration of the port pins. If a pin is general purpose I/O pin, the value in the PBDIR for that pin defines the direction of the pin. If a pin is dedicated peripheral interface pin, the value in the PBDIR for that pin may select one of two dedicated functions of the pin. The PBDIR must be initialized to '0000F'. Pins 10 to 17 are connected to the ADI port data bus, therefore their direction must be changed by software according to the data flow.

3.4.23 Port B Pin Assignment Register

The port B pin assignment register (PBPAR) configures the function of the port pins. If the value in the PBPAR for a pin is '0', the pin is general purpose I/O, otherwise the pin is a dedicated peripheral interface pin. The PBPAR must be initialized to '0000F'.

3.4.24 Port C Data Register

Port C of the slave QUICC is a 12 bit port, and each pin may be configured as general purpose I/O pin or as dedicated peripheral interface pin, with interrupt capability. The Port C data register (PCDAT) can be read to check the data at the pin. If a port pin is configured as general purpose output pin, the value in the PCDAT for that pin is driven onto the pin. It is recommended to initialize PCDAT to '000' before configuring the other port registers.

3.4.25 Port C Data Direction Register

The port C data direction register (PCDIR) has different functions according to the configuration of the port pins. If a pin is general purpose I/O pin, the value in the PCDIR for that pin defines the direction of the pin. If a pin is dedicated peripheral interface pin, the value in the PCDIR for that pin may select one of three dedicated functions of the pin. The PCDIR must be initialized to '000'.

3.4.26 Port C Pin Assignment Register

The port C pin assignment register (PCPAR) configures the function of the port pins, along with PCDIR and PCSO. The PCPAR must be initialized to '000'.

3.4.27 Port C Special Options Register

The port C special options register (PCSO) configures the CDx and CTSx pins. Port C can detect changes on the CTS and CD lines and assert the corresponding interrupt while the SCC simultaneously uses those lines. The PCSO must be initialized to '030'.

4 - FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter details the hardware design of the M68360QUADS-040, and describes each module in order to simplify the design.

4.2 Master MC68EC040

The CPU on the M68360QUADS-040 is a 33 MHz MC68EC040, running at 25 MHz, which uses the slave QUICC's "68EC040 companion mode" as the memory controller, the interrupt controller, bus arbiter and other system functions usually provided by dedicated logic or peripherals. Due to this "companion" mode support, the MC68EC040 interfaces gluelessly to the QUICC, while some of the QUICC pins change their function to match these of the 68EC040.

The MC68EC040 is unbuffered from the slave QUICC and the other peripherals (except for the externally multiplexed DRAM address lines). In order to demonstrate the "glueless" concept under practical test and evaluation.

Address lines A(28:31) of the slave QUICC are used in their alternate function as WE(0:3)~ to avoid having to generate them externally. As a result only 256 MByte of memory may be accessed by both the 68EC040 and the QUICC with chip-select support.

All the pins of the MC68EC040 device are available **unbuffered** to the user through the logic analyzer connectors. The user can monitor the 040 activity during its development stage.

4.2.1 RESET for the 68EC040 & the QUICC

There are four basic types of reset, regarding their source and consequence, available on the M68360QUADS-040 board:

1. QUICC Generated Reset - These types of reset are generated internally by the QUICC and include: Power-up & Software Watch-Dog. Double-Bus-Fault reset is not supported when the QUICC is in EC040 companion mode.
2. SOFT Reset - may be caused by either depressing the SOFT-RESET push-button or when the ADI-port's soft-reset signal is asserted by the remote host. When either happens, the 040 is reset while the QUICC is soft-reset, i.e., the configuration of the QUICC is unchanged, preserving the contents of the DRAM.
3. HARD-RESET - may be generated by either depressing SOFT-RESET in conjunction with the ABORT push-button or when the ADI-port's hard-reset signal is asserted by the remote host. When either happens, the 040 is reset and the QUICC is hard-reset, i.e., all the QUICC's sub-modules are reset, including configuration and clock logic.
4. RESET Instruction - When the RESET instruction is executed by the MC68EC040, RESETS* line is asserted to the QUICC, which in turn, asserts this line to complete 512 clock cycles. Execution of RESET instruction does not cause the reset of the MC68EC040 itself, therefore not interrupting the software flow.[1]

1. It was observed that the EC040 may start the next bus cycle faster than the QUICC can recover from the reset; therefore, it is recommended that the RESET instruction is loaded to an even cache-line address and executed from the cache.

4.2.2 Utilizing the MC68EC040 Data Cache

In order to achieve best performance out of the MC68EC040, both caches, Instruction and Data, are used. Since the bus interface of the EC040 and the QUICC's DMA are different, snooping is not supported on the M68360QUADS-040. Therefore, when the Data cache is enabled and used, two basic problems arise:

1. When registers or buffer descriptors are changed values by hardware or DMA are to be polled, they should not be cached, otherwise they will be polled indefinitely from the data cache, while their value may change outside, unnoticed by application software.
2. Transmit or Receive buffers should not be cached, since they are being used only once, therefore, not only caching them will not contribute to better performance, but rather will harm it, since it will keep the replacement mechanism busier.

To answer the above problems, the following measures were taken on the M68360QUADS-040:

1. The QUICC internal memory map area, including the registers and buffer-descriptors spaces, was moved to the second 16 Mbyte block[1], where it is marked as Non-cashable in the DTTR1 register of the 68EC040.
2. To allow for memory areas containing Transmit or Receive buffers to avoid being cached, the Hardware Breakpoint mechanism may be utilized as a caching shield. The BKPTO* signal of the QUICC is connected via a jumper - J7, to the TCI* signal of the EC040, which when asserted at the beginning of a data-cache line read cycle, avoids the caching of that line in the data-cache. As the BKAR and BKCR are programmed to match the address, size, and attributes of the desired memory space[2] to be shielded, BKPTO* will be asserted on the relevant access to that space and avoid redundant caching.

4.3 Interrupts on the M68360QUADS-040

In slave mode (including 68EC040 companion) the QUICC serves as an interrupt encoder for the master processor. It integrates all internal and external interrupt sources and encodes them to IOUT(0:2)~ to be connected to standard 68000 IPL~ lines. Since the parity lines are used on the M68360QUADS-040, IOUT(0:2)~ are used on the expense of IRQ1~, IRQ4~ and IRQ6~ of the slave QUICC.

There are 5 external[3] interrupt sources on the M68360QUADS-040:

1. ABORT push-button - non-maskable, level 7.
2. Host NMI via ADI port - non-maskable, level 7.
3. Hardware-Breakpoint - non-maskable, optional, level 7.
4. Parity error, generated by the slave QUICC's parity logic - maskable, level 5.
5. Host Request / Acknowledge from ADI port - maskable, level 2.

All the level - 7 interrupt source are registered and two of them are available in the status register, this to allow software to detect the source of the of the interrupt. The interrupts on levels 5 and 2 are most likely to use the autovector mechanism of the QUICC.

4.3.1 ABORT Push-button

When the ABORT push button - SW2 is depressed, a non-maskable, level-7 interrupt is generated to the EC040 by the QUICC. When the ABORT push-button is depressed in conjunction with the SOFT-RESET

---

1. There is no MMU on the MC68EC040, therefore use must be done with one of the two DTTRs - Data Transparent Translation Registers, of the EC040. These registers can address memory blocks no smaller than 16 MBytes. Since the first 16 MByte block on board, holds memories that are to be data-cached, the QUICC was moved to the second block.
2. Not bigger than 32K Bytes.
3. Off QUICC.

push-button - SW1, HARD - reset is generated to board. Indication for the occurrence of that interrupt is concluded from the absence of both Host NMI and Hardware-Breakpoint indications in the status register.

4.3.2 Host - NMI

When a host is connected to the M68360QUADS-040 via the ADI port, it is possible for the host to generate a level - 7 interrupt via the ADI port, allowing for full[1] remote control over the board. To generate that interrupt, the host computer needs to assert and deassert the ADS_BRK signal of the ADI port. That interrupt is indicated via the H_NMI~ bit in the status register.

4.3.3 Hardware-Breakpoint Interrupt[2]

To support Hardware-Breakpoint, the BKPTO~ signal of the QUICC may be connected via jumper - J7 (1-2) to the level - 7 interrupt generation logic. When a Hardware Breakpoint is reached and J7 pins 2-3 are connected, a level - 7 interrupt is generated,and the indication is shown by the BKINT~ bit in the status register.

4.3.4 Parity[3] Error Interrupt

It is possible to generate a level - 5, maskable interrupt to the EC040 in case a parity error occurs during dram or bursting sram read. The QUICC's PERR~ (Parity Error) signal is connected to IRQ5~ signal of the QUICC.

4.3.5 Host Request / Acknowledge Interrupt[4]

To support interrup based handshaking with the host computer via the ADI port, it is possible for the assertion (by the host computer) of either HOST_REQ or HOST_ACK signals, when the board is selected, to generate a level 2, maskable interrupt to the EC040.

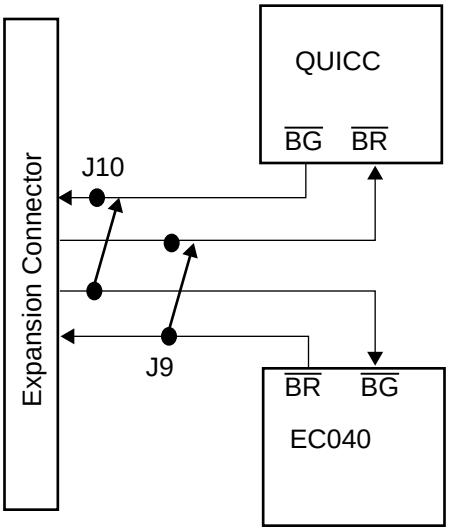
4.4 Bus Arbitration

When a QUICC is configured in 68EC040 companion mode, its arbiter lines do not change function and the QUICC remainsbus arbiter (rather than a requester as in other slave modes). The 68EC040 arbitration lines are connected gluelessly to those of the QUICC. The LOCK~ signal of the 68EC040 is connected also to support indivisible bus cycles.

When the QUICC doesn't need the bus, it asserts BG~ constantly for the 040 to reduce arbitration overhead time for the 040, and therefore improving its performance. To support external master connection via the expansion connectors, the BR* BG* pairs are connected to each other via jumpers and appear also at the expansion connector, thus enabling an external arbiter to be located off-board. The arbitration logic scheme is demonstrated in FIGURE 4-1 on page 29.

1. In conjunction with remote SOFT & HARD resets capability.
2. It is important to remember that the Hardware-Breakpoint and the memory caching shield operation is MUTUALY EXCLUSIVE, that is, when the data-caching shield is operating (J7 2-3) the Hardware - Breakpoint use is not available and vice-versa.
3. Parity in not enabled during normal operation. It is up to the users to enable the parity logic to their desire.
4. During normal operation these interrupts are masked and a polling handshake takes place between the board and the host computer.

FIGURE 4-1 Arbitration Scheme:



Since the level of priority associated with the BR~ input is lower (8) than the SDMA's, no use is done with the BCLRO~ signal of the QUICC is not used. In sake of simplicity, no use is done with the IPEND~ is not used as a BCLI~ for the QUICC.

4.5 System Utilities

The slave QUICC provides the M68360QUADS-040 with the following system utilities, usually provided by external logic:

1. Breakpoint generation
2. Bus Monitor (also known as hardware watch-dog)
3. Spurious Interrupt Monitor
4. Software watch-dog
5. Periodic Interval Timer (also known as real-time-clock or tic-timer)

4.5.1 Breakpoints Generator

The QUICC may be used as a hardware breakpoint generator for the 68EC040. When the 68EC040 initiates a bus cycle by asserting TS~, the breakpoint logic compares the cycle's address to the address in the BKAR and to the access attributes in the BKCR. If there is a match, the BKPTO* signal is asserted by the QUICC. Since TS~ is asserted only at the beginning of the cycle, no address comparison is done for the rest of the access (burst access). The BKPTO* of the slave QUICC is wired via a jumper to generate a non-maskable interrupt on level 7.

If the EC040 performs a breakpoint instruction, the QUICC will not respond, letting the bus monitor terminate the cycle with TEA~.

4.5.2 Bus Monitor

The QUICC monitors for unterminated bus cycles, performed either by the 68EC040 or by the QUICC's internal masters. If a bus cycle fails to terminate with TA~ or TEA~ (DSACK~ or BERR) during a programmable period of time, the bus monitor terminates the cycle, by asserting TEA~ for the EC040 (or BERR~ for an internal master). Upon reset, the bus monitor is initialized to expire after 1K system clocks (CLKO1 clocks).

4.5.3 Spurious Interrupt Monitor

In EC040 mode, the QUICC monitors for spurious interrupt cycles performed by the EC040. This support is limited to those levels supported internally by the QUICC interrupter, i.e., only on those levels used by the CPM and the SIM60. If such a condition occurs, the QUICC terminates the cycle with TEA~.

4.5.4 software Watch-Dog

The software watch-dog on the M68360QUADS-040 may be programmed to generate a system reset when an application software is stuck in an endless loop. The software watch dog is disabled after reset and it may be enabled if the users want it enabled.

4.5.5 Periodic Interval Timer - PIT

If desired, the QUICC's PIT may be used to generate periodic interrupt in favor of real-time kernel. The PIT is disabled after reset.

4.6 Clock Generator

There are two main clocks available on the M68360QUADS-040:

1. 25Mhz system clock, which supplies BCLK for the EC040 and EXTAL clock input for the QUICC. This clock is supplied via four buffers to the different board area.
2. 50Mhz clock, which supplies the PCLK for the EC040 and is generated using the QUICC's PLL via CLKO2. During reset, CLKO2 reflects the state of the EXTAL input and becomes 2 X EXTAL after the QUICC's PLL is locked.

The 25Mhz clock is generated by an external crystal oscillator (U37) which is divided by 2 to yield a 50% duty cycle (U39) which is buffered (U38) and distributed to all board consumers.

4.7 Flash PROM

The Flash PROM on the M68360QUADS-040 is constructed of four Am29F010-12 devices providing a total of 512 KBytes. The Am29F010 is a 5 V programmable, with 8 - sectors' protection capability, 120 nsec access time, 128 KByte device, accessed with 3 wait-states @ 25 Mhz system clock. An option is made to use bigger Flash PROMs up to the Am29F040. The Flash PROM is used to store the resident debugger and other necessary drivers, which reside in 4 protected sectors. The rest of the sectors are available for on-board user programming. The Flash PROM is selected using the Global CS (CS0) of the slave QUICC.

To program the Flash PROM, the program (and / or data) should be downloaded to the DRAM (or BSRAM) and then programmed into the Flash Prom by a dedicated debugger command. If a dedicated programming routine is to be used it is important to remember that the Flash Prom can NOT be accessed normally during the programming process. Therefore, the programming routine should reside in another memory.

4.8 Bursting SRAM

The bursting sram on the M68360QUADS-040 is constructed of two[1] banks, each containing 4 MCM62940AFN12 32K X 9SRAM chips. This RAM provides fast access times for the EC040: 3,1,1,1 clock cycles for burst access and 3 clock cycles for normal access.

If desired, the volume of the BSRAM may be doubled, this, by soldering identical memory components to the empty locations designated by U27, U28, U29 & U30.

1. One populated and the other optional

WARNNING

Additional BSRAM components should be soldered with care. Otherwise permanent damage may be inflicted to the M68360QUADS-040.

The bursting sram may be accessed by both the EC040 and the DMA, however access by the QUICC must be **EVEN WORD** aligned.

4.9 EEPROM

The EEPROM used in the M68360QUADS-040 is Motorola MCM2814, 256 byte serial EEPROM (U14). The slave QUICC provides 4 signals to control accesses to the EEPROM.

The MCM2814 has internal hardware protection against inadvertent writes to the EEPROM that might happen at power up or power down time.

4.10 DRAM

The M68360QUADS-040 is supplied with 1 Mbyte of Dynamic RAM, which is implemented by the MCM36256S-60 DRAM module. The module is a 72 lead SIMM, 60 nsec access time, organized as 256K x 36 bit for data and parity signals, and is accessed with 3,2,2,2 clock cycles during burst cycles and 3 clocks during normal read / write access.

It is possible to replace the supplied DRAM SIMM with a higher density module in order to increase the DRAM memory space up to 8 Mbyte. The higher density modules may require using RAS1 and RAS2 signals of the slave QUICC if they are organized as two memory banks. After hard / power-up reset, the status register is read to detect the kind of dram SIMM inserted, in order to initialize the CS registers with the correct data regarding the dram's size and delay.

The DRAM is controlled by the slave QUICC device, using its DRAM controller function for normal accesses, burst mode accesses, and refresh accesses. The DRAM can be accessed by the master 68EC040 and the slave QUICC's DMA channels.

NOTE:

Due to problems of implementation, the QUICC's support for 68EC040's burst mode inhibits the support for internal page mode. Therefore, the I/SDMAs access the DRAM using normal access pattern only.

4.11 Slave QUICC

During normal operation, the CPU of the slave QUICC is disabled, and the device is used to implement the following functions on the ADS:

1. DRAM Controller
2. Chip Select TA~ and DSACK~ generator.
3. Parallel port (ADI) controller.
4. UART for terminal or host computer connection.
5. Ethernet controller.

The address of the MBAR register is configured to $0033FF00.

The QUICC's peripherals (such as the IDMA and SDMA) can request the bus and become bus master, even though the CPU is disabled.

4.11.1 DRAM Controller

The slave QUICC device provides the necessary control signals for the DRAM module. The debugger on the M68360QUADS-040 reads the presence detect pins (SIMM1 - SIMM4) of the SIMM found in the status register and sets the DRAM Controller parameters according to the DRAM module's size and access time. The available combinations of the presence detect pins are described in TABLE 4-1.

TABLE 4-1. DRAM SIMM Types

SIMM(4:1)	SIMM Type	SIMM Organization	Access Time (nsec)	Control Signals
0000	MCM36100S10	1M x 36	100	RAS1
0001	MCM36512S10	512K x 36	100	RAS1, RAS2
0010	MCM36256S10	256K x 36	100	RAS1
0011	MCM36200S10	2M x 36	100	RAS1, RAS2
0100	MCM36100S80	1M x 36	80	RAS1
0101	MCM36512S80	512K x 36	80	RAS1, RAS2
0110	MCM36256S80	256K x 36	80	RAS1
0111	MCM36200S80	2M x 36	80	RAS1, RAS2
1000	MCM36100S70	1M x 36	70	RAS1
1001	MCM36512S70	512K x 36	70	RAS1, RAS2
1010	MCM36256S70	256K x 36	70	RAS1
1011	MCM36200S70	2M x 36	70	RAS1, RAS2
1100	MCM36B100ASG60	1M x 36	60	RAS1
1101	MCM36B512ASG60	512K x 36	60	RAS1, RAS2
1110	MCM36B256ASG60	256K x 36	60	RAS1
1111	MCM36B200ASG60	2M x 36	60	RAS1, RAS2

The hardware connection of the slave QUICC to the DRAM module is straight-forward. Since the slave QUICC doesn't support address multiplexing for external masters, external address multiplexers are used to drive the DRAM address lines.

4.11.2 Chip Select TA~ and DSACK~ Generator

The slave QUICC device provides the Chip Select signals for the DRAM, EPROM, bursting EPROM, and bursting SRAM on the ADS. It also generates the TA~ signal for the 68EC040 during master accesses and DSACK~ signals for the QUICC during internal accesses, this, according to the access time of the devices and the working frequency of the board. No external logic is required for the connection of the slave QUICC to the devices.

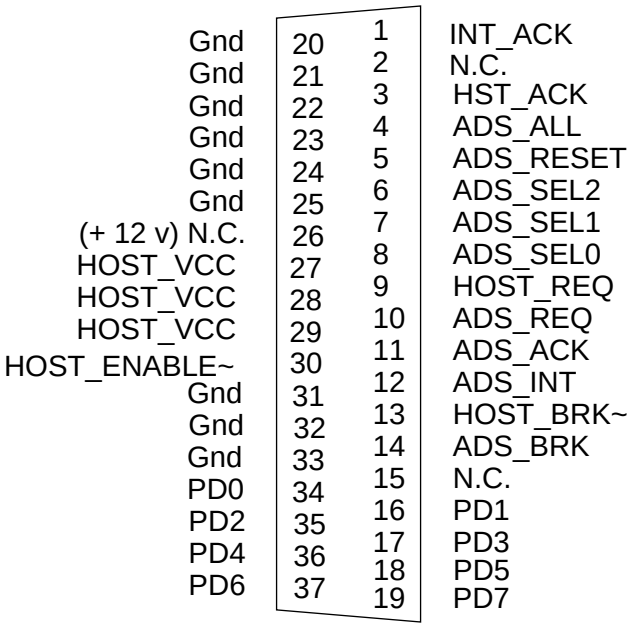
4.11.3 ADI Port

The ADI parallel port supplies the parallel link from the M68360QUADS-040 to various host computers. This port is connected via a 37 line cable to a special board called ADI (Application Development Interface) installed in the host computer. Two versions of the ADI board are available to support connection to IBM-PC/XT/AT and SUN-4 SPARC stations. It is possible to connect the M68360QUADS-040 board to these computers provided that the appropriate software drivers are installed on them.

Each M68360QUADS-040 can have 8 possible slave addresses set for its ADI port, enabling up to 8 M68360QUADS-040 boards to be connected to the same ADI board.

The ADI port connector is a 37 pin, male, D type connector. The connection between the M68360QUADS-040 and the host computer is by a 37 line flat cable, supplied with the ADI board. FIGURE 4-2 below shows the pin configuration of the connector.

FIGURE 4-2 ADI Port Connector



NOTE: Pin 26 on the ADI is connected to +12 v power supply, but it is not used in the M68360QUADS-040.

4.11.3.1 ADI Port Signal Description

The ADI port on the QUADS-040 was slightly modified to generate either hard reset or soft reset. This feature was added to comply with the QUICC's reset mechanism. The host software written for the QUADS-040 should be able to work properly with existing ADS boards, such as the M68302ADS.

In the list below, the directions 'I', 'O', and 'I/O' are relative to the M68360QUADS-040 board. (I.E. 'I' means input to the M68360QUADS-040)

NOTE:

Since the ADI was originated for the DSP56001ADS, some of its signals throughout the boards it was used with, were designated with the prefix "ADS". This convention is kept with this design also.

- ADS_SEL(0:2) - 'I'

  These three input lines determine the slave address of the M68360QUADS-040 being accessed by the host computer. Up to 8 boards can be addressed by one ADI board.

- ADS_ALL - 'I'

  This input line is used to reset or abort program execution on all M68360QUADS-040 development boards that are connected to the same ADI board.

- HOST_ENABLE~ - 'I'

  This line is always driven low by the ADI board. The M68360QUADS-040 software uses this line to determine if a host is connected to the ADI port.

- ADS_BRK - 'I'

  When a host is connected, this line is used in conjunction with the addressing lines or with the ADS_ALL line to generate a non-maskable interrupt (interrupt level 7) to the QUICC.

- ADS_RESET - 'I'

  When a host is connected, this line is used in conjunction with the addressing lines or with the ADS_ALL line to generate a reset (Hard or Soft) to the M68360QUADS-040 board.

- HOST_REQ -'I'

  This signal initiates a host to M68360QUADS-040 write cycle.

- ADS_ACK - 'O'

  This signal is the M68360QUADS-040 response to the HOST_REQ signal, indicating that the board has detected the assertion of HOST_REQ.

- ADS_REQ - 'O'

  This signal initiates an M68360QUADS-040 to host write cycle.

- HST_ACK - 'I'

  This signal serves as the host's response to the ADS_REQ signal.

- HOST_BRK~ - 'O'

  This open-collector signal generates an interrupt to the host. This signal is common to all M68360QUADS-040 boards that are connected to the same ADI.

- ADS_INT - 'O'

  This line is polled by the host computer during its interrupt acknowledge cycle to determine which M68360QUADS-040 board has generated the interrupt.

- INT_ACK - 'I'

  This line is asserted by the host at the end of its interrupt acknowledge cycle. This signal is used by the M68360QUADS-040 hardware to negate the HOST_BRK~ signal. The software in the M68360QUADS-040 must negate the ADS_INT signal upon detecting the assertion of INT_ACK to support the daisy-chain interrupt structure.

  In addition, this signal selects between the type of reset applied to the selected board(s). When '1' is driven, SOFT reset is applied and when '0' - HARD reset is applied.

- HOST_VCC - 'I' (three lines)

  These lines are power lines from the host computer. In the M68360QUADS-040, these lines are used by the software to determine if the host computer is powered on.

- PD(0:7) - 'I/O'

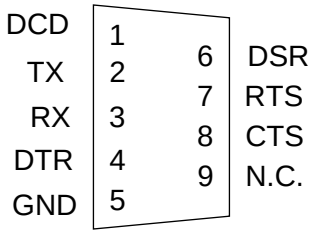
  These eight I/O lines are the parallel data bus. This bus is used to transmit and receive data from the host computer.

4.11.4 RS-232 Serial Port

The serial port is provided by one of the slave QUICC serial channels. The M68360QUADS-040 can be connected to a VT100 compatible terminal or to a host computer through the serial port.

The RS-232 serial port connector is a 9 pin, male, D-type connector as shown in FIGURE 2-6.

FIGURE 4-3 RS-232 Serial Port Connector



4.11.4.1 RS-232 Port Signal Description

In the list below, the directions 'I', 'O', and 'I/O' are relative to the M68360QUADS-040 board. (I.E. 'I' means input to the M68360QUADS-040)

- CD (O) - Data Carrier Detect. This line is always asserted by the ADS.
- TX (O) - Transmit Data.
- RX (I) - Receive Data.
- DTR (I) - Data Terminal Ready. This signal is used by the software in the ADS to detect if a terminal is connected to the ADS board.
- DSR (O) - Data Set Ready. This line is always asserted by the ADS.
- RTS (I) - Request To Send. This line is not connected in the ADS.
- CTS (O) - Clear To Send. This line is always asserted by the ADS.

4.11.5 M68360QUADS-040 Status Register

The status register is a 16 bit wide READ ONLY register used to hold board status, level 7 interrupt source identification and an input register for ADI interface signals.

FIGURE 4-4 Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTR*	H_NMI*	INACK*	ADSSEL	HSREQ*	HSACK*	HSTEN	HSVCC*	SIMM4	SIMM3	SIMM2	SIMM1	BKINT*	OPT0*	OPT1*	OPT2*

4.11.5.1 Status Register Bits Description

- DTR* - When active '0', indicates that a terminal is connected to the serial port.
- H_NMI* - When active '0', indicates that the last level 7 interrupt (NMI) was generated from the host via the ADI port.
- INACK - When active '0', indicates that a Host Interrupt Acknowledge cycle is in progress.
- ADSSEL - When active '1', indicates that the board is selected by the ADI port.
- HSREQ* - When active '0', indicates that the host request to write a data byte to the board via the ADI port.
- HSACK* - When active '0', indicates that the host has successfully read a byte of data written to it by the board via the ADI port.
- HSTEN - When active '1', indicates that the board is connected to an ADI port.
- HSVCC* - When active '0', indicates that the host computer is alive (not turned off).

- SIMM4 to SIMM1 - These four bits, encode the data identifying the DRAM SIMM connected to the M68360QUADS-040. For the various DRAM types supported, refer to TABLE 4-1.
- BKINT* - When active '0', indicates that the last level 7 interrupt (NMI) was generated by the Hardware Breakpoint logic.
- OPT0* - When active '1', indicates that switch #5 in DSW1 is in ON position
- OPT1* - When active '1', indicates that switch #4 in DSW1 is in ON position
- OPT2* - When active '1', indicates that switch #3 in DSW1 is in ON position

4.11.6 Ethernet Controller

There are TWO ethernet ports on the M68360QUADS-040 implemented via SCC1 and SCC2 of the QUICC.

The first Ethernet port is implemented by connecting SCC1 to Motorola's MC68160 EEST device. The MC68160 provides two Ethernet interfaces: AUI (P3) and Twisted-Pair (P4). The connection between the MC68160 and the QUICC is straight forward, and does not require external glue logic.

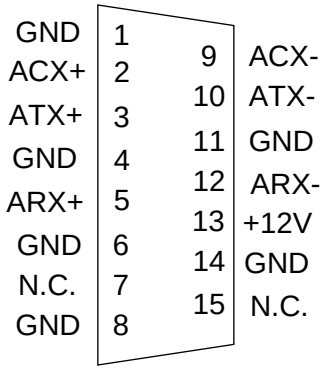
The second Ethernet port is implemented by connecting SCC2 to AMD's SIA (Am7992) device. In this case however, only AUI port is implemented via P5.

To support other uses of SCC2, it's signals are available also at the expansion connectors and the SIA (U4) is mounted on a socket. That way the SIA can be removed freeing SCC2 signals for other use via the expansion connector - P11.

4.11.6.1 Ethernet AUI Ports Signal Description

The AUI port connectors P3 and P5 are 15 pin, female, D-type connectors as shown in FIGURE 2-6.

FIGURE 4-5 Ethernet AUI Port Connector



The list below describes the port signals. The directions 'I', 'O', and 'I/O' are relative to the M68360QUADS-040 board. (I.E. 'I' means input to the M68360QUADS-040)

- ACX+ (I) - Collision Input (positive).
- ATX+ (O) - Transmit Data (positive).
- ARX+ (I) - Receive Data (positive).
- ACX- (I) - Collision Input (negative).
- ATX- (O) - Transmit Data (negative).
- ARX- (I) - Receive Data (negative).

- +12V (O) - +12V power supply from the M68360QUADS-040.

4.11.6.2 Ethernet Twisted-Pair Port Signal Description

The twisted-pair port connector P4 is a 8 pin, RJ-45 connector as shown in FIGURE 2-6.

FIGURE 4-6 Ethernet Twisted-Pair Port Connector

TPTX+	1
TPTX-	2
TPRX+	3
N.C.	4
N.C.	5
TPRX-	6
N.C.	7
N.C.	8

The list below describes the port signals. The directions 'I', 'O', and 'I/O' are relative to the M68360QUADS-040 board. (I.E. 'I' means input to the M68360QUADS-040)

- TPTX+ (O) - Transmit Data (positive).
- TPTX- (O) - Transmit Data (negative).
- TPRX+ (I) - Receive Data (positive).
- TPRX- (I) - Receive Data (negative).

4.11.7 Serial EEPROM

The MCM2814 Serial EEPROM (U14) is a 256 bytes EEPROM with SPI interface. It is controlled by the SPI port of the slave QUICC (pins 1,2 and 3 of port B), and by a general purpose output pin (pin 0 of port B). The SPI port operates in master mode.

The serial EEPROM serves as non-volatile memory on the M68360QUADS-040 and may be used to store software parameters to be protected from power-downs.

4.11.8 Slave QUICC General Purpose I/O Pins

The slave QUICC has three ports, A, B, and C, whose pins can be individually configured by software to be general purpose I/O pin or dedicated peripheral function. The QUICC also has another port, E, whose pins are not general purpose I/O, but they can be configured to operate in one of two possible modes.

The following subsections describe the slave QUICC ports. Refer to 3.4 on page 21 for the required programming information.

4.11.8.1 Slave QUICC Port A

Port A is 16 pins port. TABLE 4-2 describes the configuration of port A.

TABLE 4-2 Port A Pins Description

Pin	Pin Name	Description
0	EEST RX	This pin is connected to the receive data output of the EEST. It is configured as the receive data of SCC1 in the slave QUICC.
1	EEST TX	This pin is connected to the transmit data input of the EEST. It is configured as the transmit data of SCC1 in the slave QUICC.
2	SIA RX	This pin is connected to the receive data output of the SIA. It is configured as the receive data of SCC2 in the slave QUICC.
3	SIA TX	This pin is connected to the transmit data input of the SIA. It is configured as the transmit data of SCC2 in the slave QUICC.
4	RS-232 RX	This pin is connected to the receive data output of the RS-232 transceiver U23. It is configured as the receive data of SCC3 in the slave QUICC.
5	RS-232 TX	This pin is connected to the transmit data input of the RS-232 transceiver U23. It is configured as the transmit data of SCC3 in the slave QUICC.
6	PA6	This pin is connected to The expansion connector (P11) and may be utilized for user's applications.
7	PA7	This pin is connected to The expansion connector (P11) and may be utilized for user's applications.
8	EEST TCLK	This pin is connected to the transmit clock output of the EEST. It is configured as the transmit clock of SCC1 in the slave QUICC.
9	EEST RCLK	This pin is connected to the receive clock output of the EEST. It is configured as the receive clock of SCC1 in the slave QUICC.
10	SIA TCLK	This pin is connected to the transmit clock output of the SIA. It is configured as the transmit clock of SCC2 in the slave QUICC.
11	SIA RCLK	This pin is connected to the receive clock output of the SIA. It is configured as the receive clock of SCC2 in the slave QUICC.
12	ADS ACK~	This pin is connected to the ADI port signal ADS_ACK through the buffer U1. It is configured as output pin in the slave QUICC.
13	ADS REQ~	This pin is connected to the ADI port signal ADS_REQ through the buffer U1. It is configured as output pin in the slave QUICC.
14	ADS G~	This pin is connected to the ADI port logic. It is configured as output pin in the slave QUICC, and it is used by the ADI logic to control the ADI data transceiver.
15	ADS INT~	This pin is connected to the ADI port signal ADS_INT through the buffer U1. It is configured as output pin in the slave QUICC, and it is also used by the ADI logic to interrupt the host computer.

4.11.8.2 Slave QUICC Port B

Port B is 18 pins port. TABLE 4-2 describes the configuration of port B.

TABLE 4-3 Port B Pins Description

Pin	Pin Name	Description
0	EEPROM Select	This pin is connected to the select input of the EEPROM, and it is configured as output pin in the slave QUICC.
1	EEPROM CLK	This pin is connected to the clock input of the EEPROM, and it is configured as the SPI clock of the slave QUICC.
2	EEPROM Serial In	This pin is connected to the serial data input of the EEPROM, and it is configured as the SPI MOSI of the slave QUICC.
3	EEPROM Serial Out	This pin is connected to the serial data output of the EEPROM, and it is configured as the SPI MISO of the slave QUICC.
4 - 9	PB4 - PB9	These pins are connected to the expansion connector P11 and may be used by user's applications.
10	ADI Data 0	This pin is connected to the ADI port signal PD0 through the data bus transceiver U13, and it is configured as I/O pin.
11	ADI Data 1	This pin is connected to the ADI port signal PD1 through the data bus transceiver U13, and it is configured as I/O pin.
12	ADI Data 2	This pin is connected to the ADI port signal PD2 through the data bus transceiver U13, and it is configured as I/O pin.
13	ADI Data 3	This pin is connected to the ADI port signal PD3 through the data bus transceiver U13, and it is configured as I/O pin.
14	ADI Data 4	This pin is connected to the ADI port signal PD4 through the data bus transceiver U13, and it is configured as I/O pin.
15	ADI Data 5	This pin is connected to the ADI port signal PD5 through the data bus transceiver U13, and it is configured as I/O pin.
16	ADI Data 6	This pin is connected to the ADI port signal PD6 through the data bus transceiver U13, and it is configured as I/O pin.
17	ADI Data 7	This pin is connected to the ADI port signal PD7 through the data bus transceiver U13, and it is configured as I/O pin.

4.11.8.3 Slave QUICC Port C

Port C is 12 pins port. TABLE 4-2 describes the configuration of port C.

TABLE 4-4 Port C Pins Description

Pin	Pin Name	Description
0	EEST TENA	This pin is connected to the TENA input of the EEST. It is configured as the RTS signal of SCC1 in the slave QUICC.
1	SIA TENA	This pin is connected to the TENA input of the SIA. It is configured as the RTS signal of SCC2 in the slave QUICC.
2 - 3	PC2 - PC3	These pins are connected to the expansion connector P11 and may be used by user's applications.
4	EEST CLSN	This pin is connected to the CLSN output of the EEST. It is configured as the CTS signal of SCC1 in the slave QUICC.
5	EEST RENA	This pin is connected to the RENA output of the EEST. It is configured as the CD signal of SCC1 in the slave QUICC.
6	SIA CLSN	This pin is connected to the CLSN output of the EEST. It is configured as the CTS signal of SCC2 in the slave QUICC.
7	SIA RENA	This pin is connected to the RENA output of the EEST. It is configured as the CD signal of SCC2 in the slave QUICC.
8 - 11	PC8 - PC11	These pins are connected to the expansion connector P11 and may be used by user's applications.

4.11.8.4 Slave QUICC Port E

Port E pins can be configured to operate in one of two dedicated peripheral functions. The PEPAR register configures the operation mode, as described in section 3.4.5 on page 21.

5 - SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the interconnection signals, parts list, and schematic diagrams of the M68360QUADS-040 board.

5.2 INTERCONNECT SIGNALS

The M68360QUADS-040 board interconnects with external devices through the following connectors:

- P1 is 37 pin, male D type connector, for the ADI port.
- P2 is 9 pin, female D type connector, for the RS-232 port.
- P3 is 15 pin, female D type connector, for AUI connection to the EEST Ethernet port.
- P4 is 8 pin, RJ-45 connector, for twisted-pair connection to the EEST Ethernet port.
- P5 is 15 pin, female D type connector, for AUI connection to the (AMD's) SIA Ethernet port.
- P6 is 3 pin connector for 5v power supply input: GND (x2) and +5V
- P7 is 2 pin connector for 12v power supply input: GND and +12V
- P8 and P9 are 96 pin DIN connectors for Logic analyzer connection.
- P10[1] & P11[2] are 96 pin DIN connectors for off-board hardware expansions.

5.2.1 Connector P1 Interconnect Signals

Connector P4 is a 37 pin, male D-type connector. It is the ADI port of the M68360QUADS-040. TABLE 5-1 describes the P1 connector signals.

TABLE 5-1 Connector P1 Interconnect Signals

Pin No.	Signal Name	Description
1	INT_ACK	Interrupt Acknowledge input signal from the host
2	-	Not connected
3	HST_ACK	Host Acknowledge input signal from the host
4	ADS_ALL	QUADS-040 All input signal from the host
5	ADS_RESET	QUADS-040 Reset input signal from the host
6	ADS_SEL2	QUADS-040 Select 2 input signal from the host
7	ADS_SEL1	QUADS-040 Select 1 input signal from the host
8	ADS_SEL0	QUADS-040 Select 0 input signal from the host
9	HOST_REQ	HOST Request input signal from the host
10	ADS_REQ	QUADS-040 Request output signal from the M68360QUADS-040 to the host
11	ADS_ACK	QUADS-040 Acknowledge output signal from the M68360QUADS-040 to the host
12	ADS_INT	QUADS-040 Interrupt output signal from the M68360QUADS-040 to the host
13	HOST_BRK~	HOST Break open collector output signal from the M68360QUADS-040 to the host
14	ADS_BRK	QUADS-040 Break input signal from the host

1. Connector P10 has identical pinout to P8
2. Connector P11 has identical pinout to P9

TABLE 5-1 Connector P1 Interconnect Signals

Pin No.	Signal Name	Description
15	-	Not connected
16	PD1	Bit 1 of the ADI port data bus
17	PD3	Bit 3 of the ADI port data bus
18	PD5	Bit 5 of the ADI port data bus
19	PD7	Bit 7 of the ADI port data bus
20 - 25	GND	Ground signal of the M68360QUADS-040
26	-	Not connected. The host supplies +12V on this pin, but it is not connected on the M68360QUADS-040
27 - 29	HOST_VCC	HOST VCC input from the host. The M68360QUADS-040 does not use these inputs for power supply.
30	HOST_ENABLE~	HOST Enable input signal from the host.
31 - 33	GND	Ground signal of the M68360QUADS-040
34	PD0	Bit 0 of the ADI port data bus
35	PD2	Bit 2 of the ADI port data bus
36	PD4	Bit 4 of the ADI port data bus
37	PD6	Bit 6 of the ADI port data bus

5.2.2 Connector P2 Interconnect Signals

Connector P2 is a 9 pin, female D type connector. It is the RS-232 serial port of the M68360QUADS-040. TABLE 5-1 describes the P5 connector signals.

TABLE 5-2 Connector P2 Interconnect Signals

Pin No.	Signal Name	Description
1	CD	Carrier Detect output from the M68360QUADS-040.
2	TX	Transmit Data output from the M68360QUADS-040.
3	RX	Receive Data input to the M68360QUADS-040.
4	DTR	Data Terminal Ready input to the M68360QUADS-040.
5	GND	Ground signal of the M68360QUADS-040.
6	DSR	Data Set Ready output from the M68360QUADS-040.
7	RTS (N.C.)	Request To Send. This line is not connected in the M68360QUADS-040.
8	CTS	Clear To Send output from the M68360QUADS-040.
9	-	Not connected

5.2.3 Connector P3 Interconnect Signals

Connector P3 is 15 pin, female D type connector. It is the EEST AUI Ethernet port of the M68360QUADS-040 board. TABLE 5-1 describes the P3 connector signals.

TABLE 5-3 Connector P3 Interconnect Signals

Pin No.	Signal Name	Description
1	GND	Ground signal of the M68360QUADS-040.

TABLE 5-3 Connector P3 Interconnect Signals

Pin No.	Signal Name	Description
2	ACX+	Collision detect positive input to the M68360QUADS-040.
3	ATX+	Transmit Data positive output from the M68360QUADS-040.
4	GND	Ground signal of the M68360QUADS-040.
5	ARX+	Receive Data positive input to the M68360QUADS-040.
6	GND	Ground signal of the M68360QUADS-040.
7	-	Not connected
8	GND	Ground signal of the M68360QUADS-040.
9	ACX-	Collision detect negative input to the M68360QUADS-040.
10	ATX-	Transmit Data negative output from the M68360QUADS-040.
11	GND	Ground signal of the M68360QUADS-040.
12	ARX-	Receive Data negative input to the M68360QUADS-040.
13	VPP	+12V power supply from the M68360QUADS-040.
14	GND	Ground signal of the M68360QUADS-040.
15	-	Not connected

5.2.4 Connector P4 Interconnect Signals

Connector P4 is 8 pin, RJ-45 connector. It is the twisted-pair Ethernet port of the M68360QUADS-040 board. TABLE 5-1 describes the P8 connector signals.

TABLE 5-4 Connector P8 Interconnect Signals

Pin No.	Signal Name	Description
1	TPTX+	Twisted-Pair Transmit Data positive output from the M68360QUADS-040.
2	TPTX-	Twisted-Pair Transmit Data negative output from the M68360QUADS-040.
3	TPRX+	Twisted-Pair Receive Data positive input to the M68360QUADS-040.
4	-	Not connected
5	-	Not connected
6	TPRX-	Twisted-Pair Receive Data negative input to the M68360QUADS-040.
7	-	Not connected
8	-	Not connected

5.2.5 Connector P5 Interconnect Signals

Connector P5 is 15 pin, female D type connector. It is the SIA AUI Ethernet port of the M68360QUADS-040 board. TABLE 5-1 describes the P3 connector signals.

TABLE 5-5 Connector P5 Interconnect Signals

Pin No.	Signal Name	Description
1	GND	Ground signal of the M68360QUADS-040.
2	ACX+	Collision detect positive input to the M68360QUADS-040.
3	ATX+	Transmit Data positive output from the M68360QUADS-040.
4	GND	Ground signal of the M68360QUADS-040.

TABLE 5-5 Connector P5 Interconnect Signals

Pin No.	Signal Name	Description
5	ARX+	Receive Data positive input to the M68360QUADS-040.
6	GND	Ground signal of the M68360QUADS-040.
7	-	Not connected
8	GND	Ground signal of the M68360QUADS-040.
9	ACX-	Collision detect negative input to the M68360QUADS-040.
10	ATX-	Transmit Data negative output from the M68360QUADS-040.
11	GND	Ground signal of the M68360QUADS-040.
12	ARX-	Receive Data negative input to the M68360QUADS-040.
13	VPP	+12V power supply from the M68360QUADS-040.
14	GND	Ground signal of the M68360QUADS-040.
15	-	Not connected

5.2.6 Connector P6 Interconnect Signals

Connector P6 is 3 pin connector for 5v power supply. The connector is supplied with 3 pin plug for convenient connection to the power supply. TABLE 5-1 describes the P6 connector signals.

TABLE 5-6 Connector P6 Interconnect Signals

Pin No.	Signal Name	Description
1	VCC	+5V connection to the power supply.
2	GND	Ground connection to the power supply.
3	GND	Ground connection to the power supply.

5.2.7 Connector P7 Interconnect Signals

Connector P7 is a 2 pin connector for 12v power supply. The connector is supplied with 2 pin plug for convenient connection to the power supply. TABLE 5-1 describes the P7 connector signals.

TABLE 5-7 Connector P7 Interconnect Signals

Pin No.	Signal Name	Description
1	VPP	+12V connection to the power supply.
2	GND	Ground connection to the power supply.

5.2.8 Connector P8 Interconnect Signals

Connector P8 is a triple-row, 96 pin, male DIN connector. P8 and P9 Logic-Analyzer connectors provide most of the signals of the slave QUICC and the MC68EC040's. TABLE 5-1 describes the P8 connector signals.

TABLE 5-8 Connector P8 Interconnect Signals

Pin No.	Signal Name	Description
A1 - A32	A0 - A31	Address lines 0 to 31 of the EC040 and slave QUICC[a]
B1 - B32	D0 - D31	Data lines 0 to 31 of the EC040 and slave QUICC
C1 - C3	TM0 - TM2	Transfer Modifier lines 0 to 2 of the EC040

TABLE 5-8 Connector P8 Interconnect Signals

Pin No.	Signal Name	Description
C4	TT0	Transfer Type signal 0 pin of the EC040
C5	GND	M68360QUADS-040 board Ground.
C6 - C7	SIZ0 - SIZ1	EC040's Access Size indicators 0 to 1
C8	BRQ~	Quicc's Bus Request
C9	BGQ~	Quicc's Bus Grant
C10	BB~	Bus Busy
C11	AS~	Quicc's Address Strobe
C12	GND	Board Ground
C13	TT1	EC040's Transfer Type 1
C14	R/W~	Read / Write
C15	GND	Board Ground
C16	LOCK~	EC040 Locked (RMW) Cycle indicator
C17	DD2~	Quicc's RAS Double Drive 2
C18	TBI~	EC040's Transfer Burst Inhibit
C19	TA~	EC040's Transfer Acknowledge
C20	TEA~	EC040's Transfer Error Acknowledge
C21	VCC	Board's VCC plane
C22	RSTH~	Hard reset pin of the QUICC
C23	RSTS~	Soft reset pin of the QUICC
C24	PERR~	Parity error pin of the QUICC
C25	VCC	Board's VCC plane
C26	TS~	EC040's Transfer Start
C27	WE0~	Quicc's Write Enable 0
C28	WE1~	Quicc's Write Enable 1
C29	GND	Board's Ground
C30	WE2~	Quicc's Write Enable 2
C31	GND	Board's Ground
C32	WE3~	Quicc's Write Enable 3

a. Quicc's A28 - A31 are used as Write Enables, therefore not connected to EC040's corresponding signals

5.2.9 Connector P9 Interconnect Signals

Connector P9 is a triple-row, 96 pin, male DIN connector. P8 and P9 Logic-Analyzer connectors provide most of the signals of the slave QUICC and the MC68EC040's. TABLE 5-1 describes the P9 connector signals.

TABLE 5-9 Connector P9 Interconnect Signals

Pin No.	Signal Name	Description
A1	CLK4	Buffered System clock
A2	GND	Board's Ground
A3	SIA_RX	SIA Receive Data. Also SCC2's Receive Data

TABLE 5-9 Connector P9 Interconnect Signals

Pin No.	Signal Name	Description
A4	SIA_TX	SIA Transmit Data. Also SCC2's Transmit Data
A5 - A6	GND	Board's GND
A7 - A8	PA6 - PA7	Port A 6 - 7 Parallel I/O lines
A9	GND	Board's Ground
A10	CLKO1	Quicc's Clock Out 1
A11	GND	Board's Ground
A12 - A14	VCC	Board's VCC plane
A15	SIATCK	SIA's Transmit Clock. Also Quicc's CLK3.
A16	SIARCK	SIA's Receive Clock. Also Quicc's CLK4.
A17	VCC	Board's VCC plane
A18 - A21	PRTY0 - PRTY3	Quicc's Parity lines
A22 - A24	GND	Board's Ground
A25 - A26	IRQ2~ IRQ3~	Quicc's Interrupt Requests 2 - 3
A27	VCC	Board's VCC plane
A28	IRQ5~	Quicc's Interrupt Request 5
A29 - A31	VCC	Board's VCC plane
A32	GND	Board's Ground
B1 - B2	TLN0 - TLN1	EC040's Transfer Line indicators
B3 - B4	UPA0 - UPA1	EC040's User's Programmable Attributes.
B5 - B10	PB4 - PB9	Quicc's Port B's Parallel I/O lines 4 - 9
B11	TIP~	EC040's Transfer In Progress
B12	BR040~	EC040's Bus Request
B13	BG040~	EC040's Bus Grant
B14 - B17	PST0 - PST3	EC040's Processor Status 0 - 3
B18 - B19	SC0 - SC1	EC040's Snoop Control 0 - 1
B20	GND	Board's Ground
B21	S_TENA	SIA's Transmit Enable Input
B22 - B23	PC2 - PC3	Quicc's Port C Parallel I/O lines 2 - 3
B24 - B25	GND	Board's Ground
B26	S_CLSN	SIA's Collision Indicator
B27	S_RENA	SIA's Receive Enable Output
B28 - B31	PC8 - PC11	Quicc's Port C Parallel I/O lines 8 - 11
B32	GND	Board's Ground
C1 - C4	CAS0~ - CAS3~	QUICC's Column Address Strobe outputs 0 -3
C5 - C10	VCC	Board's VCC plane
C11	GND	Board's Ground
C12 - C13	CS6~ - CS7~	Quicc Chip-Select outputs 6 - 7
C14	GND	Board's Ground
C15	LOCKE~	EC040 Lock End output
C16	TCI~	EC040's Transfer Cache Inhibit input

TABLE 5-9 Connector P9 Interconnect Signals

Pin No.	Signal Name	Description
C17	MI~	EC040's Memory Inhibit output
C18	CIOUT~	EC040 Cache Inhibit Out
C19	IPEND~	EC040 Interrupt Pending output
C20	CDIS~	EC040's Cache Disable input
C21	BKPTO~	Quicc's BreakPoint Output
C22	RSTH~	Quicc's Hard Reset signal
C23	RSTS~	Quicc's Soft Reset signal
C24	BADD3	Quicc's Burst Address line 3
C25	MDIS~[a]	LC040's Memory Management Unit Disable Input.
C26	BADD2	Quicc's Burst Address line 2
C27	DD1~	Quicc's RAS Double Drive output 1
C28 - C32	GND	Board's Ground

a. Applicable only if MC68**LC**040 processor is installed.

5.2.10 Connector P10 Interconnect Signals

Connector P10 is a 96 pin, Female, 90º, DIN connector, serving as an expansion connector for off-board hardware applications. It is identical in pin out to P8. For interconnect signal reference, see TABLE 5-1 on page 41.

5.2.11 Connector P11 Interconnect Signals

Connector P11 is a 96 pin, Female, 90º, DIN connector, serving as an expansion connector for off-board hardware applications. It is identical in pin out to P9. For interconnect signal reference, see TABLE 5-1 on page 41.

5.3 M68360QUADS-040 Parts List

The components of the M68360QUADS-040 and their reference designation are listed in TABLE 5-10.

TABLE 5-10 Parts List

Reference Designation	Part Description	Notes
C1	Capacitor 100 µF electrolytic	T.H.
C2, C3, C8 - C10, C12, C13, C18, C19, C21 - C28, C30, C31, C34 - C49, C51 - C109	Capacitor 0.1 µF	SMD
C4 - C7	Capacitor 10 µF electrolytic	SMD
C11	Capacitor 4700 pF	SMD
C14	Capacitor 680 pF	SMD
C15	Capacitor 20 pF	SMD

TABLE 5-10 Parts List

Reference Designation	Part Description	Notes
C16, C17	Capacitor 100 pF	SMD
C20	Capacitor 0.039 µF	SMD
C29	Capacitor 3900 pF	SMD
C32, C33	Capacitor 68 pF	SMD
C50	Capacitor 390 pF	SMD
D1	MBRD620CT	SMD
D2	1SMC5.0AT3 (zener)	SMD
DSW1	DIP-SWITCH, SPST 8	SMD
F1	Fuse Block, with 5A fuse	5V power supply
J1 - J6, J8 - J10	Jumper Header, 2 pole, with fabricated jumper	
J7	Jumper Header, 3 pole, with fabricated jumper	
LD1, LD4, LD6, LD10	LED RED	SMD
LD2, LD3, LD8	LED GREEN	SMD
LD5, LD7, LD9	LED YELLOW	SMD
P1	Connector 37 pin D type male	
P2	Connector 9 pin D type female	
P3, P5	Connector 15 pin D type female	
P4	Connector 8 pin RJ-45	
P6	Power connector, 3 pin with plug	5v power supply
P7	Power connector, 2 pin with plug	12v power supply
P8, P9	Connector 96 pin DIN male straight	Logic analyzer
P10, P11	Connector 96 pin DIN female 90º. Compatible wire-wrap connectors are supplied with the M68360QUADS-040.	Expansion
R1 - R3, R12 - R14, R18 - R21	Resistor 39.1 Ω	SMD
R4, R11, R17, R23, R29 - R37	Resistor 4.7 KΩ	SMD
R5	Resistor 240 Ω	SMD
R6 - R10	Resistor 330 Ω	SMD
R15	Resistor 3 KΩ	SMD
R16	Resistor 510 Ω	SMD
R22	Resistor 290 Ω	SMD

TABLE 5-10 Parts List

Reference Designation	Part Description	Notes
R24	Resistor 100 Ω	SMD
R25 - R28	Resistor 150 Ω	SMD
RN1 RN2	Resistor network 16 pin, 8 resistors 22 Ω	SMD
RN3 - RN10	Resistor network 14 pin, 13 resistors 4.7 KΩ	SMD
SW1, SW2	S.P.D.T. push button	
T1, T3	I.C. PE64503	DIP
T2	I.C. PE65263	DIP
T4	I.C. PE65260	DIP
U1- U2	I.C. 74LS240	SMD
U3	I.C. MC145407	SMD
U4	I.C. Am7992	CDIP socket mounted
U5	LAF10T-7B Ethernet filter	SIL
U6	LAF10T-3B Ethernet filter	SIL
U7	I.C. MC68160 (EEST)	PQFP
U8 - U9	I.C. 74LS373	SMD
U10 - U11	I.C. PAL20RA10-20	DIP socket mounted
U12	I.C. PAL22V10-25	DIP socket mounted
U13	I.C. 74LS245	SMD
U14	I.C. MCM2814	DIP
U15	I.C. 74LS85	SMD
U16, U38	I.C. 74ACT86	SMD
U17, U26, U31	I.C. 74F157	SMD
U18 - U21	I.C. Am29F010-12	SMD socket mounted
U22	I.C. MCM36256 DRAM SIMM	SIMM socket mounted
U23	I.C. PAL22V10-15	DIP socket mounted
U24	MC68EC040FE33	CQFP
U25	MC68360 QUICC	PGA socket mounted
U27 - U30, U33 - U36[a]	MCM62940AFN	SMD
U32	I.C. PAL16R4-7	DIP socket mounted
U37	I.C. Clock Generator 50 Mhz, CMOS / TTL levels	DIP socket mounted
U39	I.C. 74ACT74	SMD
Y1, Y2	Crystal Resonator 20MHz	SMD

a. Only U33 - U36 are factory populated. U27 - U30 are user optional.

APPENDIX A - ADI BOARD INSTALLATION

A.1 INTRODUCTION

This appendix describes the hardware installation of the ADI board into various host computers.

The installation instructions cover the following host computers:

1. IBM-PC/XT/AT
2. SUN - 4 (SBus interface)

A.2 IBM-PC/XT/AT to M68360QUADS-040 Interface

The ADI board should be installed in one of the IBM-PC/XT/AT motherboard system expansion slots. A single ADI can control up to eight M68360QUADS-040 boards. The ADI address in the computer is configured to be at I/O memory addresses 100-102 (hex), but it may be reconfigured for an alternate address space.

CAUTION

BEFORE REMOVING OR INSTALLING ANY EQUIPMENT IN THE IBM-PC/XT/AT COMPUTER, TURN THE POWER OFF AND REMOVE THE POWER CORD.

A.2.1 ADI Installation in IBM-PC/XT/AT

Refer to the appropriate Installation and Setup manual of the IBM-PC/XT/AT computer for instructions on removing the computer cover.

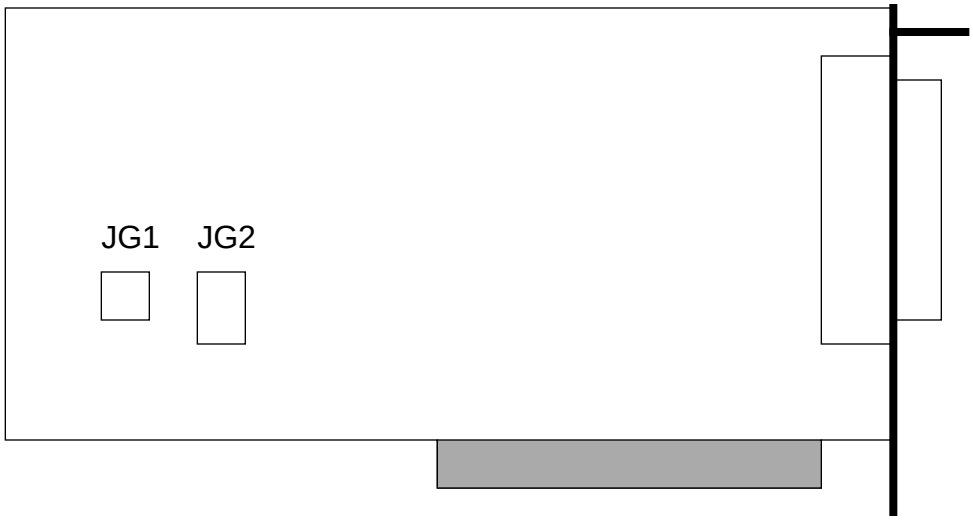
The ADI board address block should be configured at a free I/O address space in the computer. The address must be unique and it must not fall within the address range of another card installed in the computer.

The ADI board address block can be configured to start at one of the three following addresses:

- $100 - This address is unassigned in the IBM-PC
- $200 - This address is usually used for the game port
- $300 - This address is defined as a prototype port

The ADI board is factory configured for address decoding at 100-102 hex in the IBM-PC/XT/AT I/O address map. These are undefined peripheral addresses.

FIGURE A-1 Physical Location of jumper JG1 and JG2



NOTE: Jumper JG2 should be left unconnected.

The following figure shows the required jumper connection for each address configuration. Address 0 hex is not recommended, and its usage might cause problems.

FIGURE A-2 JG1 Configuration Options

To properly install the ADI board, position its front bottom corner in the plastic card guide channel at the front of the IBM-PC/XT/AT chassis. Keeping the top of the ADI board level and any ribbon cables out of the way, lower the board until its connectors are aligned with the computer expansion slot connectors. Using evenly distributed pressure, press the ADI board straight down until it seats in the expansion slot.

Secure the ADI board to the computer chassis using the bracket retaining screw. Refer to the computer Installation and Setup manual for instructions on reinstalling the computer cover.

A.3 SUN-4 to M68360QUADS-040 Interface

The ADI board should be installed in one of the SBus expansion slots in the Sun-4 SPARCstation computer. A single ADI can control up to eight M68360QUADS-040 boards.

CAUTION

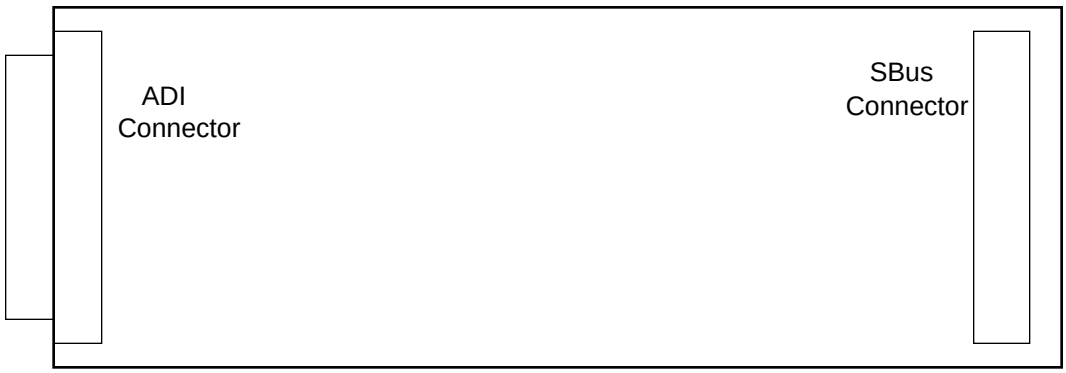
BEFORE REMOVING OR INSTALLING ANY EQUIPMENT IN THE SUN-4 COMPUTER, TURN THE POWER OFF AND REMOVE THE POWER CORD.

A.3.1 ADI Installation in the SUN-4

There are no jumper options on the ADI board for the Sun-4 computer. The ADI board can be inserted into any available SBus expansion slot on the motherboard.

Refer to the appropriate Installation and Setup manual for the Sun-4 computer for instructions on removing the computer cover and installing the board in an expansion slot.

FIGURE A-3 ADI board for SBus



Following is a summary of the Instructions in the Sun manual:

1. Turn off power to the system, but keep the power cord plugged in. Be sure to save all open files and then the following steps should shut down your system:
   - hostname% /bin/su
   - Password: mypasswd
   - hostname# /usr/etc/halt
   - wait for the following messages.

     Syncing file systems... done

     Halted

     Program Terminated

     Type b(boot), c(continue), n(new command mode)
   - When these messages appear, you can safely turn off the power to the system unit.
2. Open the system unit. Be sure to attach a grounding strap to your wrist and to the metal casing of the power supply. Follow the instructions supplied with your system to gain access to the SBus slots.
3. Remove the SBus slot filler panel for the desired slot from the inner surface of the back panel of the system unit. Note that the ADI board is a slave only board and thus will function in any available SBus slot.
4. Slide the ADI board at an angle into the back panel of the system unit. Make sure that the mounting plate on the ADI board hooks into the holes on the back panel of the system unit.

5. Push the ADI board against the back panel and align the connector with its mate and gently press the corners of the board to seat the connector firmly.
6. Close the system unit.
7. Connect the 37 pin interface flat cable to the ADI board and secure.
8. Turn power on to the system unit and check for proper operation.

APPENDIX B - ADI PORT HANDSHAKE DESCRIPTION

B.1 INTRODUCTION

In this appendix, the ADI port signals and the handshake procedure are explained. The M68360QUADS-040 ADI port can be connected to an ADI board mounted in a host computer.

There are ADI boards for the following host computers:

1. IBM-PC/XT/AT
2. SUN - 4 (SBus interface)

B.2 ADI Port Concept and Operation Description

Each ADI board can be connected to up to 8 M68360QUADS-040 boards. Each M68360QUADS-040 has its own address which is fixed by setting Dip-Switch DSW1 on the board. Refer to section 2.3.1 on page 13.

The following operations can be performed using the ADI port :

- The host computer can write a byte to the M68360QUADS-040
- The M68360QUADS-040 can write a byte to the host computer
- The M68360QUADS-040 can interrupt the host computer
- The host computer can interrupt the M68360QUADS-040 (interrupt level 7)
- The host computer can reset (soft or hard) the M68360QUADS-040

If more than one M68360QUADS-040 is connected to the same ADI board, the host computer can perform the following operations simultaneously on all M68360QUADS-040 boards :

- Abort all boards (interrupt level 7)
- Reset all boards

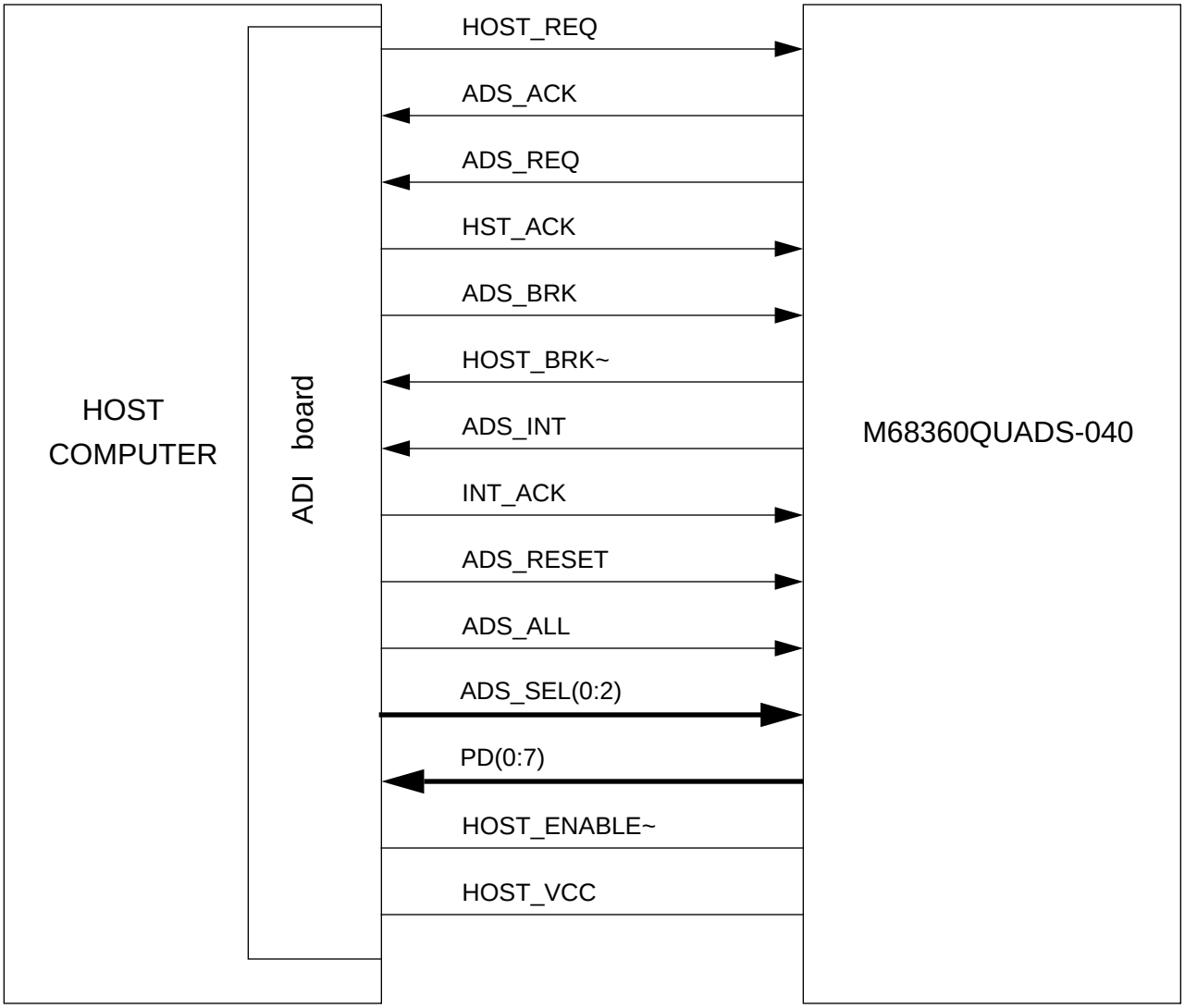
B.3 Handshake Description

Every action between the M68360QUADS-040 and the host is asynchronous and is implemented by asserting and negating handshake signals by software.

All signals have TTL levels. A control signal is asserted if it is driven to logic '1' TTL level, and it is negated if it is driven to logic '0' level.

The connection between the host computer and the M68360QUADS-040 is shown in FIGURE B-1 below.

FIGURE B-1 Host Computer (ADI) to M68360QUADS-040 Connection



B.3.1 Write Cycle from Host to M68360QUADS-040

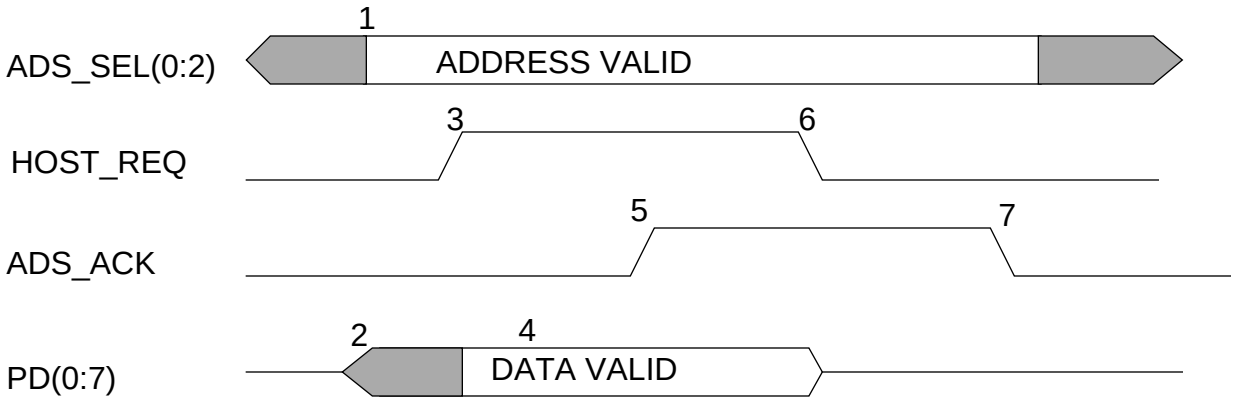
The application software in the Host uses the handshake signals to coordinate data transfer across the parallel link. The QUICC040bug software in the M68360QUADS-040 is responsible for accepting the data and responding to the handshake signals. The signals are shown in FIGURE B-2.

The sequence of events during a byte write to the M68360QUADS-040 is as follows:

1. The Host selects the M68360QUADS-040 board by putting the board's address on the ADS_SEL(0:2) signals.
2. The Host places a data byte in the data bus latch (buffer is in high-impedance state).
3. The Host asserts the HOST_REQ signal (the data buffer is enabled, data appears on the bus).
4. The M68360QUADS-040 detects the HOST_REQ signal and reads the data byte.
5. The M68360QUADS-040 asserts the ADS_ACK signal.

6. The Host detects the ADS_ACK signal and negates the HOST_REQ signal (data buffer is disabled).
7. The M68360QUADS-040 detects the negation of HOST_REQ signal and negates ADS_ACK to end the cycle.

FIGURE B-2 Host Write to M68360QUADS-040

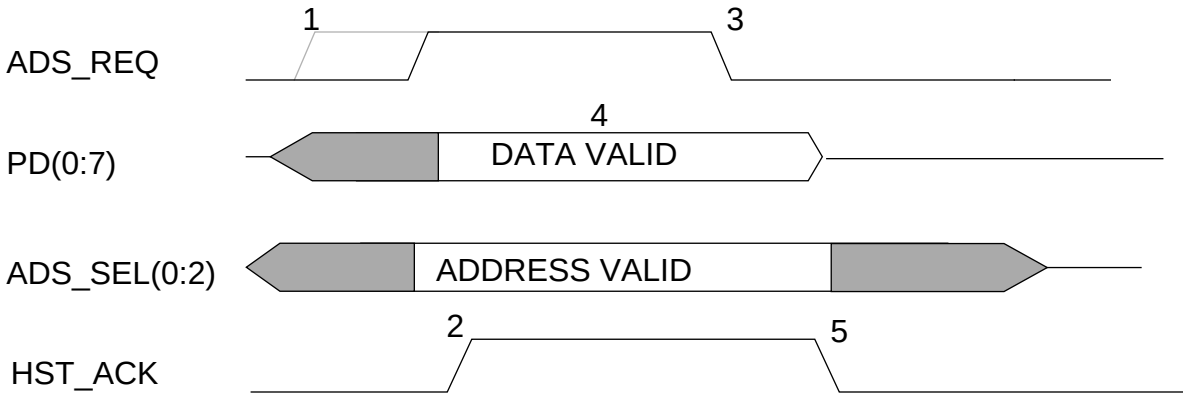


B.3.2 Write Cycle from M68360QUADS-040 to Host

The signal handshake during an M68360QUADS-040 to Host write cycle is shown in FIGURE B-3. The sequence of events is as follows:

1. The M68360QUADS-040 places a data byte on the parallel port data bus (buffer disabled) and asserts the ADS_REQ signal (the ADS_REQ signal will not appear on the port until the board is selected by the Host).
2. The Host polls each M68360QUADS-040 address and detects the ADS_REQ signal from the requesting board. The Host asserts the HST_ACK signal in response, which enables the data buffer in the M68360QUADS-040.
3. The M68360QUADS-040 negates the ADS_REQ signal. The data appears on the bus as long as the HST_ACK signal is asserted.
4. The Host reads the data.
5. The Host negates the HST_ACK signal to end the cycle. The M68360QUADS-040 ends the cycle.

FIGURE B-3 M68360QUADS-040 Write Cycle to Host



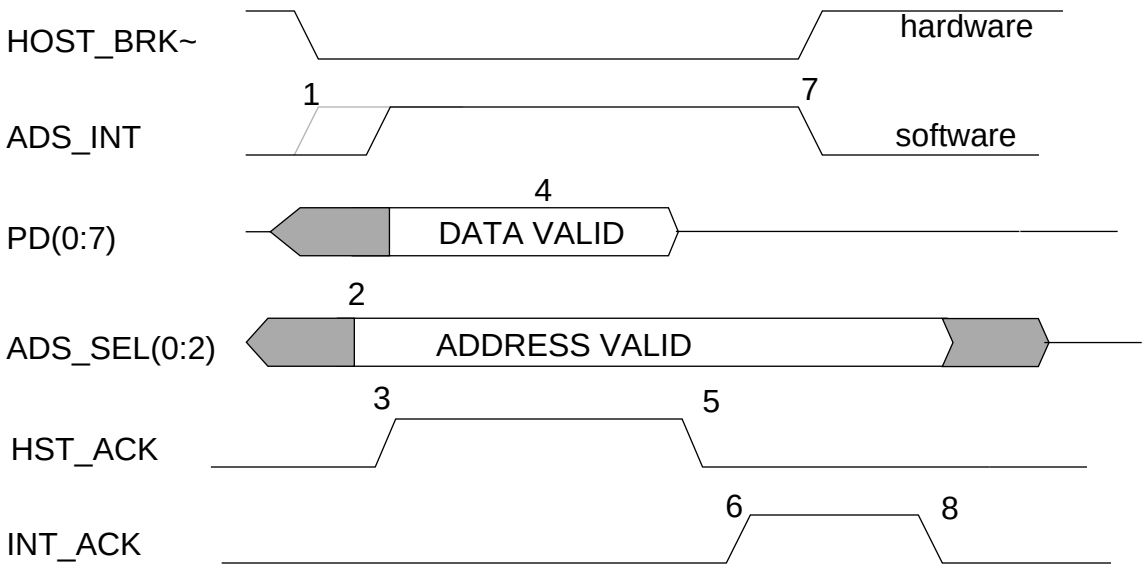
B.3.3 M68360QUADS-040 Interrupt to the Host

The M68360QUADS-040 can generate an interrupt to the Host. The interrupt request and acknowledge sequence is shown in FIGURE B-4.

The sequence is as follows:

1. The M68360QUADS-040 places a service request code on the parallel port data bus (buffer disabled) and asserts the ADS_INT and the HOST_BRK~ signals. The HOST_BRK~ signal is an open-collector signal, asserted low, common to all M68360QUADS-040 boards which will appear immediately on the port. The ADS_INT signal will not appear on the port until the board is selected by the Host.
2. The Host detects the HOST_BRK~ signal and polls each M68360QUADS-040 address to determine the interrupting board.
3. The Host asserts the HST_ACK signal, enabling the data buffer in the M68360QUADS-040.
4. The Host reads the service request code on the data bus.
5. The Host negates the HST_ACK signal.
6. The Host asserts the INT_ACK signal, which resets the HOST_BRK latch in the M68360QUADS-040 and negates the HOST_BRK~ signal. the HOST_BRK~ signal can still be low (asserted) if another M68360QUADS-040 board is driving it low.
7. The selected M68360QUADS-040 detects the INT_ACK signal and negates the ADS_INT signal.
8. The Host negates the INT_ACK signal and ends the cycle.

FIGURE B-4 M68360QUADS-040 Interrupt to Host



B.3.4 Host Interrupt to the M68360QUADS-040

The Host can interrupt the M68360QUADS-040 (interrupt level 7) to abort the execution of programs running on the board. This is done by selecting the address of the required M68360QUADS-040 and momentarily asserting the ADS_BRK signal, which sets a latch in the M68360QUADS-040. The output of the latch interrupts the EC040 on the M68360QUADS-040. The latch is cleared by the interrupt handling software on the M68360QUADS-040.

B.3.5 Host Reset to the M68360QUADS-040

The Host can perform either hard reset or soft reset on the M68360QUADS-040. Soft reset is done by selecting the address of the required board and asserting the ADS_RESET signal for more than 26 microseconds. Hard reset is done by selecting the address of the required board, asserting INT_ACK signal, and asserting the ADS_RESET signal for more than 26 microseconds.

B.3.6 Addressing All M68360QUADS-040

The Host can reset or interrupt all M68360QUADS-040 boards that are connected to the same ADI. The Host should assert the ADS_ALL signal in conjunction with either ADS_RESET or ADS_BRK. The contents of the ADS_SEL(0:2) lines have no affect.

APPENDIX C - PALS' EQUATIONS

C.1 U10 - Indicators Logic

```
  TITLE        INDICATR
  PATTERN      INDICATR.PDS
  REVISION     PILOT.0
   DATE        8,8,93
;*********************************************************
  CHIP INDIC PAL20RA10
;****************************

 PL PST0 PST1 PST2 PST3 TIP AS ADSNT BKCLR CK_NMI CS5 GND
; 1   2    3    4    5    6  7    8     9     10    11  12

 OE NC NC NC NC H_BRK H_BRK_ H_NMI HLT RUNDM RUN040 VCC
; 13 14 15 16 17  18     19    20   21   22     23    24

;*********************************************************************
; This pal serves as indicators logic, adi interrupts logic
; and future support for MC68040 buffers configuration (via IPL).
; RUN040 drives the run040 led when TIP is active (low).
; RUNDM drives the rundma led when AS is active (low).
; HLT drives the halt led according to the state of PST(0:3).
; H_NMI serves as a FF for the host generated level 7 interrupt.
; H_BRK_ is a simulated o.c. output for the ADI's host break, OE
; of which is driven by H_BRK.
;*********************************************************************



  EQUATIONS
;**************

  /RUN040 = VCC
  RUN040.TRST = /TIP
  RUN040.RSTF = VCC  ; bypass
  RUN040.SETF = VCC

  /RUNDM = VCC
  RUNDM.TRST = /AS
  RUNDM.RSTF = VCC   ; bypass
  RUNDM.SETF = VCC
```

```
/HLT = VCC
HLT.TRST = /PST3 * PST2 * /PST1 * PST0    ; halted state
HLT.RSTF = VCC; bypass
HLT.SETF = VCC


H_NMI.CLKF = CK_NMI      ; rising edge of CK_NMI
/H_NMI := VCC
H_NMI.TRST = VCC
H_NMI.RSTF = /CS5
H_NMI.SETF = GND

H_BRK_ = GND
H_BRK_.TRST = H_BRK
H_BRK_.RSTF = VCC        ; bypass
H_BRK_.SETF = VCC

H_BRK.CLKF = /ADSNT    ; rising edge of ADSNT~
H_BRK := VCC
H_BRK.TRST = VCC
H_BRK.RSTF = GND
H_BRK.SETF = /BKCLR
```

C.2 U11 - Reset & Abort Generator

```
  TITLE        RSTABR
  PATTERN      RSTABR.PDS
  REVISION     PILOT.0
   DATE        8,8,93
;*********************************************************
  CHIP RSTABR PAL20RA10
;***************************
; This pal is used as a reset and abort generator for the QUICC040EVB.
; DEB1 serves as a debouncer for the reset push-button and DEB2 serves
; a debouncer for the abort p.b.
; IRQ7 which is the logical sum of all events causing level 7 interrupt,
; i.e., abort push button, breakpoint and host nmi, (drives the OE of
; IRQ7 to simulate open collector. - ABORT was removed since its pin was
; needed for RSTI, therefore, IRQ7* at the connector SHOULD NEVER BE
; DRIVEN FROM OUTSIDE)
; ABRT serves a FF holding the request for the abort push button
```

```
; BKINT serves as a FF holding the request from the breakpoint logic.
; RSTS_ is a simulated o.c. driving the soft reset line of the quicc, while
; its OE is driven by RSTS
; RSTH_ is a simulated o.c. driving the hard reset line of the quicc, while
; its OE is driven by RSTH
; RSTS logically sums the conditions for soft reset: push-button, host
; soft reset and reset instruction (RSTO).
; RSTI logically sums the conditions for 040 reset: HARD reset
; (both push-buttons are depressed), P.B. SOFT reset, HOST hard and soft
; reset, P.U. reset and software watch-dog reset.
; RSTI is separated from RSTH_ in order of supporting soft reset as well.
;*******************************************************************************

  PL RST1 RST2 ABR1 ABR2 H_RSTH H_RSTS RSTO CS5 H_NMI BKPTO GND
; 1  2    3    4    5     6     7    8    9   10    11   12


    OE RSTI DEB2 DEB1 ABRT RSTS RSTH BKINT IRQ7 RSTS_ RSTH_ VCC
;   13  14   15   16   17   18   19   20   21   22   23   24


;*******************************************************************************

  EQUATIONS
;**************

  /IRQ7 = /ABRT ; abort p.b. FF
       + /H_NMI; host nmi
       + /BKINT; breakpoint logic
  IRQ7.TRST = VCC
  IRQ7.RSTF = VCC; bypass
  IRQ7.SETF = VCC

  DEB1.TRST = VCC
  DEB1.RSTF = /RST2
  DEB1.SETF = /RST1     ;reset debouncer

  DEB2.TRST = VCC
  DEB2.RSTF = /ABR2
  DEB2.SETF = /ABR1     ;abort debouncer
```

```
ABRT.CLKF = DEB2      ; rising edge of abort debouncer.
/ABRT := VCC          ; active low.
ABRT.TRST = VCC
ABRT.RSTF = /CS5      ; reset the FF ('1')
ABRT.SETF = GND

RSTS = H_RSTS         ; host generated SOFT reset
    + DEB1 * /DEB2    ; SOFT reset push button depressed
    + /RSTO           ; reset instruction
RSTS.TRST = VCC
RSTS.RSTF = VCC       ; bypass
RSTS.SETF = VCC


RSTH = H_RSTH         ; host generated HARD reset
    + DEB1 * DEB2     ; BOTH push buttons depressed
RSTH.TRST = VCC
RSTH.RSTF = VCC       ; bypass
RSTH.SETF = VCC



BKINT.CLKF = /BKPTO   ; falling edge of BKPTO.
/BKINT := VCC         ; active low.
BKINT.TRST = VCC
BKINT.RSTF = /CS5     ; reset the FF ('1')
BKINT.SETF = GND


/RSTI = /RSTH_        ; Quicc generated resets + HOST hard reset
     + DEB1           ; P.B. hard + soft reset
     + H_RSTS         ; HOST soft reset
RSTI.TRST = VCC
RSTI.RSTF = VCC       ; bypass
RSTI.SETF = VCC


/RSTS_ = VCC          ; active low
RSTS_.TRST = RSTS
RSTS_.RSTF = VCC      ; bypass
RSTS_.SETF = VCC

/RSTH_ = VCC          ; active low
```

```
  RSTH_.TRST = RSTH
  RSTH_.RSTF = VCC       ; bypass
  RSTH_.SETF = VCC
```

C.3 U12 - ADI Controller

```
; Reference Designation - U3
  Title       PARALLEL_CONT
  Pattern     PARCONT.pds
  Revision    A.0
  Date        23,12,92
;*********************************************************
  CHIP PARCONT  PAL22V10
;***************************

  ADS_G RSTS HSVCC ADRST ADALL ADBRK HSTEN HSACK HSREQ INACK NC GND
;   1    2   3    4    5    6    7    8    9    10  11  12


  ADSSEL ADI_RD CK_NMI BKCLR NC NC ADIAC H_RSTH H_RSTS ADI_G ADIDIR
;   13    14    15   16   17 18  19    20    21    22    23

  VCC GLOBAL
;   24  THE 25'TH PIN
;*****************************************************************
; This pal serves as an ADI controller for the M68360QUADS-040.
; H_RSTS generates soft reset for the evb
; H_RSTH generates hard reset for the evb
; CK_NMI generates the level 7 interrupt
; BKCLR resets the host break FF
; ADI_RD open the strobes buffer towards the ADI
; ADI_G enables the data buffer
; ADI_AC generates interrupt upon HOST request or acknowledge.
; ADIDIR controls the direction of the data buffer: 0 - outside.
;*****************************************************************

  EQUATIONS
;**************

   H_RSTS = HSTEN * /HSVCC * /ADRST * ADSSEL
        + HSTEN * /HSVCC * /ADRST * /ADALL
```

H_RSTH = HSTEN * /HSVCC * /ADRST * ADSSEL * /INACK
+ HSTEN * /HSVCC * /ADRST * /ADALL * /INACK

CK_NMI = HSTEN * /HSVCC * /ADBRK * ADSSEL
+ HSTEN * /HSVCC * /ADBRK * /ADALL

/BKCLR = /RSTS
+ /INACK * HSTEN * /HSVCC * ADSSEL

/ADI_RD = HSTEN * ADSSEL * /HSVCC

/ADI_G = HSTEN * /HSVCC * ADSSEL * /HSACK; host reads
+ HSTEN * /HSVCC * ADSSEL * /ADS_G; local read
+ HSTEN * /HSVCC * /ADALL * /ADS_G; local read

/ADIAC = HSTEN * /HSVCC * /HSREQ * /ADALL
+ HSTEN * /HSVCC * /HSREQ * ADSSEL
+ HSTEN * /HSVCC * /HSACK * ADSSEL

/ADIDIR = HSTEN * ADS_G * /HSVCC * ADSSEL * /HSACK; host read only

C.4 U23 - Core Disable Logic

```
TITLE    DISCPU
PATTERN  dis_bug.pds
Revision PILOT.0
DATE     9,8,93

;*******************************************************************************
; This pal is meant to fix the core-disable problem in the quicc.
; It contains a 6 bit synchronous counter, which starts counting after
; RESETH_ is asserted.
; During the first 64 clocks since RESETH_ is asserted, CONF2 is held at
; '1' to allow reset of the CORE. On the next clock CONF2 is driven low
; until RESETH_ is negated. After that CONF2 is tri-stated and held down
; by an external pull-down resistor.
;
```

```
; S_RST: Synchronized RESETH
; DS_RST: Double synchronized RESETH
; D_RST: Detect RESETH asserted.
; CONF2: QUICC CONFIG2 pin, which determines core disable.
; Q0 - Q5: counter stages
; RESETH: QUICCs hard reset i/o pin - active low.
; CIN: Active high count enable.
;*********************************************************************


 CHIP DIS_BUG PAL22V10
;**********************

  CLK  NC NC NC NC NC NC NC CIN  NC RESETH  GND
; I1   I2 I3 I4 I5 I6 I7 I8  I9  I10   I11    12

  NC   Q5    Q4    Q3    Q2    Q1    Q0    CONF2  D_RST DS_RST S_RST   VCC
; I13  O14   O15   O16   O17   O18   O19   O20    O21    O22    O23     24

GLOBAL

EQUATIONS
;*************

S_RST := RESETH; Sync RESETH

S_RST.TRST = VCC

DS_RST := S_RST; Double sync RESETH

DS_RST.TRST = VCC

/D_RST = /S_RST * DS_RST     ; Identifying RESETH falling edge to
                             ; synchronously reset the counter

Q0 :=  /Q0 * D_RST * CIN         ; Counter LSB
    + Q0 * D_RST * /CIN

Q0.TRST = VCC

Q1 := /Q1 * Q0 * D_RST * CIN
    + Q1 * /Q0 * D_RST * CIN
    + Q1 * D_RST * /CIN
```

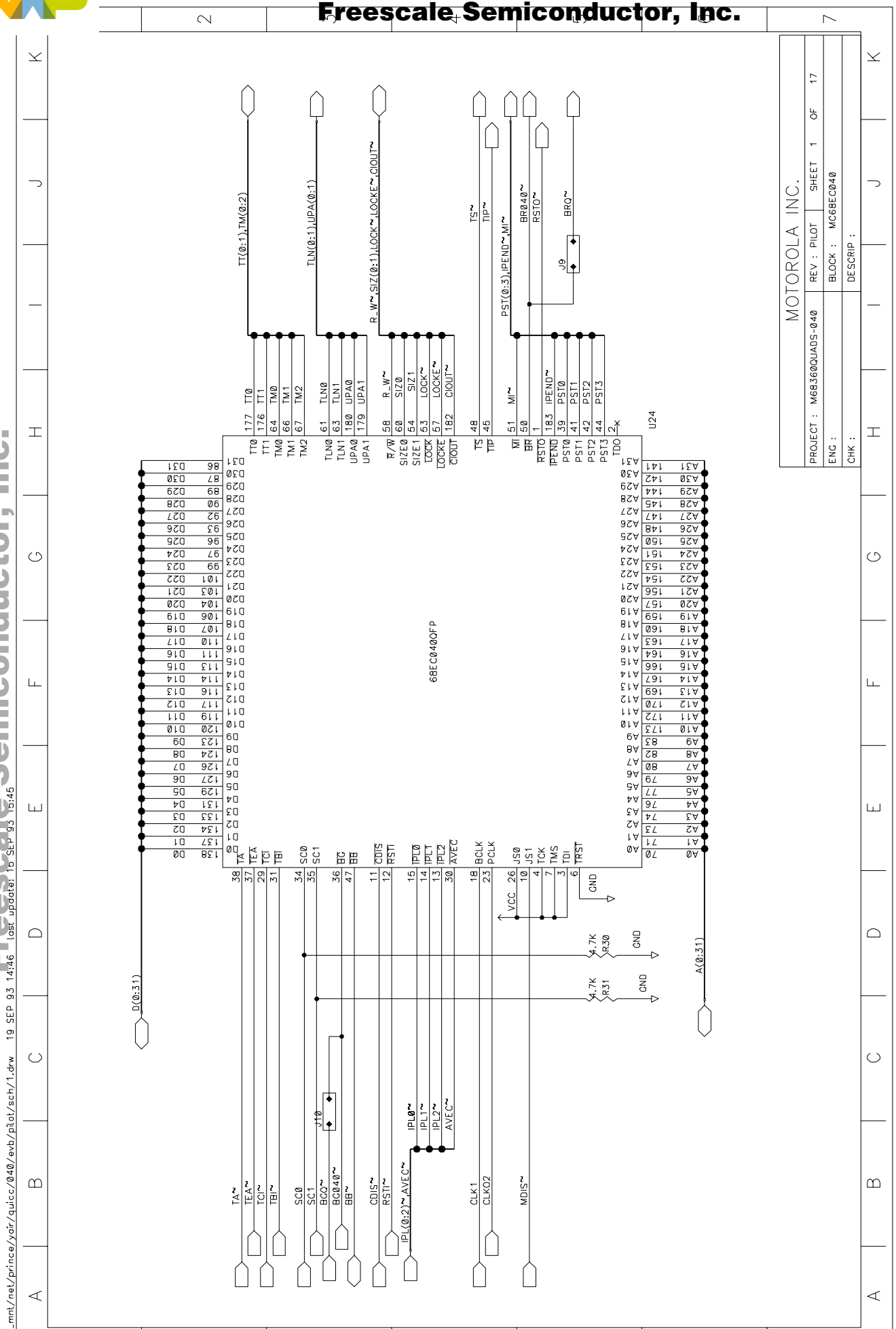
```
Q1.TRST = VCC

Q2 := Q2 * /Q1 * D_RST * CIN
    + Q2 * /Q0 * D_RST * CIN
    + /Q2 * Q1 * Q0 * D_RST * CIN
    + Q2 * D_RST * /CIN

Q2.TRST = VCC

Q3 := Q3 * /Q2 * D_RST * CIN
    + Q3 * /Q1 * D_RST * CIN
    + Q3 * /Q0 * D_RST * CIN
    + /Q3 * Q2 * Q1 * Q0 * D_RST * CIN
    + Q3 * D_RST * /CIN

Q3.TRST = VCC

Q4 := Q4 * /Q3 * D_RST * CIN
    + Q4 * /Q2 * D_RST * CIN
    + Q4 * /Q1 * D_RST * CIN
    + Q4 * /Q0 * D_RST * CIN
    + /Q4 * Q3 * Q2 * Q1 * Q0 * D_RST * CIN
    + Q4 * D_RST * /CIN

Q4.TRST = VCC

Q5 := Q5 * /Q4 * D_RST * CIN       ; Counter MSB
    + Q5 * /Q3 * D_RST * CIN
    + Q5 * /Q2 * D_RST * CIN
    + Q5 * /Q1 * D_RST * CIN
    + Q5 * /Q0 * D_RST * CIN
    + /Q5 * Q4 * Q3 * Q2 * Q1* Q0 * D_RST * CIN
    + Q5 * D_RST * /CIN

Q5.TRST = VCC


/CONF2 = Q1 * Q2 * Q3 * Q4 * Q5             ; End of count

CONF2.TRST = /RESETH                        ; Tristated after RESETH rising edge
```

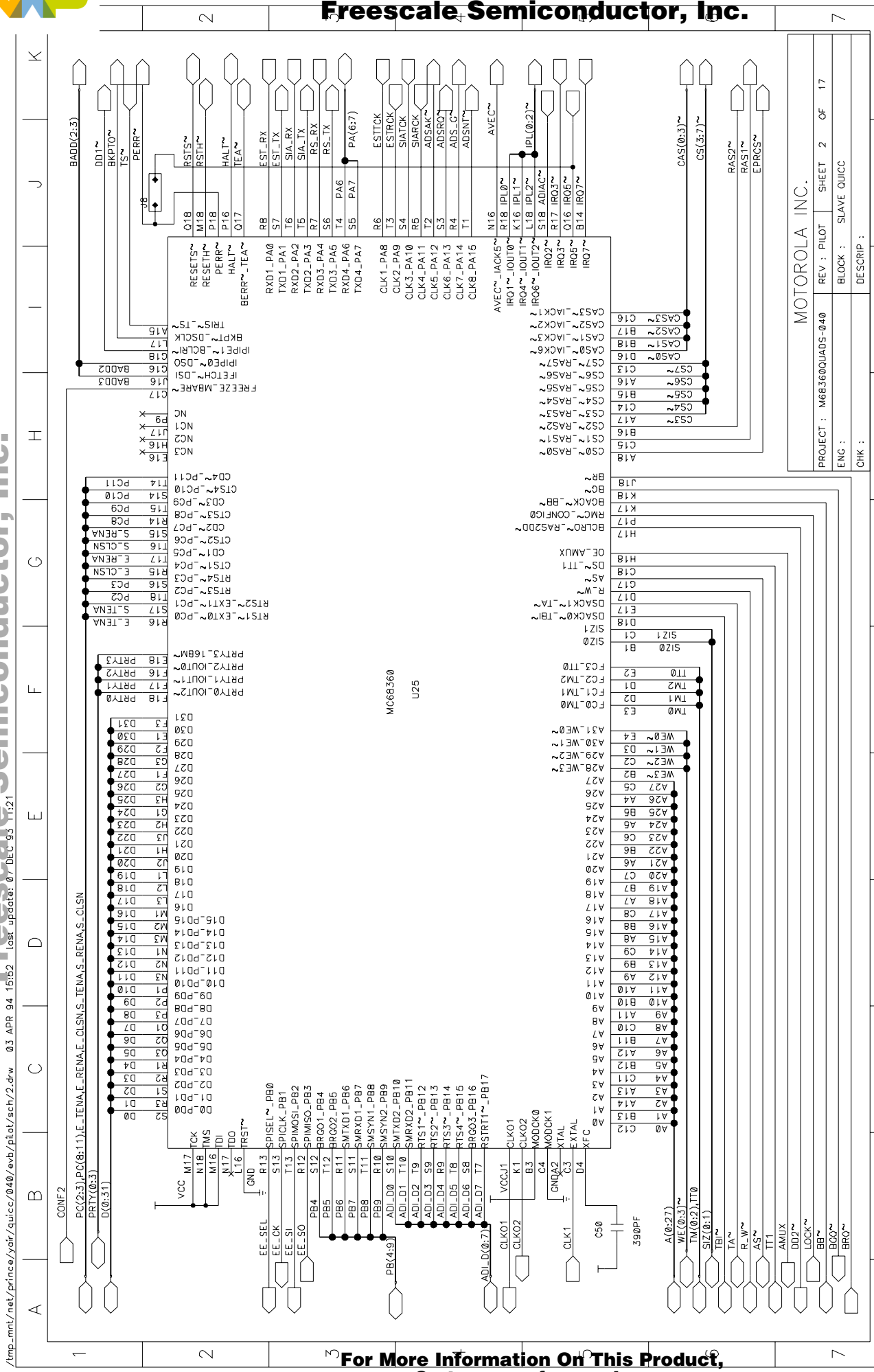
```
GLOBAL.SETF = GND

GLOBAL.RSTF = GND
```

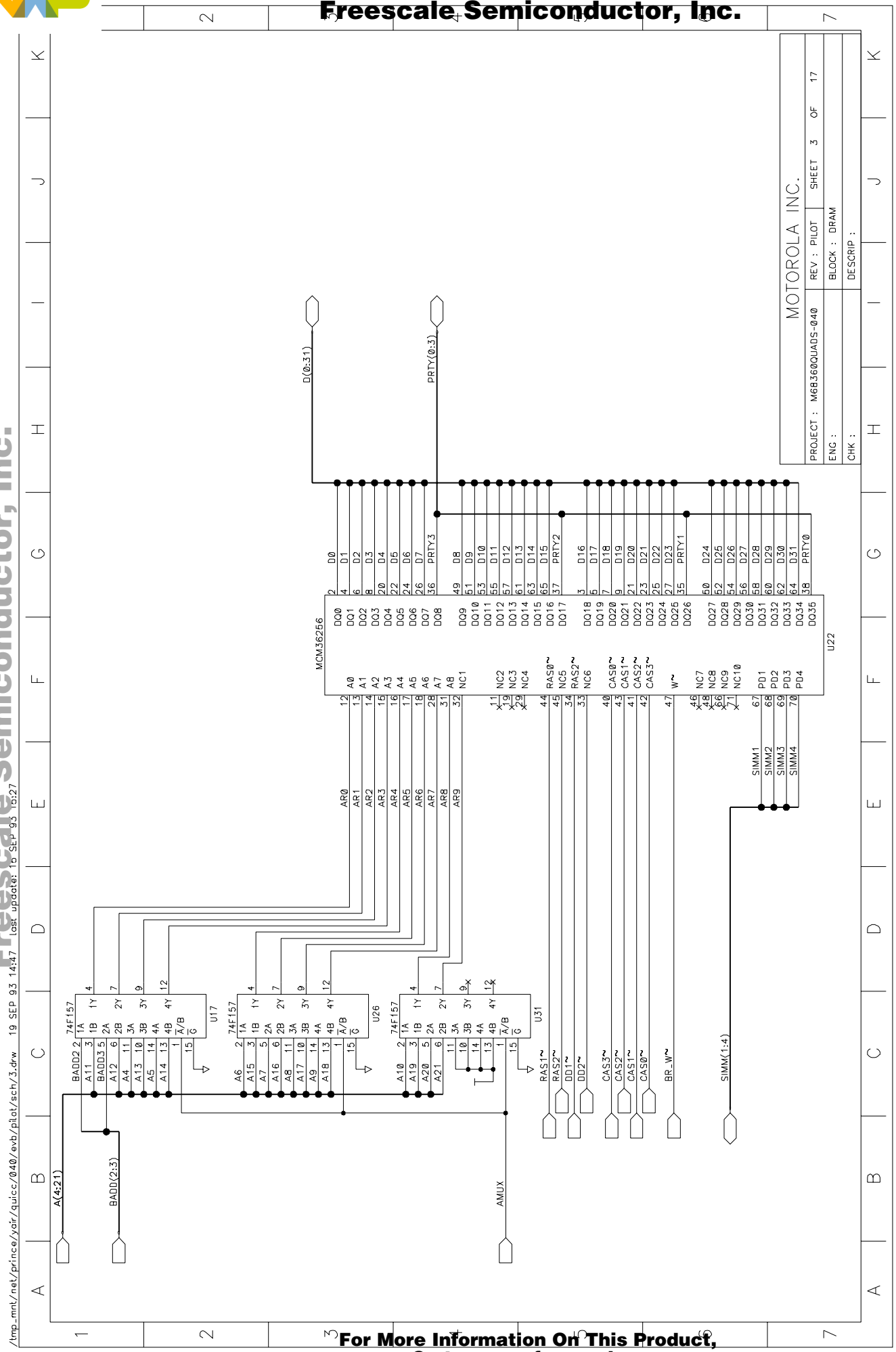
C.5 U32 - Bursting Sram Controller

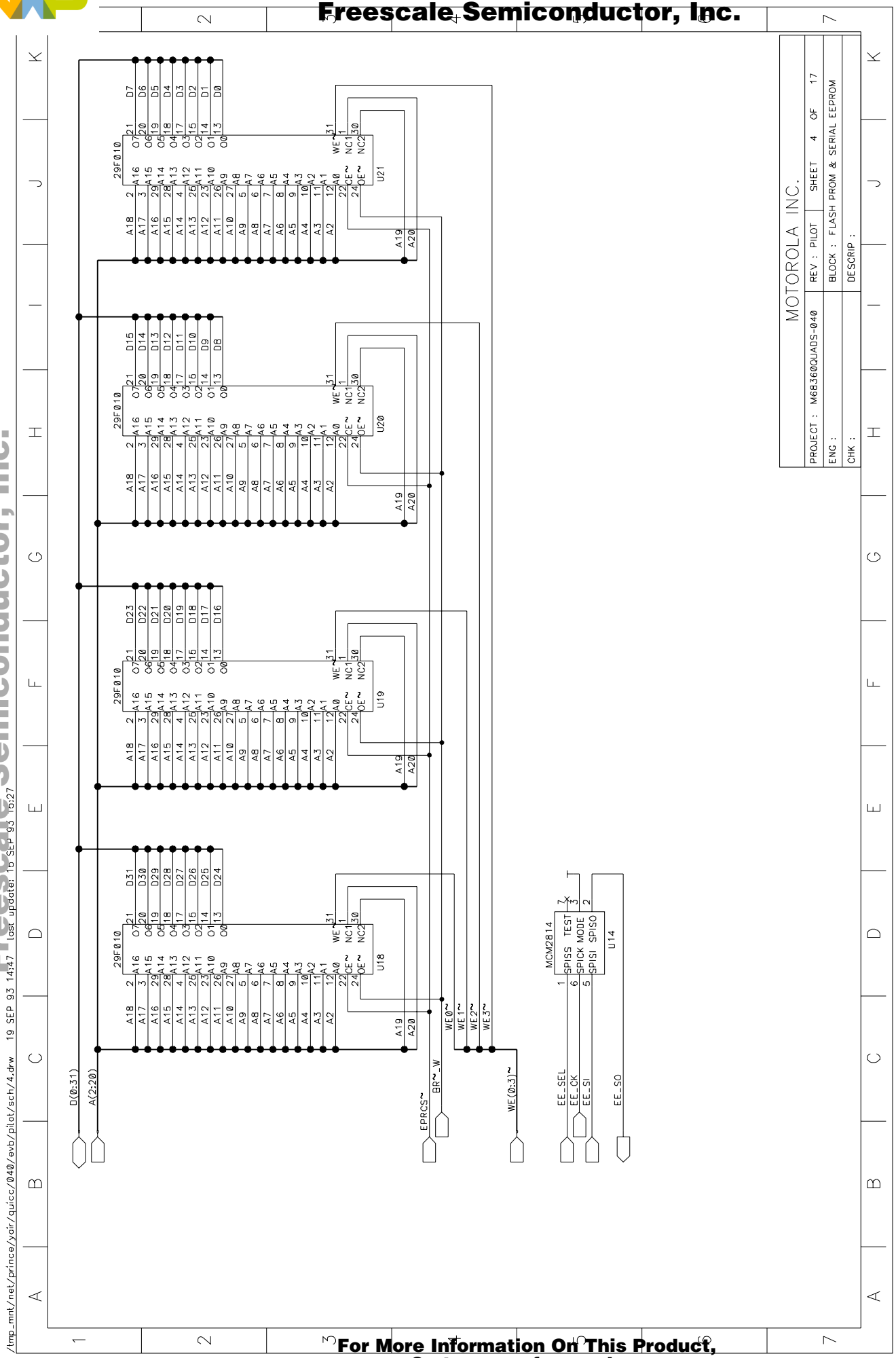
```
  Title       SRAMCONT
  Pattern     SRAMCNT.pds
  Revision    PILOT.0
  Date        15,8,93
;*************************************************************
  CHIP  SRAMCNT  PAL16R4
;*************************************************************************
; This pal serves as a bursting sram controller, for the QUICC040EVB.
; SRMG(1:2) are active-low G (oe) for the sram banks.
; TSC is a delayed TS~
; BAA(1:2) are active-low Burst Address Advance for the srams.
; BAA should be driven to the srams only during burst access and in
; burst write cycle one clock later than in burst read.
; SAS is a one clock delayed AS.
;*************************************************************************

  CLK  CS3 TS TIP AS SIZ0 SIZ1 TA R_W GND
;  1    2  3   4  5    6    7  8   9  10

  OE   CS4 NC SAS BAA2 TSC BAA1 SRMG2 SRMG1 VCC
;  11   12  13 14   15  16   17   18    19    20

;*************************************************************

  EQUATIONS
;**************

  /SRMG1 = /CS3 * R_W

  SRMG1.TRST = VCC

  /SRMG2 = /CS4 * R_W

  SRMG2.TRST = VCC

  /TSC := /TS
       + /AS * SAS
```

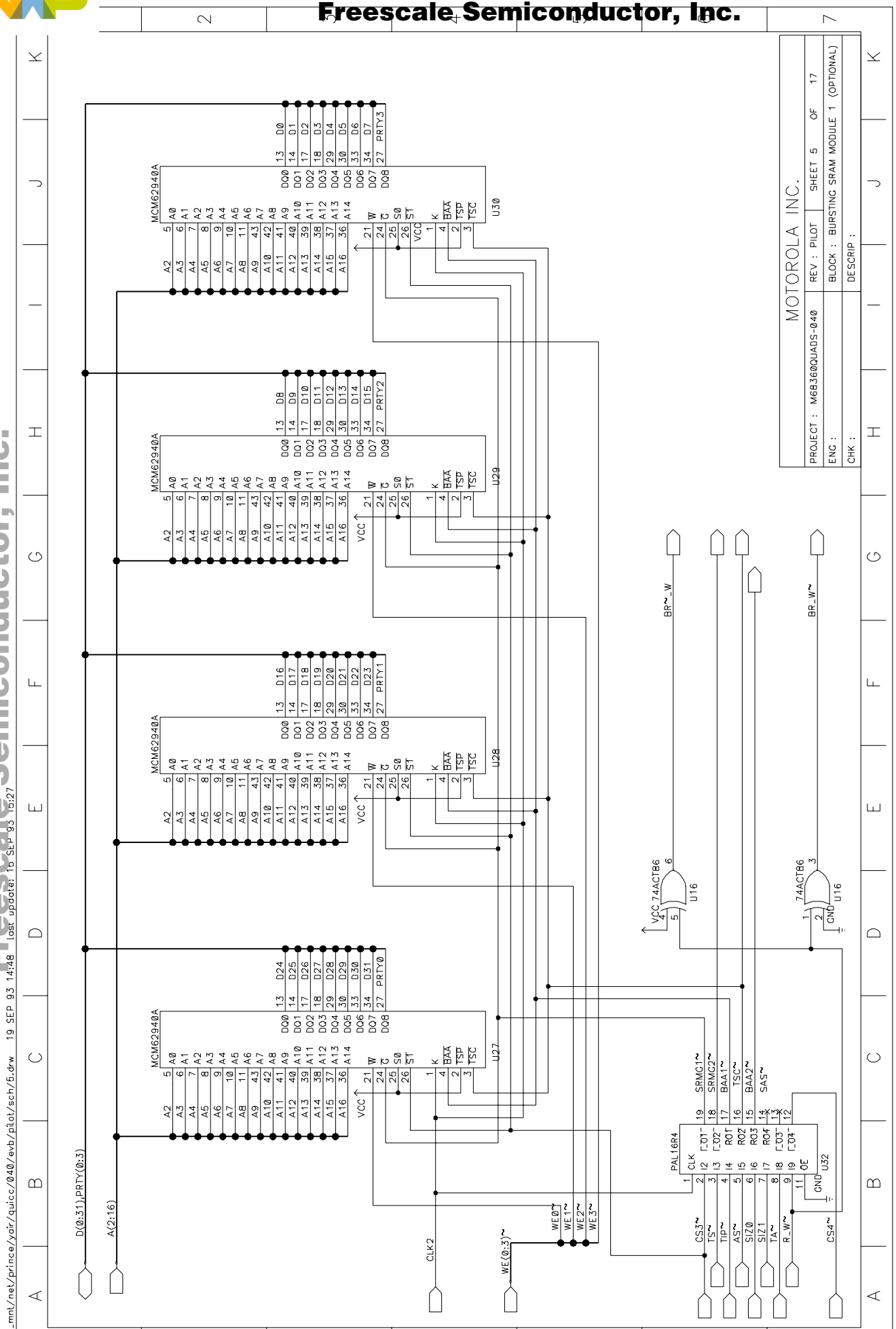
```
/BAA1 := SIZ1 * SIZ0 * /TSC * /CS3 * R_W * TA * /TIP  ; burst read
      + SIZ1 * SIZ0 * TSC * /CS3 * /R_W * /TA * /TIP      ; burst write BAA~ should be asserted
                                                            ; one clock later
      + /BAA1 * /CS3

/BAA2 := SIZ1 * SIZ0 * /TSC * /CS4 * R_W * TA * /TIP   ; burst read
      + SIZ1 * SIZ0 * TSC * /CS4 * /R_W * /TA * /TIP       ; burst write BAA~ should be asserted
                                                            ; one clock later
      + /BAA2 * /CS4

/SAS := /AS


CS4.TRST = GND; input
```











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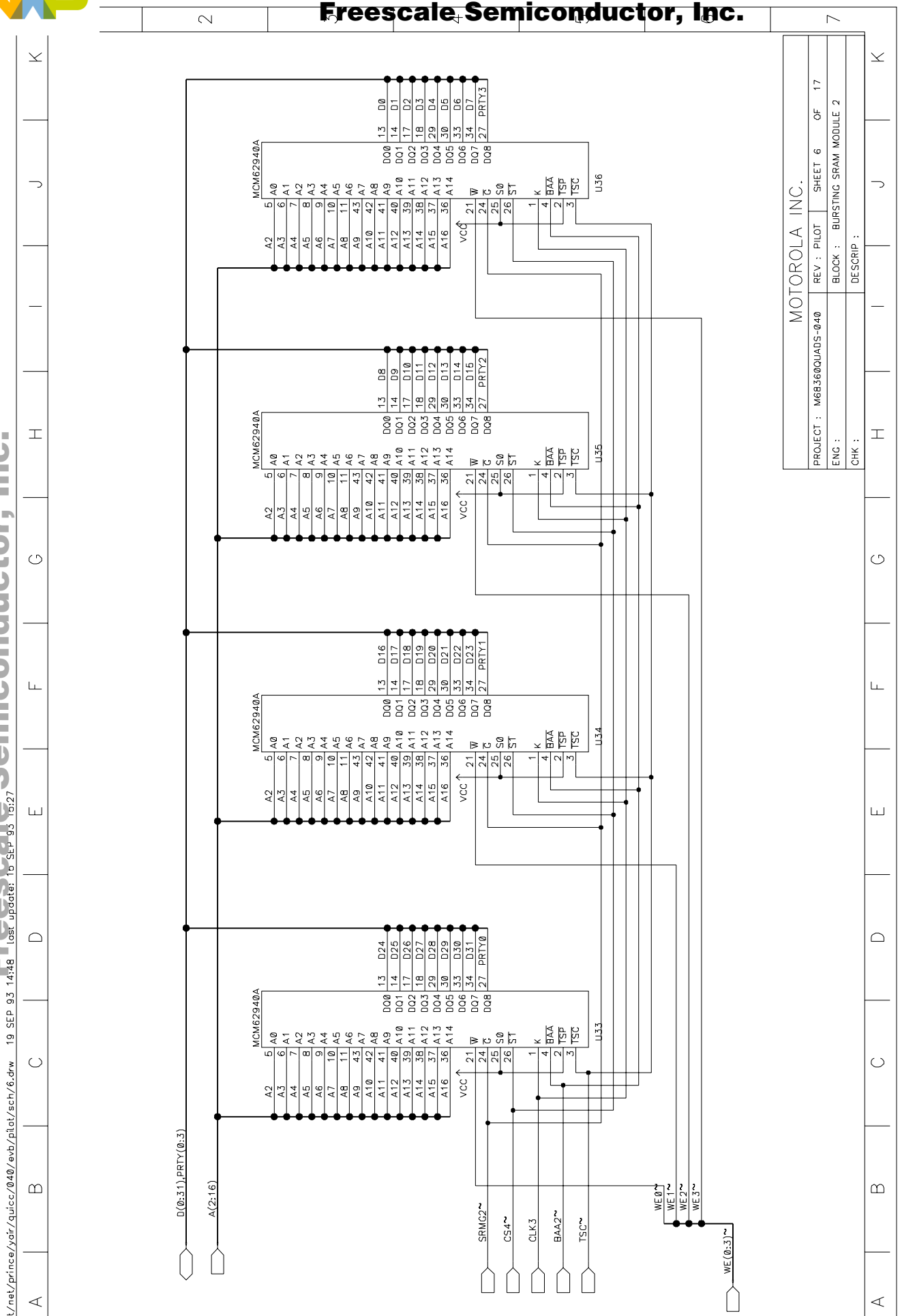

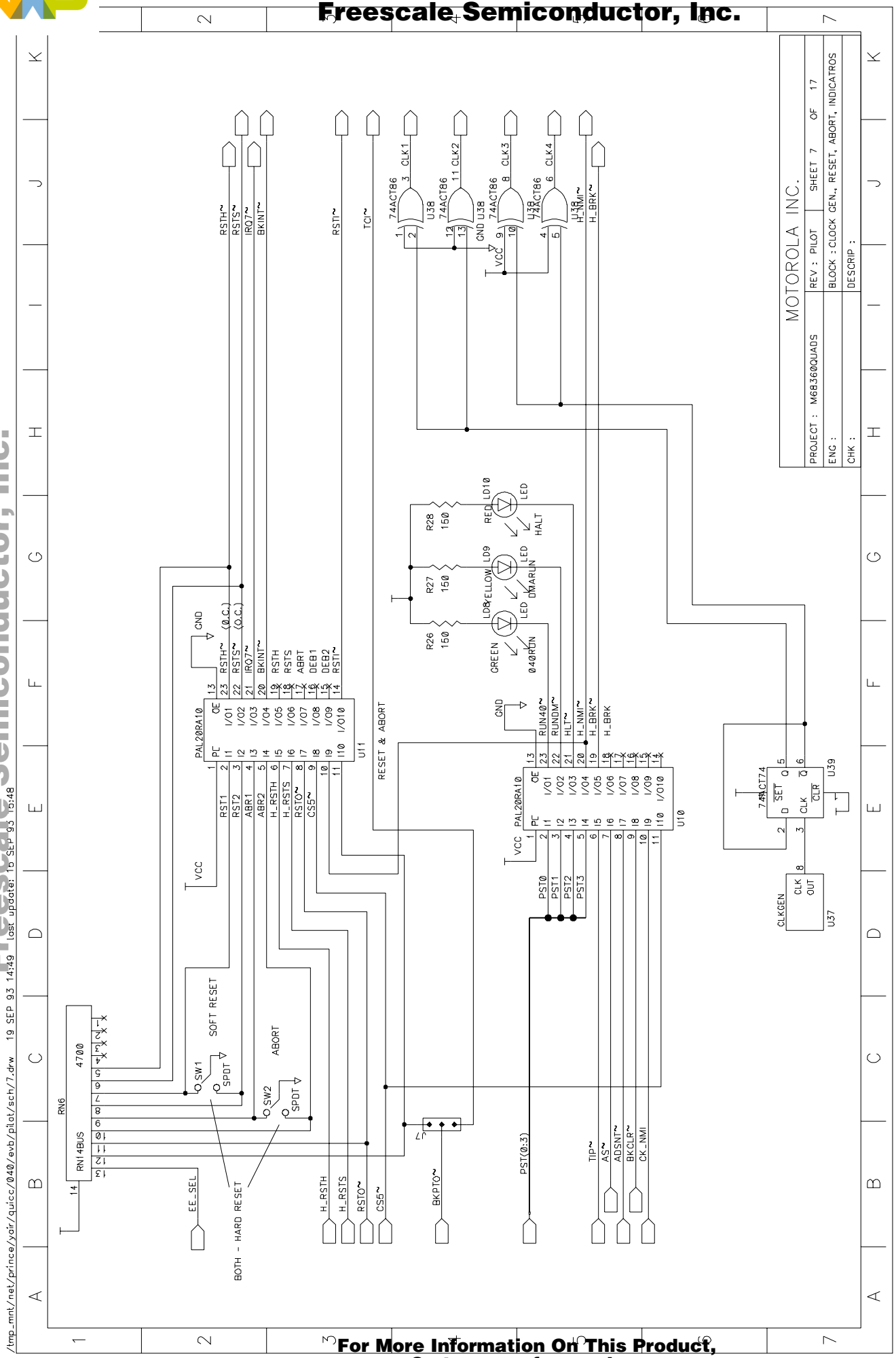

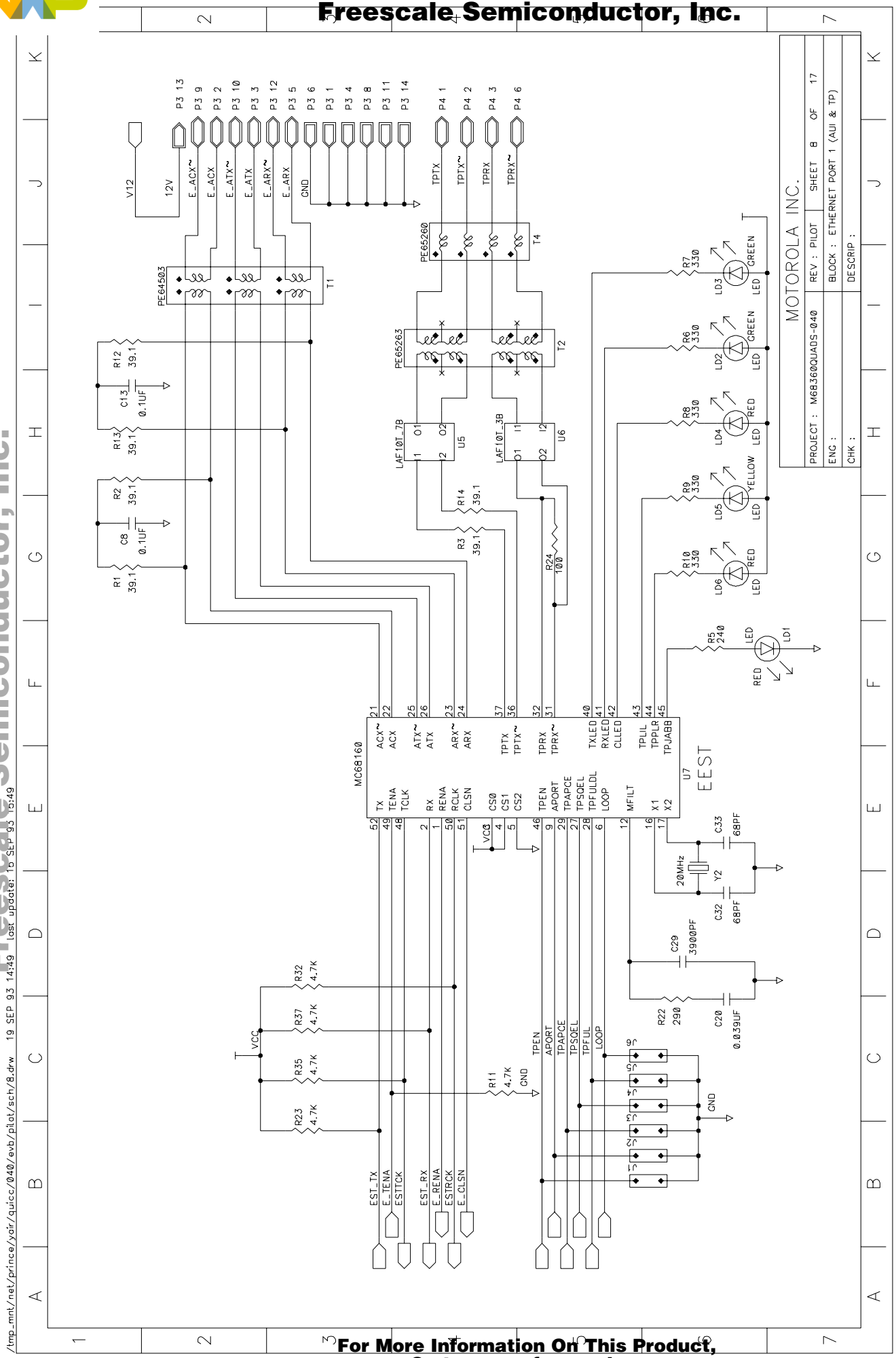
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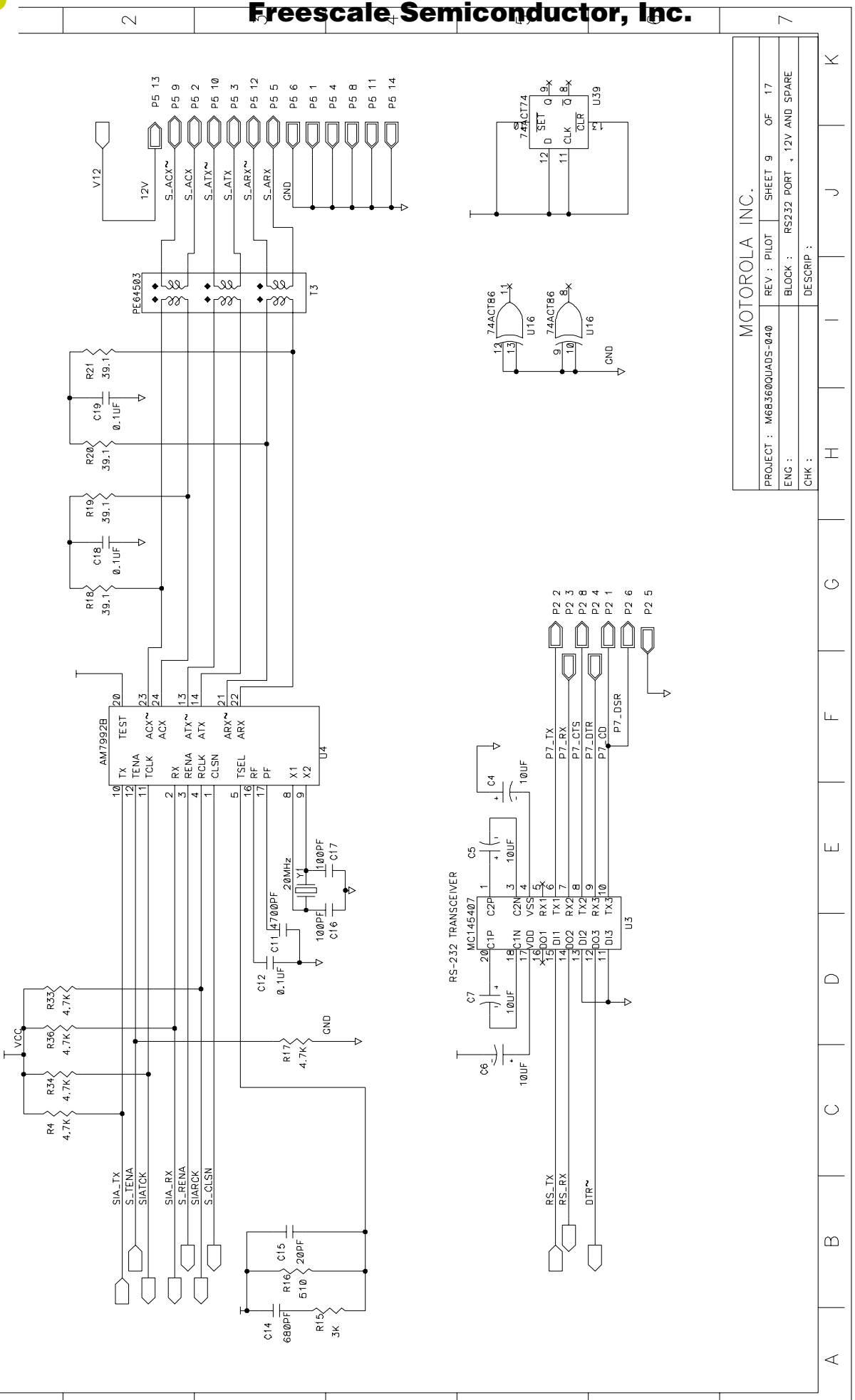
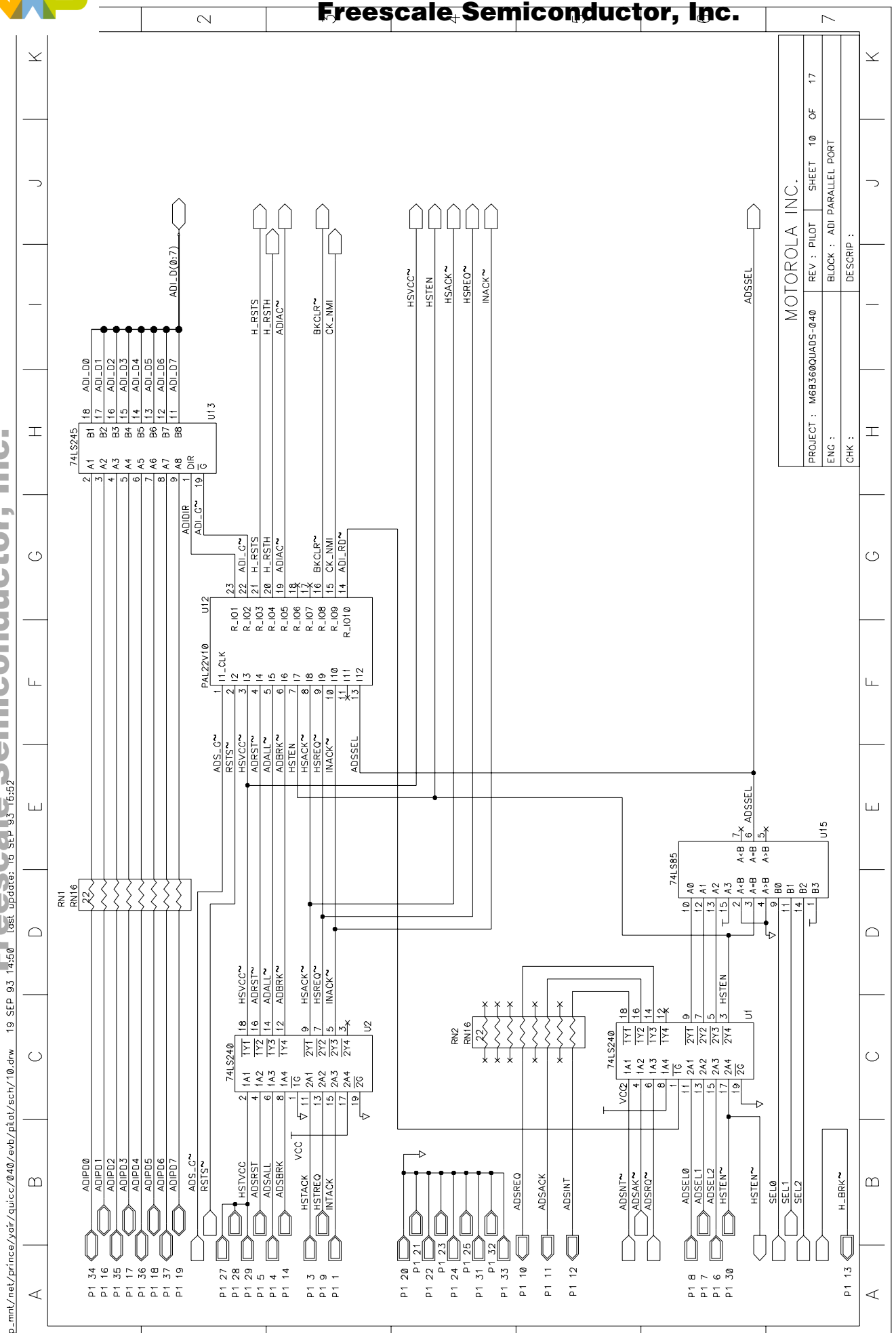
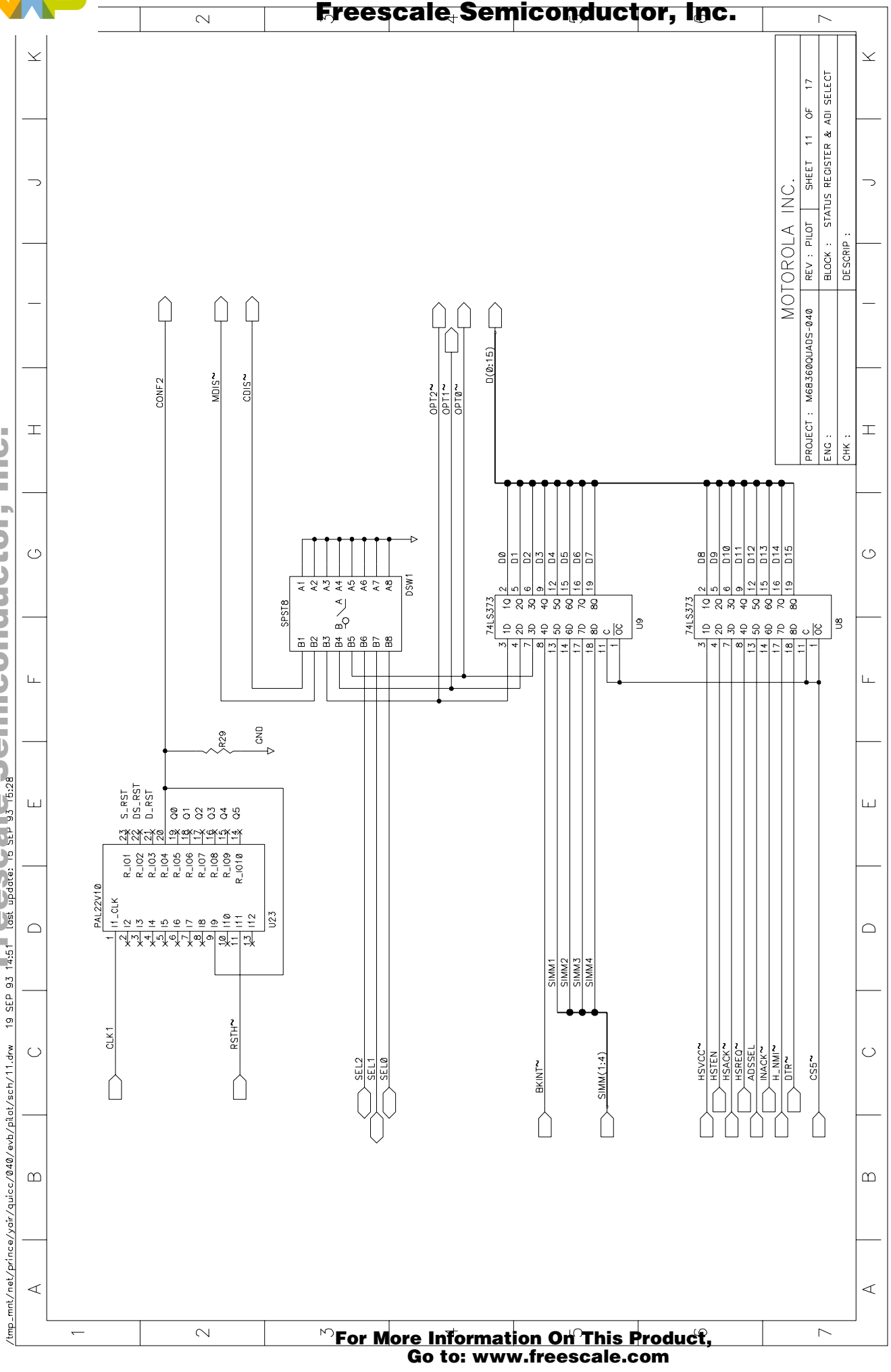
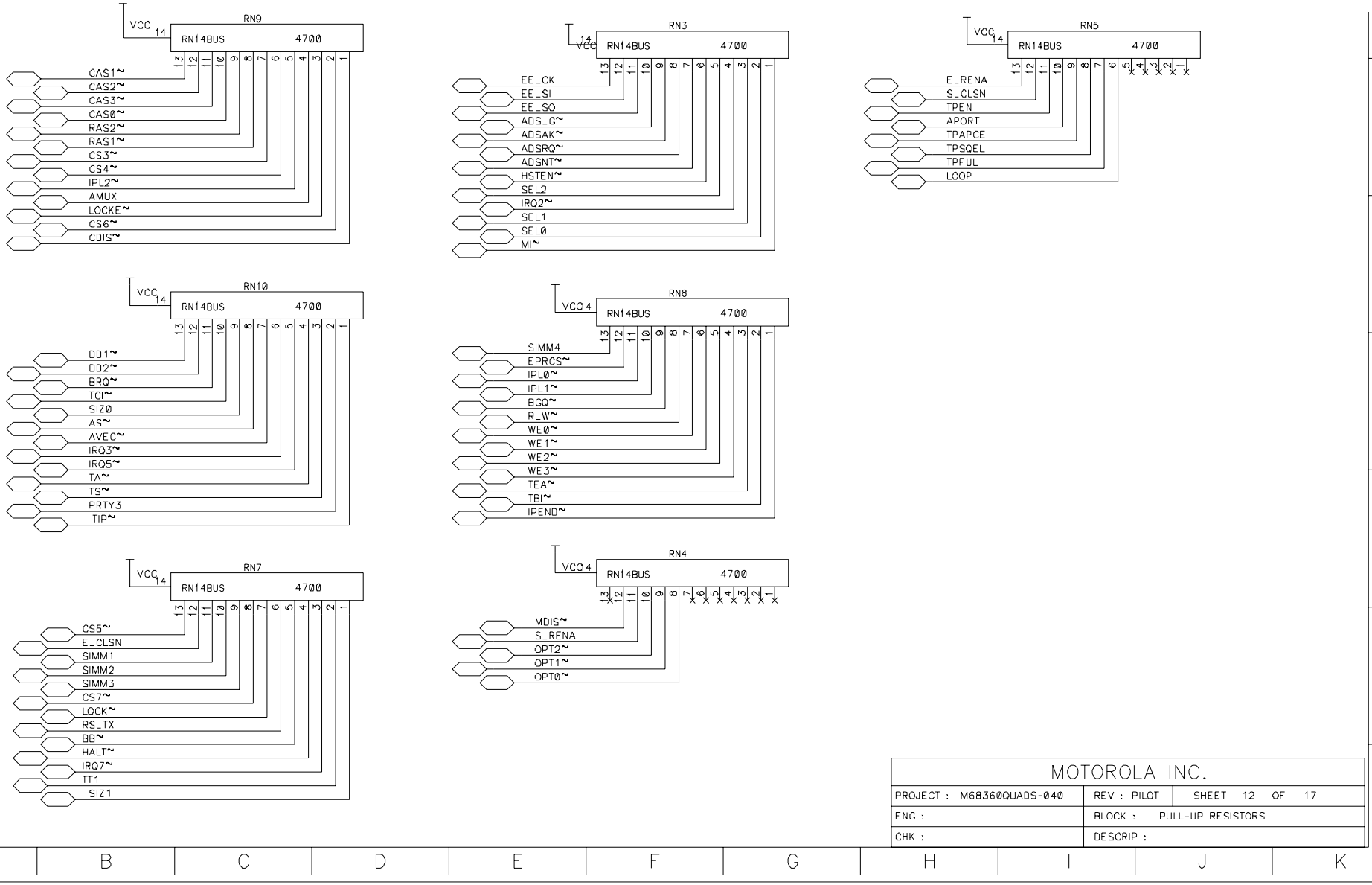
PROJECT : M68360QUADS-040
REV : PILOT
SHEET 8 OF 17
ENG :
BLOCK : ETHERNET PORT 1 (AUI & TP)
CHK :
DESCRIP :
/tmp_mnt/net/prince/yair/quicc/040/evb/pilot/sch/8.drw 19 SEP 93 14:49 last update: 16 SEP 93 15:49
Freescale Semiconductor, Inc.
MC68160
EEST
U7
PE64503
PE65260
PE65263
LAF10T_7B
LAF10T_3B
20MHz
V12
12V
GND
VCC
LED
RED
YELLOW
GREEN

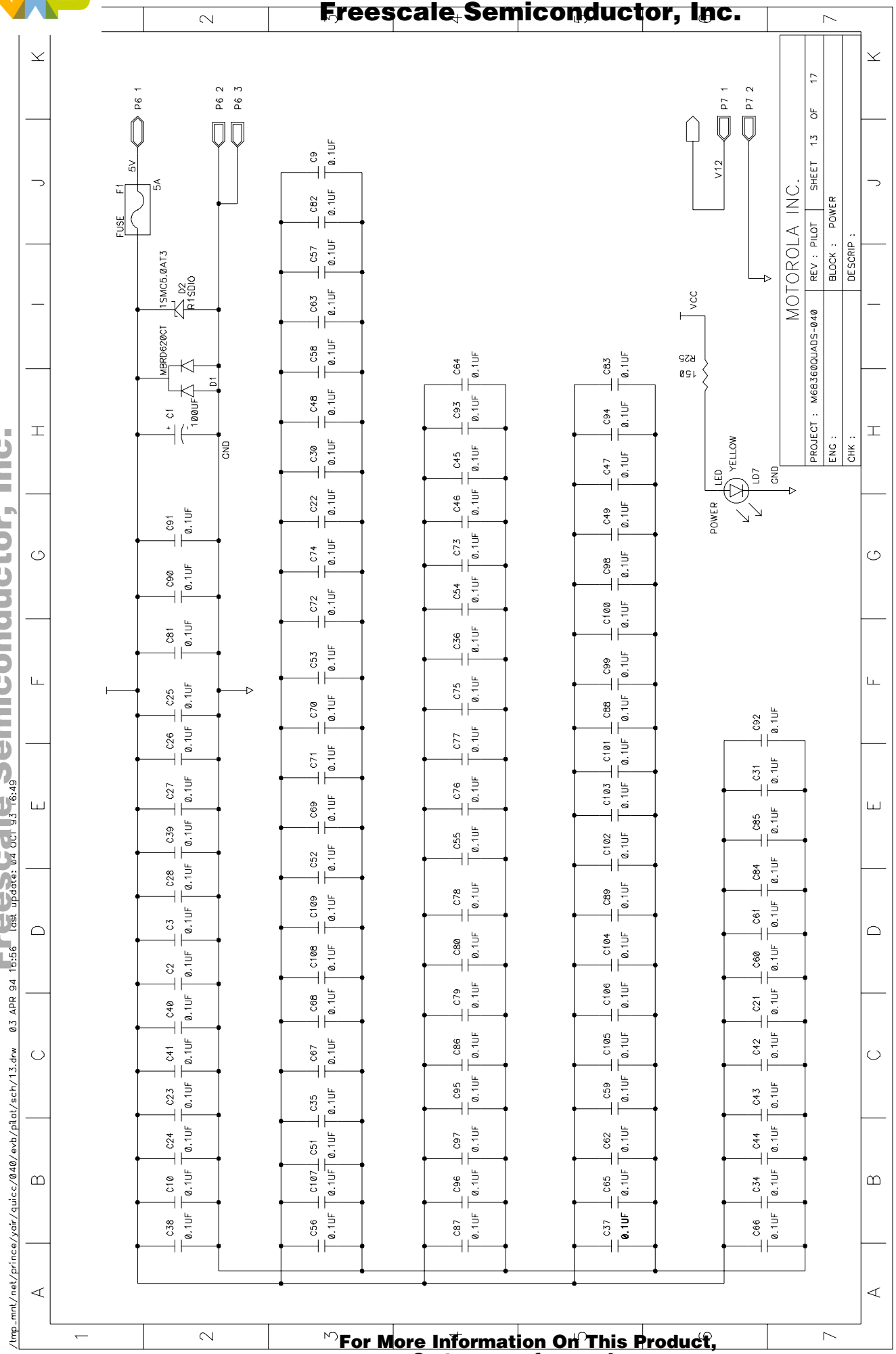


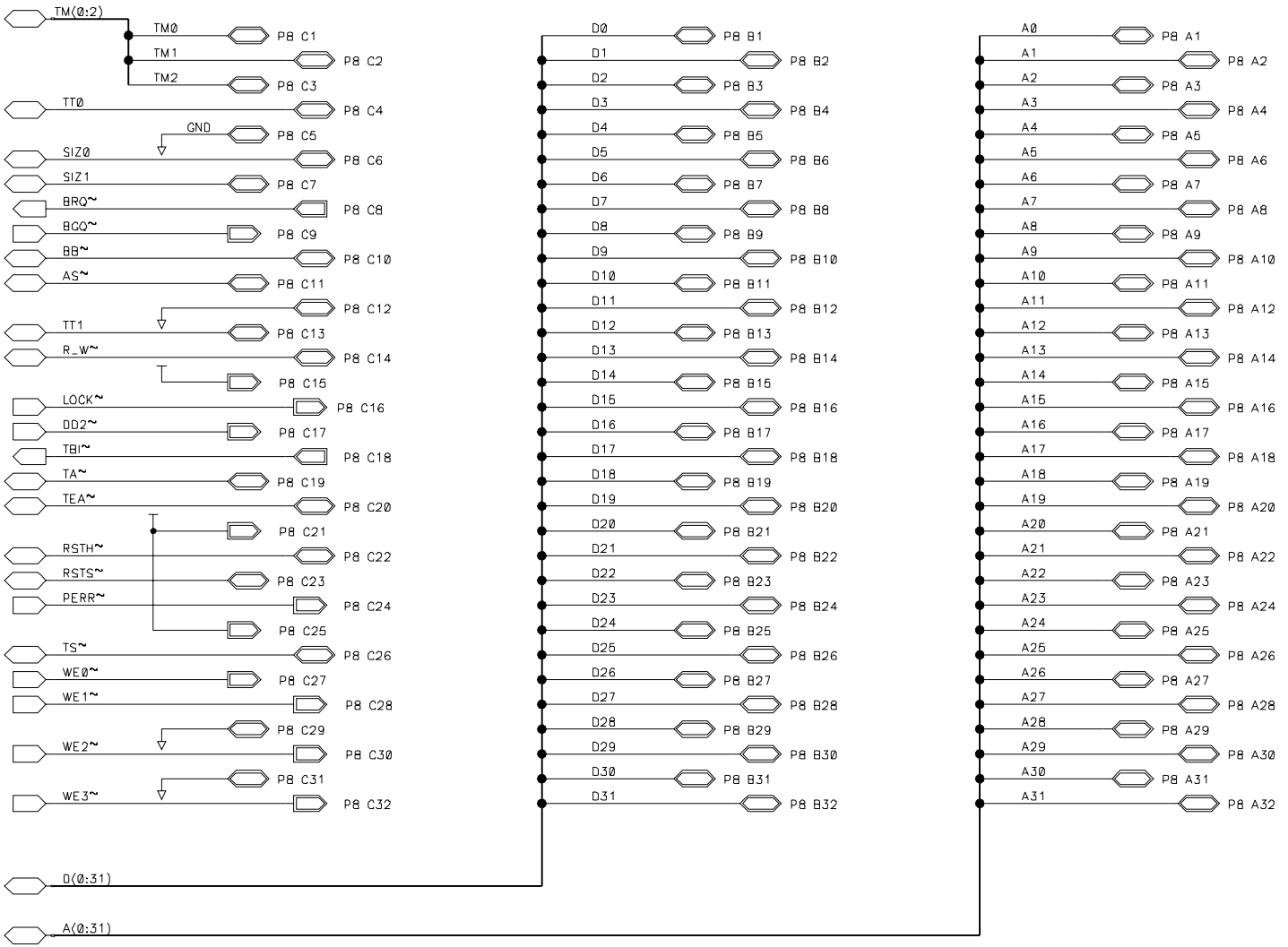




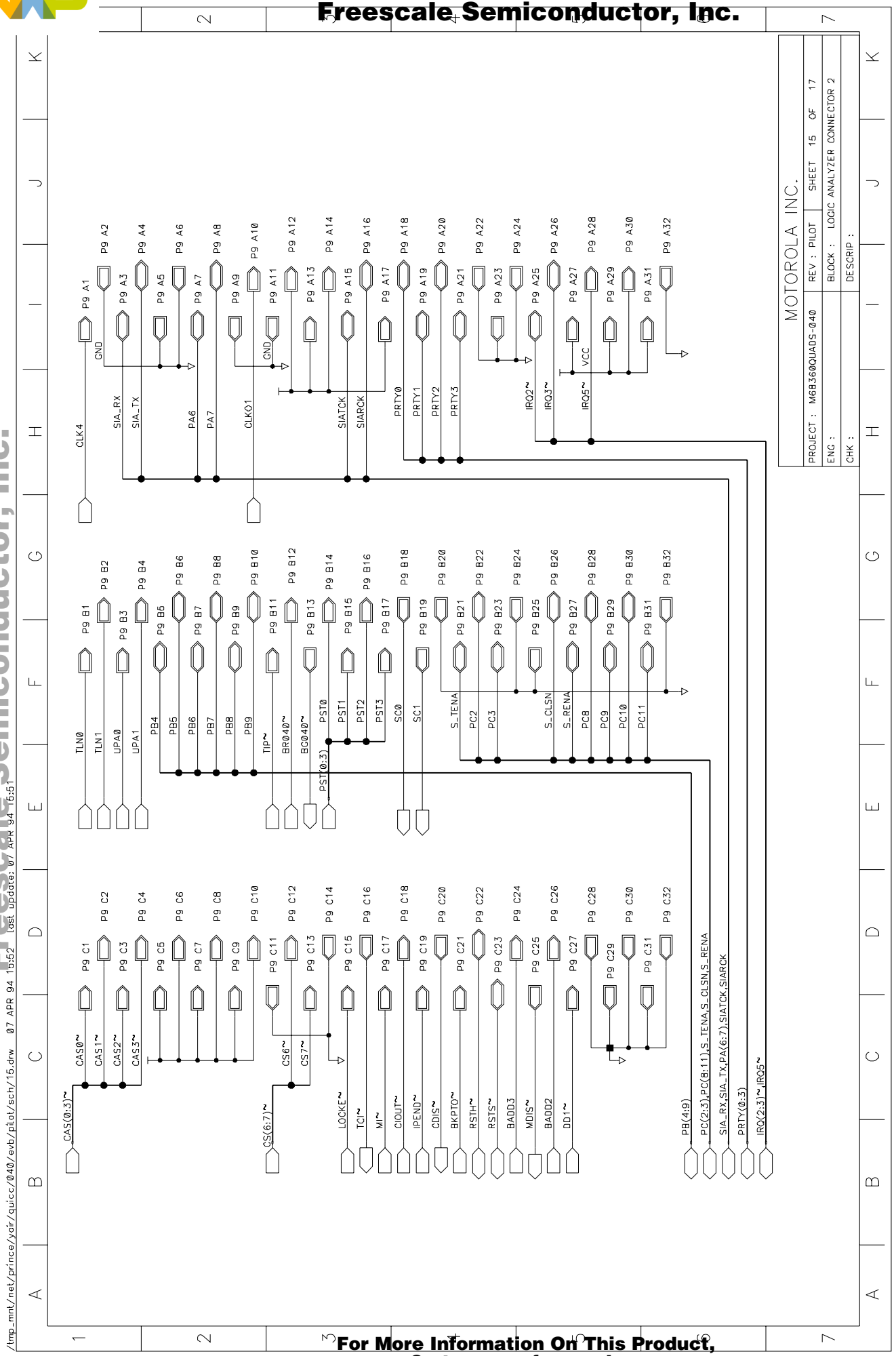


MOTOROLA INC.		
PROJECT : M68360QUADS-040	REV : PILOT	SHEET 12 OF 17
ENG :	BLOCK : PULL-UP RESISTORS	
CHK :	DESCRIP :	





MOTOROLA INC.		
PROJECT : M68360QUADS -040	REV : PILOT	SHEET 14 OF 17
ENG :	BLOCK : LOGIC ANALYZER CONNECTORS 1	
CHK :	DESCRIP :	



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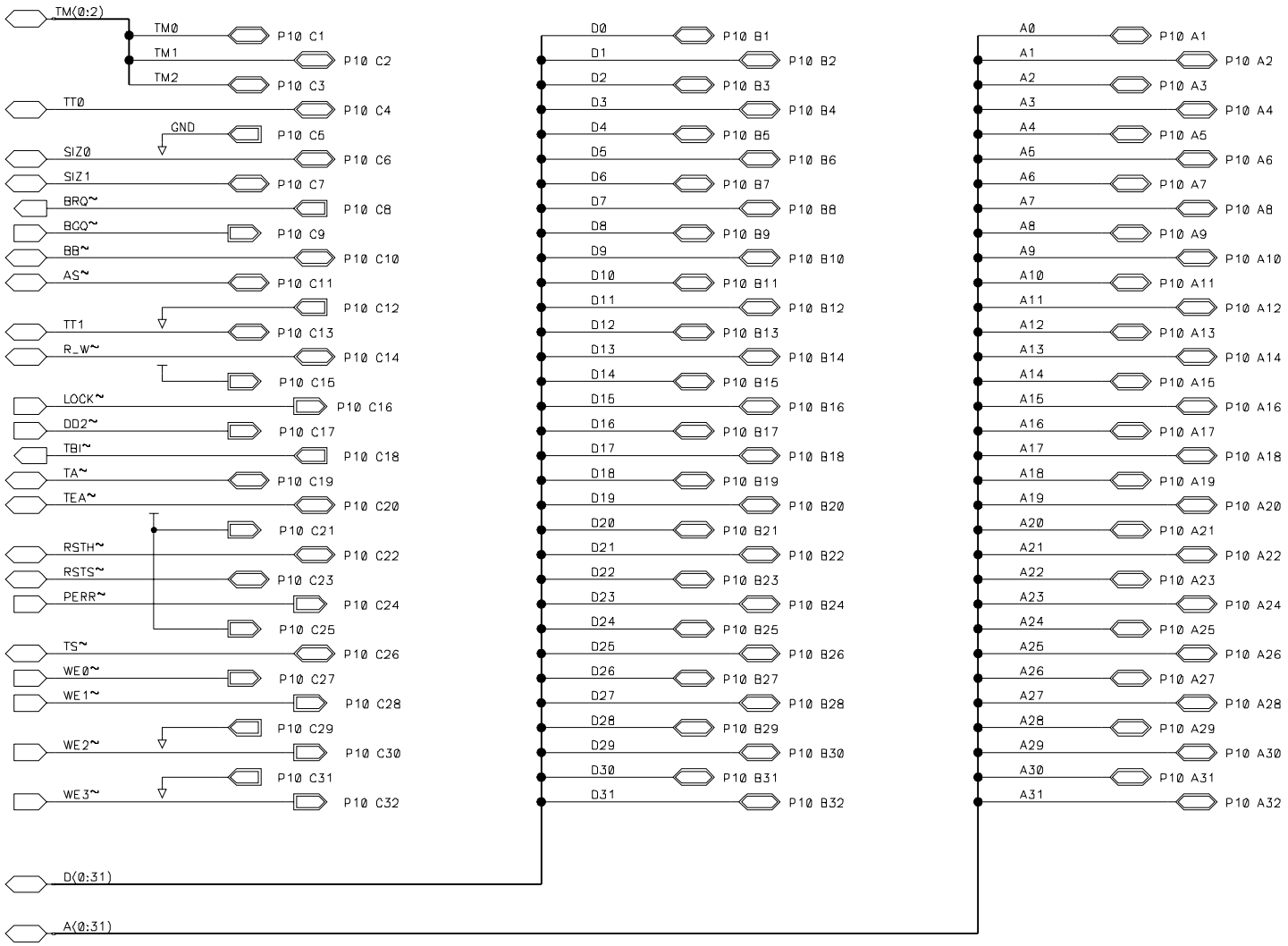
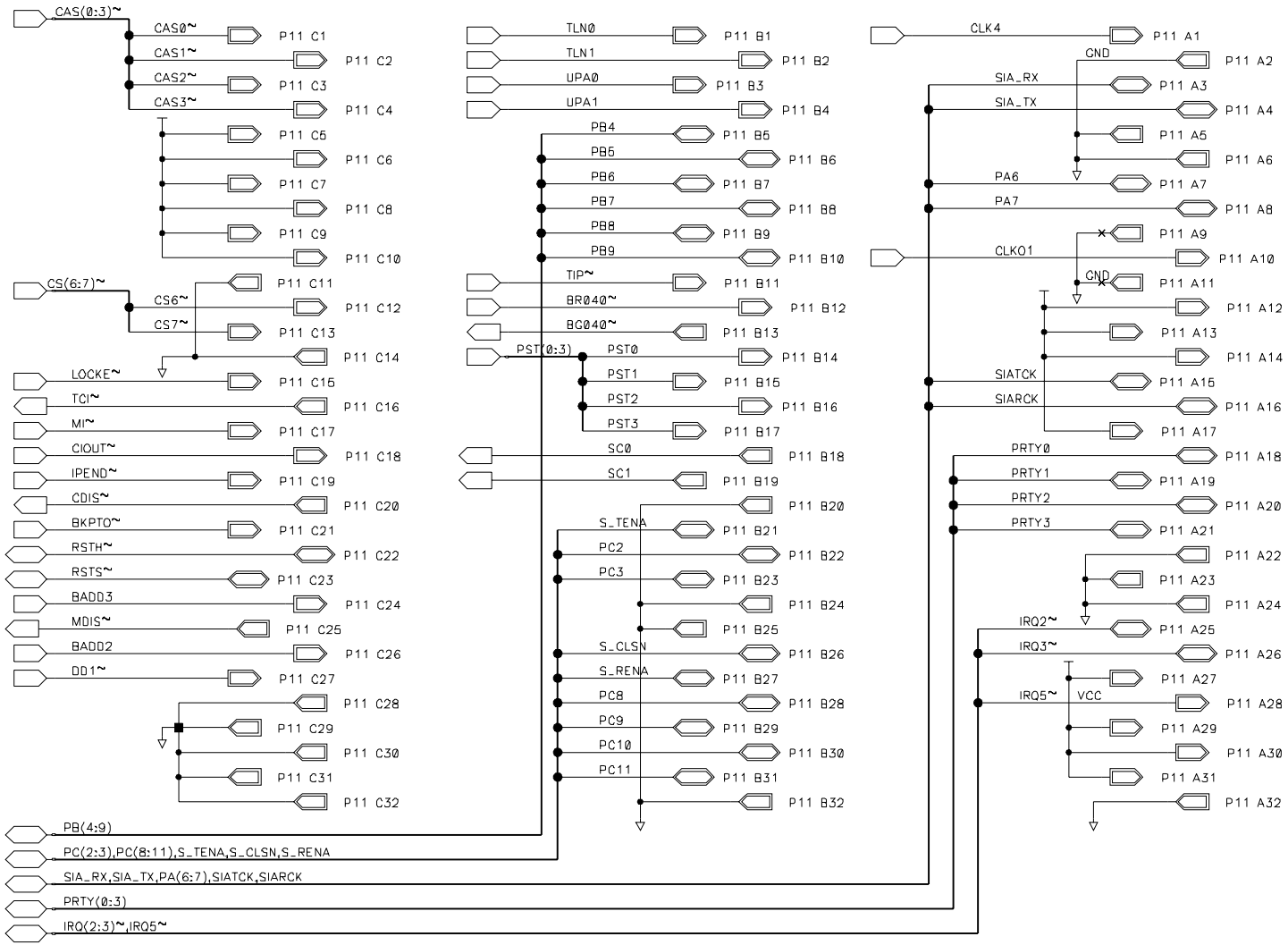


MOTOROLA INC.		
PROJECT : M68360QUADS-040	REV : PILOT	SHEET 16 OF 17
ENG :	BLOCK : EXPANSION CONNECTOR no. 1	
CHK :	DESCRIP :	



MOTOROLA INC.		
PROJECT : M68360QUADS-040	REV : PILOT	SHEET 17 OF 17
ENG :	BLOCK : EXPANSION CONNECTOR no. 2	
CHK :	DESCRIP :	