MPC8555E Configurable Development System Reference Manual

Supports
MPC8555E
MPC8541E

MPC8555CDSx3RM
Rev. 1, 11/2006

freescale semiconductor

Contents

Contents

Chapter 4
CDS Daughtercard Architecture

Contents

Chapter 5
Arcadia Motherboard Architecture

Contents

Contents

Contents

Figures

Figures

Tables

Tables

About This Book

The primary objective of this reference manual is to define the functionality of the MPC8555E configurable development system (CDS). It is also intended to describe in detail the configurability of the CDS through the description of individual components and their interchangeability. Included is detailed descriptions of the physical design, device architecture, and testing/debugging procedures.

Audience

It is assumed that the reader understands operating systems, microprocessor system design, and the basic principles of RISC processing.

Organization

Following is a summary and a brief description of the major parts of this reference manual:

- Chapter 1, "Introduction," provides a high-level description of features and functionality of the CDS. Included is a list of the configurable features, as well as basic block diagrams.
- Chapter 2, "Quick Start-Up Guide," describes step-by-step how to bring up a CDS development board.
- Chapter 3, "CDS Carrier Architecture," describes in detail the CDS carrier system. It describes the physical layout and assembly, as well as basic and detailed system architecture. It elaborates on usage and testing/debugging procedures.
- Chapter 4, "CDS Daughtercard Architecture," covers the CDS daughtercard design in more detail. It describes the physical layout as well as part connections and device interfaces. It includes a detailed description of the system architecture, along with the device configuration and debugging procedures.
- Chapter 5, "Arcadia Motherboard Architecture," describes the design information on the Arcadia reference platform.
- Chapter 6, "CDS IOCard Architecture," describes in detail the IOCard. It elaborates on the physical architecture and device connections, as well as the power management and usage.
- Chapter 7, "uTCOM Architecture," describes the uTCOM interface, as well as its physical properties.
- Appendix A, "Revision History," describes the major differences between revisions of this reference manual.
- Appendix B, "Pinouts," contains detailed pinout specifications for the CDS. It includes:
  - Carrier/daughtercard connectors pinout
  - IOCard connector pinout
  - uTCOM connector pinout

- Appendix C, “CDS Carrier BOM, Rev. 1.2”
- Appendix D, “CDS Carrier Schematics, Rev. 1.2”
- Appendix E, “CDS Carrier BOM, Rev. 1.3”
- Appendix F, “CDS Carrier Schematics, Rev. 1.3”
- Appendix G, “CDS CDC BOM”
- Appendix H, “CDS CPU Schematics (CDC)”
- Appendix I, “CDS I/O Board Schematics”
- Appendix J, “CDS uTCOM Schematics”
- Appendix K, “CDS Arcadia BOM”
- Appendix L, “CDS Arcadia X3 Schematics”
- This reference manual also includes a glossary.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the architecture.

General Information

The following documentation provides useful information about the CDS architecture:

- *The PowerPC Architecture: A Specification for a New Family of RISC Processors*, Second Edition, by International Business Machines, Inc.

  For updates to the specification, see http://www.austin.ibm.com/tech/ppc-chg.html.
- *Computer Architecture: A Quantitative Approach*, Third Edition, by John L. Hennessy and David A. Patterson.
- *Computer Organization and Design: The Hardware/Software Interface*, Second Edition, by David A. Patterson and John L. Hennessy.

Signal Conventions

$\overline{\text{OVERBAR}}$	An overbar indicates that a signal is active-low.
lowercase_italics	Lowercase italics is used to indicate internal signals.
lowercase_plaintext	Lowercase plain text is used to indicate signals that are used for configuration.

Acronyms and Abbreviations

Table i contains acronyms and abbreviations used in this document.

Table i. Glossary of Terms

Term	Description
ATM	Asynchronous transfer mode
CARRIER	HIP-compliant HIPcard such as CDS, Elysium, etc.
CDC	CPU daughtercard
CDS	Configurable development system; customer development system
CPM	Communications processing machine
Daughtercard	CPU-specific daughtercard which connects to a carrier board
DDR	Double-data rate
GMII	Gigabit media-independent interface
HIP	Hardware interoperability platform
IOCARD	IO breakout card for a carrier board
LB	Local bus (that is, Flash/SRAM/SDRAM interface)
MAC	Media access control
MII	Media-independent interface
Motherboard	HIP-compliant motherboard such as Arcadia, etc.
OUI	Organizationally unique identifier
PC-1600	DDR providing 1600 MB/s bandwidth (@8 bytes/clk = 200 MHz)
PC-2100	DDR providing 2100 MB/s bandwidth (@8 bytes/clk = 266 MHz)
PHY	Physical interface
PM	Performance monitor
RIO	RapidIO
TSEC	Triple-speed Ethernet controller (10/100/1G speeds)
TWG	Technical working group

Chapter 1
Introduction

1.1 Background

The configurable development system (CDS) was developed to support a wide range of Power Architecture™ processors, such as the MPC8555E and the MPC8541E. . The system is primarily a development and evaluation system, which is enhanced by its modular design, making it highly configurable.

1.2 Scope

This reference manual describes the Freescale CDS development platform. It provides details on the MPC8555E CDS hardware configuration and functionality. It is intended primarily as a guide for hardware and software designers.

1.3 Overview

The CDS system is the middle ground between evaluation and test boards. It is more configurable and flexible than an evaluation board, but it is not as configurable as a test board, in which every component can be tested and examined. Where it lacks configurability, its design has options for the most common settings.

Two MPC8555E CDS development system configurations are described. The configurations consist of different board revisions which are referenced throughout this manual as Configuration 1 or Configuration 2. The configurations are:

- Configuration 1
  - Arcadia, Rev. 3.1
  - Carrier card, Rev. 1.2
  - CPU card, Rev. 1.1
  - I/O card, Rev. 1.1
- Configuration 2
  - Arcadia, Rev. 3.1
  - Carrier card, Rev. 1.3
  - CPU card, Rev. 1.1

Refer to Appendix F, “CDS Carrier Schematics, Rev. 1.3,” Table F-1, for hardware differences between carrier card, Rev. 1.2 and Rev. 1.3.

1.3.1 Features

NOTE

The CDS system can be configured to boot as MPC8555E or MPC8541E. The CDS system by default is configured as MPC8555E. To evaluate the CDS system as MPC8541E, refer to Section 2.5, "Default Switch Configuration Table," switch-4, bit-4 on CPU card.

A CDS system includes the following features:

- Processor-specific daughtercard, featuring
  - One or more Freescale MPC8555E processor(s)
  - ECC-compatible DDR-I (processor-specific type)
  - Test features (JTAG, P6880 passive probe for critical routes only)
    - P6880 'banjo' header probing critical signals only
    - All other debug is via carrier or DIMM debug module
  - Local support for secondary interfaces (such as PCI) as needed
    - PCI32 header (3.3 V, 32-bit, PCI-X, 33/66 MHz compatible) where required
  - Local switching power supply, supplying VDD (VCORE)
    - Supplies up to 15 W (~1.1 V at 12 A)
    - Derivable from +5 or +3.3 V (not +12 V)
    - Programmable voltage via I2C configuration
  - I2C bus
    - ID EEPROM (256b) for card at 0x50
    - Configurable EEPROM (8K) for CPU at 0x57
    - Memory SPD EEPROM for memory at 0x51
    - Voltage monitoring
    - Configuration control
  - Local bus generation
    - Includes any necessary demultiplexing
    - Local SDRAM support (as appropriate)
  - High-speed/high-density connectors for all CPU signals except core power and memory
  - Configuration options
    - Switch programmable defaults
    - I2C remote configuration/override
  - Debug support
    - JTAG (COP) header
    - Monitoring LEDs
- Carrier board
  - Supports numerous processor daughtercards

— Supports two Ethernet ports on the carrier card at MII/GMII, and two Ethernet ports on the I/O adapter at MII/GMII, 10/100 or 1G rates (Configuration 1).

NOTE

In Configuration 1, Ethernet port #4 on the I/O card is not functional.

— Supports all four Ethernet ports on the carrier card. MII/GMII on Ethernet ports #1 and #2. RGMII on Ethernet ports #3 and #4, 10/100 or 1G rates (Configuration 2).

— Quickswitch-controlled routing of selected CPM signals between uTCOM header and local peripherals (optical ATM OC3/OC12 and/or 10/100 console Ethernet).

— UTOPIA L2/AdTech connector for OC12 ATM port

— Supports USB connector (as wires only—USB PHY is on the daughtercard, if needed)

— Supports serial port for Linux/U-Boot console I/O

— Differential probing on receive path with Tek P6880

— PCI/PCI-X 32/64 bits, 33/66 MHz

NOTE

PCI arbitration is not supported on the carrier card. The MPC8555CDS board does not support PCI-X mode.

— Includes IO adapter board (Configuration 1)

1.3.2 Diagrams

Figure 1-1 is a diagram of the CDS system for Configuration 1.

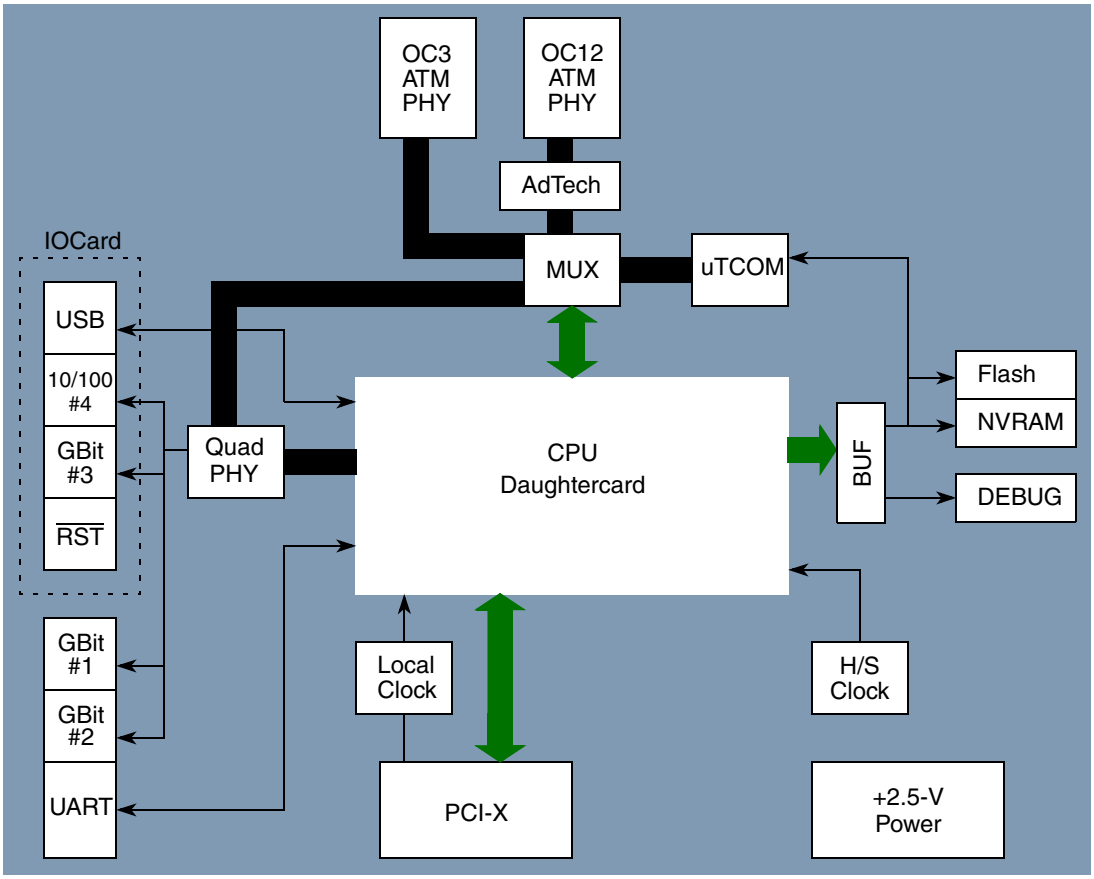


Figure 1-1. Carrier Block Diagram (Configuration 1)

Figure 1-2 is a diagram of the CDS system for Configuration 2.

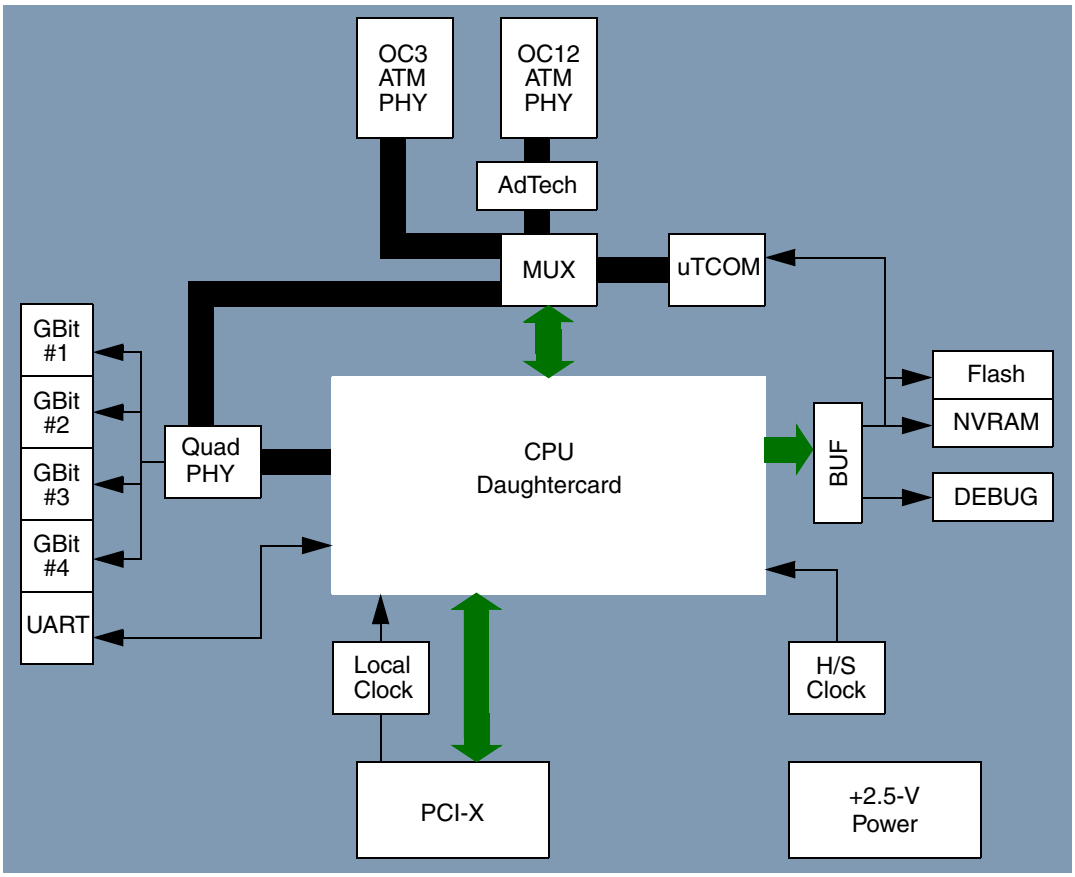


Figure 1-2. Carrier Block Diagram (Configuration 2)

Figure 1-3 is a diagram of a CDS daughtercard, or a CDC.

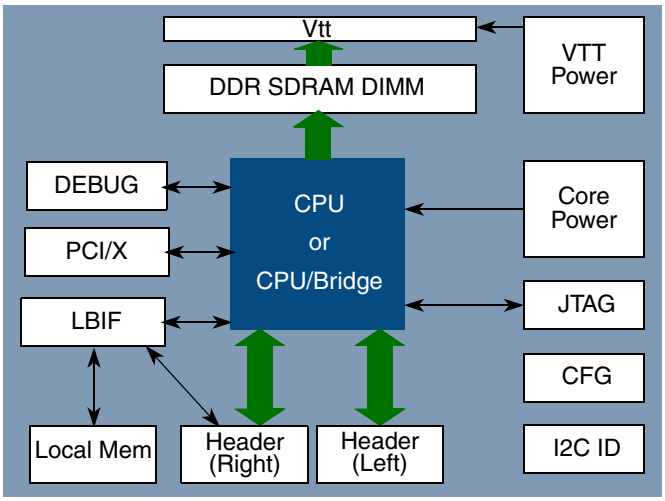


Figure 1-3. Daughtercard Block Diagram

This representation shows only one design, other daughtercards can be designed for different CPUs.

Chapter 2
Quick Start-Up Guide

This chapter provides a step-by-step guide for bringing up a CDS.

2.1 Hardware List

The hardware configurations consist of different board revisions which are referenced throughout this manual as Configuration 1 or Configuration 2. Refer to Appendix F, “CDS Carrier Schematics, Rev. 1.3,” Table F-1, for hardware differences between carrier card, Rev. 1.2 and Rev. 1.3. The configurations are:

- Configuration 1
  - Arcadia, Rev. 3.1
  - Carrier card, Rev. 1.2
  - CPU card, Rev. 1.1
  - I/O card, Rev. 1.1
- Configuration 2
  - Arcadia, Rev. 3.1
  - Carrier card, Rev. 1.3
  - CPU card, Rev. 1.1

The CDS system is installed in a PC box and includes a power supply. The CDS system is preloaded with U-boot and Linux BSP.

2.2 Hardware Installation

Remove the CDS system chassis from the cartons and perform the following steps:

NOTE

The carrier card and processor card are packaged together.

1. Insert memory module, noting the correct KEYING orientation, and snap into the socket. See Figure 2-1.

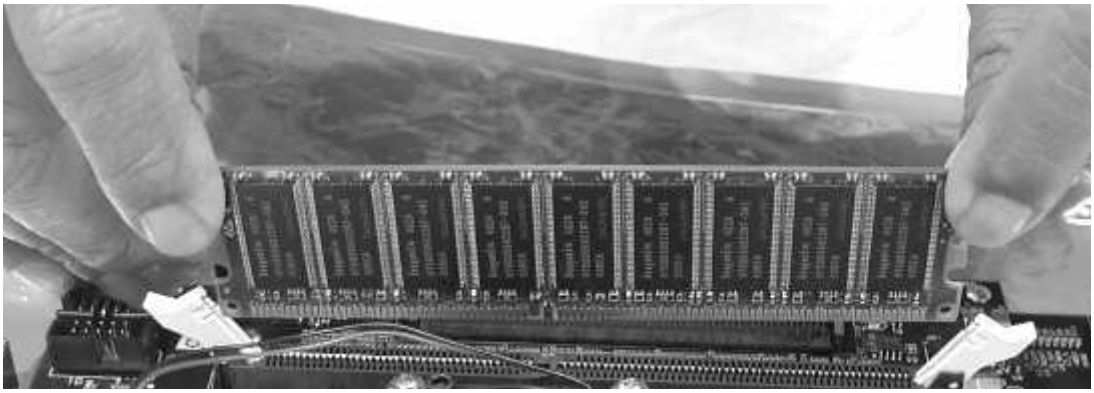


Figure 2-1. Inserting Memory Module

2. To remove the top chassis cover, stand chassis on end and remove the two top thumb screws located in back of the chassis. See Figure 2-2.

Figure 2-2. Removing Chassis Thumb Screws

3. Slide top cover toward the back while lifting, and remove. See Figure 2-3.

Figure 2-3. Removing Chassis Top Cover

4. Remove both side covers by lifting straight up. See Figure 2-4.

Figure 2-4. Removing Chassis Side Panel

5. Now lay chassis on the side with the motherboard exposed.
6. Remove PCI bracket screws. See Figure 2-5.

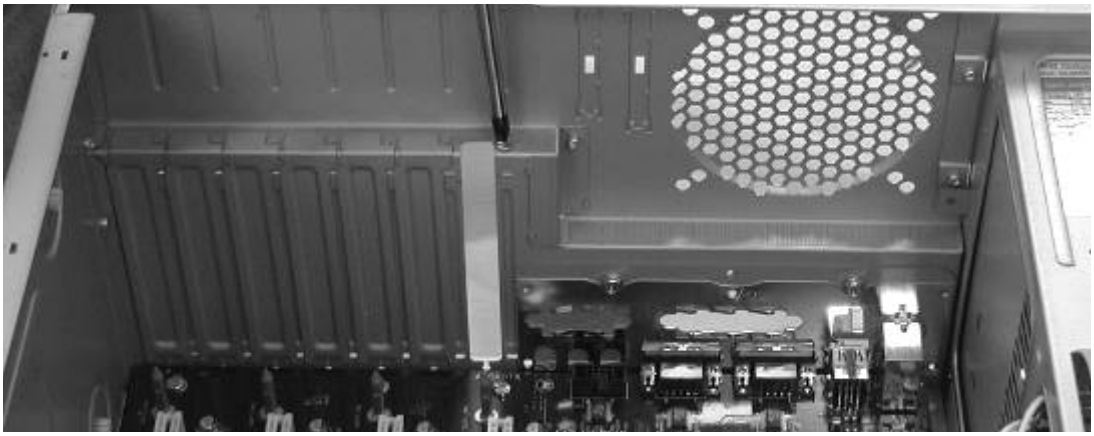


Figure 2-5. Removing PCI Slot Bracket Screws

7. Insert carrier card assembly into the PCI Slot 1. See Figure 2-6 and Figure 2-7.

NOTE

The alignment pins to guide the carrier card into the proper position are on the Arcadia motherboard.

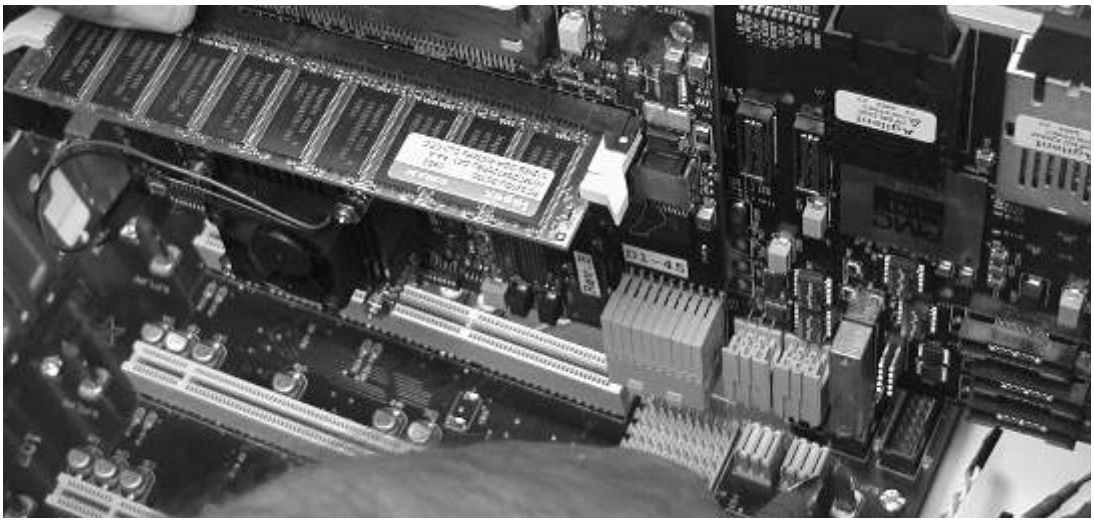


Figure 2-6. Install Carrier Card into PCI Slot

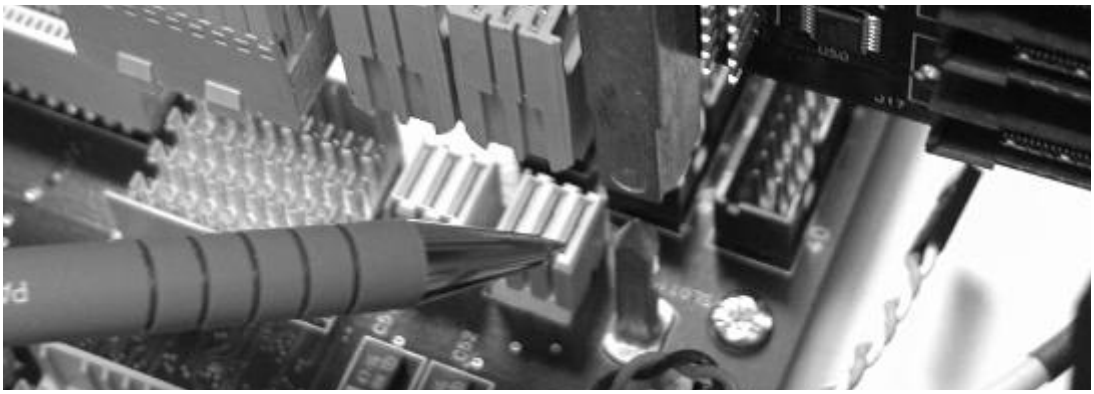


Figure 2-7. Guide Pin Alignment

8. Push the carrier card assembly down firmly to fully seat connectors.

9. Re-install the PCI bracket screws. See Figure 2-8.

Figure 2-8. Install PCI Bracket Screws

2.3 Quick Start-Up

1. Connect the CDS system to a 120-V AC power source. (For outside the U.S., a 240-V power supply must be installed in the box and connected to an AC power source.)
2. Connect the null modem serial cable between the carrier board COM1 port and the PC workstation serial port (COM1 or COM2).
3. Start up the terminal emulator program, (i.e., HyperTerminal) and setup the PC terminal program to use the following settings:
   - Bits per second: 115200
   - Data bits: 8
   - Parity: none
   - Stop bits: 1
   - Flow control: none
4. Turn on the CDS system by pushing the power switch on the front of the PC box.
5. After power-up by default, the system autoboots in Linux. However, if the autoboot is halted, the user should see the U-boot prompt. The following is only an example of a U-boot screen dump at bootup. The actual screen dump may vary depending on specific system configurations.

```
U-Boot 1.1.3 (FSL Development) (Oct 27 2006 - 10:43:18)
CPU:   8555, Version: 1.1, (0x80790011)
Core:  E500, Version: 2.0, (0x80200020)
Clock Configuration:
       CPU: 833 MHz, CCB: 333 MHz,
       DDR: 166 MHz, LBC:  83 MHz
L1:    D-cache 32 kB enabled
       I-cache 32 kB enabled
Board: CDS Version 0x13
```

```
CPU Board Revision 0.0 (0x0000)
    PCI1: 32 bit, 33 MHz, sync
    PCI2: 32 bit, 66 MHz, async
I2C:   ready
DRAM:  Initializing
    SDRAM: 64 MB
    DDR: 256 MB
FLASH: 16 MB
L2 cache 256KB: enabled
In:    serial
Out:   serial
Err:   serial
Net:   TSEC0: PHY is Marvell 88E1145 (1410cd4)
TSEC1: PHY is Marvell 88E1145 (1410cd4)
TSEC0, TSEC1
The IP address of the board is currently set to 169.254.113.58
The MAC address is 00:04:9F:00:28:C8
If they don't match your network environment, please change them in U-Boot and kernel
manually.
Hit any key to stop autoboot:  0
=>
```

6. By typing ‘boot’ at command prompt the system will boot to Linux.

2.4 How to Re-Flash U-Boot/Linux Image Using U-Boot

There are two banks of Flash memory in the CDS system, and are selected by switch 2, bits 1 and 2 on the carrier card. Following are the instructions to program the U-boot binary file Linux image into the bank of Flash memory as sent from the factory:

- To re-flash the U-boot follow steps 1 to 7.
- To re-flash Linux image follow steps 8 to 12.
- Requirement:
  - A running TFTP server who hosts the u-boot.bin file
  - The running U-boot should have the correct ‘ipaddr’, ‘serverip’, and ‘netmask’ parameters. The parameters can be modified by command ‘setenv <VARIABLE NAME> <VARIABLE VALUE>’

1. Boot the CDS with U-boot, hit any key to stop the timer
2. tftp 1000000 u-boot.bin
3. prot off all
4. erase fff80000 ffffffff
5. cp.b 1000000 fff80000 80000
6. reset
7. The new U-boot will boot up, hit any key to stop the timer
8. tftp 1000000 vmlinux.219
9. tftp 2000000 ramdisk.u-boot

10. erase ff800000 ffdfffff
11. cp.b 1000000 ff800000 1fffff
12. cp.b 2000000 ffa00000 3fffff

Steps 13 to 16 are required to update the environment variables.

13. setenv bootargs root=/dev/ram rw console=ttyS1,115200
14. setenv bootcmd bootm ff800000 ffa00000
15. saveenv
16. reset

2.5 Default Switch Configuration Table

The CDS system has several options for the switch settings to allow users to easily change the configuration. Table 2-1, Table 2-2, and Table 2-3 show the default switch settings for targeted applications. For the processor board (CPU card) switches shown in Table 2-1 and the carrier board switches shown in Table 2-2, in order to set an option value to 1, set the switch to ON; to set an option value to 0, set the switch to OFF. For the Arcadia board switches shown in Table 2-3, in order to set an option value to 1, set the switch to ON; to set an option value to 0, set the switch to OFF.

Table 2-1. Default Status of Processor Board (CPU Card) Switches

SW	Bit	Name	Default (1 = ON)	Note
1	1	PCI1 bus impedance	1	0 25 Ω 1 42 Ω (Default)
	2	PCI1 debug enable	1	Default
	3	DDR debug enable	1	
	4	Memory debug enable	1	
	5	Local bus hold LWE[0:1]	1	00 One extra delay 01 Two extra delays 10 Three extra delays 11 Default/specified AC timing
	6		1	
	7	PCI1 clock select	1	1 Sync (use SYSCLK) default 0 Async (use PCI1CLK)
	8	PCI2 clock select	0	1 Sync (use SYSCLK) 0 Async (use PCI2CLK) default

Table 2-1. Default Status of Processor Board (CPU Card) Switches (continued)

SW	Bit	Name	Default (1 = ON)	Note
2	1	Core voltage	1	10011 1.200 V
	2		0	
	3		0	
	4		1	
	5		1	
	6	Local bus size	1	0 8-bit Flash 1 16-bit Flash (default)
	7	Memory ECC Mux	1	0 Switch MECC to debug header 1 Connect MECC to DIMM, normally
	8	PCI dual	1	1 PCI1 is 32-bit, PCI2 is 32-bit 0 PCI1 is 64-bit (or 32-bit), PCI2 is OFF
3	1	Reserved	0	00 (default) Reserved
	2		0	
	3	Core clock PLL[0:1]	0	00 2:1 01 5:2 (default) 10 3:1 11 7:2
	4		1	
	5	CCB clock PLL[0:3]	1	0000 16:1 0010 2:1 0011 3:1 0100 4:1 0101 5:1 0110 6:1 1000 8:1 1001 9:1 1010 10:1(default) 1100 12:1 Rest Reserved
	6		0	
	7		1	
	8		0	
4	1	Boot sequencer [0:1]	1	01 Standard I2C EEPROM 10 Extended I2C EEPROM 11 No EEPROM
	2		1	
	3	CPU boot enable	1	Halt CPU until external host enable it Allow CPU to run immediately after reset
	4	Processor identity	—	0 MPC8541E 1 MPC8555E
	5	PCI host/agent	1	0 = Agent 1 = Host (default)
	6	Boot location	1	000 Boot from PCI bus #1 001 Boot from DDR 010 Boot from PCI bus #2 101 Boot from local bus, 8-bit 110 Boot from local bus, 16-bit 111 Boot from local bus, 32-bit
	7		1	
	8		0	

Table 2-2. Default Status of Carrier Board Switches (Configuration 1)

SW	Bit	Name	Default (1 = ON)	Note
1	1	SYSCLK SEL	0	0 PCICLK used for SYSCLK 1 LCLCLK used for SYSCLK
	2	Synchronizer	1	1 Must be 1 at all times (PHY CLK/FPGA CLK)
	3	Reserved	1	See Note 1
	4	Local clock S(2:0)	0	01 Part of 33 MHz SYSCLK
	5		1	
	6		1	
	7	Local clock R(4:3)	0	00 Part of 33 MHz SYSCLK
	8		0	
2	1	Boot select	0	00 Flash bank 1, bank 2 available 01 Flash bank 2, bank 1 available 10 Promjet, bank 1 available 11 Promjet, bank 2 available
	2		0	
	3	NVRAM enable	1	0 NVRAM disable 1 NVRAM available
	4	Event select	1	0 $\overline{\text{UDE}}$ 1 $\overline{\text{SRESET}}$
	5	Reserved	1	1 Reserved
	6	Reserved	1	1 Reserved, see Note 2
	7	User defined	0	00 User defined, software readable
	8		0	
3	1	Reserved	1	1 Reserved
	2	DUART output select	1	0 DUART channel #2 to 2x5 (AT) header DUART channel #1 to DB9 connector
				1 DUART channel #2 to DB9 connector DUART channel #1 to 2x5 (AT) header
	3	ATM 2 enable	1	0 ATM2/155 enabled 1 ATM2/155 disabled
	4	ATM 1 width	1	0 ATM1/16-bit IO enabled 1 ATM1/16-bit IO disabled
	5	ADTech select	0	0 AdTech disabled 1 AdTech enabled
	6	FE select	0	0 FCC3->Cicada MII#4 enabled 1 FCC3->Cicada MII#4 disabled
	7	ATM2 select	1	0 FCC2->PMC 155M ATM enabled 1 FCC2->PMC 155M ATM disabled
	8	ATM1 select	1	0 FCC1->PMC 625M ATM enabled 1 FCC1->PMC 625M ATM disabled

Table 2-2. Default Status of Carrier Board Switches (Configuration 1) (continued)

SW	Bit	Name	Default (1 = ON)	Note
4	1	Local clock R(2:1)	1	10 Part of 33 MHz SYSCLK
	2		0	
	3	Local clock V(6:1)	0	001000 Part of 33 MHz SYSCLK
	4		0	
	5		1	
	6		0	
	7		0	
	8		0	

Notes:
1. SW1(3) for Configuration 2 is PCI CLK SEL and must be set to 1.
2. SW2(6) for Configuration 2 is PCI Select PCI = 1 and PCIX = 0.

Table 2-3. Default Status of Arcadia Board Switches (Arcadia C3.*n*)

SW	Bit	Name	Default (1 = ON)	Note
1	1	TSI310: BAR_EN	0	0 BAR0 disabled 1 BAR0 enabled
	2	Secondary bus internal arbiter enable TSI310: S_INT_ARB_EN	0	0 Use internal arbiter 1 Use external arbiter
	3	Physical width of the PCI-X device TSI310: 64_BIT_DEVICE	0	0 Bridge is a 64-bit bus 1 Bridge is a 32-bit bus
	4	Opaque region enable TSI310: OPAQUE_EN	0	0 Opaque memory enable 1 Opaque memory enable
	5	Secondary PCI IDSEL remap TSI310: IDSEL_REROUTE_EN	0	0 IDSEL remap mask is 0000_0000 1 IDSEL remap mask is 22F2_0000
	6	Secondary high-speed rate select TSI310: S_SEL100	1	0 PCI-X highest speed is 133 MHz 1 PCI-X highest speed is 100 MHz
	7	Primary configuration busy TSI310: P_CFG_BUSY	0	0 Primary side responds to configuration cycles normally 1 Primary side configuration cycles are retried until bit 2 of the miscellaneous control registers is set to 0 by a secondary configuration cycle write
	8	Primary driver mode control TSI310: P_DRVR_MODE	0	0 Normal impedance 1 Lower impedance for heavier loads

Table 2-3. Default Status of Arcadia Board Switches (Arcadia C3.*n*) (continued)

SW	Bit	Name	Default (1 = ON)	Note
2	1	ARC0	0	0 SIOINT -> PCIB3_INT0 1 SIOINT -> PCIB3_INT1
	2	ARC1	1	Reserved
	3	ARC2	1	Reserved
	4 [1]	G0	1	User defined
	5 [1]	G1	1	User defined
	6 [2]	LPCWP*	1	User defined
	7	Reserved	1	N/A
	8	Reserved	1	N/A
3	1	Isolate slow PCI bus segment ISOLATE_3_4	0	0 PCIB3 connected to PCIB4 1 PCIB3 isolated from PCIB4
	2	TSI310 PCI bridge enable BRIDGE_EN*	0	0 PCI bridge responds to config cycles 1 PCI bridge ignores all config cycles
	3	PCI A (fast) bus speed force PCIA_FRC1	11	00 AUTO (33 MHz when M66_EN input is 0 or 66 MHz when M66_EN is a 1 (M66_EN pin is three-stated) 01 PCIA forced to 66 MHz PCI mode (M66_EN pin is three-stated) 10 PCIA forced to 33 MHz PCI mode (M66_EN pin is driven with logic 0) 11 PCIA forced to 33 MHz PCI mode (M66_EN pin is driven with logic 0)
	4	PCI A (fast) bus speed force PCIA_FRC0		
	5	RTK8139 Ethernet enable ENET_DIS*	1	0 RealTek 8139 may be accessed 1 RealTek 8139 cannot be accessed
	6	PCI bus interrupt connection PCI_INT_BRIDGE*	0	0 PCIA and PCIB interrupts are directly connected (wire-or'd) 1 PCIA and PCIB interrupts are isolated
	7 [3]	PrPMC IDSEL enabled PRPMC_IDSELEN*	1	0 PrPMC can be target selected 1 PrPMC cannot be target selected
	8 [4]	MONARCH*	1	0 PrPMC is PCIB controller 1 PrPMC is not PCIB controller

Notes:

1. Software-defined switches.
2. Optional feature.
3. Some PCI devices do not allow their own IDSEL to be asserted when operating as the PCI host; if so, use this switch to disable IDSEL. Not applicable for PCI agents.
4. This switch configures the MPMC card into the system controller, a mode which is required for normal PCI use. Disabling is provided for testing purposes only.

Chapter 3
CDS Carrier Architecture

This chapter describes in detail the CDS carrier system. It describes the physical layout and assembly, as well as basic and detailed system architecture. This chapter elaborates on usage and testing/debugging procedures.

The CDS carrier is the backbone of the CDS system. It facilitates communication between the components as well as with outside parts through the PCI port.

3.1 Overview

The following sections give the CDS board measurements and block diagram.

3.1.1 Board Measurements

For the CDS carrier, the mechanical dimensions are driven by the *RapidIO Hardware Interoperability Platform* standard. The placement of the RapidIO header (redefined for the CDS system as a flexible high-speed port), the additional power connectors, and the guide pins are detailed in this manual.

3.1.2 Block Diagrams

Figure 3-1 is a diagram of the CDS board for Configuration 1.

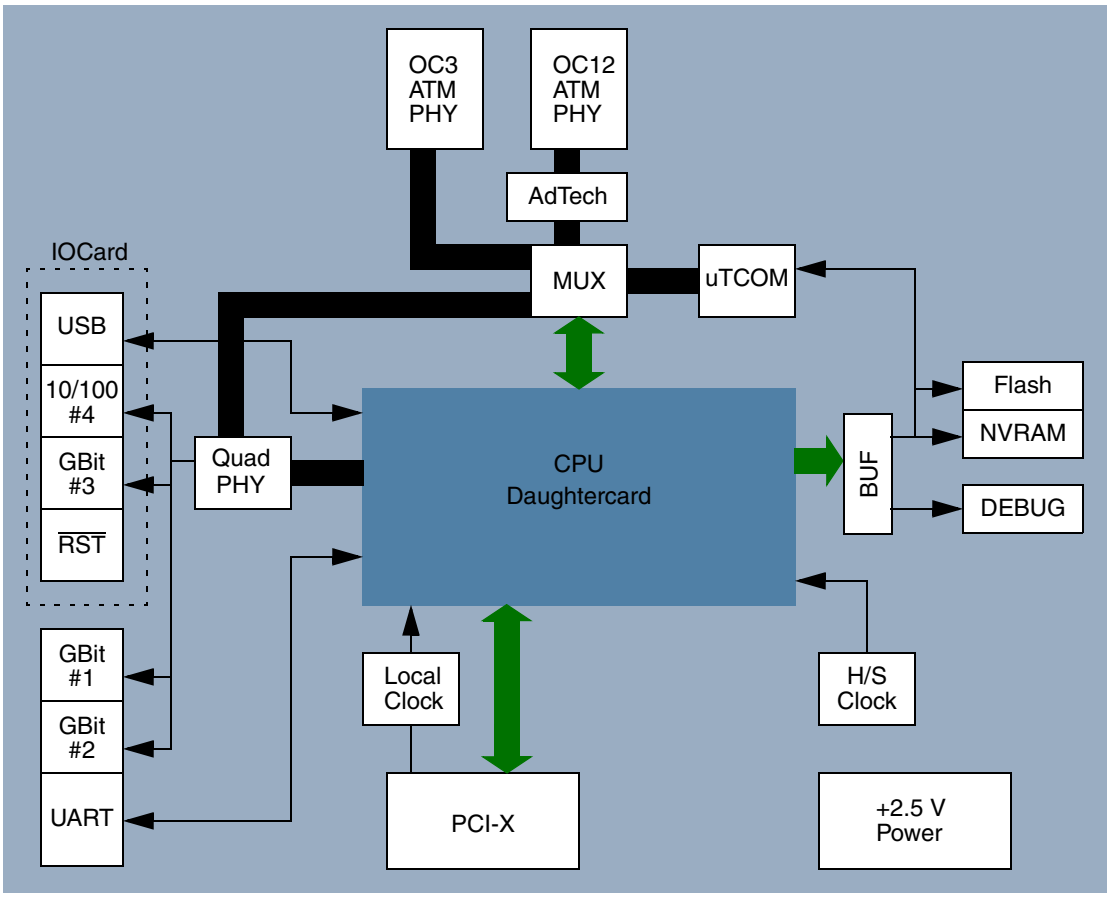


Figure 3-1. Carrier Block Diagram (Configuration 1)

Figure 3-2 is a diagram of the CDS system for Configuration 2.

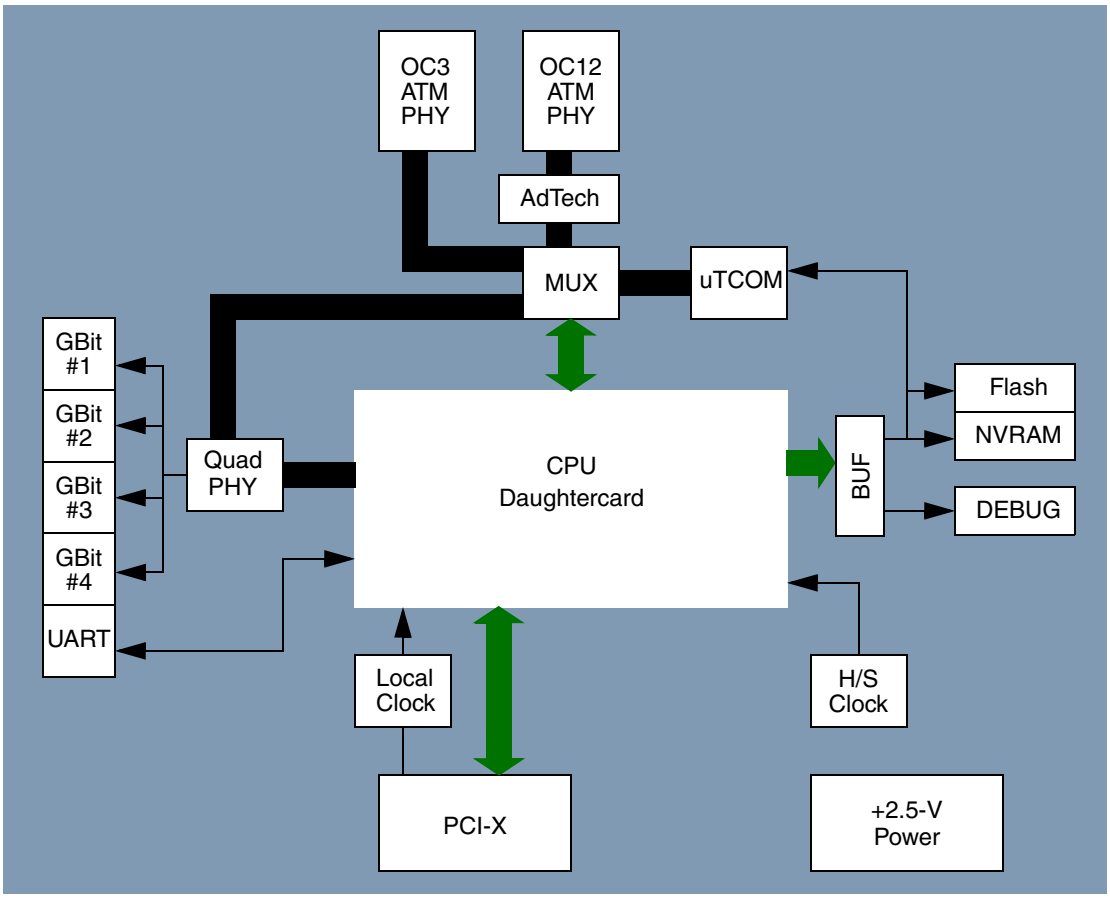


Figure 3-2. Carrier Block Diagram (Configuration 2)

3.2 Carrier Pinouts

For a detailed pinout, including the numbering, refer to Appendix B.1, "Carrier/DaughterCard Connectors Pinout."

3.3 System Logic

The CDS board contains an FPGA/CPLD called Cadmus which collects various logic and performs system control functions, including:

- System reset sequencer
- System logic address map
- PCI bus speed monitor
- LED monitors
- Peripheral bus development (chip select, address align)
- System controls

3.3.1 System Address Map

Table 3-1 describes the CDS memory map as implemented for U-Boot and Linux platform. Cadmus uses the local bus chip selects to implement the following two critical features:

- Boot flash redirection
- Cadmus register intervention

Table 3-1. Memory Map

Chip Select	Description	Base Address[1]	Size
LCS0	Flash (boot bank)	0xFF80_0000 -----0xFFFF_FFFF	8M
LCS1	Flash (2nd bank)	0xFF00_0000 -----0xFF7F_FFFF	8M
LCS3	NVRAM/CADMUS[1]	0xF800_0000 ----- 0xF80F_FFFF	1M
LCS2	SDRAM[2]	0xF000_0000 ----- 0xF7FF_FFFF	128M
—	PCI2 IO	0xE300_0000 ----- 0xE3FF_FFFF	16M
—	PCI1 IO	0xE200_0000 ----- 0xE2FF_FFFF	16M
—	CCSR	0xE000_0000 ----- 0xE00F_FFFF	1M
—	PCI2 MEM	0xA000_0000 ----- 0xBFFF_FFFF	512M
—	PCI1 MEM	0x8000_0000 ----- 0x9FFF_FFFF	512M
—	DDR	0x0000_0000 ----- 0x7FFF_FFFF	2G
LCS4	Reserved		
LCS5	UTCOM		
LCS6	UTCOM		
LCS7	Reserved		

1 The CADMUS registers are connected to CS3 on the CDS. The new memory map places CADMUS at 0xF8000000.

2 Base Register 2 and Option Register 2 configure the SDRAM. The SDRAM base address, CFG_LBC_SDRAM_BASE, is 0xF0000000.

Note: These addresses are specific to the addresses specified by Linux, other OS/Boot code may/will use different base addresses.

Note: Addresses may vary widely by processor and bridge logic that is present on the CDC; refer to the specification for details.

Most chip-selects are passed through to the device as-is, with the exception of LCS3. This chip-select is used to implement the Cadmus register set and is shared with the external 4-KB NVRAM device.

3.3.2 System Logic Registers

The system logic contains several software-accessible registers which are accessed from the base address described in Section 3.3.1, “System Address Map.” Table 3-2 shows the address map of the Cadmus device.

Table 3-2. Cadmus Address Map

Base Address Offset	Register	Access	Reset
0x00	System version register (CM_VER)	R	0x11
0x01	General control/status register (CM_CSR)	R/W	0x00
0x02	Reset control register (CM_RST)	R/W	0x00
0x03	Reserved	—	—
0x04	Reserved	—	—
0x05	LED data register (CM_LED)	R/W	0x00
0x06	PCI control/status register (CM_PCI)	R/W	0x00
0x07	DMA control register (CM_DMA)	R/W	0x77
0x08-0xFF	Reserved	Reserved	Undefined

3.3.2.1 Version Register (CM_VER)

The version register contains the board and CPLD revision information.

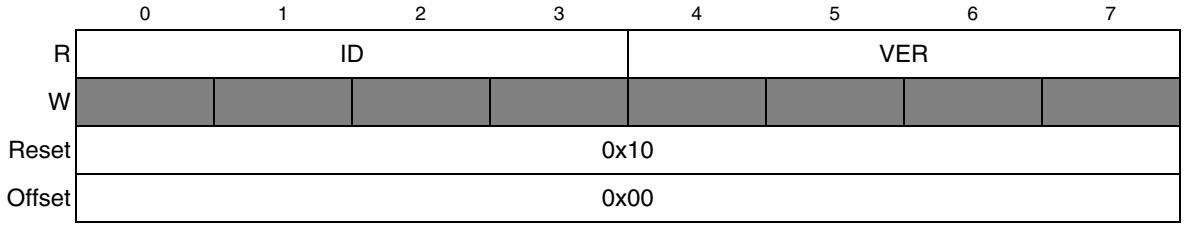


Figure 3-3. Version Register (CM_VER)

Table 3-3. CM_VER Field Descriptions

Bits	Name	Description
0–3	ID	Board identification
4–7	REV	Revision number (starts with 0)

NOTE

The board revision applies only to the carrier, because different CPU daughtercards could be present. The I2C-based CDC ID EEPROM can be queried for further details.

3.3.2.2 General Control Register (CM_CSR)

The CM_CSR register contains various control and status fields, as described below.

	0	1	2	3	4	5	6	7
R	USER		-rsv-	-rsv-	EPHY(4:2)			LED
W								
Reset	0	0	0	0	0	0	0	0
Offset	0x01							

Figure 3-4. Reset Control Register (CM_CSR)

Table 3-4. CM_CSR Field Descriptions

Bits	Name	Description
0–1	USER	Reflects the settings of the USER switches on the carrier. Software may make use of these bits; CDS does not do anything with them.
2–3	Reserved	
4–6	EPHY	This field sets the most-significant 3 bits of the Ethernet PHY address (the least 2 bits are internally used to select 1 of 4 PHY devices).
7	LED	If set, the internal LED buffers are driven by the contents of the CM_LEDCTL register; if clear (default), the contents are driven by various activities.

3.3.2.3 Reset Control Register (CM_RST)

The reset control register contains enables and assertion bits for reset controls.

	0	1	2	3	4	5	6	7
R	XRSTEN	PHYRST	ATM1RST	ATM2RST	MEMRST	UTRST	-rsv-	SRESET
W								
Reset	0	0	0	0	0	0	0	0
Offset	0x02							

Figure 3-5. Reset Control Register (CM_RST)

Table 3-5. CM_RST Field Descriptions

Bits	Name	Description
0	XRSTEN	This bit, if set, allows the NVRAM watchdog timer to function as a general reset input.
1	PHYRST	This bit allows software to issue a reset to the Ethernet PHY.
2	ATM1RST	This bit allows software to issue a reset to the FCC1/ATM1 PHY.
3	ATM2RST	This bit allows software to issue a reset to the FCC2/ATM2 PHY.
4	MEMRST	This bit allows memory devices on the daughtercard to be reset (the carrier does not make use of it).
5	UTRST	This bit allows the TCOM/ECOM boards (via the uTCOM adapter) to be individually reset.

Table 3-5. CM_RST Field Descriptions (continued)

Bits	Name	Description
6	HRESET	This bit allows a device to assert HRESET to itself. As HRESET may be a level-sensitive signal (device-dependent), it is a self-resetting bit.
7	SRESET	This bit allows a device to assert SRESET to itself. As SRESET may be a level-sensitive signal (device-dependent), it is a self-resetting bit.

3.3.2.4 LED Data Register

The LED data register can be used to directly control the LED monitoring outputs, when CM_XCSR[LED] is set to one.

	0	1	2	3	4	5	6	7
R	LED							
W								
Reset	0	0	0	0	0	0	0	0
Offset	0x05							

Figure 3-6. Reset Control Register (CM_LED)

Table 3-6. CM_LED Field Descriptions

Bits	Name	Description
0–7	LED	Corresponding values for CDC monitoring LEDs L0–L7. Setting a bit to one illuminates the LED.

3.3.2.5 PCI Control/Status Register

The PCI control/status register monitors and controls the PCI environment.

	0	1	2	3	4	5	6	7
R	M66O	PCIXCO	M66S	DUAL	PSPEED		PCIX	$\overline{\text{PCIEN}}$
W	0	0						
Reset	0	0	0	0	0	0	0	0
Offset	0x06							

Figure 3-7. PCI Control/Status Register (CM_PCI)

Table 3-7. CM_PCI Field Descriptions

Bits	Name	Description
0	M66O	If set, the M66EN signal is forced low; otherwise, the M66EN pin is three-stated and the PCI bus speed is set by the daughtercard settings and/or the PCIXCAP/PCIXCO settings. **Note:** It is a violation of PCI protocol to change M66EN after $\overline{\text{PCIRST}}$ has been released; the effects of this bit are system-dependent.
1	PCIXCO	If set, the PCIXCAP signal is forced low; otherwise, the PCIXCAP pin is three-stated and the PCI bus speed is set by the daughtercard settings and/or the M66EN/M66O settings. **Note:** It is a violation of PCI protocol to change PCIXCAP after $\overline{\text{PCIRST}}$ has been released; the effects of this bit are system-dependent.
2	M66S	M66EN sense. If set to 1, PCI V2.3 mode or earlier is operating at 66 MHz; otherwise, 33 MHz is selected.
3	DUAL	Daughtercard has selected dual PCI-mode (if any).
4–5	PSPEED	PSPEED indicates the detected PCI speed, as follows: PCI: 00 33 MHz 01 66 MHz 1X Reserved PCI-X: 00 33 MHz 01 66 MHz 1X Reserved
6	PCIX	If set, the PCI edge connector is connected to a PCI-X backplane; otherwise, conventional PCI is active.
7	$\overline{\text{PCIEN}}$	Reflects the status of the $\overline{\text{PCIEN}}$ switch. If 0, the PCI backplane is assumed active; otherwise, it may not be present.

3.3.2.6 DMA Control Register

The DMACTL register allows limited control and exercise of the DMA interface of various processors (where supported).

	0	1	2	3	4	5	6	7
R	-rsv-	DMARQ0	DMACK0	DMADN0	-rsv-	DMARQ1	DMACK1	DMADN1
W								
Reset	0	1	1	1	0	1	1	1
Offset	0x07							

Figure 3-8. Reset Control Register (CM_DMA)

Table 3-8. CM_DMA Field Descriptions

Bits	Name	Description
1 5	DMARQ0 DMARQ1	Sets the corresponding $\overline{\text{DMARQ}}$ line to the value written
2 6	DMACK0 DMACK1	Reflects the status of the corresponding $\overline{\text{DMACK}}$ line
3 7	DMADN0 DMADN1	Reflects the status of the corresponding $\overline{\text{DMADN}}$ line

3.4 CPM Connections

The CDS carrier supports some peripherals for evaluating Ethernet and ATM interfaces for those processors which support CPM or CPM-compatible communications machines. If the CPUCard does not support this interface, the signals are simply ignored (that is, MPC8555E CDS daughterboard only supports FCC1 and FCC2; FCC3 is not supported on the MPC8555E device).

All other interfaces are evaluated and supported on external IO cards, such as the ECOM and TCOM. This allows evaluation of the SCC, multi-PHY, and other interfaces. To support this facility, selected signals are extracted from the CPM pins and either routed to the appropriate interface or to the uTCOM header. The overall logic is shown in Figure 3-9.

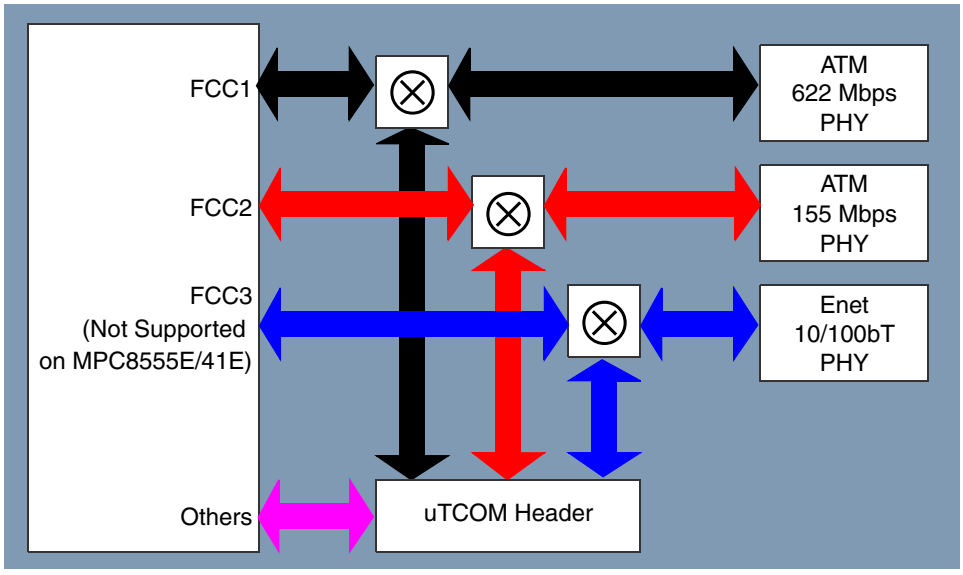


Figure 3-9. CE/CPM Architecture

The processor CE/CPM (if any) signals are largely routed directly to the uTCOM connector, with the exceptions noted in Table 3-9.

Table 3-9. CDS CPM/CE Connection Options

CE/CPM Port	Definition	Switch	Switch = 0 Definition	Switch = 1 Definition	Notes
FCC1	OC12	SW3–8	622 Mbps ATM PHY	uTCOM	UTOPIA 8 only Adtech support
FCC2	OC3	SW3–7	155 Mbps ATM PHY	uTCOM	No UTOPIA connection No Adtech support
FCC3	10/100	SW3–6	FEthernet	uTCOM	FCC 3 not supported on MPC8555E/41E

The specific CPM/CE port bits that need to be switched for each mode are listed in Table 3-10 and Table 3-11.

Table 3-10. CPM Port Routing for FCC1 in ATM622/UTOPIA 8 Mode

ATM Signal	Group Bit															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXDATA(15:0)									PA18	PA19	PA20	PA21	PA22	PA23	PA24	PA25
TXSOC	PA29															
TXENB	PA31															
TXPRTY	PD16															
TXADD(4:0)												PD19	PD7	PC7	PC13	PC15
TXCLAV	PA30															
TXCLK	PC20															
RXDATA(15:0)									PA17	PA16	PA15	PA14	PA13	PA12	PA11	PA10
RXSOC	PA27															
RXENB	PA28															
RXPRTY	PD17															
RXADD(4:0)												PD18	PD29	PC6	PC12	PC14
RXCLAV	PA26															
RXCLK	PC21															

Table 3-11. CPM Port Routing for FCC2 in ATM155 Mode

ATM Signal	Group Bit															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXDATA(15:0)	n/a								PB22	PB23	PB24	PB25	PD31	PD22	PB26	PB27
TXSOC																PB30
TXENB																PD30
TXPRTY																PC4
TXADD(4:0)												PD7	PD19	PC9	PC11	PC17
TXCLAV																PD25
TXCLK																PC18
RXDATA(15:0)	N/A								PB21	PB20	PB19	PB18	PD21	PD20	PD15	PD14
RXSOC																PB31
RXENB																PD24
RXPRTY																PC1

Table 3-11. CPM Port Routing for FCC2 in ATM155 Mode (continued)

ATM Signal	Group Bit															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RXADD(4:0)												PD29	PD18	PC10	PC23	PC16
RXCLAV																PB29
RXCLK																PC19

Because not all of the CPM signals are optionally re-routed, some of the connections sent to the uTCOM header are from the switch device, and others are from the CPM port of the processor. This is summarized in Table 3-12.

Table 3-12. CPM/CE Switch Summary

Port	Bits	Type
PA	0-5	Switched
	6-9	Pass-through
	10-31	Switched
PB	4-6	Switched
	7	Pass
	8-27	SW
	28	Pass-through
	29-31	Switched
PC	0-1	Pass-through
	2-21	Switched
	22-31	Pass-through
PD	4	Pass-through
	5-6	Switched
	7	Pass-through
	8-11	Switched
	12-13	Pass-through
	14-18	Switched
	19	Pass-through
	20	Switched
	21	SW
	22-28	Pass
	29	Pass-through
	30	Switched
	31	Pass-through

3.5 ATM Interfaces

The CDS carrier card provides two dedicated ATM ports, one at 622 Mbps and the other at 155 Mbps. The general architecture is shown in Figure 3-10.

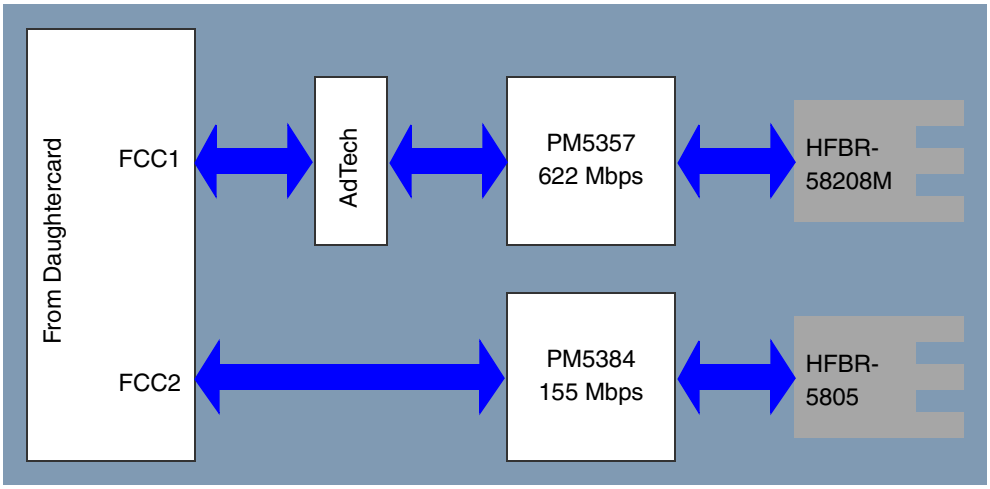


Figure 3-10. CDS ATM Architecture

Table 3-13 describes the details of the ATM interface.

Table 3-13. ATM Port Overview

Feature	ATM1	ATM2
CE/CPM connection	FCC1	FCC2
UTOPIA interface	16	8
Adtech support?	Yes	No
PHY	PMC-Sierra PM5357	PMC-Sierra PM5384
Optical transceiver	Agilent HFBR-5208M	Agilent HFBR-5805

3.6 Ethernet Ports

In Configuration 1, the CDS carrier card provides four 10/100 1GB-baseT Ethernet ports. Two are located on the basic carrier board and the other two on the IOCard expansion. The four ports are controlled by a Cicada CS8204 quad-PHY, which in turn receives data from three dedicated MII/GMII daughtercard connections.

In Configuration 2, all four Ethernet ports on the carrier card are supported by a Marvell 88E1145. MII/GMII on Ethernet ports #1 and #2. RGMII on Ethernet ports #3 and #4, 10/100 or 1G rates.

NOTE

In Configuration 1, TBI, RTBI, RMII, and RGMII interface modes are not supported.

In Configuration 1, Ethernet port #4 on the I/O card is not functional.

In Configuration 2, RGMII is supported only on Ethernet ports #3 and #4.

The fourth port is optionally extracted from the FCC3 pins on port B pins of the CPM engine as detailed in Section 3.4, "CPM Connections." In addition to the special pins, the fourth port is only connected as a 10/100baseT port.

The PHY addresses are numbered 0–3, corresponding with the 4 internal PHY devices. The MSB bits (3 of them) of the address can be changed by writing to the CM register, however the lower 2 bits are always mapped internally by the CIS8204 as shown in Table 3-14. The Ethernet PHY addresses are fixed in Configuration 2.

Table 3-14. PHY Address Options (Configuration 1)

CM_CSR EPHY[4:2]	CIS8204 Port	PHY Address
000 (Default)	0	0x00
	1	0x01
	2	0x02
	3	0x03
001	0	0x04
	1	0x05
	2	0x06
	3	0x07
...	...	...
111	0	0x1C
	1	0x1D
	2	0x1E
	3	0x1F

These connections and the interface logic are shown in Figure 3-11 for Configuration 1 and Figure 3-12 for Configuration 2.

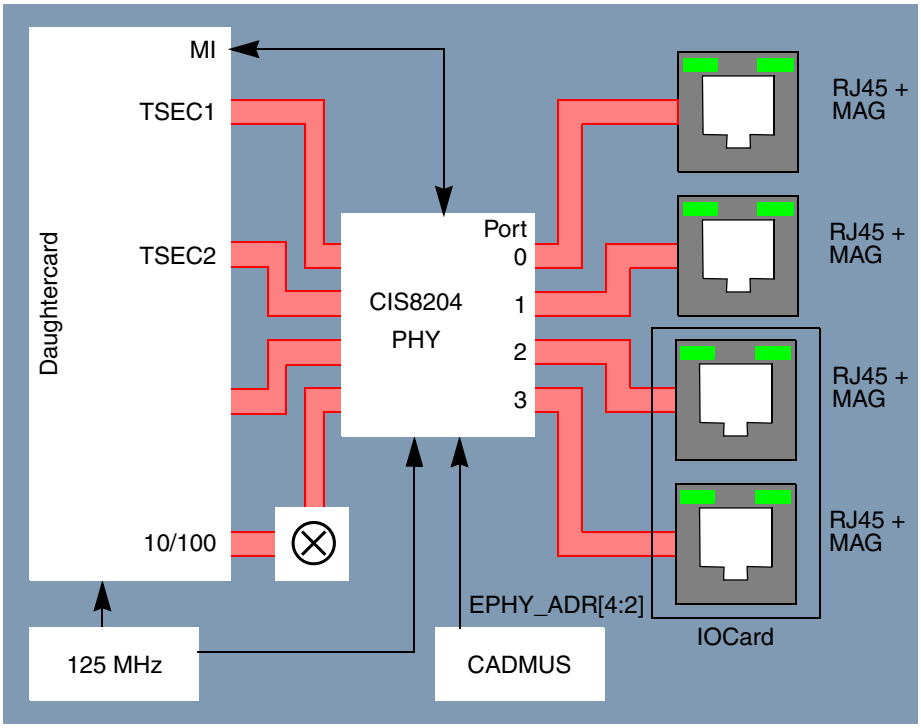


Figure 3-11. CDS Ethernet Architecture (Configuration 1)

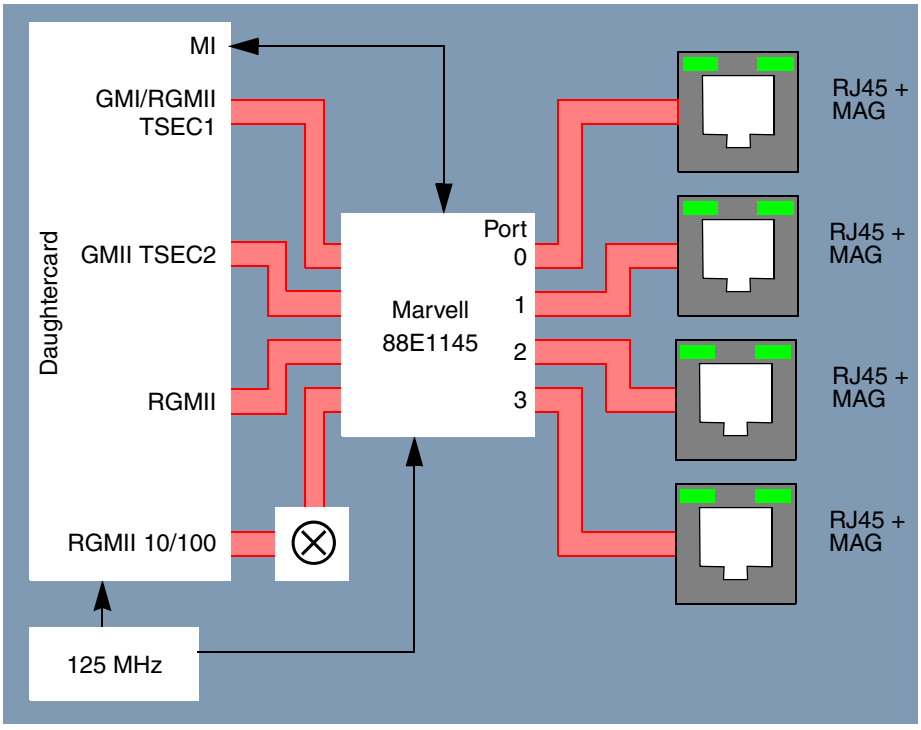


Figure 3-12. CDS Ethernet Architecture (Configuration 2)

Table 3-15 summarizes the connections to the TSEC interface and associated PHY.

Table 3-15. CDS TSEC Interface Summary

TSEC Signal	TSEC Signal Type	TSECx Bus Connect	Description	CS8204 PHY or Marvell 88E1145	Notes
TSECx_TXD[7:0]	O	7–0	Transmit data inputs	TXD[7:0]	3
TSECx_TX_EN	O	8	Transmit enable input	TX_EN	
TSECx_TX_ER	O	9	Transmit error input	TX_ER	
TSECx_TX_CLK	I	10	N/A	N/A	1
TSECx_GTX_CLK	O	11	Transmit clock output	GTX_CLK	
TSECx_CRS	I	12	Carrier sense	CRS	
TSECx_COL	I	13	Collision detect	COL	
TSECx_RXD[7:0]	I	21–14	Receiver data output	RXD[7:0]	
TSECx_RX_DV	I	22	Receiver data valid output	RX_DV	
TSECx_RX_ER	I	23	Receiver error output	RX_ER	
TSECx_RX_CLK	I	24	Receiver clock output	RX_CK	
MDC	O		Management data clock	MDC	
MDIO	I/O		Management data I/O	MDIO	
GTX_CLK125	I		Reference 125 MHz clock	N/A	2

Notes:
1. TX_CLK is not used in GMII mode, only MII.
2. Reference clock is derived from the global 125-MHz reference clock.

Each TSEC has LEDs to monitor activity in the RJ45 connector.

3.7 Local Bus

The CDS carrier card provides a local bus, which supports commonly required memory and other devices. It does so at a significantly slower speed than the CPU daughtercard, and only expects that the daughtercard present a consistent address interface at a high bus load. The local bus includes:

- Two separate, bootable banks of Flash memory
  - AMD Am29LV641DH-120 (or faster)
  - 64 Mb each
  - 8- or 16-bit access sizes supported
- One bank of RTC/NVRAM
  - Maxim DS1553WP, 8KB with battery backup
- Three Mictor headers for local bus debug
- uTCOM interface port
- ATM PHY registers

The bus is treated as a general-purpose interface and leaves decisions such as chip select to the daughtercard. The connections and accompanying interface logic is shown in Figure 3-13.

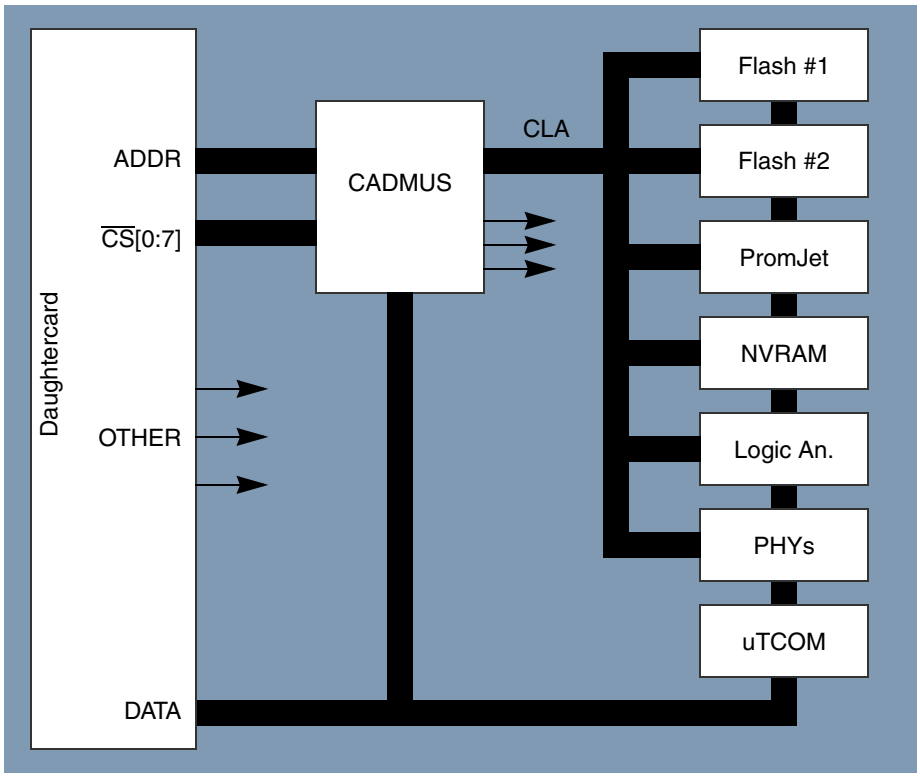


Figure 3-13. CDS Local Bus Architecture

Table 3-16 lists the pins of the daughtercard connector.

Table 3-16. CDS Carrier Local Bus Signals

Signal Group	Signal Name	Signal Count	Notes
Address	LB_A(0:31)	32	LB_A0 is MSB
Data	LB_D(0:31)	32	LB_D0 is MSB
Data parity	LB_DP(0:3)	4	LB_DP(0) pairs with LB_D(0:7), etc.
Output enable	$\overline{\text{LB\_OE}}$	1	
Write strobes	$\overline{\text{LB\_WE}}$(0:3)	4	

Table 3-16. CDS Carrier Local Bus Signals (continued)

Signal Group	Signal Name	Signal Count	Notes
Chip selects	$\overline{\text{LB\_CS0}}$	8	Connects to Flash device #1 (carrier card)
	$\overline{\text{LB\_CS1}}$		Connects to Flash device #2 (carrier card)
	$\overline{\text{LB\_CS2}}$		Connects to SRAM/SDRAM port (CPU card)
	$\overline{\text{LB\_CS3}}$		Connects to RTC/NVRAM
	$\overline{\text{LB\_CS4}}$		Connects to uTCOM port
	$\overline{\text{LB\_CS5}}$		Reserved
	$\overline{\text{LB\_CS6}}$		Reserved
	$\overline{\text{LB\_CS7}}$		Reserved
Address latch	LALE	4	For systems with multiple LALE signals implemented only LALE is guaranteed; LALE(1:*n*) are for reference purposes only.
Control	LBCTL	1	
Misc	LGP(0:5)	6	
Clock	LB_CLK	1	Signals such as LB_CLK(1:2) are optional
Device size	LBSZ(0:1)	2	Local bus device width control: 00 = 8-bit 01 = 16-bit 10 = 32-bit 11 = Reserved
Subtotal		95	
Spares		5	
Total		100	

Note: The signal names do not necessarily map directly to the equivalent signal names on the daughtercard.

3.7.1 NCDS Local Bus Signals

The CDS local bus generates several signals in the pins of Table 3-16. Table 3-17 describes these signals.

Table 3-17. CDS Cxx Local Bus Signals

Signal Name	Description	Notes
CLA(23:0)	CDS local address	CLA(23) is MSB
$\overline{\text{LB\_RD}}$	Local bus read/output enable	
$\overline{\text{LB\_WR}}$	Local bus write	
$\overline{\text{FLASH0\_CS}}$	Flash bank 0 chip select	Default boot device
$\overline{\text{FLASH1\_CS}}$	Flash bank 1 chip select	Alternate boot
$\overline{\text{PJET\_CS}}$	PromJet chip select	External boot select
$\overline{\text{NVRAM\_CS}}$	NVRAM/RTC chip select	

Table 3-17. CDS Cxx Local Bus Signals (continued)

Signal Name	Description	Notes
$\overline{\text{ATM1\_CS}}$	ATM PHY #1 chip select	ATM622 Mbps device
$\overline{\text{ATM2\_CS}}$	ATM PHY #2 chip select	ATM155 Mbps device
$\overline{\text{ATM1X\_CS}}$	AdTech PHY chip select	AdTech external chip select

Table 3-18 is an example of how the local bus address (LB_A(0:31)) is converted into the size-aligned address suitable for the local bus.

Table 3-18. CLA Mapping

LBSZ(0:1) Setting	CLS Generation
00 (8-bit)	CLA(23) = LB_A(8) CLA(22) = LB_A(9) ... CLA(01) = LB_A(30) CLA(00) = LB_A(31)
01 (16-bit)	CLA(23) = LB_A(7) CLA(22) = LB_A(8) ... CLA(01) = LB_A(29) CLA(00) = LB_A(30)
10 (32-bit)	CLA(23) = LB_A(6) CLA(22) = LB_A(7) ... CLA(01) = LB_A(28) CLA(00) = LB_A(29)
11	Reserved

3.8 Clock

The CDS carrier board contains four independent clock domains:

SYSCLK	–for CPU and/or alternate PCI clock
PCICLK	–for primary PCI bus
125-MHz reference	–for PHY reference clocks
Timebase/performance monitor clock	–miscellaneous

Note that the daughtercard may elect to generate or derive any other subsidiary clocks for its own purpose.

The SYSCLK signal is generally the primary clock source for the Freescale PowerPC processor and is typically related to the PCICLK of the carrier board by some configurable ratio.

In a HIP environment, the PCICLK source from the PCI edge connector may be 0 MHz (that is, PCI disabled), 33, or 66 MHz.

The 125-MHz PHY reference clock (fixed frequency), the 16-MHz timebase reference (fixed frequency), and the external high-speed reference clock are independent.

The CDS carrier clock resources are summarized in Table 3-19.

Table 3-19. CDS Clock Requirements Summary

Clock Signal	Frequency Range	Voltage Level	Require	Notes
PCICLK	33/66 MHz	3.3V LVTTL	PCI interface of daughtercard	
SYSCLK	10–200 MHz	3.3V LVTTL		
PHYCLK	125 MHz	3.3V LVTTL	QuadPHY on CDS main board	
RTC_CLK	16 MHz	3.3V LVTTL	Timing base for the performance monitor	

The overall clock architecture is shown in Figure 3-14.

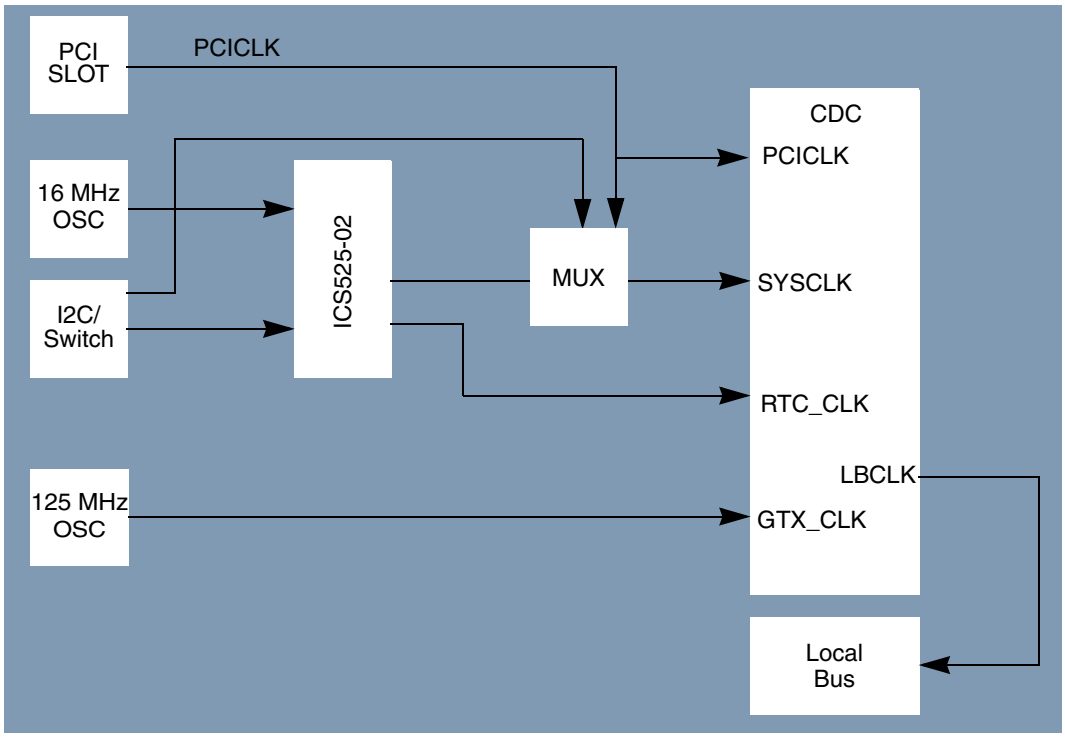


Figure 3-14. CDS Clock Architecture

The clock logic is straightforward. The primary SYSCLK is taken from the local clock (ICS I CPICLK signal, depending on whether the PCI bus is active. The local clock is sent to the CDC (regardless of the PCI clock) to support asynchronous PCI/processor operations.

The 125-MHz clocks are used to drive the PHYs.

3.9 PCI-X

The CDS card provides a standard PCI edge connector for use in PCI or PCI-X motherboards. As a HIP-compatible card, CDS must operate without the presence of the PCI bus. Therefore, while signals such as $\overline{\text{PCIRST}}$ and PCICLK may be used, the carrier must contain additional circuitry to allow it to operate without the presence of the bus signals

NOTE

It is not possible to disable the PCI bus when an active PCI bus is present on the motherboard; that is, there is no isolation circuitry between the processor PCI interface and the PCI edge connector, so when CDS is plugged into a PCI slot, it must be configured to be PCI enabled.

The general PCI architecture is shown for Rev. 1.1 CDC in Figure 3-15.

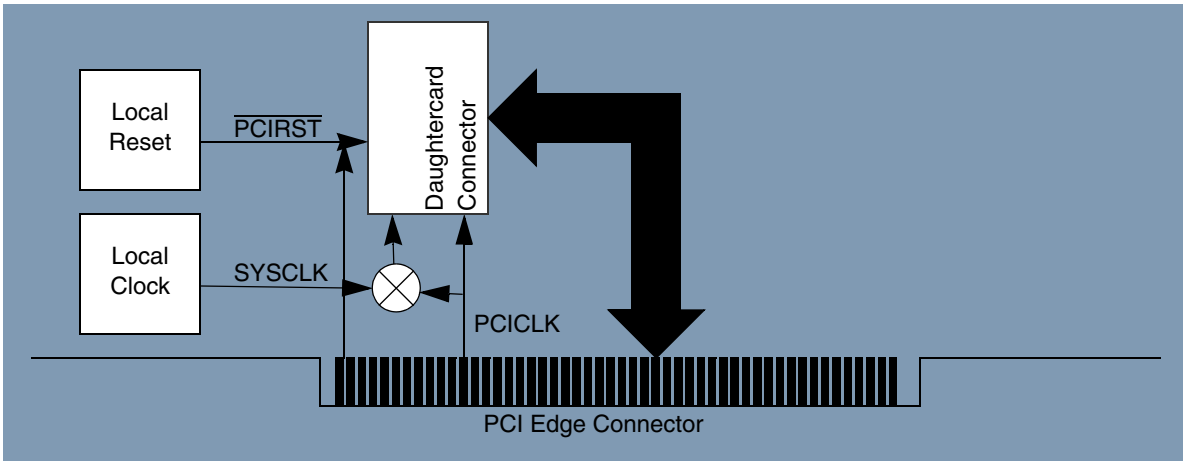


Figure 3-15. CDS PCI Architecture

The connections for the PCI bus are summarized in Table 3-20. Except as noted, connections are point to point from the card edge connector to the daughtercard connector.

Table 3-20. CDS PCI Properties

Edge Connection	Destination	Notes
PCICLK	To local clock/PCI clock switch	1
$\overline{\text{PCIRST}}$	CM FPGA for local/debug reset merging, then to daughtercard (as $\overline{\text{HRESET}}$)	
$\overline{\text{C/BE}}$[7:0]$\overline{\text{FRAME}}$ $\overline{\text{STOP}}$ $\overline{\text{PERR}}$ $\overline{\text{SERR}}$ IDSEL PAR PAR64 $\overline{\text{REQ64}}$ $\overline{\text{ACK64}}$ $\overline{\text{REQ}}$ $\overline{\text{GNT}}$	To daughtercard	
$\overline{\text{DEVSEL}}$ $\overline{\text{IRDY}}$ $\overline{\text{TRDY}}$ M66EN PCIXCAP	To daughtercard and CM (through passive probes)	

Note:

1. Per the PCI specifications, the effective clock trace length from the edge connector to the MPC85X0 (including intervening connection control logic) must be 5 cm (2.5”).

3.9.1 PCI Arbitration

PCI cards cannot provide system-side bus arbitration and HIP cards do not even require the bus to be present. Due to this, CDS does not provide any sort of PCI arbitration controls, even if the processor or daughtercard could handle it. Regardless of the ability to supply arbitration, the CPU or the bridge on the

daughtercard can be configured to act as a system host: accepting inbound PCI traffic and performing system enumerations.

This does not mean that the CDS cannot function as the PCI host, in fact in most shipped system, the CDS will be the PCI host. Arbitration and host/agent functions are associated, but entirely separable.

3.9.2 PCI-X System Control

PCIXCAP settings are determined by the daughtercard. The CM FPGA has the capability to overdrive the PCIXCAP and M66EN signals (to force them low). See the system logic registers for further details.

This is only useful if the card will be asserting system reset for other devices, and making changes is only useful before a reset.

3.10 Exceptions

CDS collects several exception (interrupts and signals) from various resources and presents them to the daughtercard for handling. Monitored interrupt sources include:

- PCI interrupts $\overline{\text{INT}}$(A:D)
- Ethernet Quad-PHY
- ATM PHYs
- Periodic timer interrupt
- Debug events

Figure 3-16 shows the overall interrupt architecture.

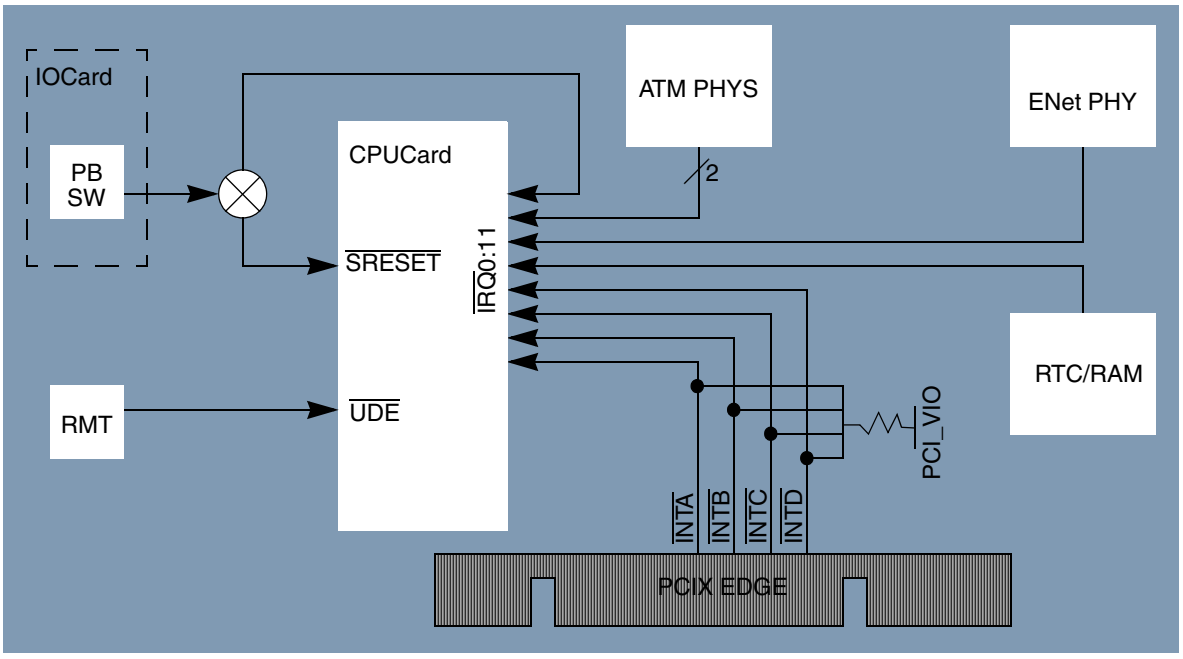


Figure 3-16. CDS Exception Architecture

The resulting connections and notes are listed in Table 3-21.

Table 3-21. CDS Exception Properties

CDC Signal	Connection	Routing	Notes
IRQ0	$\overline{\text{INTA}}$	PCI edge connector $\overline{\text{INTA}}$	1, 2
IRQ1	$\overline{\text{INTB}}$	PCI edge connector $\overline{\text{INTB}}$ PCI2 slot connector $\overline{\text{INTB}}$	1, 2, 7
IRQ2	$\overline{\text{INTC}}$	PCI edge connector $\overline{\text{INTC}}$ PCI2 slot connector $\overline{\text{INTC}}$	1, 2, 7
IRQ3	$\overline{\text{INTD}}$	PCI edge connector $\overline{\text{INTD}}$ PCI2 slot connector $\overline{\text{INTD}}$	1, 2, 7
IRQ4	Reserved	Reserved	3
IRQ5	$\overline{\text{MDINT}}$	On-board QuadPHY	3
IRQ6	$\overline{\text{ATMINT}}$	ATM PHY interrupt	3
IRQ7	$\overline{\text{CMINT}}$	CPLD interrupt (typically DMA)	3
IRQ8	Reserved	Reserved	3
IRQ9	$\overline{\text{NVINT}}$	NVRAM/RTC periodic interval timer	3
IRQ10	$\overline{\text{DEBUG}}$	Debug event switch (s/w managed)	5
IRQ11	$\overline{\text{PCI2\_INTA}}$	Second PCI bus slot interrupts	3, 4
$\overline{\text{UDE}}$	$\overline{\text{UDE}}$	Open-drain drive from remote header	
$\overline{\text{SRESET}}$	$\overline{\text{EVE1}}$	Debounced push button switch	6

Notes:

1. PCI interrupts $\overline{\text{INTA}}$–$\overline{\text{INTD}}$ are very weakly pulled-up with a 100-KΩ resistor so that the signals do not float low. This is in technically a violation of the PCI specification for plug-in cards, but is required for PCI-based HIP cards. The maximum of 4 slots produces a maximum effective pullup of 50 KΩ in addition to the HIP motherboard pullup, if any. The overall effect is deemed negligible. $\overline{\text{INTA}}$–$\overline{\text{INTD}}$ must be driven, if at all, on the daughtercard with an open-drain driver in order to assert interrupts to remote hosts. The carrier does not enforce how this is implemented.
2. These interrupts should be programmed to active-low, level-sensitive modes for PCI compatibility.
3. Unused interrupts are pulled high; the carrier need not add pullups to unused resources.
4. PCI2 interrupts are optional sources, from daughtercards with secondary PCI slot capability.
5. The software debug event is strictly a debounced switch from the viewpoint of the board and the processor; software must handle the ‘debug’ aspects. Or, just ignore it.
6. The event switch is assignable to $\overline{\text{IRQ10}}$ or $\overline{\text{SRESET}}$.
7. For the second PCI/PCI2 slot, if any.

3.10.1 Software Triggered Exceptions

Software can trigger an $\overline{\text{IRQ9}}$ event by writing to appropriate registers in the Dallas DS1553WP non-volatile SRAM/RTC. The following sequence is recommended:

Set the WatchDog Register (offset 0x1FF7 from the LCS2* base (typically 0xFD00_0000)) to

RB(1:0) = %00 (1/16 second resolution)

BMB(4:0) = %00001 (minimum delay)

WDS = %0 (assert $\overline{\text{IRQ9}}$)

After 1/16 of a second, the $\overline{\text{IRQ9}}$ interrupt will be asserted. The $\overline{\text{IRQ9}}$ handler must clear the interrupt by disabling the WatchDog timer, by writing a zero to the WatchDog Register.

3.11 Reset

The reset architecture of CDS is shown in Figure 3-17.

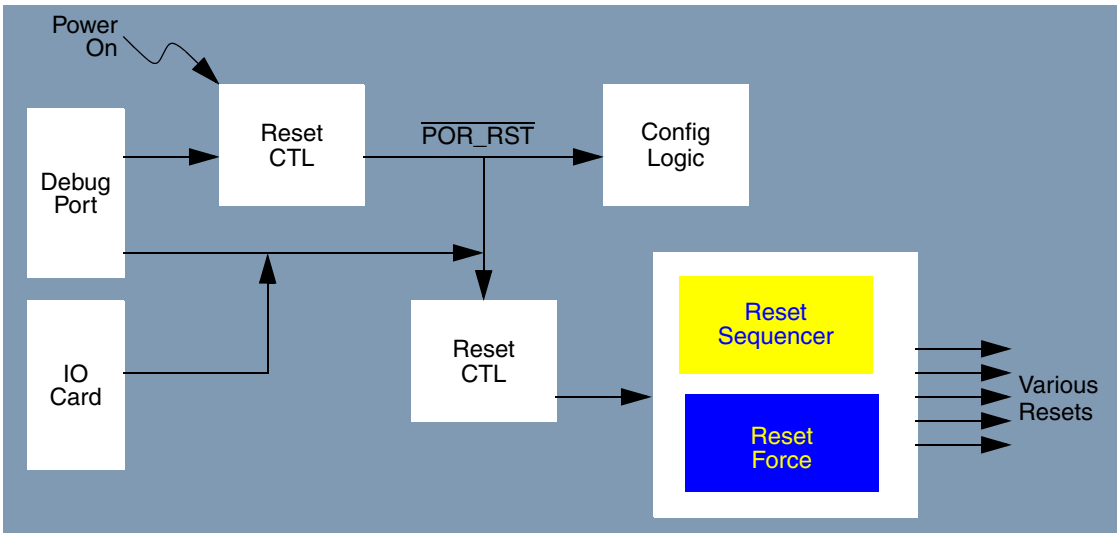


Figure 3-17. CDS Carrier Reset Architecture

The CDS has two separate resets, $\overline{\text{POR\_RST}}$ and $\overline{\text{SYS\_RST}}$. The only difference between the two is that $\overline{\text{POR\_RST}}$ resets the I2C configuration-override logic. This allows software to configure the board and still assert reset to begin repeatable tests. Asserting $\overline{\text{POR\_RST}}$ removes software overrides and then equivalently resets the target.

In addition, the system logic contains software-programmable registers which allow individual reset outputs to be asserted.

Reset sources are listed in Table 3-22, while reset outputs are listed in Table 3-23.

Table 3-22. CDS Reset Sources

Source	How Asserted	Type
Carrier	Power cycle	$\overline{\text{POR\_RST}}$
Remote control port	High-to-low transition of $\overline{\text{RMT\_POR}}$	$\overline{\text{POR\_RST}}$
Remote control port	High-to-low transition of $\overline{\text{RMT\_RST}}$	$\overline{\text{SYS\_RST}}$
Processor	High-to-low transition of $\overline{\text{HRESET\_REQ}}$	$\overline{\text{SYS\_RST}}$
NVRAM watchdog	High-to-low transition of $\overline{\text{NVRST}}$ (maskable)	$\overline{\text{SYS\_RST}}$

Table 3-23. CDS Reset Outputs

Signal	Description	How Asserted	Notes
$\overline{\text{CFGRST}}$	Configuration logic reset	Power cycle or $\overline{\text{RMT\_POR}}$ assertion	
$\overline{\text{HRESET}}$	Processor hard reset	Power cycle, $\overline{\text{HRESET\_REQ}}$, $\overline{\text{RMT\_POR}}$ or $\overline{\text{RMT\_RST}}$	
$\overline{\text{CFGDRV}}$	Configuration logic	$\overline{\text{HRESET}}$ (asserted for one extra cycle)	
$\overline{\text{ATM1\_RST}}$	Reset ATM1 PHY device	$\overline{\text{HRESET}}$ or CM_RST[ATM1_RST] asserted	
$\overline{\text{ATM2\_RST}}$	Reset ATM2 PHY device	$\overline{\text{HRESET}}$ or CM_RST[ATM2_RST] asserted	
$\overline{\text{ENET\_RST}}$	Reset quad Ethernet PHY	$\overline{\text{HRESET}}$ or CM_RST[ENET_RST] asserted	1
$\overline{\text{SYSRST}}$	Motherboard reset	$\overline{\text{HRESET}}$ or CM_RST[SYS_RST] asserted	2
$\overline{\text{MEM\_RST}}$	Memory device reset	$\overline{\text{HRESET}}$ or CM_RST[MEM_RST] asserted	3
$\overline{\text{UTCOM\_RST}}$	UTCOM_RST	$\overline{\text{HRESET}}$ or CM_RST[UTC_RST] asserted	

Notes:

1. Reset will affect all (up to four) Ethernet devices using the four-port PHY.
2. Non-standard on true HIP motherboard, but implemented on Arcadia-class motherboard.
3, If any; mostly only registered DIMMs will implement the reset input.

3.11.1 Software Triggered Resets

Software can trigger most reset events by writing to a register in the system logic. A self-reset can be achieved in the following ways:

- Assert the $\overline{\text{HRESET\_REQ}}$ signal (processor-dependent)
- Assert the CM_RST[SYS_RST] bit (motherboard-dependent)
- Use the NVRAM watchdog timer

The first option is processor-specific, consult the processor's reference manual for details. The second option is detailed in the system logic section (refer to Section 3.3, "System Logic"). For a detailed pinout, including the numbering, refer to Appendix B.1, "Carrier/DaughterCard Connectors Pinout."

The third option, using the NVRAM watchdog timer, can be triggered by writing to appropriate registers in the Dallas DS1553WP non-volatile SRAM/RTC. The following sequence is recommended:

1. Enable the WatchDog reset in the System Control register CM_RST (see Section 3.3.2, "System Logic Registers").

2. Set the WatchDog Register (offset 0x1FF7 from the LCS2* base (typically 0xFD00_0000)) to:
   RB(1:0) = %00 (1/16 second resolution)
   BMB(4:0) = %00001 (minimum delay)
   WDS = %1 (assert $\overline{\text{NVRST}}$ (which will assert $\overline{\text{HRESET}}$ to the processor and other devices)).

NOTE

The system startup code must initialize the WatchDog timer by writing a zero to the WatchDog register. Otherwise, the system will continually reset until power is cycled (because this is, as you might have guessed, a watchdog timer).

3.12 I2C

CDS makes extensive use of the I2C bus for a variety of purposes, including:

- System configuration
- Non-PCI (local) clock speed selection
- Remote control bus
- Module and system identification

Many of these functions are also available on the daughtercard, so familiarity with the CDC card in use is assumed. All current carrier cards implement the architecture of the I2C bus as shown in Figure 3-18.

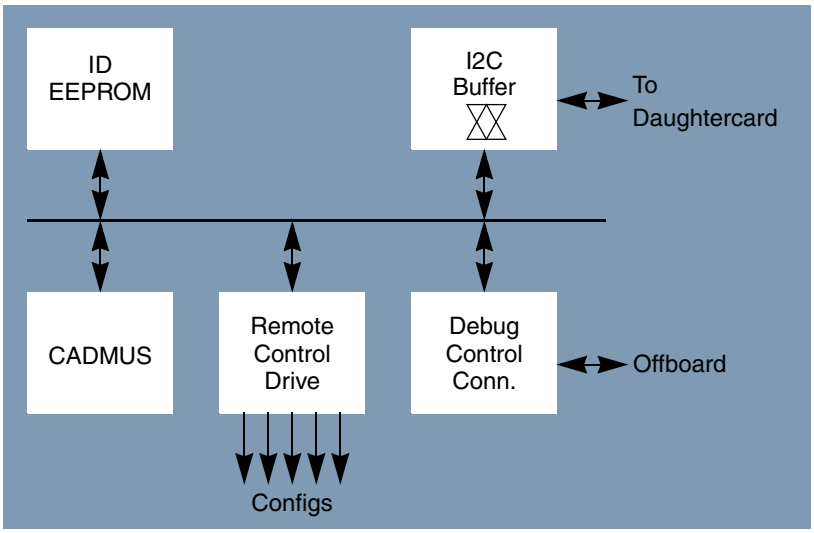


Figure 3-18. CDS Carrier I2C Architecture

Table 3-24 contains a summary of the various features of the I2C devices. Refer to the programming manual for detailed programming information, and refer to other sections of this manual for details on how the I2C-control features are implemented (specifically, Section 3.13, “Configuration”).

Table 3-24. CDS I2C Bus Properties

I2C Device	I2C Device	I2C Address	Data Size	Notes
CDC system ID EEPROM	AT24C64A	0x56 (1010_110x)	8192	
Remote control/configuration port	PCA9557	0x1C (0011_100x) 0x1D (0011_101x) 0x1E (0011_110x) 0x1F (0011_111x)	8	1, 2

Notes:
1. CDC daughtercards may also have configuration switches, at addresses 0x18.01B.
2. These devices are at different addresses and have different programming sequences as compared to the Elysium use of dual PCF9555s.

3.13 Configuration

The CDS contains many configuration options to allow it to adapt to the user's application. Many of these options are static: set at startup and remain unchanged. Others are asserted during the reset sequence (generally, this occurs on the processor/system bridge, that is, on the CDC) and after reset is concluded, revert to some other function.

Table 3-25. CDS Configuration Parameters

Configuration Option	Config. Signal	Control Method	I2C Config Port		Switch	Default
			Dev	Bits		
ATM1 mux disable	ATM1_SEL	Switch or I2C	0x24	0	SW3(8)	1 = CPM->ATM1
ATM2 mux disable	ATM2_SEL	Switch or I2C		1	SW3(7)	1 = CPM->ATM2
FE mux disable	FE_SEL	Switch or I2C		2	SW3(6)	1 = CPM->FE
ADTech select	ADT_SEL	Switch or I2C		3	SW3(5)	0 = AdTech NOT active
ATM1 width	$\overline{\text{ATM1\_16BIT}}$	Switch or I2C		4	SW3(4)	1 = ATM1 16-bit IO
ATM2 enable	$\overline{\text{ATM2\_EN}}$	Switch or I2C		5	SW3(3)	1 = ATM2 enabled
Uart_Sel		Switch or I2C		6	SW3(2)	1 = Uart_Sel
Reserved		Switch or I2C		7	SW3(1)	1 = Reserved
User-defined	USERMODE(0:1)	Switch or I2C	0x25	1–0	SW2(8:7)	00 = User defined
Reserved		Switch or I2C		2	SW2(6)	1 = Reserved [1]
Reserved		Switch or I2C		3	SW2(5)	1 = Reserved
Event select	EVE_SEL	Switch or I2C		4	SW2(4)	1 = EVE = SRESET
NVRAM disable	$\overline{\text{NVRAM\_DIS}}$	Switch or I2C		5	SW2(3)	1 = NVRAM available
Flash boot select	ROMMODE(0:1)	Switch or I2C		7–6	SW2(2:1)	00 = Standard Flash
Local clock V(6:1) select	LCLK_V(6:1)	Switch or I2C	0x26	5–0	SW4(3:8)	001000 = Part of 33MHz SYSCLK
Local clock R(2:1) select	LCLK_R(2:1)	Switch or I2C		7–6	SW4(1:2)	10 = Part of 33MHz SYSCLK

Table 3-25. CDS Configuration Parameters

Configuration Option	Config. Signal	Control Method	I2C Config Port		Switch	Default
			Dev	Bits		
Local clock R(4:3) select	LCLK_R(4:3)	Switch or I2C	0x27	1–0	SW1(7:8)	00
Local clock S(2:0) select	LCLK_S(2:0)	Switch or I2C		4–2	SW1(4:6)	011
Reserved		Switch or I2C		5	SW1(3)	1 = Reserved [2]
Synchronizer	$\overline{\text{SYNCHRO}}$	Switch or I2C		6	SW1(2)	1 = Non-synchronized
PCI enable	$\overline{\text{PCIEN}}$	Switch		7	SW1(1)	0 = PCI environment
Ext ref clock enable	$\overline{\text{MCLK\_DIS}}$	Install R168			0 Ω	

Notes:
1. SW1(3) for Configuration 2 is PCI CLK SEL and must be set to 1.
2. SW2(6) for Configuration 2 is PCI Select PCI = 1 and PCIX = 0.

CDS uses part of the reset sequence to support the options in the table above, as well as to allow hardware/software to easily change the configuration. The reset logic is executed by three-state transceivers receiving signals from the MPC85xx. The transceivers are, in turn, controlled by the CFGDRV signal, as in Table 3-25. The reset values which are configured using I2C switches, are shown in Figure 3-19.

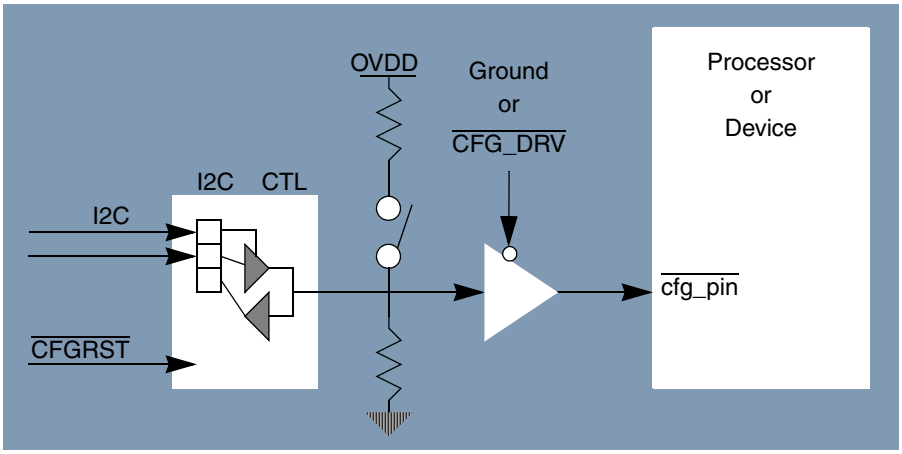


Figure 3-19. CDS Configuration Logic

The output buffer depends on the inputs, whether multipurpose or dedicated. The buffer is driven only during $\overline{\text{CFGDRV}}$ for multi-purpose inputs, but always driven for dedicated inputs.

The I2C control device powers up as an input, preventing it from interfering with either the weak external pulldown or the switch-selected, normal-strength pullup resistors. The exception is when the active drive is enabled. With the I2C three-stated, the buffer converts a resistive high or low into a clean LVTTL configuration level.

Once a particular I2C control output has been programmed, the rail-to-rail output FETs in the PCA9557 will overdrive the weaker pullup/pulldowns, granting the I2C output register direct control over the configuration logic.

Note that the I2C I/O controller outputs remain constant even when $\overline{\text{HRESET}}$ is asserted. Only a power-up reset, or the special $\overline{\text{POR\_RST}}$ signal (effectively $\overline{\text{CFGRST}}$) can reset the I2C I/O device to three-state, allowing the user-specified switch settings to take effect.

This allows the remote control system to configure the board but not have to monitor reset events (via COP or switch) and be required to intervene and reconfigure the board. This allows for the remote control system to configure the board, while removing the need for a reset monitor or reconfiguration.

3.14 Power

The power provided to the CDS system is standard, 5 and 3.3 V. It is delivered through the HIP power connectors, though additional power (if necessary) must be obtained from the PCI/PCI-X connector which can provide 5, 3.3, and 12 V as required. Table 3-20 shows the power architecture.

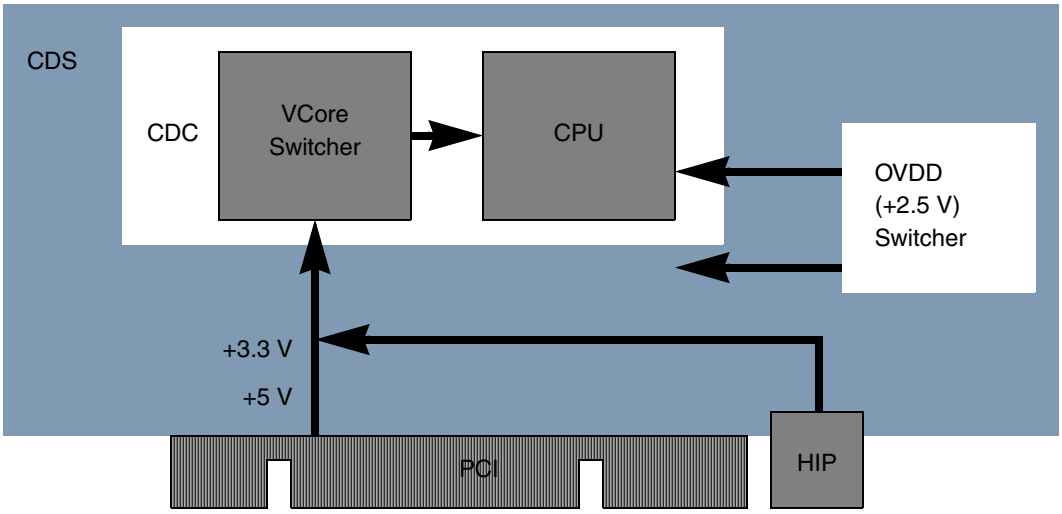


Figure 3-20. CDS Power Architecture

Table 3-26 summarizes the power available to CDS cards.

Table 3-26. CDS Available Power

Power	Source	Current	Power
5 V	HIP	2 x 7.8 A	78 W
	PCI	5 A	25 W
	Total	20.6 A	103 W
3.3 V	HIP	2 x 7.8 A	52 W
	PCI	7.6 A	25 W
	Total	23.2 A	77 W

Table 3-26. CDS Available Power (continued)

Power	Source	Current	Power
+12 V	HIP	—	—
	PCI	1 A	12 W
	Total	1 A	12 W
–12 V	HIP	—	—
	PCI	1A	12 W
	Total	1A	12 W

The power budget must be compared to the two separate 5-/3.3-V rating limits (78 W + 52 W and 103 W + 77 W, respectively) to determine if the board can be operated in a non-PCI-based environment.

3.14.1 +2.5-V Power

The +2.5-V power source is supplied by a switching power supply module. It supplies +2.5-V power to components on the carrier as well as the daughtercard, generally for I/O power or miscellaneous discrete logic. The output voltage is not digitally adjustable, though resistor options are provided for minor tweaking/experimentation. The current is measured in the same way as the processor core power.

3.14.2 Power Management

There are no power management facilities on CDS.

3.15 Diagnostic Features

CDS contains as many debug/analysis support features as may be reasonably accommodated in the compact size allocated to it. The following features are supported:

- Local bus analyzer header
- Remote control port
- LEDs

Note that features such as DDR memory bus and COP/JTAG ports are handled on the daughtercard; see the respective section/reference manual for details.

3.15.1 Analyzer Headers

The local bus may be debugged using three Mictor headers, compatible with Tektronix and Agilent logic analyzers. No shrouds are provided, but a dual footprint is provided to support installation of either the small Tektronix or the larger Agilent shrouds. Table 3-27, Table 3-28, and Table 3-29 show the pinouts for the local-bus debug headers.

Table 3-27. CDS Local Bus 'STAT' Header Definition

Pin	Signal	Mictor Definition
3	LBCLK2	Even clock
4	LBCTL	Even D15 (MSB)
5	$\overline{WE3}/\overline{BS3}$	Even D14
6	$\overline{WE2}/\overline{BS2}$	Even D13
7	$\overline{WE1}/\overline{BS1}$	Even D12
8	$\overline{WE0}/\overline{BS0}$	Even D11
9	CDC_SPR1	Even D10
10	CDC_SPR2	Even D9
11		Even D8
12		Even D7
13		Even D6
14	GPL5	Even D5
15	GPL4	Even D4
16	GPL3	Even D3
17	GPL2	Even D2
18	GPL1	Even D1
19	GPL0	Even D0 (LSB)
36	LALE	Odd clock
35		Odd D15 (MSB)
34	$\overline{RD}$	Odd D14
33	$\overline{WR}$	Odd D13
32	DP3	Odd D12
31	DP2	Odd D11
30	DP1	Odd D10
29	DP0	Odd D9
28		Odd D8
27	$\overline{CS7}$	Odd D7
26	$\overline{CS6}$	Odd D6
25	$\overline{CS5}$	Odd D5
24	$\overline{CS4}$	Odd D4
23	$\overline{CS3}$	Odd D3
22	$\overline{CS2}$	Odd D2
21	$\overline{CS1}$	Odd D1
20	$\overline{CS0}$	Odd D0 (LSB)

Table 3-28. CDS Local Bus 'ADDR' Header Definition

Pin	Signal	Mictor Definition
3	LACLK	Even clock
4	$\overline{\text{LCL\_RST}}$	Even D15 (MSB)
5	$\overline{\text{IRQ0}}$	Even D14
6	TP28	Even D13
7		Even D12
8		Even D11
9		Even D10
10		Even D9
11		Even D8
12	CLA23 (MSB)	Even D7
13	CLA22	Even D6
14	CLA21	Even D5
15	CLA20	Even D4
16	CLA19	Even D3
17	CLA18	Even D2
18	CLA17	Even D1
19	CLA16	Even D0 (LSB)
36	PCICLK	Odd clock
35	CLA15	Odd D15 (MSB)
34	CLA14	Odd D14
33	CLA13	Odd D13
32	CLA12	Odd D12
31	CLA11	Odd D11
30	CLA10	Odd D10
29	CLA9	Odd D9
28	CLA8	Odd D8
27	CLA7	Odd D7
26	CLA6	Odd D6
25	CLA5	Odd D5
24	CLA4	Odd D4
23	CLA3	Odd D3
22	CLA2	Odd D2
21	CLA1	Odd D1
20	CLA0 (LSB)	Odd D0 (LSB)

Table 3-29. CDS Local Bus 'DATA' Header Definition

Pin	Signal	Mictor Definition
3		Even clock
4	LB_D0 (MSB)	Even D15 (MSB)
5	LB_D1	Even D14
6	LB_D2	Even D13
7	LB_D3	Even D12
8	LB_D4	Even D11
9	LB_D5	Even D10
10	LB_D6	Even D9
11	LB_D7	Even D8
12	LB_D8	Even D7
13	LB_D9	Even D6
14	LB_D10	Even D5
15	LB_D11	Even D4
16	LB_D12	Even D3
17	LB_D13	Even D2
18	LB_D14	Even D1
19	LB_D15	Even D0 (LSB)
36		Odd clock
35	LB_D16	Odd D15 (MSB)
34	LB_D17	Odd D14
33	LB_D18	Odd D13
32	LB_D19	Odd D12
31	LB_D20	Odd D11
30	LB_D21	Odd D10
29	LB_D22	Odd D9
28	LB_D23	Odd D8
27	LB_D24	Odd D7
26	LB_D25	Odd D6
25	LB_D26	Odd D5
24	LB_D27	Odd D4
23	LB_D28	Odd D3
22	LB_D29	Odd D2
21	LB_D30	Odd D1
20	LB_D31	Odd D0 (LSB)

3.15.2 Remote Debug Header

This 2x5-pin right-angle Berg header is used for special test environments. Table 3-30 shows the pin definitions.

Table 3-30. CDS Remote Header

Pin	Signal	Definition
1	SCL	I2C serial clock
2	SDA	I2C serial data
3	GND	System ground
4	GND	System ground
5	N/C	
6	N/C	
7	RMT_UDE	$\overline{\text{UDE}}$ drive (open-drain). Pulled up to 3.3 V.
8	N/C	
9	RMT_RST	Open-collector active-low reset input. Pulled up to ~3 V.
10	RMT_POR	Open-collector active-low power-on reset input. Pulled up to ~3 V.

The connectors are physically arranged as shown in Table 3-31.

Table 3-31. CDS Debug Header Definition

1	2
3	4
5	6
7	8
9	10

3.15.3 Monitoring LEDs

CDS has numerous LEDs dedicated to monitoring system status, as described in Table 3-32.

Table 3-32. CDS LEDs

LED Label	LED No.	Definition
OVDD	N/A	OVDD (+2.5-V power) operational
VDD3	N/A	VDD3 (+3.3-V power) operational
L0_VDD	0	VDD (processor core) power operational
L1_PCIEN	1	PCI bus enabled
L2_PCI	2	PCI bus activity detected
L3_SLEEP	3	Processor halted/idle
L4_RESET	4	Reset asserted

Table 3-32. CDS LEDs (continued)

LED Label	LED No.	Definition
L5_CLK	5	Clock active
L6_MEM	6	Flash/local-bus memory active
L7_MISC	7	Miscellaneous reporting

Note that software can override the functions of LEDs 0–7 and replace them with user-defined activity.

Chapter 4
CDS Daughtercard Architecture

The following sections will cover the CDS daughtercard (CDC) design in more detail. Note that, because the daughtercard is the most interchangeable part of the CDS system, this section will be more general. Refer to the data sheets for more detail on a particular daughtercard.

The CDS system supports a variety of processors, both individual and integrated devices. Since there is one unique daughtercard for each unique processor footprint, each card will be slightly different.

This chapter provides details on what is supported on specific cards for the processor-specific daughtercard hardware.

4.1 Mechanical Architecture

The CPU daughtercard is sized and placed as shown in Figure 4-1.

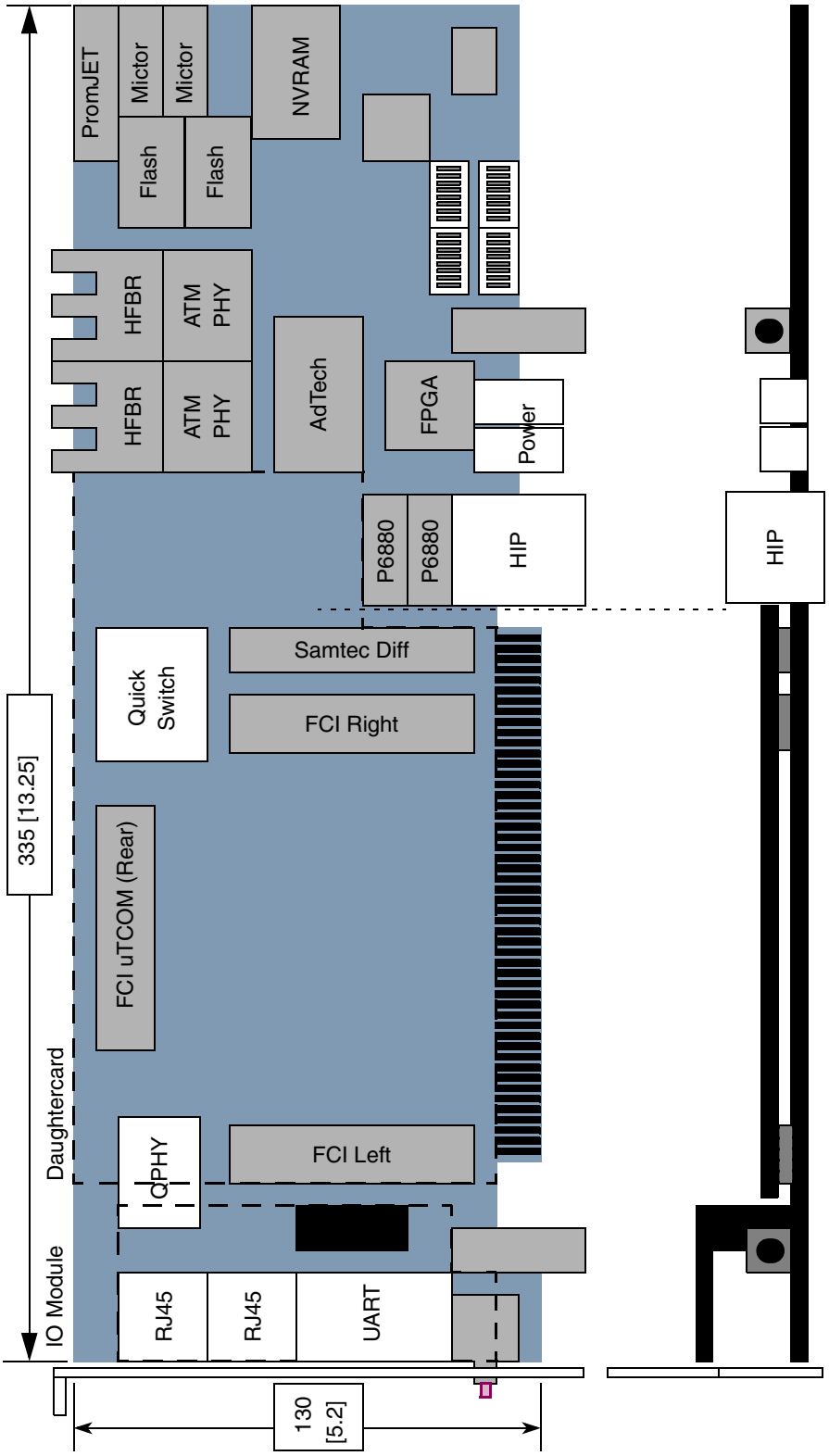


Figure 4-1. Daughtercard Placement

The daughtercard's large dimension allows multiple cards to be inserted into the Arcadia HIP motherboard, but it is not big enough to restrict access to the carrier communication components. The CDC dimensions are as follows:

- Component height at the top: 15 mm
- Component height at the bottom: 4 mm

Figure 4-2 shows the placement of the processor on the daughtercard.

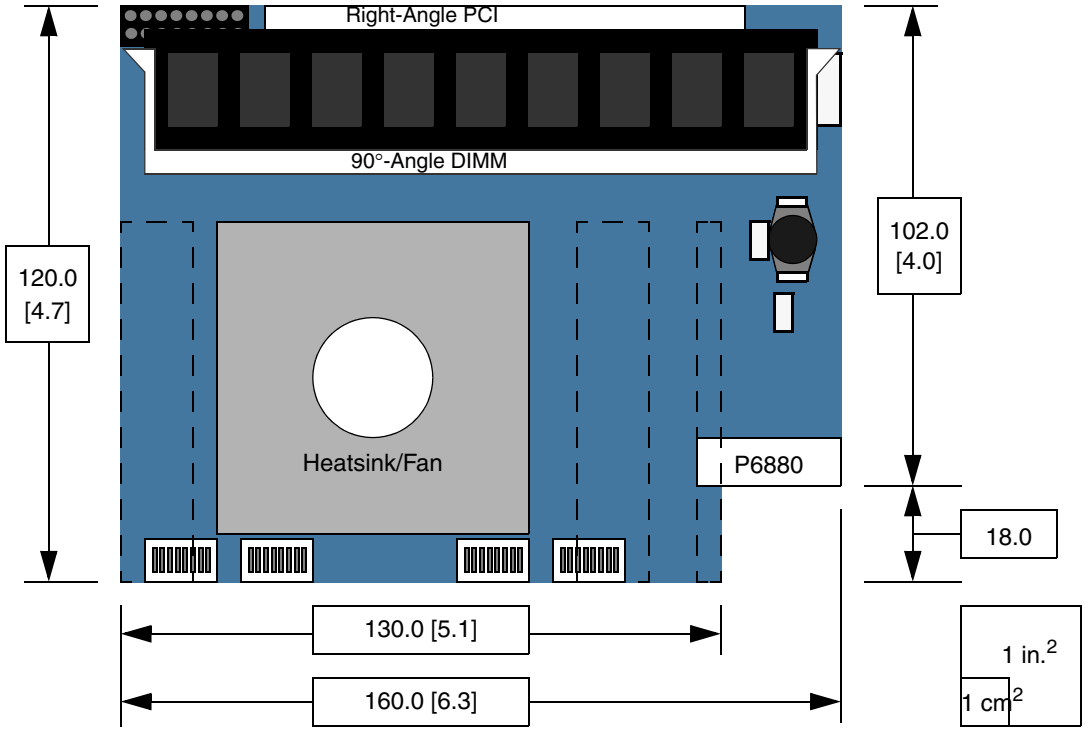


Figure 4-2. CDC with 783 BGA Processor Example

4.2 CDS Daughtercard (CDC) Block Diagram

Figure 4-3 is a diagram of a CDS daughtercard or a CDC.

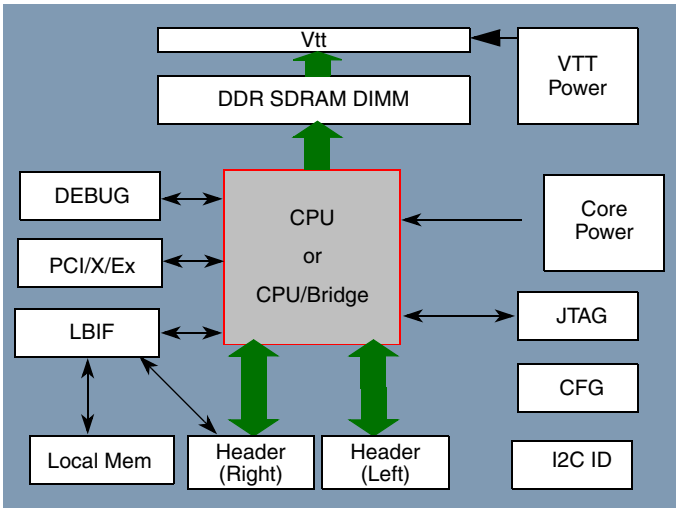


Figure 4-3. Daughtercard Block Diagram

This representation is only one, others can be designed for different CPUs.

4.3 Processor

The different processors is the primary reason for the existence of the daughtercard, and thus will vary widely in different CDCs. In general, each daughtercard will connect most of its signals to the appropriate ports on the high-density connector. Any bus which does not interface smoothly with the daughtercard/carrier architecture will be handled locally on the daughtercard. This can include:

- Secondary PCI buses
- Special power management interface
- Compact Flash/IDE interface
- Wireless interfaces

4.4 DDR Memory

The SDRAM connection of DDR-I is handled locally on the CDC. On CDS boards, the processor/DDR interface is connected to the JEDEC DDR SDRAM DIMM socket, capable of holding a maximum of 2 GB of memory. The memory interface includes all the necessary power and is routed to achieve maximum performance on the memory bus.

Further debugging support is handled by expansion logic analyzer interface cards installed in the DIMM socket.

The general DDR SDRAM architecture is shown in Figure 4-4.

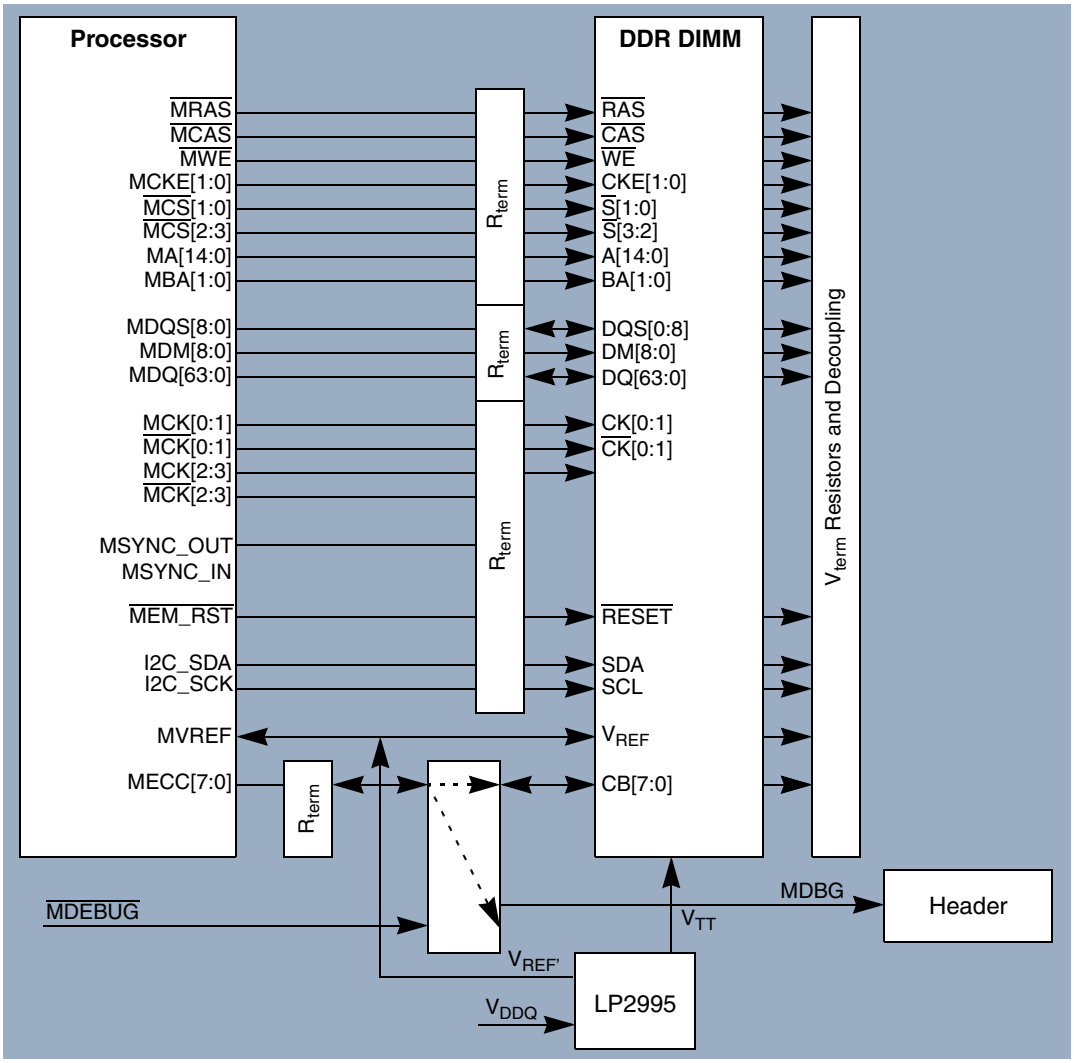


Figure 4-4. CDS Memory Architecture

The memory subsystem bus is single-endedly terminated via series and parallel terminations. Power for the termination plane (V_{TT}) is supplied through a National LP2995, which supplies up to 1.5 A continuously (3 A transient response). This is sufficient for the upper limit generally expected for DDR termination, while actual termination power requirements are significantly less.

In addition, the LP2995 supplies V_{REF} to the processor and DIMMs. The V_{REF}/V_{TT} levels are adjustable using a resistor to alter the threshold slightly. By default, V_{REF} is set to 1.25 V.

As shown in Figure 4-4, the DDR SDRAM parity/ECC pins (MECC[7:0]) are used to display debugging information in certain debug modes. In such a case, the MECC pins must be disconnected from the memory interface (since CB[7:0] from the DDR memories are bidirectional) and routed to the debugging interface connector.

The processor supplies two differential clocks to the memory modules. These signals are not parallel terminated. The signals are described in Table 4-1.

Table 4-1. CDS DDR SDRAM Properties

DDR SDRAM Signal	Description	JEDEC DDR SDRAM Module Pin		Notes
$\overline{\text{MRAS}}$	Row address strobe	$\overline{\text{RAS}}$	154	
$\overline{\text{MCAS}}$	Column address strobe	$\overline{\text{CAS}}$	65	
$\overline{\text{MCS0}}$ $\overline{\text{MCS1}}$	Module bank 0 chip select Module bank 1 chip select	$\overline{\text{S0}}$ $\overline{\text{S1}}$	157 158	
$\overline{\text{MCS2}}$ $\overline{\text{MCS3}}$	Module bank 2 chip select Module bank 3 chip select	$\overline{\text{S2}}$ $\overline{\text{S3}}$	71, 163	
$\overline{\text{MWE}}$	Write enable	$\overline{\text{WE}}$	63	
MCKE[0:1]	Clock enable	CKE0 CKE1	21 111	
MDA[0:13]	Address	A[0:13]	48, 43, 41, 130, 37, 32, 125, 29, 122, 27, 141, 118, 115, 103,	
MDA14	Address	A14	N/A	1
MBA[0:1]	Bank select	BA0, BA1	59, 52	
MDQ[0:63]	Memory data	DQ[0:63]	2, 4, 6, 8, 94, 95, 98, 99, 12, 13, 19, 20, 105, 106, 109, 110, 23, 24, 28, 31, 114, 117, 121, 123, 33, 35, 39, 40, 126, 127, 131, 133, 53, 55, 57, 60, 146, 147, 150, 151, 61, 64, 68, 69, 153, 155, 161, 162, 72, 73, 79, 80, 165, 166, 170, 171, 83, 84, 87, 88, 174, 175, 178, 179	
MDQS[0:8]	Data strobes (low)	DQS[0:8]	5, 14, 25, 36, 56, 67, 78, 86, 47	
MDM[0:8]	Data strobes (high)/data mask	DM[0:8] (DQS[9:17])	97, 107, 119, 129, 149, 159, 169, 177, 140	
MECC[0:7]	ECC data/check bits/debug	CB[0:7]	44, 45, 49, 51, 134, 135, 142, 144	
MCK[0] MCK_B[0]	Differential clocks	CK0 $\overline{\text{CK0}}$	137, 138	3
MCK[1] MCK_B[1]	Differential clocks	CK1 $\overline{\text{CK1}}$	16, 17	3
MCK[2] MCK_B[2]	Differential clocks	CK2 $\overline{\text{CK2}}$	76, 75	3
MCK[3:5] MCK_B[3:5]	Differential clocks	N/A		3
MSYNC_OUT	Reference clock output	N/A		
MSYNC_IN	Reference clock input	N/A		
MVREF	SSTL-2 reference voltage	V_{REF}	1	
$\overline{\text{MEM\_RST}}$	Reset	$\overline{\text{RESET}}$	10	
I2C_SDA	SPD I2C SDA	SDA	91	

Table 4-1. CDS DDR SDRAM Properties (continued)

DDR SDRAM Signal	Description	JEDEC DDR SDRAM Module Pin		Notes
I2C_SCK	SPD I2C SCK	SCL	92	
N/A	SPD write protect	WP	90	
<var>	SPD address	SA[0:2]	181, 182, 183	2
GVDD	Memory IO power	V_{DDQ}	15, 22, 30, 54, 62, 77, 96, 104, 112, 128, 136, 143, 156, 164, 172, 180	
GVDD	Memory power	V_{DD}	7, 38, 46, 70, 85, 108, 120,148	
GND	Ground	GND	3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 81, 89, 93, 100, 116, 124, 132, 139, 145, 152, 160, 176	
	NC	V_{DDID}	82	
	SPD EEPROM power	V_{DDSPD}	184	

Notes:

1. MA14 unused with current JEDEC DDR modules. MA14 is brought out to a termination resistor in the event a standard MA14 is defined for DDR SDRAM modules.
2. Address = 3B001 for DIMMs #1.
3. Clock (0:2) for DIMM #1 only. The remaining clock outputs are terminated to ground through a capacitor.

4.4.1 DDR Interface Termination

The termination of the DDR interface is critically important because of its ability to operate at high speeds. The general architecture of the termination is shown in Figure 4-5.

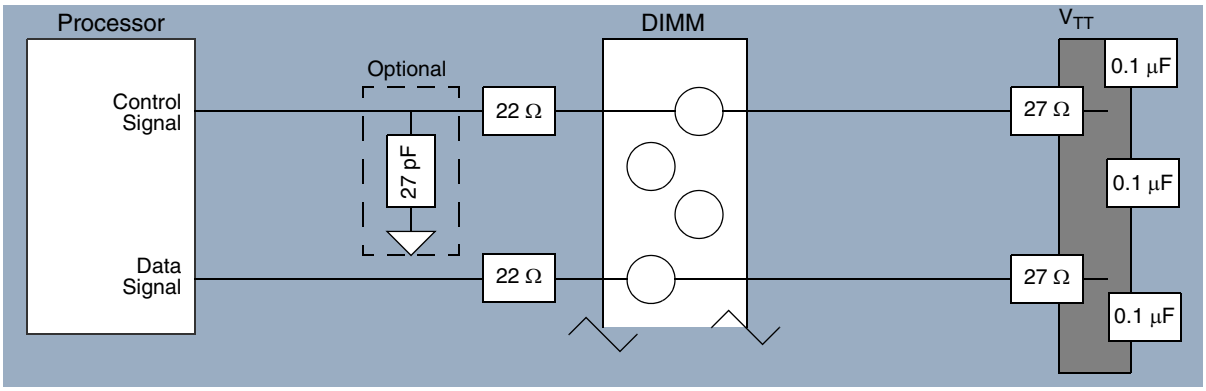


Figure 4-5. CDC Memory Termination

Unlike most series termination usage, for DDR control signals, the 22-Ω termination resistors (1%) are placed near the DDR DIMM. This facilitates routing breakout, which improves the signal integrity of data. This improvement matches the loaded impedance of unidirectional signals on the DIMM (address, command, chip-select).

A 22-Ω resistor is selected to match the processor impedance to the PWB impedance, but can be trimmed or altered as necessary. After daisy-chaining the control signals, the line is extended to a 27-Ω resistor (also 1%) which connects directly to the V_{TT} termination plane.

4.4.2 Recommended Part Numbers

For performance and compatibility purposes, only the devices shown in Table 4-2 are guaranteed to work. Other devices may operate, but architectural issues may affect performance.

Table 4-2. CDS DDR SDRAM Compatibility

Manufacturer	Size	Type	Speed	Part Number
Samsung	512 MB	Unbuff, nonECC	DDR400	M368L6523BTM-C(L)CC/C4 M368L6423FTN-C(L)CC
			DDR333	M368L6423FTN-C(L)B3
			DDR266	M368L6423FTN-C(L)AA
	512 MB	Unbuff, ECC	DDR400	M381L6423FTN-C(L)CC
			DDR333	M381L6423FTN-C(L)B3
			DDR266	M381L6423FTN-C(L)AA
	1 GB	Unbuff, nonECC	DDR400	M368L2923BTM-C(L)CC/C4
		Unbuff, ECC	DDR400	M381L2923BTM-C(L)CC/C4
Hynix	512 MB	Unbuff, nonECC	DDR400	HYMD564646A8J-D43
		Unbuff, ECC		HYMD564726A8J-D43
	1 GB	Unbuff, nonECC		HYMD512646A8J-D43
		Unbuff, ECC		HYMD512726A8J-D43

4.5 Local Bus Interface

The local bus interface of many processors varies widely, including:

- Direct connections for the Tsi106/Tsi107 family
- 32-bit multiplexed address/data of the MPC85xx family

To accommodate this flexibility, each daughtercard is responsible for presenting an abstract interface to the carrier board. This interface is designed around a typical Flash/IO-device interface.

For processors which may support high-speed SRAM or SDRAM on their local bus, the daughtercard is responsible for isolating the high-speed devices from the relatively slower-speed local bus (with respect to the carrier board). This has the advantage of supporting the flexibility of the processor local bus interface. It also electrically isolates the high-speed devices from the carrier, which tends to reduce the upper bound of their operating speed.

In addition to the standard interface signals, an additional set of signals (LB_SIZ(1:0)) are generated on the daughtercard. These signals indicate the width of the access to the boot flash and other carrier peripherals. The carrier is responsible for adjusting the local bus interface to those devices, so that they

interface properly with the peripherals supported on the carrier. If differing access sizes are needed, LB_SIZ can be generated dynamically, however, it is typically only set to one particular size.

NOTE

The data bus size option only affects how the CDC and carrier provide access to Flash memory (particularly for boot code). It does not affect the ability to generate cycles of any size to other devices; in particular, to the uTCOM/TCOM devices and/or anything else attached to the CPM interface.

Figure 4-6 shows the local bus implementation for the CDC. See Table 3-16 for a description of the local bus interface signals.

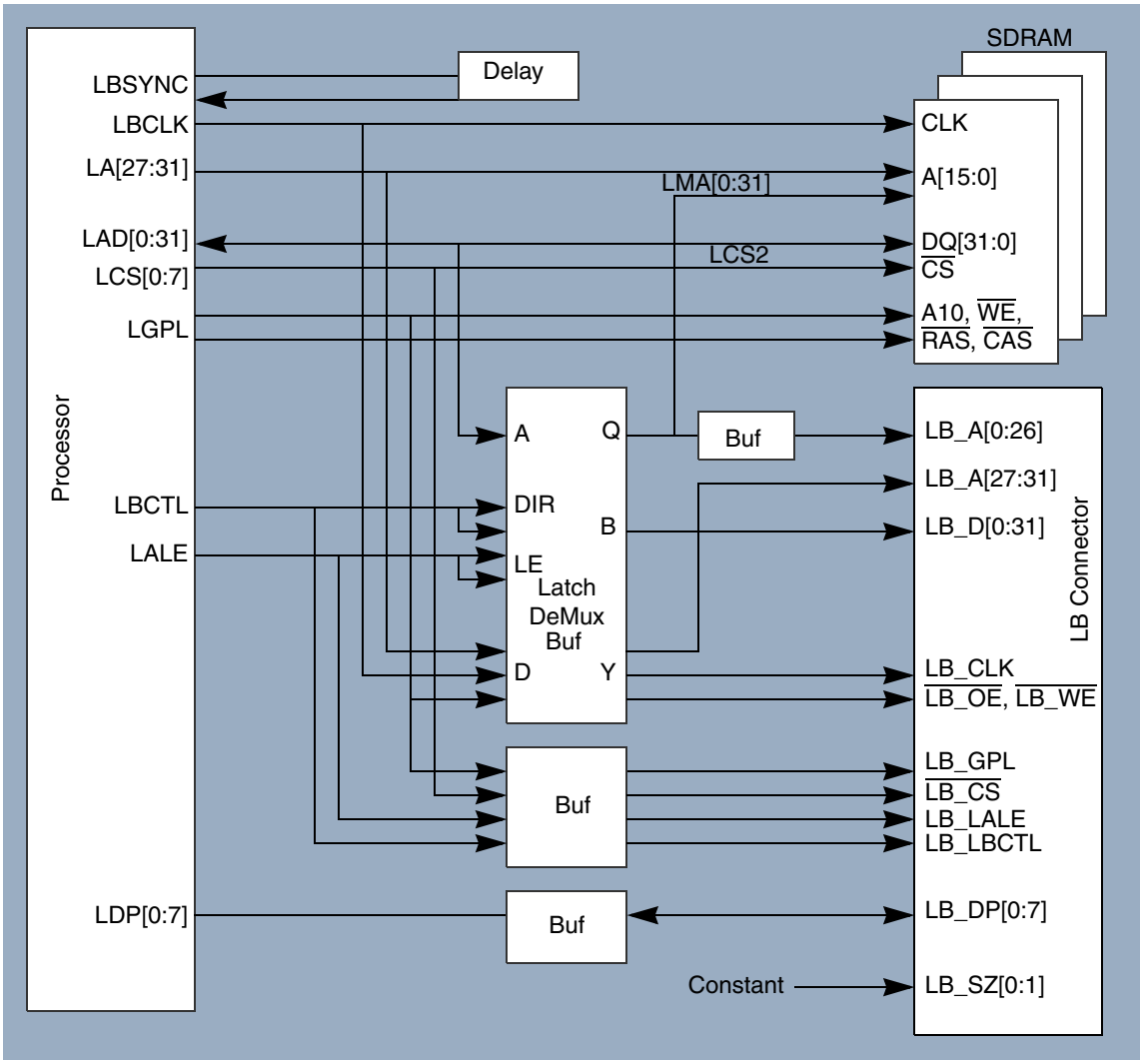


Figure 4-6. CDS Local Bus Architecture

Table 4-3 lists the daughtercard connector pins.

Table 4-3. CDS Daughtercard Local Bus Signals

Signal Name	Maximum HSBus Load	Minimum LSBus Load	Notes
LA(27:31)	4	4	
LAD(0:31)	3	4	
LDP(0:3)	2	4	
LALE(0:3)	3	2	
LBCTL	4	2	+1 for config connection
$\overline{\text{LWE}}$(0:3)	2	1	
$\overline{\text{LB\_CS0}}$	1	1	Cadmus (for Flash array #1)
$\overline{\text{LB\_CS1}}$	1	1	Cadmus (for Flash array #2)
$\overline{\text{LB\_CS2}}$	4	0	SDRAM
$\overline{\text{LB\_CS3}}$	1	0	Cadmus (for NVRAM/RTC/Cadmus regs)
$\overline{\text{LB\_CS4}}$	1	0	
$\overline{\text{LB\_CS5}}$	1	0	Typically TCOM interface
$\overline{\text{LB\_CS6}}$	1	1	Typically TCOM interface
$\overline{\text{LB\_CS7}}$	1	0	
LCKE	4	0	
LCLK(0:1)	2	0	
LCLK(2)	1	1	
LGPL	4	2	
LSYNC	1	0	

The local bus should be routed with careful attention to loading, which is nominally from 6–24 pF. The design goal is 166-MHz operation. The buffered local bus signals are much less critical, typically operating 90–120 ns Flash devices, etc.

4.5.1 Local Bus SDRAM Memory

NOTE

Parity/ECC is not supported on this interface.

4.6 Passive Connections

Almost all buses on the processor are routed to the carrier board through a high-speed, high-density connection. The exceptions are DDR memory, local bus demultiplexing, local bus memory, and an

optional second PCI slot. There are two separate connectors to provide easier routing and vacate the area under the processor for mechanical reasons.

The connectors and brief pinout are described in Table 4-4.

Table 4-4. CDS Daughtercard Connector Overview

Signal Group	Signals	Left Pin Count	Right Pin Count	Notes
CPM base	PA(0:31), PB(4:31), PC(0:31), PD(4:31)	60	60	
CPM expansion	CX(0:59)		32	Expansion for CE engines
PCI	AD[63:0] C_BE[7:0] PAR PAR64 FRAME_B TRDY_B IRDY_B STOP_B DEVSEL_B IDSEL REQ64_B ACK64_B PERR_B SERR_B REQ_B GNT_B LOCK M66EN PCIXCAP PCIRST PCI_DUAL	89	2	
Enet MI	MDC, MDIO	2		
I2C	SDA, SCL		2	
TSEC1	TSEC1(24:0)	25		
TSEC2	TSEC2(24:0)	25		
TSEC3	TSEC3(24:0)	25		
Local Bus	LB_A(0:31) LB_D(0:31) LB_DP(0:3) LB_WE(0:3) LB_CS(0:7) LALE LBCTL LGPL(0:5) LB_CLK LBSIZ(0:1)		91	
DMA	DMARQ(0:1) DMACK(0:1) DMADN(0:1)		6	
Interrupt	IRQ(0:11)		12	
System Control	PWRGD, MCP, UDE, HRESET, SRESET, CFGRST, CFGDRV, HRESETREQ, ASLEEP	6	2	
DUART	S1_SI, S1_SO, S1_RTS, S1_CTS S2_SI, S2_SO, S2_RTS, S2_CTS	8		
I2C	SDA, SCK	2		
Clock	SYSCLK	1		
	PCICLK	1		
	GTXCLK	1		125 MHz PHY clock
	RTC		1	
Misc	OVM		1	
Power 5.0V	VCC_5	0	16	Imax = 7.2 A, Pmax = 36.0 W
Power 3.3V	VCC_3.3	17	13	Imax = 13.5 A, Pmax = 44.5 W
Power 2.5V	VCC_2.5	22	19	Imax = 18.5 A, Pmax = 46.2 W

Table 4-4. CDS Daughtercard Connector Overview (continued)

Signal Group	Signals	Left Pin Count	Right Pin Count	Notes
Power +12V	VCC_12V	2	0	Imax = 0.9 A, Pmax = 10.8 W
Power –12V	VCC_12N	0	1	Imax = 0.5 A, Pmax = 5.4 W
Ground	GND	95	86	
USB 2.0	U1_TP, U1_TN, U1_OC U2_TP, U2_TN, U2_OC	6		
Subtotal		387	344	
Spares		13	56	Bring up to next connector size
Total		400	400	

Note: The FCI connector supports 0.45 A/pin.

4.7 Carrier Pinouts

For a detailed pinout, including numbering, refer to Appendix B.1, “Carrier/DaughterCard Connectors Pinout.”

4.8 Clock

There are five pre-defined clock sources available to the CDC, as detailed in Table 4-5.

Table 4-5. CDC Clocks

Clock Signal	Interface	Rate	Notes
PCICLK	LVTTL	33–66 MHz	Generally supplied by either the PCI clock of the HIP motherboard, or the local clock of the carrier. Used by processors/bridge logic which operate synchronous to the PCI interface.
PCICLK2	LVTTL	66 MHz	Created by the CDC for cards with secondary PCI slots. An on-board oscillator is provided to generate this clock (which is independent of all other clocks).
SYSCLK	LVTTL	0–300 MHz	Supplied by the HIP motherboard, independent of the PCICLK rate. Used by processors/bridge logic which operate asynchronous to the PCI interface.
RTCCLK	512 MB	16 MHz	Timebase clock
GTXCLK	1 GB	125 MHz	Clock for GBit Ethernet PHYs and/or interfaces.

As discussed in Section 3.8, “Clock,” clocks may or may not be synchronous to any other clock. Also, they may or may not be synchronous to the de-assertion timing of $\overline{\text{HRESET}}$. Such an environment is determined by the carrier board.

4.9 PCI/PCI-X

The PCI/PCI-X signals from the primary PCI interface of the processor are connected to the edge connector of the CDS carrier board. In addition, some processors have a secondary PCI interface, which may operate independently of the primary PCI bus. If implemented, the optional PCI interface is connected to a PCI connector on the CDC, and is completely independent of the primary PCI interface.

For systems which switch between one 64-bit and two 32-bit PCI interfaces, isolation logic is necessary to isolate the secondary PCI interface from the 64-bit PCI extensions, as shown in Figure 4-7.

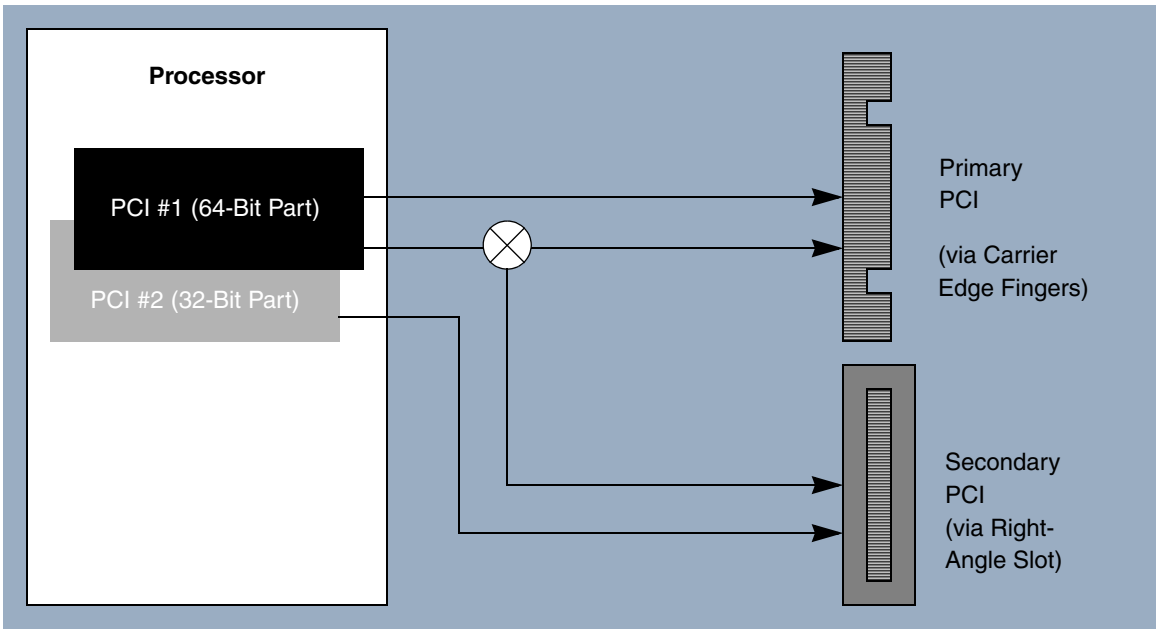


Figure 4-7. CDS Dual-PCI Architecture

NOTE

The secondary PCI interface does not detect the bus speed via M66EN/PCIXCAP; instead these settings are specified manually.

The resulting connections and notes are listed in Table 4-6.

Table 4-6. CDC PCI2 IDSEL Mapping

PCI2 IDSEL	Device
20	Processor
21	PCI2 slot

4.10 Reset

The daughtercard receives a reset signal ($\overline{\text{HRESET}}$) from the carrier board and sends it to the processor(s), bridge logic, and memory. This reset signal is merged with the JTAG header $\overline{\text{JTAG\_HRST}}$ to allow either source to reset the processor.

A second reset ($\overline{\text{CFGRST}}$) is optionally asserted along with $\overline{\text{HRESET}}$. They have the same period and edge rate, but $\overline{\text{CFGRST}}$ is delayed one clock cycle. This signal is used to drive configuration data onto processor/bridge configuration pins, which in turn are sampled at the rising edge of $\overline{\text{HRESET}}$.

The daughtercard can also drive a reset to the carrier using the signal $\overline{\text{HRST\_REQ}}$, and possibly to the motherboard (this is motherboard-dependent). Processors may use this to reset themselves, and optionally the entire system as well.

The general reset architecture is shown in Figure 4-8.

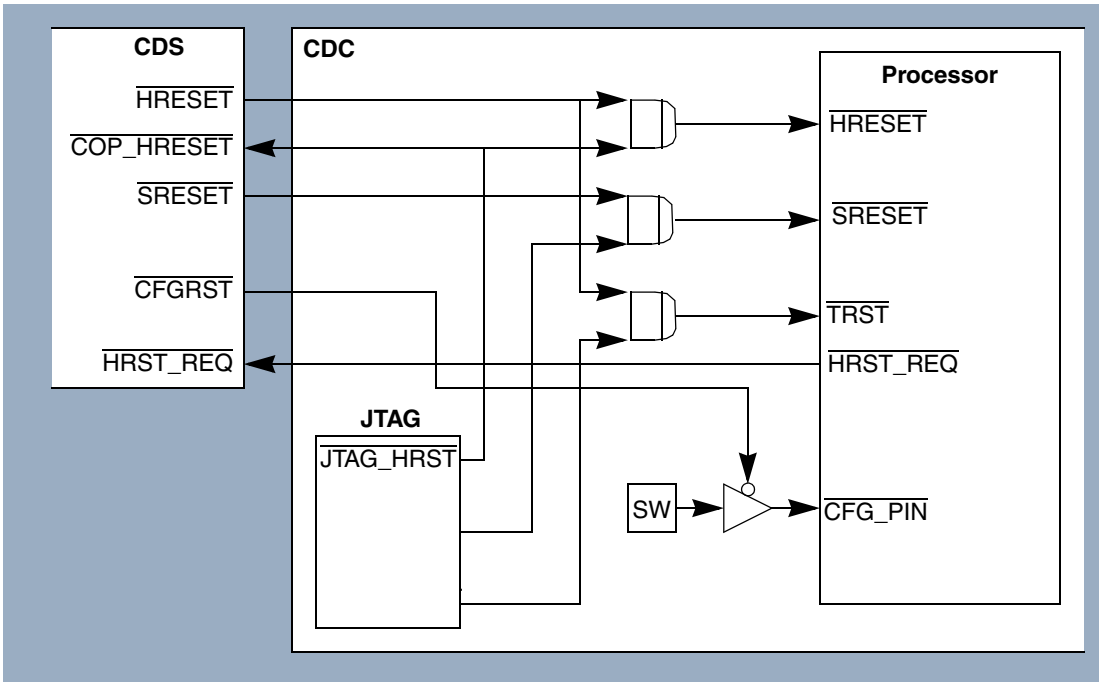


Figure 4-8. CDS Daughtercard Reset Architecture

4.11 Exceptions

Interrupts are generally handled transparently on the carrier, with little interference by the CDC. One exception is when special-purpose localized interfaces are present on the CDC (such as a second PCI interface, special PHY or other interrupt-generating device), on dedicated interfaces or the local bus.

The carrier connections and notes were previously described in Table 3-21, but they also apply to local CDC connections. Note that the CDCs are allowed considerable leeway in assigning/sharing localized and global interrupts, as long as sharing is compatible, and documented. Table 4-7 shows the properties of the local CDS exceptions as they apply to the CDC.

Table 4-7. CDS Exception Properties

CDS Signal	Carrier Connection	CPUCard Connection	Routing
IRQ0	$\overline{\text{INTA}}$		PCI edge connector $\overline{\text{INT}}$(A:D)
IRQ1	$\overline{\text{INTB}}$		
IRQ2	$\overline{\text{INTC}}$		
IRQ3	$\overline{\text{INTD}}$		
IRQ4	Reserved		Reserved
IRQ5	$\overline{\text{MDINT}}$		On-board QuadPHY
IRQ6	$\overline{\text{ATMINT}}$		ATM PHY interrupt
IRQ7	$\overline{\text{CMINT}}$		CPLD interrupt (typically DMA)
IRQ8	Reserved		Reserved
IRQ9	$\overline{\text{PERINT}}$		NVRAM/RTC periodic interval timer
IRQ10	$\overline{\text{DEBUG}}$		Debug event switch (s/w managed)
IRQ11		PCI2_INTA#	Second PCI bus slot interrupts

4.12 I2C

The processor module generally supports one or more I2C ports for storage of initialization and configuration settings. The overall block diagram of the CDC I2C bus is shown in Figure 4-9.

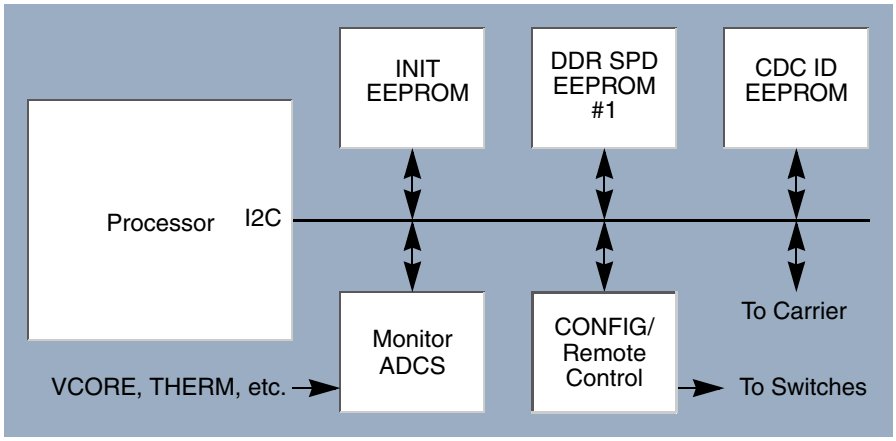


Figure 4-9. CDS Daughtercard I2C Architecture

The CDC provides the I2C resources listed in Table 4-8.

Table 4-8. CDS Daughtercard I2C Bus Properties

I2C Device	I2C Device	I2C Address	Data Size	Notes
Remote control/configuration port	PCA9555	0x18 (0011_000x) 0x19 (0011_001x) 0x1A (0011_010x) 0x1B (0011_011x)	8	
System configuration EEPROM	AT24C64A	0x50 (1010_000x)	8192	1
DDR SDRAM SPD EEPROM	AT24LC02	0x51 (1010_001x)	256	2
CDC ID EEPROM	AT24C64A	0x57 (1010_111x)	8192	
Voltage monitor ADCs	MAX1036	0xC8 (1100_100x)	16	

Notes:
1. Only extended address I2C EEPROM devices are supported.
2. Device shown is just a compatible example; this device is actually on the DIMM memory module.

4.13 Configuration

As with the CDS, CDCs include a large number of configuration options. Due to a variance in configuration needs of processors/bridge logic, this section is dependent on the CDC processor.

Some options are designed to be easily changeable, and use the same I2C-overrideable switch configuration logic used on the carrier (see Section 3.13, “Configuration”). Other infrequently used options are implemented with optional resistor installation, requiring removal and/or installation of SMT resistors.

Configuration options fall into two classes: persistent and dynamic. Persistent configuration values are connected to dedicated pins which have no other function. These signals can be connected to resistors or switches, but no other help is needed. Dynamic configuration values are determined by sampling a pin at reset, after which time the pin reverts to some other function.

4.14 Power

Power for the processor core, as well as other logic on the daughtercard, comes from the +2.5- and +3.3-V power supplies. A +12 V power supply is also available for fan-sink power and switching gate drive, but not in sufficient amperage to derive any significant power from it. Table 4-9 summarizes the available power to HIP cards.

Table 4-9. CDC Available Power

Power	Pins × Current	Current	Power
+2.5 V	41 × 0.45 A	18.5 A	46.2 W
+3.3 V	30 × 0.45 A	13.5 A	44.5 W
+5.0 V	16 × 0.45 A	7.2 A	36.0 W

Table 4-9. CDC Available Power

Power	Pins × Current	Current	Power
+12 V	2 × 0.45 A	0.9 A	10.8 W
		Total	137.5 W

The power budget must be compared to approximately 170 W available to the carrier, and to the portion of that power required for the carrier itself.

4.14.1 Processor Core Power

Core power (V_{DD}) to the processor is supplied using a switching regulator. It is capable of supplying core voltages in the range 0.925–2.0 V in 25-mV steps over the lower range (0.925 to 1.275 V), and 5-mV steps elsewhere. Up to 15 A (14–30 W) is available, though most processors use much less than that. The core power is trimmed using the standard switch +I2C override method, or using the low-power VRM encoding standards as shown in Table 4-10.

Table 4-10. CDC VDD (Vcore) Encoding Table

VID					Output Voltage	VID					Output Voltage
4	3	2	1	0		4	3	2	1	0	
1	1	1	1	1	OFF[1]	0	1	1	1	1	OFF[1]
1	1	1	1	0	0.925 V	0	1	1	1	0	1.300 V
1	1	1	0	1	0.950 V	0	1	1	0	1	1.350 V
1	1	1	0	0	0.975 V	0	1	1	0	0	1.400V
1	1	0	1	1	1.000 V	0	1	0	1	1	1.450 V
1	1	0	1	0	1.025 V	0	1	0	1	0	1.500 V
1	1	0	0	1	1.050 V	0	1	0	0	1	1.550 V
1	1	0	0	0	1.075 V	0	1	0	0	0	1.600 V
1	0	1	1	1	1.100 V	0	0	1	1	1	1.650 V
1	0	1	1	0	1.125 V	0	0	1	1	0	1.700 V
1	0	1	0	1	1.150 V	0	0	1	0	1	1.750 V
1	0	1	0	0	1.175 V	0	0	1	0	0	1.800 V
1	0	0	1	1	1.200 V	0	0	0	1	1	1.850 V
1	0	0	1	0	1.225 V	0	0	0	1	0	1.900 V
1	0	0	0	1	1.250 V	0	0	0	0	1	1.950 V
1	0	0	0	0	1.275 V	0	0	0	0	0	2.000 V

Note:

1. The 1.250- and 0.900-V options may be selected by configuring the MAX1813 to 50-mV step mode (remove resistor R___) and setting the code to 01010 or 10011, respectively. Refer to the MAX1813 datasheet for other codes when in this mode.

The processor core power flows through a Maxim (MAX4372FEUK) current-measuring device. This analog measurement circuit outputs a voltage corresponding to the current demand of the processor, measured across a low-ohm resistor. The analog signal is conditioned and measured with an I2C-based

ADC (Maxim MAX1037EKAT, channel 0). The resulting measurement is compared to a 2.048-V reference, and produces a value from 0 to 2048, corresponding to the current shown in Table 4-11.

Table 4-11. CDC ADC Current Measurement Conversion Table

CPU Current	I-to-V Output	Conditioned ADC Input	ADC Measurement
0.0 A	0.00 V	0.0 V	0
1.0 A	0.25 V	0.1 V	100
...			
10.0 A	2.50 V	1.0 V	1000
...			
15.0 A	3.75 V	1.5 V	1500
...			
20.0 A	5.00 V	2.0 V	2000

Since the ADC uses an external reference derived from the same power plane as the measured V_{DD} power controller, resulting in some inaccuracy. Software can calibrate the ADC periodically to remove the error.

4.14.2 DDR VREF/Vt Power

The DDR memory reference (MVREF) and termination power is supplied (by an LP2995) 1.5-A steady-state, and up to 3.0-A transient.

4.15 Diagnostic Features

Due to space limitations, the CDC is generally restricted in how much debugger support can be provided. Where possible, debug support was deferred to external devices, such as JTAG emulation, DDR module adapters, etc. However, a certain minimal amount of debug support is included on the CDC to support initialization, and to avoid routing signals to the carrier for debug purposes.

4.15.1 Logic Analyzer Header

The majority of the debug facilities are located on the carrier board (local bus, etc.), and some are debugged through adapter modules (DDR DIMM adapter). The few signals debugged on the daughtercard are listed in Table 4-12.

Table 4-12. CDS Daughtercard P6860 Analyzer Header Definition

Pin	Signal	Description
A1	MSRCID[0]	
A3	MSRCID[1]	
A4	MSRCID[2]	
A6	MSRCID[3]	

Table 4-12. CDS Daughtercard P6860 Analyzer Header Definition (continued)

Pin	Signal	Description
A7	MSRCID[4]	
A9	MDVAL	
A10	TRIG_OUT	
A12	TRIG_IN	
A13	CLK_OUT	
A15	$\overline{\text{HRESET}}$	
B1	MDBG(0)	
B3	MDBG(1)	
B4	MDBG(2)	
B6	MDBG(3)	
B7	MDBG(4)	
B9	MDBG(5)	
B10	MDBG(6)	
B12	MDBG(7)	

4.15.2 JTAG Header

This 2x10-pin Berg header is typically used with JTAG/ICE controllers to download target code and control code execution from a remote computer. The pinout is shown in Table 4-13.

Table 4-13. CDS JTAG Header

Pin	Signal	Definition
1	TDO	CPU JTAG TDO output
2	n/c	Pulled up to OVDD
3	TDI	CPU JTAG TDI input
4	$\overline{\text{TRST}}$	CPU JTAG $\overline{\text{TRST}}$ input
5	N/C	Pulled up to OVDD
6	VDD	+3.3 V power
7	TCK	CPU JTAG TCK input
8	CKSTP_I	CPU $\overline{\text{CHKSTP\_IN}}$ input
9	TMS	CPU JTAG TMS input
10	N/C	N/C
11	SRST	CPU $\overline{\text{SRESET}}$ input
12	GND	Ground (non-standard)

Table 4-13. CDS JTAG Header (continued)

Pin	Signal	Definition
13	HRST	CPU $\overline{\text{HRESET}}$ input
14	KEY	No pin present
15	CKSTP_O	CPU $\overline{\text{CHKSTP\_OUT}}$ output
16	GND	Ground

The connector is physically arranged as shown in Table 4-14. Other pin numbering schemes are popular, however, the correspondence between each pin and the 'picture' in Table 4-14 is correct, whatever the pin number may be.

Table 4-14. CDS COP Header Definition

1	2
3	4
5	6
7	8
9	10
11	12
13	14
15	16

4.15.3 LEDs

Table 4-15 describes the diagnostic LEDs on the CDC card.

Table 4-15. CDC Diagnostic LEDs

PCB Label	LED	Definition	Activation Method
VDD3	D4	+3.3-V power active	Power applied
OVDD	D2	+2.5-V power active	Power applied
VCORE	D3	VDD (Vcore) power active	Power applied
BOOT	D10	LCS0* active	Boot/read/write to local bus Flash
MEM	D9	LCS2* active	Read/write/refresh to DDR SDRAM
SLEEP	D8	CPU asleep (or PLL not locked)	ASLEEP asserted
PCI1	D6	PCI 1 bus activity	PCI1_DEVSEL# (resistively sampled near CPU)
PCI2	D5	PCI 2 bus activity	PCI2_DEVSEL# (resistively sampled near CPU)
DUAL	D1	PCI dual bus modes	Switch selected
CLOCK	D7	Clock active	SYSCLK and/or PCICLK running
RESET	D11	Reset active	HRESET asserted

4.15.4 Test Points

Test points are added to critical signals to aid in bringup and testing. The test point list is shown in Table 4-16.

Table 4-16. CDS Test Point List

Test Point	Definition
TP6	CPU Spare01
TP8	CPU Spare02
TP10	CPU Spare10
TP7	CPU Spare13
TP11	WP for I2C EEPROM
U7	Spare analog ADC input
U2	Spare left connector
TP1	Spare left connector
U30	Spare right connector
U31	Spare right connector

Chapter 5
Arcadia Motherboard Architecture

The following sections describe information on the Arcadia Version 3 reference platform, also referred to as Arcadia x3 or Arcadia V3. Arcadia is a flexible evaluation and development platform support, and serves several support purposes:

- As a backplane for evaluation of CDS-based boards (PowerQUICC III network host processors)
- As a backplane for high-speed communications protocols (RapidIO, PCI Express, and others) between hardware interoperability platform (HIP) compliant boards.
- Arcadia contains a pair of HIP-compliant slots, four PCI/PCI-X slots, one PrPMC connector, and sufficient system resources (clock, power, arbitration, IDE disk access, PS/2 ports) to allow the system to boot an operating system (Linux).

5.1 Features

The Arcadia development platform supports many combinations of HIP cards, PrPMC modules (including MPMC cards), and PCI/PCI-X cards (hereafter, PCI-X will be used unless PCI is specifically referred to).

Accordingly, Arcadia includes the following features:

- Two RapidIO HIP slots
  - 40 differential pairs
  - Protocol-free
  - Unlimited speed
- Six PCI slots
  - Four 3 3-V PCI-X slots and PCI bridge at 66-MHz speeds (all 32- or 64-bit)
  - Two 5-V, 32-bit PCI slots at 33-MHz speeds
- PrPMC connector
  - 33-MHz bus speeds
  - 5-V interfaces
  - PrPMC/MPMC compatible
- PCI-X/PCI bridge
  - 66-MHz PCI-X to 33-MHz PCI bridge
  - Allows fast PCI/PCI-X traffic without being limited by VIA PIPC
- PCI integrated peripheral controller (PIPC)
  - Dual UDMA100 IDE disk controller
  - Dual USB interface

  - Floppy disk controller
  - Dual serial ports
- ATX motherboard form-factor

Figure 5-1 shows a block diagram of the Arcadia motherboard.

5.2 Configurations

Arcadia's flexible, non-specific motherboard allows it to be used for several purposes, such as:

- CDS motherboard for CDS development purposes
- HIP-compatible parallel/serial RapidIO motherboard

With the on-board VIA PIPC and Ethernet, operating systems such as Linux, QNX, VxWorks, ENEA/OSE, and others can be easily ported. The use of industry-standard components means that porting existing Sandpoint BSP and application code should be relatively easy, though it is not code compatible.

5.2.1 CDS Motherboard

As a CDS motherboard, Arcadia also supports the use of CDS development/evaluation boards, such as the CDS for the MPC8555E, MPC8541E, MPC8548E, the PowerQUICC III family, and others; PMC cards such as the MPC7447-Valis, MPC7410-Altimus, MPC8245-Unity, and other network/control processor cards; and HIP boards such as the Freescale MARS:Elysium, the Freescale MARS:Auxo, and the Tundra TSI500 evaluation boards, as well as any other HIP-compatible boards.

Figure 5-1 shows an example usage in this mode.

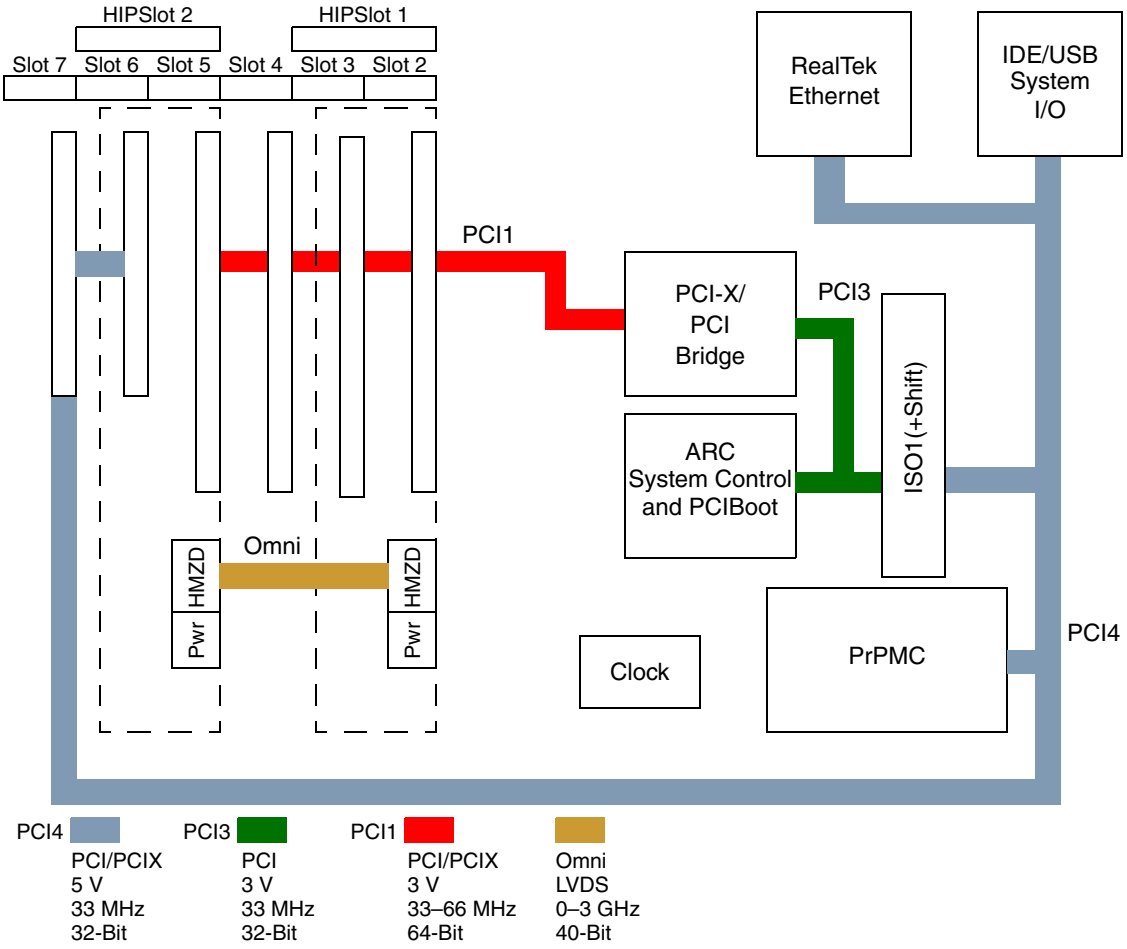


Figure 5-1. CDS-Compatible Arcadia Block Diagram

In general, the CDS view of the system exposes all the hardware resource features.

5.3 Architecture

The following sections cover the Arcadia design in more detail. The general features of Arcadia are summarized in Table 5-1.

Table 5-1. Arcadia Architecture Feature Summary

Bus	Connections	Size	Theoretical Maximum Speed	Description	Notes
Omni	HIPSlot #1 HIPSlot #2	40 differential pairs	3.2 GHz	8-bit parallel RapidIO 16-bit parallel RapidIO 1x serial RapidIO 4x serial RapidIO PCI Express	1
PCI 3/ PCI 4	PrPMC Slot #6 Slot #7 PCI bridge secondary VIA PIPC Ethernet	32-bit	33 MHz	PCI/PCI-X data bus	
PCI 1	Slot #2 Slot #3 Slot #4 Slot #5 PCI bridge primary System Control	64-bit	33–66 MHz	PCI/PCI-X data bus	2
Clocks	PrPMC and PCI	1-bit	33 MHz	Reference clock	
Interrupts	PrPMC and PCI	4-bit	N/A	Interrupt bus	
Reset	PrPMC and PCI	1-bit	N/A	PCI reset signal	
Power	HIP, PCI, and PrPMC	N/A	N/A	Card power	

Notes:

1. The maximum speed of the Omni port is limited only by the rates of the HIP cards used, and by skew and cross-talk issues on the Arcadia connector traces (if any).
2. Non-MPMC cards, such as VITA PrPMC cards, are not supported.

5.4 Omni Bus

The Arcadia platform supports a protocol-independent connection called the Omni bus. The Omni bus is a set of 40 pairs of LVDS signals, grouped into a set of unidirectional transmit and receive sets (20 pair). As long as two cards can transmit all signals on the transmit pairs, and receive correspondingly on the receive pairs, they can communicate using any protocol that will fit.

This is also the case if both the boards agree that certain signals are:

- Inputs only
- Bidirectional but open-drain driven (for example, interrupts)

Figure 5-2 shows an example of the cross-over connection that allows the two slots to communicate without the requirement of an intermediary interface (which would restrict the connection to only one type of protocol).

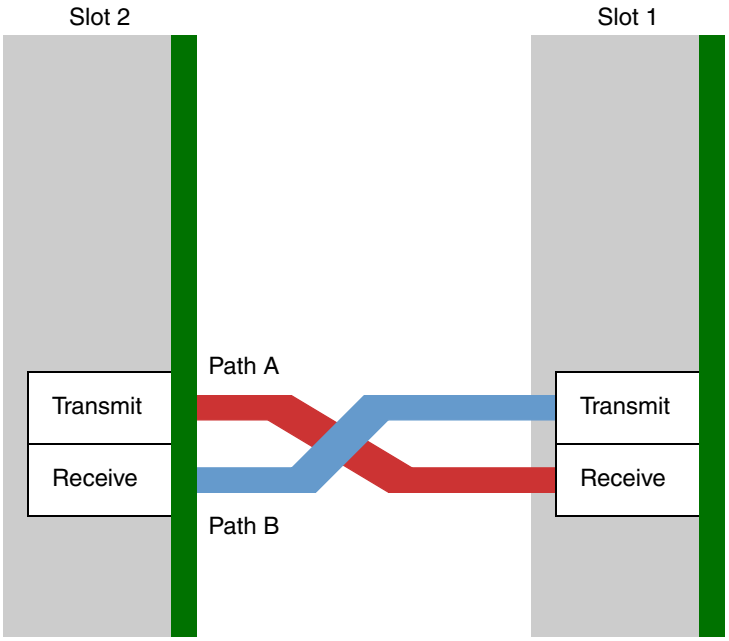


Figure 5-2. Arcadia RapidIO Port Connections

5.4.1 Parallel RapidIO

Table 5-2 describes the pinout of the high-speed port connector, when the parallel RapidIO protocol is in use. This pinout is as defined by the RapidIO Trade Association TWG document, *RapidIO Hardware Interoperability Platform (HIP) Specification*.

Table 5-2. Arcadia Parallel RapidIO Connector Definition

Pin	Definition	Pin	Definition	Pin	Definition	Pin	Definition
A1, B1	RD0, $\overline{\text{RD0}}$	C1, D1	RD8, $\overline{\text{RD8}}$	E1, F1	$\overline{\text{TFRM1}}$, TFRM1	G1, H1	$\overline{\text{TFRM}}$, TFRM
A2, B2	RD1, $\overline{\text{RD1}}$	C2, D2	RD9, $\overline{\text{RD9}}$	E2, F2	$\overline{\text{TD15}}$, TD15	G2, H2	$\overline{\text{TD7}}$, TD7
A3, B3	RD2, $\overline{\text{RD2}}$	C3, D3	RD10, $\overline{\text{RD10}}$	E3, F3	$\overline{\text{TD14}}$, TD14	G3, H3	$\overline{\text{TD6}}$, TD6
A4, B4	RD3, $\overline{\text{RD3}}$	C4, D4	RD11, $\overline{\text{RD11}}$	E4, F4	$\overline{\text{TD13}}$, TD13	G4, H4	$\overline{\text{TD5}}$, TD5
A5, B5	RCLK0, $\overline{\text{RCLK0}}$	C5, D5	RCLK1, $\overline{\text{RCLK1}}$	E5, F5	$\overline{\text{TD12}}$, TD12	G5, H5	$\overline{\text{TD4}}$, TD4
A6, B6	RD4, $\overline{\text{RD4}}$	C6, D6	RD12, $\overline{\text{RD12}}$	E6, F6	$\overline{\text{TCK1}}$, TCK1	G6, H6	$\overline{\text{TCK0}}$, TCK0
A7, B7	RD5, $\overline{\text{RD5}}$	C7, D7	RD13, $\overline{\text{RD13}}$	E7, F7	$\overline{\text{TD11}}$, TD11	G7, H7	$\overline{\text{TD3}}$, TD3
A8, B8	RD6, $\overline{\text{RD6}}$	C8, D8	RD14, $\overline{\text{RD14}}$	E8, F8	$\overline{\text{TD10}}$, TD10	G8, H8	$\overline{\text{TD2}}$, TD2
A9, B9	RD7, $\overline{\text{RD7}}$	C9, D9	RD15, $\overline{\text{RD15}}$	E9, F9	$\overline{\text{TD9}}$, TD9	G9, H9	$\overline{\text{TD1}}$, TD1
A10, B10	RFRM, $\overline{\text{RFRM}}$	C10, D10	RFRM1, $\overline{\text{RFRM1}}$	E10, F10	$\overline{\text{TD8}}$, TD8	G10, H10	$\overline{\text{TD0}}$, TD0

Note:
1. BG(1:10), DG(1:10), FG(1:10), and HG(1:10) are all connected to system ground.

5.4.2 Serial RapidIO

Table 5-3 describes the pinout of the high-speed port connector, when the parallel RapidIO protocol is in use. This pinout is as defined by the RapidIO Trade Association TWG document, *RapidIO Hardware Interoperability Platform (HIP) Specification*.

Table 5-3. Arcadia Serial RapidIO Connector Definition

Pin	Definition	Pin	Definition	Pin	Definition	Pin	Definition
A1, B1	R1D1, $\overline{\text{R1D1}}$	C1, D1	R3D1, $\overline{\text{R3D1}}$	E1, F1		G1, H1	
A2, B2		C2, D2		E2, F2		G2, H2	
A3, B3		C3, D3		E3, F3		G3, H3	
A4, B4		C4, D4		E4, F4		G4, H4	
A5, B5		C5, D5		E5, F5	$\overline{\text{T4D1}}$, T4D1	G5, H5	$\overline{\text{T2D1}}$, T2D1
A6, B6	R2D1, $\overline{\text{R2D1}}$	C6, D6	R4D1, $\overline{\text{R4D1}}$	E6, F6		G6, H6	
A7, B7		C7, D7		E7, F7		G7, H7	
A8, B8		C8, D8		E8, F8		G8, H8	
A9, B9		C9, D9		E9, F9		G9, H9	
A10, B10		C10, D10		E10, F10	$\overline{\text{T3D1}}$, T3D1	G10, H10	$\overline{\text{T1D1}}$, T1D1

Notes:
1. BG(1:10), DG(1:10), FG(1:10), and HG(1:10) are all connected to system ground.
2. Blank cells are no connect.

5.4.3 PCI Express

Table 5-4 describes the pinout of the high-speed port connector when the PCI Express protocol is used.

NOTE

This is not a standard currently supported on HIP platforms and careful interoperability setup is required.

Table 5-4. Arcadia PCIExpress Connector Definition

Pin	Definition	Pin	Definition	Pin	Definition	Pin	Definition
A1, B1	rx0 (p,n)	C1, D1	rx8 (p,n)	E1, F1		G1, H1	
A2, B2	rx1 (p,n)	C2, D2	rx9 (p,n)	E2, F2	tx15 (n,p)	G2, H2	tx7 (n,p)
A3, B3	rx2 (p,n)	C3, D3	rx10 (p,n)	E3, F3	tx14 (n,p)	G3, H3	tx6 (n,p)
A4, B4	rx3 (p,n)	C4, D4	rx11 (p,n)	E4, F4	tx13 (n,p)	G4, H4	tx5 (n,p)
A5, B5	CLK125, n/a	C5, D5		E5, F5	tx12 (n,p)	G5, H5	tx4 (n,p)
A6, B6	rx4 (p,n)	C6, D6	rx12 (p,n)	E6, F6		G6, H6	
A7, B7	rx5 (p,n)	C7, D7	rx13 (p,n)	E7, F7	tx11 (n,p)	G7, H7	tx3 (n,p)

Table 5-4. Arcadia PCIExpress Connector Definition (continued)

Pin	Definition	Pin	Definition	Pin	Definition	Pin	Definition
A8, B8	rx6 (p,n)	C8, D8	rx14 (p,n)	E8, F8	tx10 (n,p)	G8, H8	tx2 (n,p)
A9, B9	rx7 (p,n)	C9, D9	rx15 (p,n)	E9, F9	tx9 (n,p)	G9, H9	tx1 (n,p)
A10, B10	RST#, n/a	C10, D10		E10, F10	tx8 (n,p)	G10, H10	tx0 (n,p)

Notes:
1. BG(1:10), DG(1:10), FG(1:10), and HG(1:10) are all connected to system ground.
2. The notation (p,n) refers to positive and negative halves of the differential pair, and are assigned to the respective pin. The notation (n,p) is the same, but reversed.
3. Blank cells are no connect.

5.5 PCI/PCI-X Bus

The Arcadia platform contains two independent PCI buses: a low-speed legacy PCI bus (the secondary PCI bus) and a high-speed PCI/PCI-X bus (the primary PCI bus). The Tundra TSI310 PCI-to-PCI bridge spans these two buses.

All cards and devices on the secondary PCI bus operates in PCI mode (no PCI-X) and at 33 MHz only (if this is a 5-V bus); 66 MHz can be supplied, but this is not in compliance with the PCI specifications. Slots 6 and 7, the PIPC (PCI I/O), and Ethernet interfaces are present on this bus.

The primary bus supports operation at 33 and 66 MHz, using bus mode and speed detection to select the appropriate speed.

Because of the numerous PCI buses and bus-fragments, the following nomenclature is used when referring to specific portions of the PCI bus:

PCI <Bus> <Fragment> '_' PCI_Signal

where:

<Bus> 'A' for the high-speed primary bus, or
'B' for the slower secondary bus.

<Fragment> '1' for primary bus
'4' for the PrPMC part of the secondary bus, or
'3' for the 3-V isolated part of the secondary bus.

Thus, a signal such as $\overline{\text{PCIA3\_FRAME}}$ refers to the conventional PCI $\overline{\text{FRAME}}$ signal that is routed between the ISO 3 buffer and slots 4 and 5. This notation is also used on the schematics.

Table 5-5 describes the pinout of the high-speed port connector when the PCI Express protocol is used.

NOTE

This is not currently a standard supported on HIP platforms and so implies that careful interoperability setup is required.

Table 5-5. Arcadia PCIBus Name Examples

PCI Signal	Connects to
$\overline{\text{PCIA\_FRAME}}$ or $\overline{\text{PCIA1\_FRAME}}$	PCIBridge primary side, HIPSlot 1 (PCI Slot 2), PCI Slot 4, HIPSlot 1 (PCI Slot 5)
$\overline{\text{PCIB3\_FRAME}}$	PCIBridge secondary side, ARC PCI interface, PCI B isolation buffer 3
PCIB4	PCI B isolation buffer 4, Ethernet VIA PIPC PrPMC PCI Slot 6 PCI Slot 7

5.5.1 PCI Arbitration

The Arcadia contains two separate PCI buses (separated by the PCI bridge). Figure 5-3 shows a block diagram of the PCI arbitration domains.

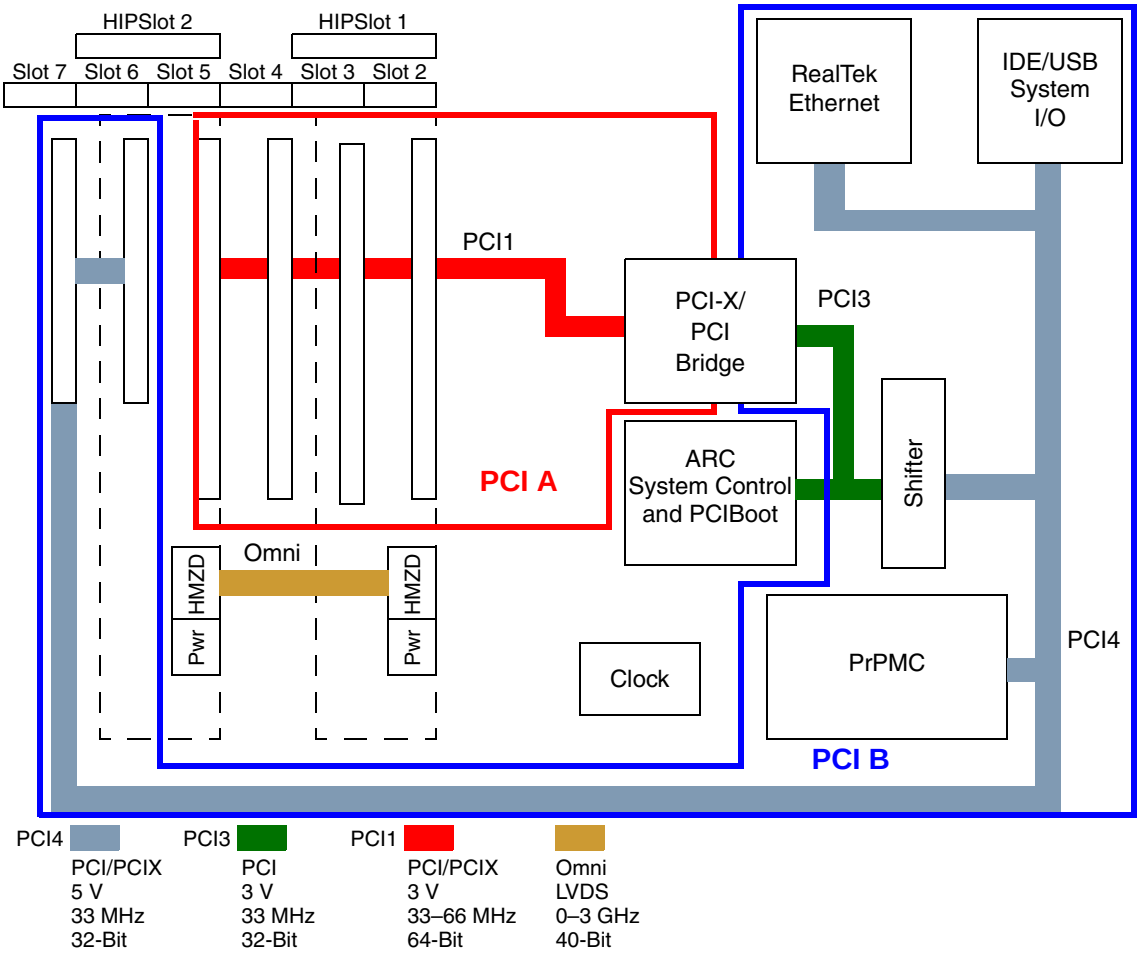


Figure 5-3. Arcadia PCI Arbitration Domains

For PCI A, the PCI/PCI-X high-speed bus, the arbitration is handled by the system control logic which provides transparent, high-speed access. For PCI B, the slow-speed bus, arbitration is handled by the Tundra TSI310.

Table 5-6. PCI Arbitration Ports

Component	Bus	Arbiter	Port	Notes
PrPMC	B4	PCIB4_REQ/GNT*(1:5)	4	
Secondary PCI Bridge	B3	PCIB3_REQ/GNT*(1:5)	N/A	Internally port 0
ARC	B3	N/A	N/A	Non-bus-master
RTK8139 Ethernet	B4	PCIB4_REQ/GNT*(1:5)	2	
VIA 82C686B	B4	PCIB4_REQ/GNT*(1:5)	3	
Slot 6	B4	PCIB4_REQ/GNT*(1:5)	1	
Slot 7	B4	PCIB4_REQ/GNT*(1:5)	5	

Table 5-6. PCI Arbitration Ports (continued)

Component	Bus	Arbiter	Port	Notes
Primary PCI Bridge	A	PCIA_REQ/GNT*(0:4)	0	
Slot 2	A		1	
Slot 3	A		2	
Slot 4	A		3	
Slot 5	A		4	

5.5.2 PCI Host Mode

As with all HIP systems, all components on the board are peers. That is, any one (or multiple) HIP and/or PrPMC cards can service interrupt requests. This is essential, as in some configurations, a HIP card or a PrPMC card may not be present.

To accommodate this maximum flexibility, Arcadia does not enforce which slot/device will serve as host. Configuration and design ensure that each device is capable of servicing an interrupt from any location.

NOTE

Despite common belief, the concept of host is not inextricably tied to being the arbiter. The arbiter can be, and indeed is, located on a central resource (the system logic) completely independent of whatever card is designated as the host.

Only one device on each PCI domain is allowed to perform configuration cycles. This is enforced by software and/or hardware slot detection.

5.5.3 PCI Bridge

The PCI/PCIX slots are isolated from the PIPC, PrPMC, and Ethernet by the Tundra TSI310 PCI-to-PCI bridge. The primary (PCI-X) interface runs at up to 66 MHz, while the secondary is limited to 33 MHz to match the capabilities of the VIA PIPC.

5.5.4 PCI Interrupts

Arcadia has several interrupt sources, including:

- Four PCI slot interrupts (shared among six slots). Four slots on primary bus and two slots on the secondary bus.
- Ethernet interrupt
- VIA southbridge interrupt (USB and IDE)
- PrPMC interrupts

Figure 5-4 shows a block diagram of the PCI interrupt flow.

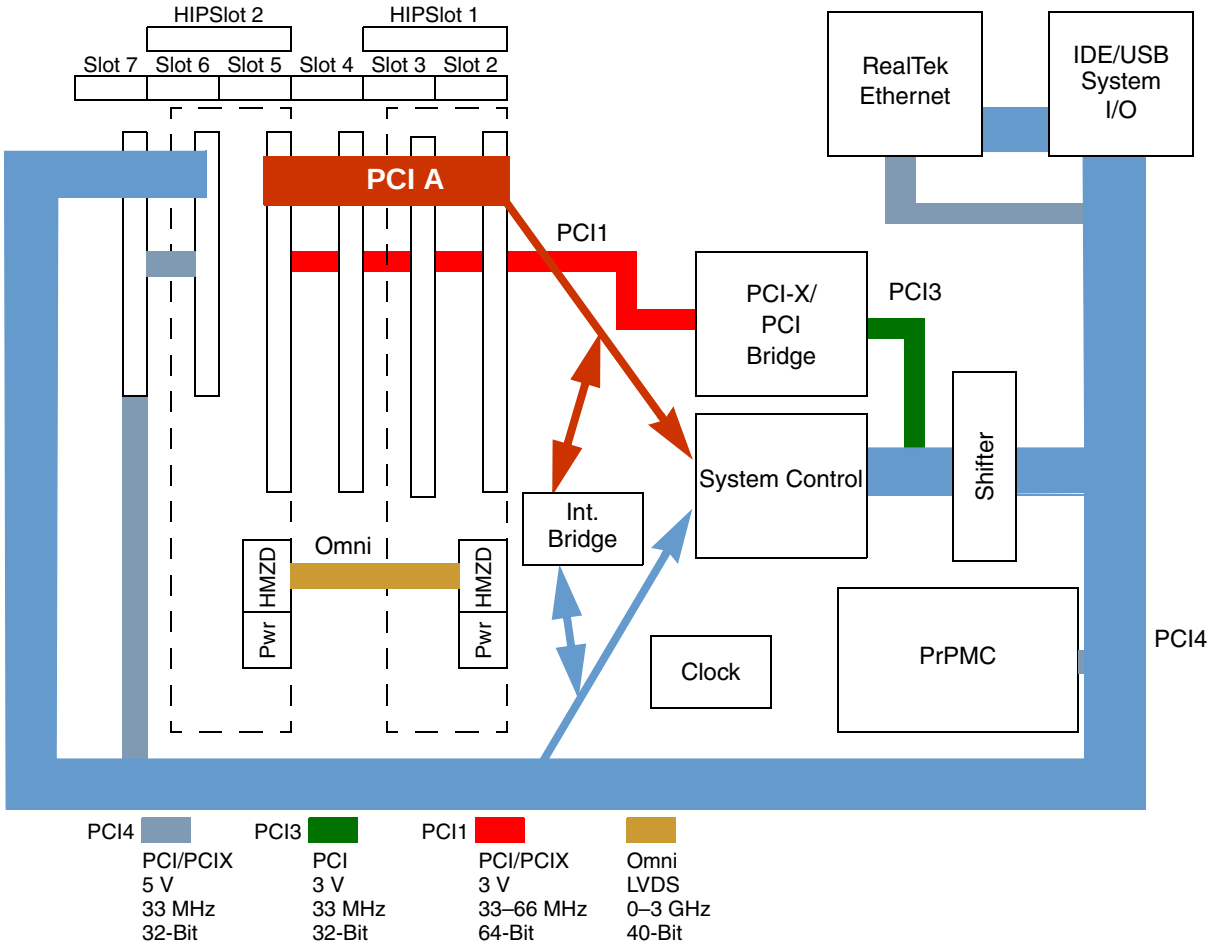


Figure 5-4. Arcadia PCI Interrupts Domains

To allow the PrPMC to service interrupts from PCI1, or HIP cards to service interrupts from the PrPMC, Southbridge, or Ethernet, the system logic contains interrupt steering logic to allow interrupts to be replicated in one direction or the other (depending on where the host is placed).

NOTE

As the PMC slot is typically occupied by a control-plane Freescale PrPMC, the standard software from Freescale and many legacy board support packages reflect this viewpoint in software initialization sequences. For a shared co-processing environment, a more complicated interrupt allocation software will be required.

The slot interrupts are assigned in a conventional rotating pattern, where the $\overline{\text{INTA}}$ output of each card is assigned to successive portions of the common $\overline{\text{INT}}$(0:3) bus, respectively.

Table 5-7. Arcadia 3.1 Interrupt Assignments

Device	PCI INT Pin	CDS Interrupt Bus	Attached Devices by Connection	Notes
Slot #2	INTA#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	2
	INTB#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	
	INTC#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	
	INTD#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	
Slot #3	INTA#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	2
	INTB#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	
	INTC#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	
	INTD#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	
Slot #4	INTA#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	2
	INTB#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	
	INTC#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	
	INTD#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	
Slot #5	INTA#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	2
	INTB#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	
	INTC#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	
	INTD#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	
PrPMC	INTA#	$\overline{\text{PCIB4\_INT0}}$	PrPMC_INTA# | VIA_INTA# | ARC_INTA# | Slot6 INTC# | Slot7 INTB#	
	INTB#	$\overline{\text{PCIB4\_INT1}}$	PrPMC_INTB# | VIA_INTB# | ARC_INTB# | Slot6 INTD# | Slot7 INTC#	
	INTC#	$\overline{\text{PCIB4\_INT2}}$	PrPMC_INTC# | VIA_INTC# | | Slot6 INTA# | Slot7 INTD#	
	INTD#	$\overline{\text{PCIB4\_INT3}}$	PrPMC_INTD# | VIA_INTD# | | Slot6 INTB# | Slot7 INTA#	
VIA VIA	INTA#	$\overline{\text{PCIB4\_INT0}}$	PrPMC_INTA# | VIA_INTA# | ARC_INTA# | Slot6 INTC# | Slot7 INTB#	
	INTB#	$\overline{\text{PCIB4\_INT1}}$	PrPMC_INTB# | VIA_INTB# | ARC_INTB# | Slot6 INTD# | Slot7 INTC#	
	INTC#	$\overline{\text{PCIB4\_INT2}}$	PrPMC_INTC# | VIA_INTC# | | Slot6 INTA# | Slot7 INTD#	
	INTD#	$\overline{\text{PCIB4\_INT3}}$	PrPMC_INTD# | VIA_INTD# | | Slot6 INTB# | Slot7 INTA#	
	SIOINT	$\overline{\text{PCIB4\_INT0}}$ $\overline{\text{PCIB4\_INT1}}$	PrPMC_INTA# | VIA_INTA# | ARC_INTA# | Slot6 INTC# | Slot7 INTB#	1
Ethernet	INTA#	$\overline{\text{PCIB4\_INT1}}$	PrPMC_INTB# | VIA_INTB# | ARC_INTB# | Slot6 INTD# | Slot7 INTC#	
Slot #6	INTA#	$\overline{\text{PCIB4\_INT2}}$	PrPMC_INTC# | VIA_INTC# | | Slot6 INTA# | Slot7 INTD#	
	INTB#	$\overline{\text{PCIB4\_INT3}}$	PrPMC_INTD# | VIA_INTD# | | Slot6 INTB# | Slot7 INTA#	
	INTC#	$\overline{\text{PCIB4\_INT0}}$	PrPMC_INTA# | VIA_INTA# | ARC_INTA# | Slot6 INTC# | Slot7 INTB#	
	INTD#	$\overline{\text{PCIB4\_INT1}}$	PrPMC_INTB# | VIA_INTB# | ARC_INTB# | Slot6 INTD# | Slot7 INTC#	

Table 5-7. Arcadia 3.1 Interrupt Assignments (continued)

Device	PCI INT Pin	CDS Interrupt Bus	Attached Devices by Connection	Notes
Slot #7	INTA#	$\overline{\text{PCIB4\_INT3}}$	PrPMC_INTD# | VIA_INTD# | | Slot6 INTB# | Slot7 INTA#	
	INTB#	$\overline{\text{PCIB4\_INT0}}$	PrPMC_INTA# | VIA_INTA# | ARC_INTA# | Slot6 INTC# | Slot7 INTB#	
	INTC#	$\overline{\text{PCIB4\_INT1}}$	PrPMC_INTB# | VIA_INTB# | ARC_INTB# | Slot6 INTD# | Slot7 INTC#	
	INTD#	$\overline{\text{PCIB4\_INT2}}$	PrPMC_INTC# | VIA_INTC# | | Slot6 INTA# | Slot7 INTD#	
ARC	INTA#	$\overline{\text{PCIB3\_INT0}}$	PrPMC_INTA# | VIA_INTA# | ARC_INTA# | Slot6 INTA# | Slot7 INTB#	1
	INTB#	$\overline{\text{PCIB3\_INT1}}$	PrPMC_INTB# | VIA_INTB# | ARC_INTB# | Slot6 INTD# | Slot7 INTC#	

Notes:
1. Note that the SIOINT signal from the VIA is converted to PCI levels and shared with other PCI devices onto PCIB3_INT bus signal 0 or 1 (software selectable).
2. Note that slots 2, 4, and 5 (the HIP/CDS slots) have paralleling interrupts in order to allow easier peer-interrupt management (i.e., the CDS cards do not need to know what slot it is in to source interrupt assignments).

NOTE

As the VIA PIPC is located behind a PCI-to-PCI bridge, interrupt acknowledge cycles cannot be used (such cycles are not forwarded across a bridge). Interrupt servicing routines for the VIA must identify interrupting resources (the 8259 core in the VIA) directly.

5.5.5 PCI Interrupt Bridge

Arcadia includes an optional switch to connect/disconnect the PCI domain interrupt pins. Connecting them via the PCI_INT_BRIDGE* switch (see Section 5.11, “Configuration”) allows interrupts to be asserted and handled on either side. Opening the bridge maintains each domain as a separate (independent) entity.

NOTE

Per the PCI bridge specification, PCI bridges such as the Tsi310 do not forward interrupt acknowledge cycles. Thus, interrupt handlers attempting to span the bridge will need to poll and/or handle interrupt clearing via software.

5.5.6 PCI Configuration

Each PCI device accessible as a target has an associated bus and device number. PCI device numbers are not globally unique, and must include the bus number. Bus 1 is the main PCI/PCI-X bus (primary), while bus 2 is the secondary, 33-MHz (nominal) PCI bus.

Although the PCI-to-PCI bridge is nominally transparent, allowing data to flow in either direction, PCI configuration cycles are one exception: only the primary PCI bus interface of the bridge converts type1 configuration cycles to type0 configuration cycles. Consequently, the high-speed PCI-X bridge (connected to the HIP/CDS slots) is the PCI bridge primary connection, allowing those cards to configure the

secondary devices if needed. Devices on the secondary interface cannot configure anything on slots 2, 3, 4, and 5.

Table 5-8. PCI Configuration Addresses

Component	Bus	Schematic Device Number	Notes
PrPMC IDSEL #1	B4	16	1
Secondary PCI bridge	B3	17	2
ARC	B3	18	
RTK8139 Ethernet	B4	21	
VIA 82C686B	B4	20	
Slot 6	B4	22	
Slot 7	B4	23	
Primary PCI bridge	A	28	
Slot 2	A	20	
Slot 3	A	21	
Slot 4	A	22	
Slot 5	A	24	

Notes:

1. IDSEL for PCI interface provided for PCI test card probing only; performing PCI configuration cycles to self may or may not be valid.
2. A configuration option; normally IDSEL is disabled on the secondary PCI bridge.

5.5.7 PrPMC Connector

The Arcadia platform contains connectors for the direct attachment of any of the Freescale PrPMC processor mezzanine cards. These cards are available with a broad spectrum of embedded processors, from the MPC603e-based, to the MPC7448-based.

The PrPMC connectors are compliant with PCI 2.3 standards. Standard 5-V PMC I/O cards such as Ethernet cards, video cards, etc., are, therefore, usable in this slot. The 5-V bus interfacing allows direct installation of existing PrPMC cards.

5.6 System Control

The Arcadia contains a second FPGA called ARC, which implements the following functions:

- Reset controller
- PCI1 bus arbitration

- VIA SIOINT to PCIB interrupt mapping
- PCIA speed detection and control
- Optional: PCI boot for PrPMCs

5.7 Clocking

Arcadia provides clocks to the PCI/PCI-X slots and devices (both buses), the AGP slot, the PrPMC connector, the arbiter/system logic, and the PCI bridge. With multiple PCI domains, each domain may operate at a different frequency than the others, as shown in Figure 5-5.

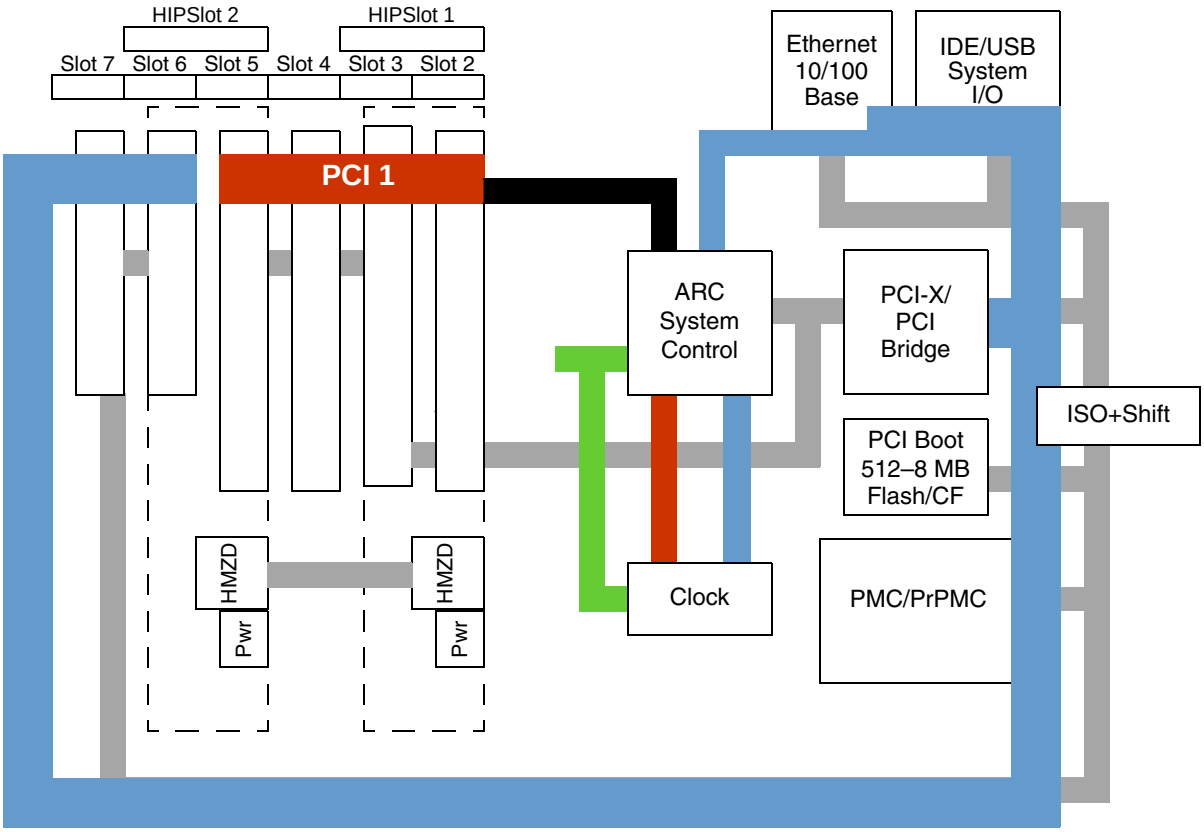


Figure 5-5. Arcadia PCI Clock Domains

The VIA PIPC is fixed at a 33-MHz frequency, so the ‘standard’ speed of the secondary PCI bus is also 33 MHz and, therefore, is the secondary interface of the PCI bridge. The PCI bridge accepts asynchronous primary and secondary clocks, so the bridge and the PIPC devices are clocked with a simple, fixed 33-MHz clock buffer.

Table 5-9. PCI Clock Domain Summary

PCI Domain	PCI Group	Device	PCI Clock	PCI Speed Range	Speed Detection	Notes
PCI A	1	PCI bridge	PCIA_CLK(0)	33–66	PCIA_M66E, PCIA_PCIXCAP, PCIA_SPEED(0:1)	
		Slot 2/HIP 1	PCIA_CLK(1)	33–66		
		ARC	PCIA_CLK(2)	33–66		2
		Slot 3	PCIA_CLK(5)	33–66		
		Slot 4	PCIA_CLK(3)	33–66		
		Slot 5/HIP 2	PCIA_CLK(4)	33–66		
PCI B	3	PCI bridge	PCIB_CLK(0)	33	N/A	1
		ARC	PCIB_CLK(1)			
	4	Ethernet	PCIB_CLK(2)			
		VIA PIPC	PCIB_CLK(3)			
		PrPMC	PCIB_CLK(4)			
		Slot 6	PCIB_CLK(5)			
		Slot 7	PCIB_CLK(6)			

Notes:
1. PCI B is fixed at 33 MHz.
2. Used to clock the primary arbiter.

The primary PCI clock varies depending on the devices installed in the PCI slots. The M66EN signal is used to select 33 or 66 MHz, while PCIXCAP is used to select between PCI and PCI-X mode, as well as for 66-MHz operation.

Configuration switches select the frequency used for the high-speed PCI clock rate. Since Arcadia lacks intelligent PCI configuration, and is not anticipated to readily support PCI-X at 133 MHz due to the number of PCI slots needed, no automatic high-speed PCI-X clock configuration is supported. Arcadia is only guaranteed to work at 66 MHz PCI/PCI-X rates; all other settings are experimental.

Lastly, the entire clock system can be switched to an external clock source for complete control over the PCICLK signals sent to cards. The overall clock architecture is shown in Figure 5-6.

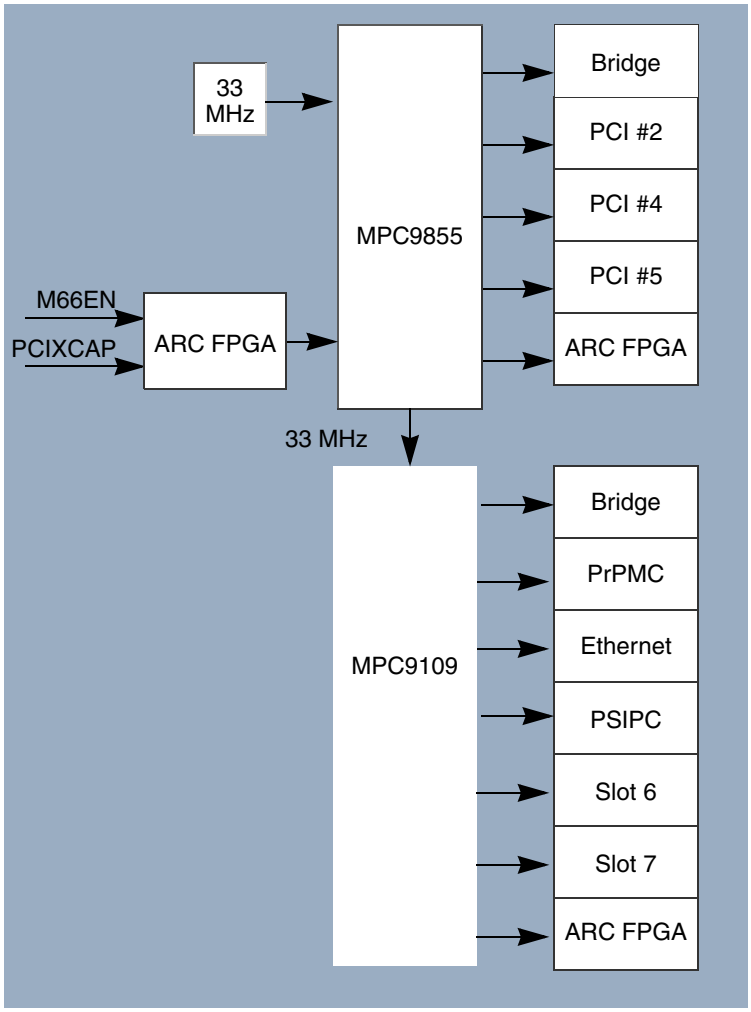


Figure 5-6. Arcadia Clock Architecture

Arcadia uses the MPC9855 clock synthesizer to generate 33/66 MHz primary PCI clock rates; 33 MHz secondary PCI clocks are generated by a buffered version of the clock input.

Note that HIP cards provide their own, locally-generated clocks for the RapidIO bus, and may or may not elect to make any use of the PCI clock signal.

5.8 Reset

The reset architecture of Arcadia is fairly straightforward. PCI cards are reset from the $\overline{\text{PCIRST}}$ signal, generated by the ATX power supply, or chassis/motherboard pushbutton switches. The general reset architecture is shown in Figure 5-7.

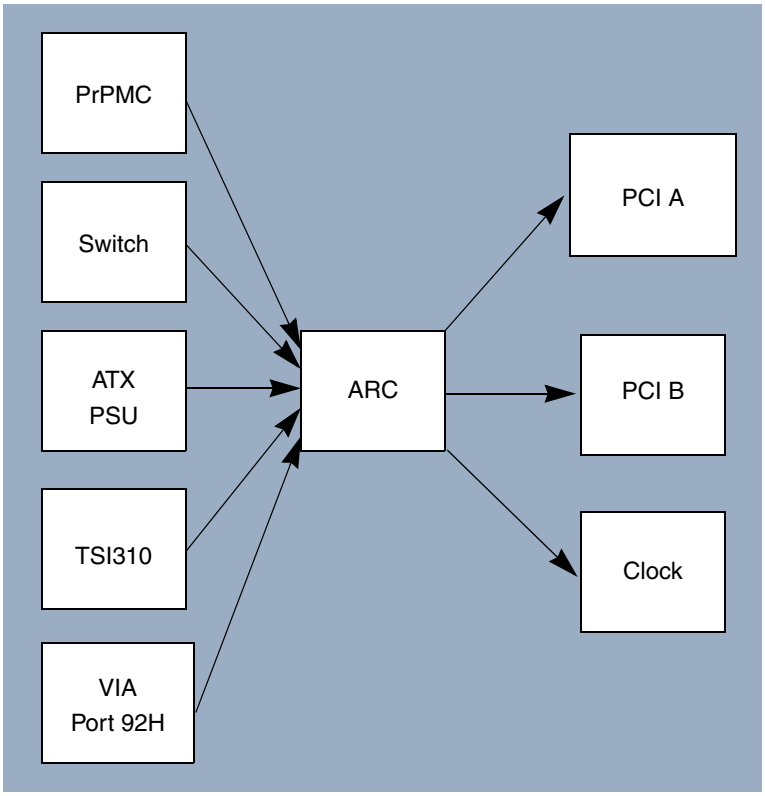


Figure 5-7. Arcadia Reset Architecture

In operation, the assertion of any the reset pushbutton switches, the power supply, or a signal from the MPMC card may initiate a system reset and cause the reset controller to drive the global reset signals low.

Note that, as PCI is optional, the HIP cards do not have a reset definition. non-PCI RapidIO cards typically use one of the following resources:

- Local reset controller (based on RapidIO power supply or local switch)
- $\overline{\text{PCIRST}}$ (even if PCI not supported, $\overline{\text{PCIRST}}$ signal may be referenced)
- RapidIO maintenance packets (software-based reset)

Since PCI is not a required feature of the RapidIO HIP platform, HIP cards should generally not rely on the $\overline{\text{PCIRST}}$ signal being available. To ease the implementation of $\overline{\text{PCIRST}}$, Arcadia includes strong drivers for the $\overline{\text{PCIRST}}$ signal, to allow HIP cards to place a pullup on the $\overline{\text{PCIRST}}$ signal such that the signal may be used on an HIP card and still operate in the absence of the PCI bus.

5.9 Power

HIP cards are provided with 5 and 3.3 V through the HIP power connectors; additional power may be obtained from the (optional) PCI/PCI-X connector, which also has 5, 3.3, and 12 V as required by the PCI V2.2 specification. Table 5-10 summarizes the available power to HIP cards.

Table 5-10. Arcadia **Slot Power Availability**

Power	Source	Current	Power
5 V	HIP	2 × 7.8 A	78 W
	PCI	5 A	25 W
	Total	20.6 A	103 W
3.3 V	HIP	2 × 7.8 A	52 W
	PCI	7.6 A	25 W
	Total	23.2 A	77 W
12 V	HIP	—	—
	PCI	0.5 A	6 W
	Total	0.5 A	6 W
–12 V	HIP	—	—
	PCI	0.1 A	1.2 W
	Total	0.1 A	1.2 W

Note that if a RapidIO HIP card requires +12 or –12 V, it will have to tap into the PCI slot or synthesize its own power using an energy conversion device. As PCI is a non-required feature of the RapidIO HIP platform, the latter is recommended.

All power is provided by the external ATX/ATX-12 V power supply, except for +2.5 V which is locally created.

5.10 Diagnostic Features

The Arcadia motherboard contains few diagnostic and debug features. PCI debug is easily facilitated through the PCI and PMC connectors, and RapidIO debug is handled on the HIP cards using a dedicated logic analyzer tap PCB pattern.

5.10.1 LEDs

Table 5-11 describes the diagnostic LEDs on the Arcadia motherboard.

Table 5-11. Arcadia Diagnostic LEDs

LED	PCB Label	Definition
D13	HOT_3V	Standby 3.3 V power working
D16	HOT_5V	Standby 5 V power working (from ATX power)
D6	3.3V	Power on, 3.3 V working
D1	2.5V	2.5-V regulator for Actel and Tsi310 working
D3	ISO	PCIB3 has been isolated from the PCIB4 domain
D14	CLKSTAT	Clock is stable

Table 5-11. Arcadia Diagnostic LEDs (continued)

LED	PCB Label	Definition
D15	PWRGD	Power is stable from ATX power supply
D17	IDE	IDE disk activity detected
D8	L1_VIA	VIA status LED
D9	L2_ISO	Bus domains are isolated
D10	L3_ARB	Arbitration activity
D11	L4_BOOT	Access to PCI Boot space detected
D12	L5_PSPD0	PCIA speed detect or user_defined
D13	L6_PSPD1	PCIA speed detect or user_defined
D14	L7_PCIA	PCIA activity detected or user_defined
D15	L8_PCIB	PCIB activity detected or user_defined

PCIA speed detect is encoded as shown in Table 5-12.

Table 5-12. Arcadia Diagnostic LEDs: PCI Speed Encoding

PSPD(1:0)		Speed
OFF	OFF	33-MHz PCI
OFF	ON	66-MHz PCI
ON	OFF	NA
ON	ON	NA

5.10.2 JTAG

Table 5-13 describes the diagnostic LEDs on the Arcadia motherboard.

Table 5-13. Arcadia JTAG Chain

Device	TDI Input Name	TDO Output Name	Notes
FPGA	(from header)	ARC_TDO	
PrPMC	ARC_TDO	PRPMC_TDO	
Tundra	PRPMC_TDO	TSI310_TDO	
Slot 2	TSI310_TDO	SLOT2_TDO	
Slot 4	SLOT2_TDO	SLOT4_TDO	
Slot 5	SLOT4_TDO	SLOT5_TDO	
Slot 6	SLOT5_TDO	SLOT6_TDO	
Slot 7	SLOT6_TDO	SLOT7_TDO	Slot 7 TDO test pad near FPGA header

5.11 Configuration

Arcadia contains several slide-switches used to configure the board, processors(s) and chipsets for the options shown in Table 5-14. Underlined entries are the defaults, as shipped. Since the switches operate by connecting a pulled-up signal to ground, setting a switch to ON is indicated as '1' in the table.

All switches are oriented so that ON = 1 = UP, where UP means toward the PCI and I/O connector back panel of the ATX chassis. If the chassis is standing up with the cover off, an alternate interpretation is ON = 1 = LEFT.

Table 5-14. Arcadia Configuration Switches

Switch	No.	Option	Description	Default Setting	Notes
SW1	1	TSI310: BAR_EN	Default 1MB BAR enable 0/OFF: BAR0 disabled by default 1/ON: BAR0 enabled by default	0	
	2	TSI310: S_INT_ARB_EN	Secondary bus internal arbiter enable 0/OFF: Use internal arbiter 1/ON: Use external arbiter	0	
	3	TSI310: 64_BIT_DEVICE	Physical width of the PCI-X device 0/OFF: Bridge is a 64-bit bus 1/ON: Bridge is a 32-bit bus	0	
	4	TSI310: OPAQUE_EN	Opaque region enable 0/OFF: Opaque memory enable = 0 1/ON: Opaque memory enable = 1	0	
	5	TSI310: IDSEL_REROUTE_EN	Secondary PCI IDSEL remap 0/OFF: IDSEL remap mask is 0000_0000 1/ON: IDSEL remap mask is 22F2_0000	0	
	6	TSI310: S_SEL100	Secondary high-speed rate select 0/OFF: PCI-X highest speed is 133 MHz 1/ON: PCI-X highest speed is 100 MHz	1	
	7	TSI310: P_CFG_BUSY	Primary configuration busy 0/OFF: Primary side responds to configuration cycles normally. 1/ON: Primary side configuration cycles are retried until bit 2 of the miscellaneous control registers is set to 0 by a secondary configuration cycle write.	0	
	8	TSI310: P_DRVR_MODE	Primary Driver mode control 0/OFF:Normal impedance 1/ON:Lower impedance for heavier loads	0	

Table 5-14. Arcadia Configuration Switches (continued)

Switch	No.	Option	Description	Default Setting	Notes
SW3	1	ISOLATE_3_4	Isolate slow PCI bus segment 0/OFF: PCIB3 connected to PCIB4 1/ON: PCIB3 isolated from PCIB4	1	
	2	BRIDGE_EN*	TSI310 PCI bridge enable 0/OFF: PCI bridge responds to config cycles 1/ON: PCI bridge ignores all config cycles	1	2
	3	PCIA_FRC1	PCI A (Fast) bus speed force FRC(1:0) 0 0 AUTO (33 MHz when M66_EN input is 0 or 66 MHz when M66_EN is a 1. M66_EN pin is three-stated.) 0 1 PCIA forced to 66 MHz PCI mode (M66_EN pin is three-stated) 1 0 PCIA forced to 33 MHz PCI mode (M66_EN pin is driven with logic 0) 1 1 PCIA forced to 33 MHz PCI mode (M66_EN pin is driven with logic 0)	11	
	4	PCIA_FRC0			
	5	ENET_DIS*	RTK8139 Ethernet enable 0/OFF RealTek 8139 may be accessed 1/ON: RealTek 8139 cannot be accessed	1	
	6	PCI_INT_BRIDGE*	PCI bus interrupt connection 0/OFF: PCIA and PCIB interrupts are directly connected (wire-OR'd) 1/ON: PCIA and PCIB interrupts are isolated	1	
	7	PRPMC_IDSELEN*	PrPMC IDSEL enabled 0/OFF: PrPMC can be target selected 1/ON: PrPMC cannot be target selected	1	5
	8	MONARCH*	0/OFF: PrPMC is PCIB controller 1/ON: PrPMC is not PCIB controller	1	1

Table 5-14. Arcadia Configuration Switches (continued)

Switch	No.	Option	Description	Default Setting	Notes
SW2	1	ARC0	0/OFF: SIOINT -> PCIB3_INT0 1/ON: SIOINT -> PCIB3_INT1	0	
	2	ARC1	Reserved	1	
	3	ARC2	Reserved	1	
	4	G0	Switch readable on VIA GPI5	1	3
	5	G1	Switch readable on VIA GPI6	1	3
	6	LPCWP*	0/ON: LPC flash is write-protected 1/OFF: LPC flash is write-enabled	1	4
	7	rsvd	N/A	1	
	8	rsvd	N/A	1	

Notes:

1. This switch configures the MPMC card into system controller, a mode which is required for normal PCI use. Disabling is provided for testing purposes only.
2. This switch allows software that does not wish to deal with PCI bridges ignore them, at the cost of access to the other PCI domain.
3. Software-defined switches.
4. Optional feature.
5. Some PCI devices do not allow their own IDSEL to be asserted when operating as the PCI host; if so, use this switch to disable IDSEL. Not applicable for PCI agents.

5.11.1 Power Supply Force Header

This 2-pin Berg header allows installation of a shorting header. When not installed, as is the default, the chassis power switch is used to turn power ON and OFF. If a header is installed across pins 1 and 2, the ATX power supply will be forced into the ON state at all times. This feature is used with non-ATX power supplies, as well as with systems requiring systems to power-up in the ON state.

Table 5-15. Arcadia Power Supply Force Header

Pin	Definition
1	$\overline{\text{PSON}}$; open-drain signal pulled up to 5 V
2	Chassis ground

5.12 Mechanical

The following sections discuss mechanical issues of the Arcadia board, including board layout, thermal/heatsink issues, and placement. Nothing in this section should be considered a substitute for mechanical drawings.

5.13 Motherboard Dimensions

Arcadia is a standard 12.0 × 9.6 inch (305 × 244 cm (the specification is written in inches)) motherboard, and follows standard ATX 2.01 clearance requirements. Arcadia implements the standard set of mounting holes for chassis attachment, with the addition of ATX 2.01 mounting hole F, located near the communications port adapter as shown in Figure 5-8.

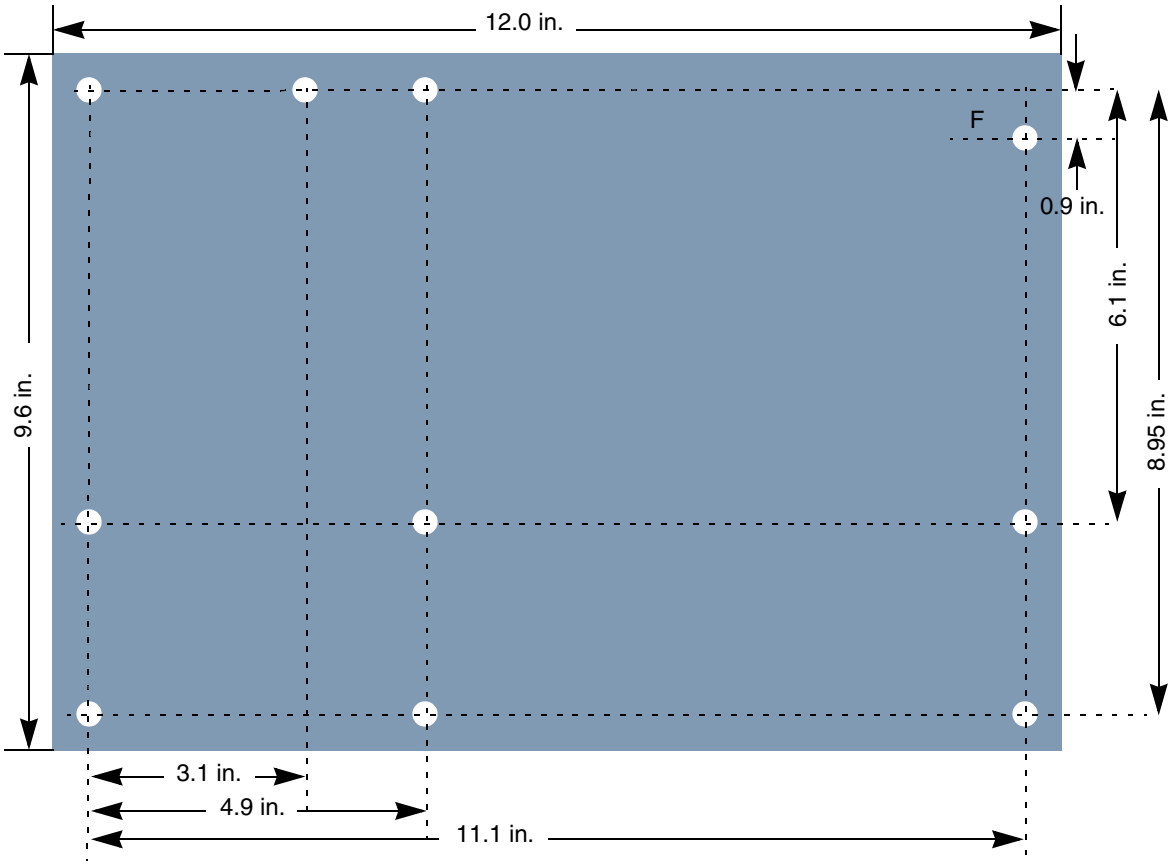


Figure 5-8. Arcadia ATX Chassis Mounting Holes

Hole F is required for ATX 2.01 standards and is needed for mechanical rigidity for Arcadia; most standard chassis punchouts implement the standard support area.

5.14 Placement

The general placement of components on the Arcadia motherboard is shown in Figure 5-9.

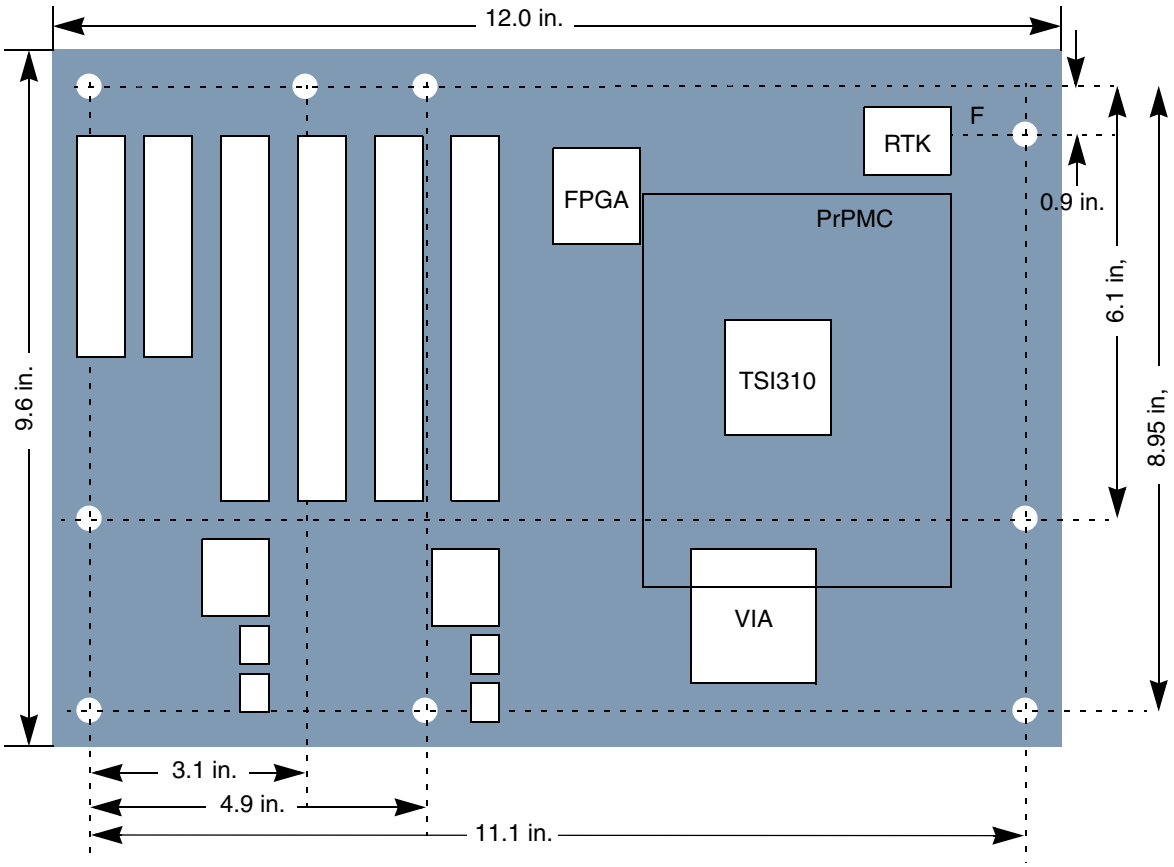


Figure 5-9. Component Placement

Chapter 6
CDS IOCard Architecture

This chapter describes the IOCard in detail. It elaborates on the physical architecture and device connections, as well as the power management and usage.

6.1 Mechanical Properties

The CDS IOCard is essentially a PCB and connector implementing a passive but high-quality, balanced connection between communications devices and the connectors. To maximize the available back-panel I/O space available with a double-width PCI form-factor, CDS uses a small card near the IO escape end of the board. The use of small modules to allow flexibility on the CPM interface is the primary driving factor behind the connector solution. The module must be positioned such that any I/O from a module will be properly aligned with the adjacent PCI slot (recall that HIP cards are twice the PCI card width). The CDS system routes its dedicated I/O to the first slot in the chassis opening. The optical connectors are routed to the adjacent opening.

Figure 6-1 shows a block diagram of a CDS daughtercard, for reference purposes.

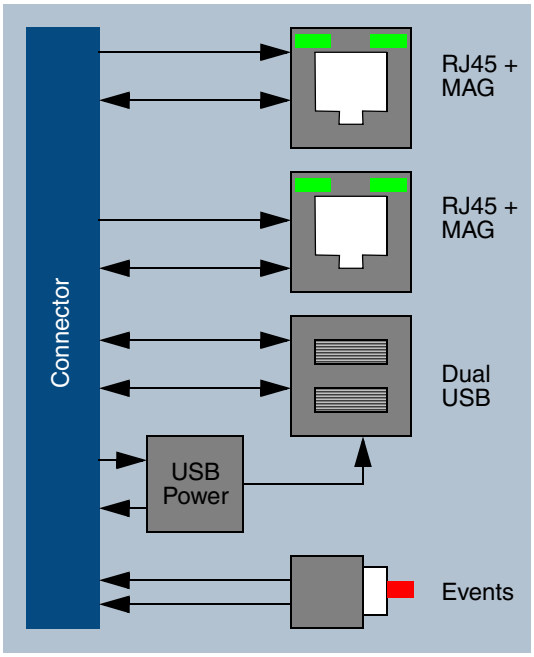


Figure 6-1. CDS IOCard Block Diagram

The approximate placement and component sizes of the CDS IOCard are shown in Figure 6-2.

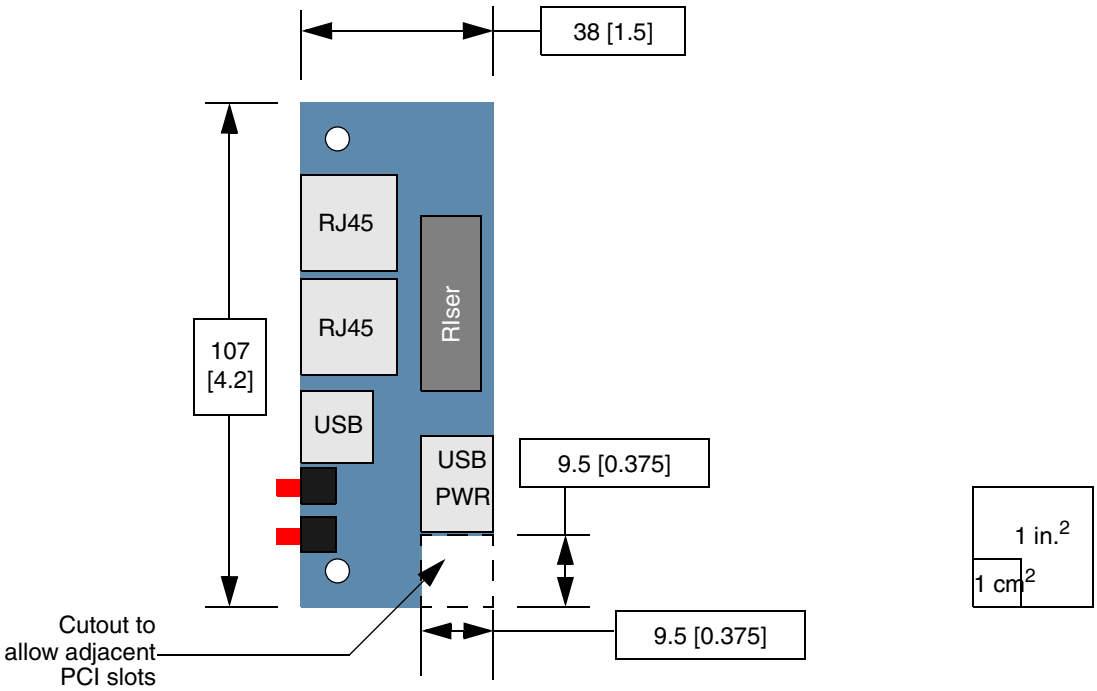


Figure 6-2. CDS IOCard Physical Dimensions

6.2 IOCard Connector

The IOCard uses a high-speed, high-density connector. Table 6-1 lists the pins of the daughtercard connector.

Table 6-1. CDS IOCard Connector Details

Signal Group	Signal	Pin Count	Notes
TSEC3	T3_TXI[P,N][A:D]	8	Differential routing matched-length routing
	T3_LED(1:4)	4	—
TSEC4	T4_TXI[P,N][A:D]	8	Differential routing matched-length routing
	T4_LED(1:4)	4	—
USB	U1_TN, U1_TP	2	Differential routing matched-length routing
	U2_TN, U2_TP	2	Differential routing matched-length routing
	$\overline{\text{U1\_OC}}$, $\overline{\text{U2\_OC}}$	2	—
Signal	$\overline{\text{EVENT1}}$, $\overline{\text{EVENT2}}$	2	Reset/IRQ/event signal
Power	VCC_3.3	10	—
	VCC_5	6	Needed for USB power
	GND	46	—
Total	Total	94	—

Table 6-1. CDS IOCard Connector Details (continued)

Signal Group	Signal	Pin Count	Notes
Spares	Spares	6	Bring up to next connector size
Total	Total	100	—

6.3 IOCard Connector Pinout

For a detailed pinout, including numbering, refer to Appendix B.2, “IOCard Connector Pinout.”

6.4 IO Power

IO power is obtained from the carrier, which supplies +2.5- and +3.3-V power. This power is shared with numerous resources, excluding the daughtercard, which derives its power separately.

Chapter 7
uTCOM Architecture

This chapter describes the interface of the uTCOM, as well as its physical properties. The uTCOM is an adaptation of the TCOM expansion board. Essentially, it is the same, just shrunk to fit the CDC. The uTCOM board is a separate adapter, with its own specification document.

7.1 Overview

The general uTCOM interface architecture is shown in Figure 7-1.

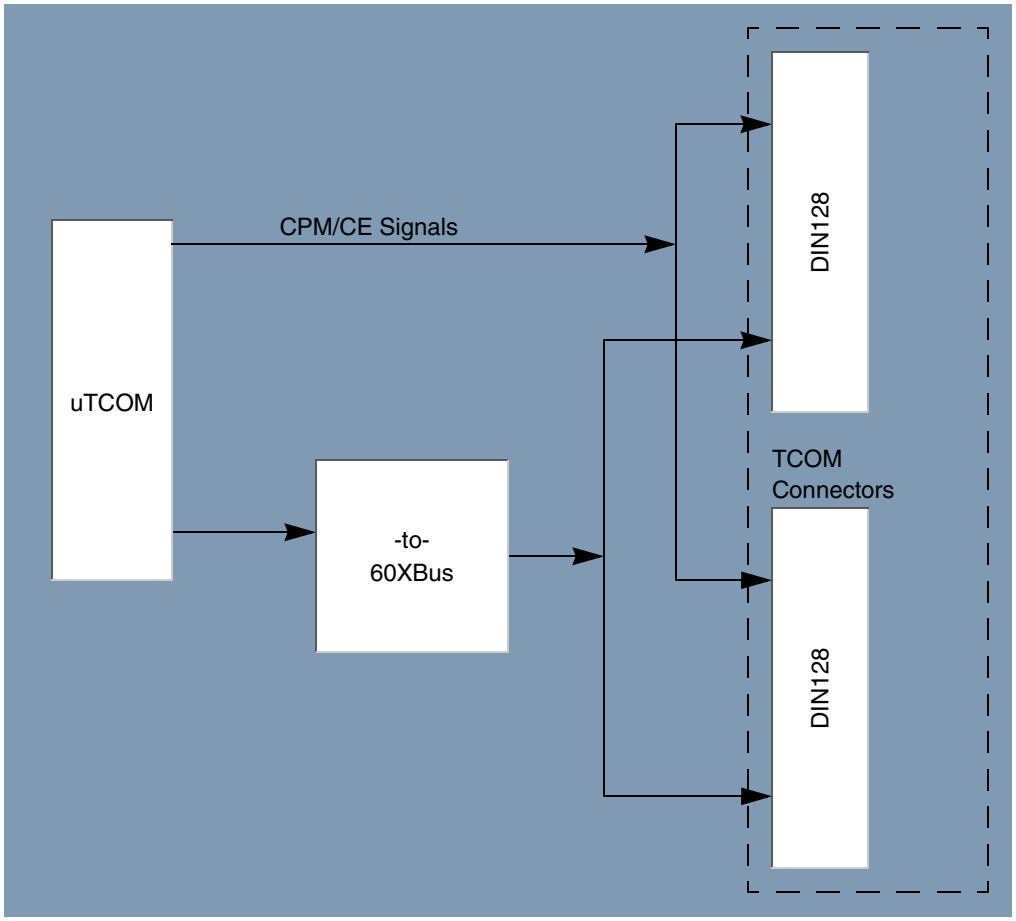


Figure 7-1. CDS uTCOM/TCOM Interface

7.2 Mechanical Architecture

7.2.1 uTCOM Connector

- The uTCOM connector is used to connect the CDS carrier card to one of several special-purpose test/evaluation boards, most commonly the TCOM board. This card has numerous I/O, debug and communications configurations, and is connected to via two 128-pin DIN connectors. These connectors are too large to be accommodated on the CDS carrier, therefore, CDS uses a 400-pin connector on the back of the board (the same FCI connector is used for the daughtercard connection). This connector mates to a special adapter board, which converts the FCI footprint to the TCOM footprint. The adapter board also contains:
- Interface logic that allows the CDS local bus to communicate with the TCOM
- Optional USB 1.1 interface to support certain processors
- Additional power supply access points
- Mechanical bracing mechanisms for rigidity

7.2.2 uTCOM Connector Signals

Table 7-1 lists the signals of the uTCOM connector.

Table 7-1. CDS uTCOM Connector Details

Signal	Notes
PA(0:31)	
PB(4:31)	
PC(0:31)	
PD(4:31)	
CX(0:60)	CE/future expansion
LB_A(0:15)	Lower 16 addresses
LB_D(0:15)	16-bit data bus
LB_CS(6:7)	
$\overline{\text{LB\_BS/WE}}$(0:3)	
LALE	
LBCTL	
LGP(0:5)	
LBCLK	
CFGDRV	
TCM_RST	
$\overline{\text{IRQ}}$(6:7)	
MDIO	

Table 7-1. CDS uTCOM Connector Details (continued)

Signal	Notes
MDC	
5V	
3.3V	
Ground	
Total	
Spares	Bring up to next connector size
Total	

7.3 uTCOM Pinout

For a detailed pinout, including numbering, refer to Appendix B.3, "uTCOM Connector Pinout."

The following tables detail the pinout interface between CDS uTCOM board P1 and P2 connector, to TCOM board (Table 7-2 and Table 7-3).

Table 7-2. uTCOM Pin Routing to TCOM Board (P1 Connector)

MPC8555E CPM (Port Name)	Male	uTCOM Sweezler <->	Female	TCOM (Port Name)
PA31–PA26		FCC1–FEC		A31–PA26
PA21–PA14		FCC1–FEC		PA21–PA14
PA21–PA14		FCC1–FEC		PA21–PA14
PC21	CLK11	FCC1-FEC	RXCLK	PC21
PC20	CLK12	FCC1-FEC	TXCLK	PC20
PB30	FCC2-FEC	RxDV	FCC3-FEC	PB17
PB28	FCC2-FEC	RxER	FCC3-FEC	PB16
PB31	FCC2-FEC	TxER	FCC3-FEC	PB15
PB29	FCC2-FEC	TxEN	FCC3-FEC	PB14
PB27	FCC2-FEC	COL	FCC3-FEC	PB13
PB26	FCC2-FEC	CRS	FCC3-FEC	PB12
PB18	FCC2-FEC	RxD3	FCC3-FEC	PB11
PB19	FCC2-FEC	RxD2	FCC3-FEC	PB10
PB20	FCC2-FEC	RxD1	FCC3-FEC	PB9
PB21	FCC2-FEC	RxD0	FCC3-FEC	PB8
PB22	FCC2-FEC	TxD0	FCC3-FEC	PB7
PB23	FCC2-FEC	TxD1	FCC3-FEC	PB6

Table 7-2. uTCOM Pin Routing to TCOM Board (P1 Connector) (continued)

MPC8555E CPM (Port Name)	Male	uTCOM Sweezler <->	Female	TCOM (Port Name)
PB24	FCC2-FEC	TxD2	FCC3-FEC	PB5
PB25	FCC2-FEC	TxD3	FCC3-FEC	PB4
PC17	CLK15	FCC2-FEC	RXCLK	PC17
PC16	CLK16	FCC2-FEC	TXCLK	PC16
PD22	TDMA2	TxD	TDMB1	PD13
PD21	TDMA2	RxD	TDMB1	PD12
PC9	TDMA2	Tsync	TDMB1	PD11
PD20	TDMA2	Rsync	TDMB1	PD10
PD30		EN_T1_2		PD5
PC27	CLK5	TDMA2	T1_2_RXCLK	PC23
PC26	CLK6	TDMA2	T1_2_TXCLK	PC22
PB27	TDMB2	TxD	TDMB2	PB31
PB26	TDMB2	RxD	TDMB2	PB30
PB25	TDMB2	Tsync	TDMB2	PB28
PB24	TDMB2	Rsync	TDMB2	PB29
PD31		EN_T1_6		PD9
PC29	CLK3	TDMB2	T1_6_RXCLK	PC17
PC28	CLK4	TDMB2	T1_6_TXCLK	PC16
PA9	TDMC2	TxD	TDMA1	PA9
PA8	TDMC2	RxD	TDMA1	PA8
PB28	TDMC2	Tsync	TDMA1	PA7
PC1	TDMC2	Rsync	TDMA1	PA6
PD29		EN_T1_1		PD4
PC19	CLK13	TDMC2	T1_1_RXCLK	PC31
PC18	CLK14	TDMC2	T1_1_TXCLK	PC30
—		VCC		—
—		GND		—
—		VCC	VDS3EN1	PD25
—		VCC	VDS3EN2	PA4
—		GND	DS3 LB	PA5
—		GND	DS3LB	PC13

Table 7-2. uTCOM Pin Routing to TCOM Board (P1 Connector) (continued)

MPC8555E CPM (Port Name)	Male	uTCOM Sweezler <->	Female	TCOM (Port Name)
PD23		EN_T1_3		PD6
PD24		EN_T1_4		PD7
PD25		EN_T1_5		PD8
PD14		EN_T1_7		PD18
PD15		EN_T1_8		PD19
All other	—	NC	—	All other
PC9	—	MIIMDIO	—	PC9
PC10	—	MIIMDC	—	PC10

Table 7-3. uTCOM Pin Routing to TCOM Board (P2 Connector)

MPC8555E CPM (Port Name)	Male	uTCOM Sweezler <->	Female	TCOM (Port Name)
—	MIIMDIO	MIIMDIO	Connector P1	PC9
—	MIIMDC	MIIMDC	Connector P1	PC10
All other	—	Pin-to-pin	—	All other

NOTE

The MIIMDIO and MIIMDC signals of the TCOM are connected to both uTCOM expansions, P1 and P2 (for compatibility reasons).

Appendix A
Revision History

This appendix provides a list of the major differences between the *MPC8555E Configurable Development System Reference Manual*, Revision 0 through the *MPC8555E Configurable Development System Reference Manual*, Revision 1.

A.1 Changes From Revision 0 to Revision 1

Major changes to the *MPC8555E Configurable Development System Reference Manual*, from Revision 0 to Revision 1 are as follows:

Section, Page	Changes
Book	Change 33-66 MHz to 33/66 MHz.
About This Book, xiv	In the “Organization” section, change the nineth and tenth bullets to read • Appendix C, “CDS Carrier BOM, Rev. 1.2” • Appendix D, “CDS Carrier Schematics, Rev. 1.2” After the tenth bullet, insert two new bullets and renumber the remaining appendices as follows: • Appendix E, “CDS Carrier BOM, Rev. 1.3” • Appendix F, “CDS Carrier Schematics, Rev. 1.3”
1.1, 1-1	Replace the first sentence with the following: The configurable development system (CDS) was developed to support a wide range of Power Architecture™ processors, such as the MPC8555E and the MPC8541E.
1.2, 1-1	Replace the first paragraph with the following: This reference manual describes the Freescale CDS development platform. It provides details on the MPC8555E CDS hardware configuration and functionality. It is intended primarily as a guide for hardware and software designers.
1.3, 1-1	Replace the entire section with the following: The CDS system is the middle ground between evaluation and test boards. It is more configurable and flexible than an evaluation board, but it is not as configurable as a test board, in which every component can be tested and examined. Where it lacks configurability, its design has options for the most common settings. Two MPC8555E CDS development system configurations are described. The configurations consist of different board revisions which are referenced

throughout this manual as Configuration 1 or Configuration 2. The configurations are:

- Configuration 1
  - — Arcadia, Rev. 3.1
  - — Carrier card, Rev. 1.2
  - — CPU card, Rev. 1.1
  - — I/O card, Rev. 1.1
- Configuration 2
  - — Arcadia, Rev. 3.1
  - — Carrier card, Rev. 1.3
  - — CPU card, Rev. 1.1

Refer to Appendix F, “CDS Carrier Schematics, Rev. 1.3,” Table F-1, for hardware differences between carrier card, Rev. 1.2 and Rev. 1.3.

1.3.1, 1.2 Last bullet, second dash, replace with the following:

— Supports two Ethernet ports on the carrier card at MII/GMII, and two Ethernet ports on the I/O adapter at MII/GMII, 10/100 or 1G rates (Configuration 1).

NOTE

In Configuration 1, Ethernet port #4 on the I/O card is not functional.

— Supports all four Ethernet ports on the carrier card. MII/GMII on ports #1 and #2. Ethernet ports #3 and #4, 10/100 or 1G rates (Configuration 2).

1.3.1, 1-2 Last dash on page, replace with the following:

— PCI/PCI-X 32/64 bits, 33/66 MHz

1.3.1, 1-3 Last two bullets, replace with the following:

— Includes I/O adapter board (Configuration_1)

1.3.2, 1-3 Replace the first paragraph with the following:

Figure 1-1 is a diagram of the CDS system for Configuration 1.

1.3.2, 1-3 Change Figure 1-1 caption to the following:

Figure 1-1. Carrier Block Diagram (Configuration 1)

1.3.2, 1-3 After Figure 1-1, add the following paragraph and figure:

Figure 1-2 is a diagram of the CDS system for Configuration 2.

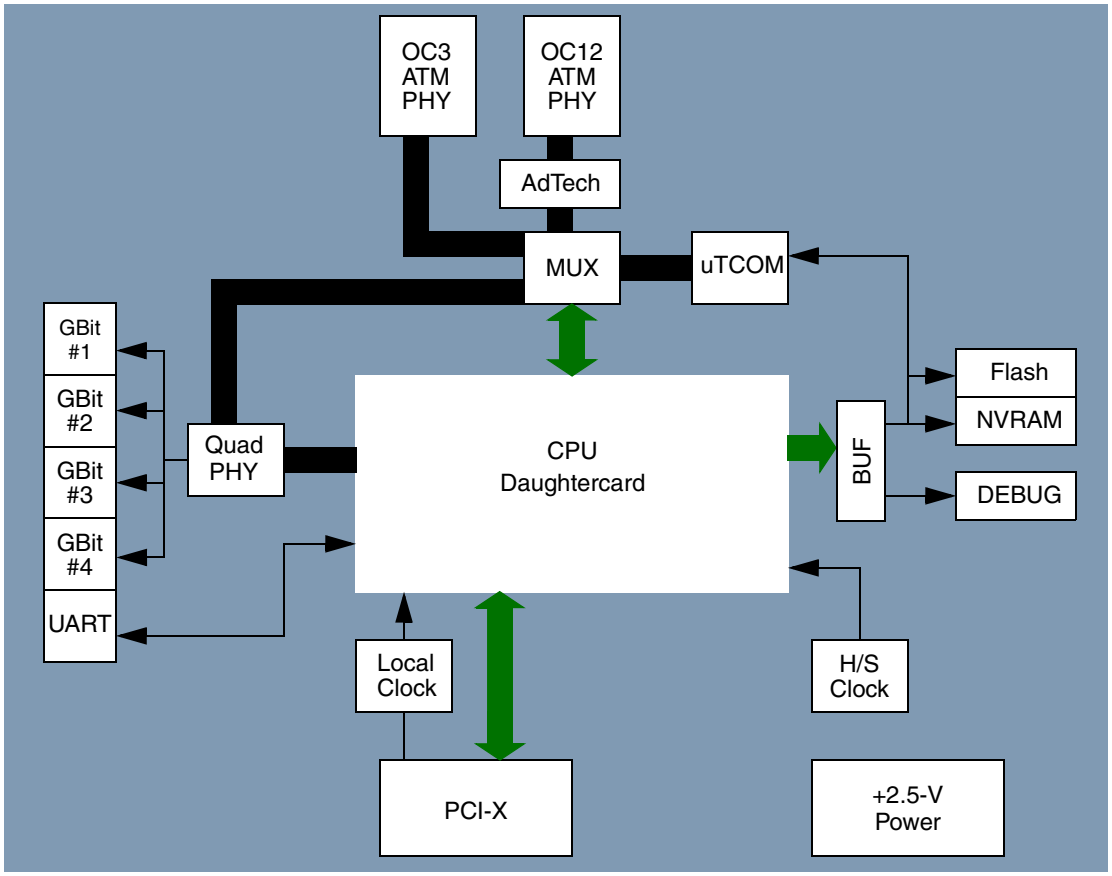


Figure 1-2. Carrier Block Diagram (Configuration 2)

1.3.2, 1-4 Renumber Figure 1-2 to Figure 1-3.

Chapter 2, 2-1 Replace the first paragraph with the following:

This chapter provides a step-by-step guide for bringing up a CDS.

2.1, 2-1 Replace the first paragraph, four bullets, and note with the following:

The hardware configurations consist of different board revisions which are referenced throughout this manual as Configuration 1 or Configuration 2. Refer to Appendix F, “CDS Carrier Schematics, Rev. 1.3,” Table F-1, for hardware differences between carrier card, Rev. 1.2 and Rev. 1.3. The configurations are:

- Configuration 1
  - Arcadia, Rev. 3.1
  - Carrier card, Rev. 1.2
  - CPU card, Rev. 1.1
  - I/O card, Rev. 1.1
- Configuration 2
  - Arcadia, Rev. 3.1
  - Carrier card, Rev. 1.3
  - CPU card, Rev. 1.1

2.2,2-1 Replace the first sentence in the note to read:

The carrier card and processor card are packaged together.

2.2, 2-1 Delete Step 1 and renumber the rest.

2.3, 2-5 Item No. 5, replace the U-boot screen dump with the following:

```
U-Boot 1.1.3 (FSL Development) (Oct 27 2006 - 10:43:18)
CPU:   8555, Version: 1.1, (0x80790011)
Core:  E500, Version: 2.0, (0x80200020)
Clock Configuration:
       CPU: 833 MHz, CCB: 333 MHz,
       DDR: 166 MHz, LBC:  83 MHz
L1:    D-cache 32 kB enabled
       I-cache 32 kB enabled
Board: CDS Version 0x13
CPU Board Revision 0.0 (0x0000)
    PCI1: 32 bit, 33 MHz, sync
    PCI2: 32 bit, 66 MHz, async
I2C:   ready
DRAM:  Initializing
    SDRAM: 64 MB
    DDR: 256 MB
FLASH: 16 MB
L2 cache 256KB: enabled
In:    serial
Out:   serial
Err:   serial
Net:   TSEC0: PHY is Marvell 88E1145 (1410cd4)
TSEC1: PHY is Marvell 88E1145 (1410cd4)
TSEC0, TSEC1
The IP address of the board is currently set to 169.254.113.58
The MAC address is 00:04:9F:00:28:C8
If they don't match your network environment, please change them in U-Boot and kernel
manually.
Hit any key to stop autoboot:  0
=>
```

2.5, 2-9 Change the title of Table 2-2 to read: “Default Status of Carrier Board Switches (Configuration 1).”

2.5, 2-9 In Table 2-2, replace the rows for SW 1, Bits 2 and 3 with the following:

1	2	Synchronizer	1	1 Must be 1 at all times (PHY CLK/FPGA CLK)
	3	Reserved	1	See Note 1

2.5, 2-9 In Table 2-2, replace the rows for SW 2, Bits 5 and 6 with the following:

2	5	Reserved	1	1 Reserved
	6	Reserved	1	1 Reserved, see Note 2

2.5, 2-10 In Table 2-2, replace the row for SW 3, Bit 2 with the following:

3	2	DUART output select	1	0 DUART channel #2 to 2x5 (AT) header DUART channel #1 to DB9 connector
				1 DUART channel #2 to DB9 connector DUART channel #1 to 2x5 (AT) header

2.5, 2-10 In Table 2-2, replace the row for SW 3, Bits 6 with the following:

3	6	FE select	0	0 FCC3->Cicada MII#4 enabled 1 FCC3->Cicada MII#4 disabled

2.5, 2-10 In Table 2-2, add the following notes to the end of the table:

Notes:

1. SW1(3) for Configuration 2 is PCI CLK SEL and must be set to 1.
2. SW2(6) for Configuration 2 is PCI Select PCI = 1 and PCIX = 0.

2.5, 2-11 Change the title of Table 2-3 to read: “Default Status of Arcadia Board Switches (Arcadia C3.n).”

2.5, 2-11 In Table 2-3, replace the rows for SW 2, Bits 4–8 and SW 3, Bits 1 and 2 with the following:

2	4 [1]	G0	1	User defined
	5 [1]	G1	1	User defined
	6 [2]	LPCWP*	1	User defined
	7	Reserved	1	N/A
	8	Reserved	1	N/A
3	1	Isolate slow PCI bus segment ISOLATE_3_4	0	0 PCIB3 connected to PCIB4 1 PCIB3 isolated from PCIB4
	2	TSI310 PCI bridge enable BRIDGE_EN*	0	0 PCI bridge responds to config cycles 1 PCI bridge ignores all config cycles

2.5, 2-11 In Table 2-3, replace the rows for SW 3, Bits 6, 7, and 8; and replace the notes with the following:

3	5	RTK8139 Ethernet enable ENET_DIS*	1	0 RealTek 8139 may be accessed 1 RealTek 8139 cannot be accessed
	6	PCI bus interrupt connection PCI_INT_BRIDGE*	0	0 PCIA and PCIB interrupts are directly connected (wire-or'd) 1 PCIA and PCIB interrupts are isolated
	7 [3]	PrPMC IDSEL enabled PRPMC_IDSELEN*	1	0 PrPMC can be target selected 1 PrPMC cannot be target selected
	8 [4]	MONARCH*	1	0 PrPMC is PCIB controller 1 PrPMC is not PCIB controller

Notes:

1. Software-defined switches.
2. Optional feature.
3. Some PCI devices do not allow their own IDSEL to be asserted when operating as the PCI host; if so, use this switch to disable IDSEL. Not applicable for PCI agents.
4. This switch configures the MPMC card into the system controller, a mode which is required for normal PCI use. Disabling is provided for testing purposes only.

3.1.1, 3-1 Delete the first 2 paragraphs, 2 bullets, and Figure 3-1.

3.1.2, 3-2 Replace the first paragraph with the following:

Figure 3-1 is a diagram of the CDS board for Configuration 1.

3.1.2, 3-2 Change Figure 3-2 caption to the following:

Figure 3-1. Carrier Block Diagram (Configuration 1)

3.1.2, 3-2 After Figure 3-2, add the following paragraph and figure:

Figure 3-2 is a diagram of the CDS system for Configuration 2.

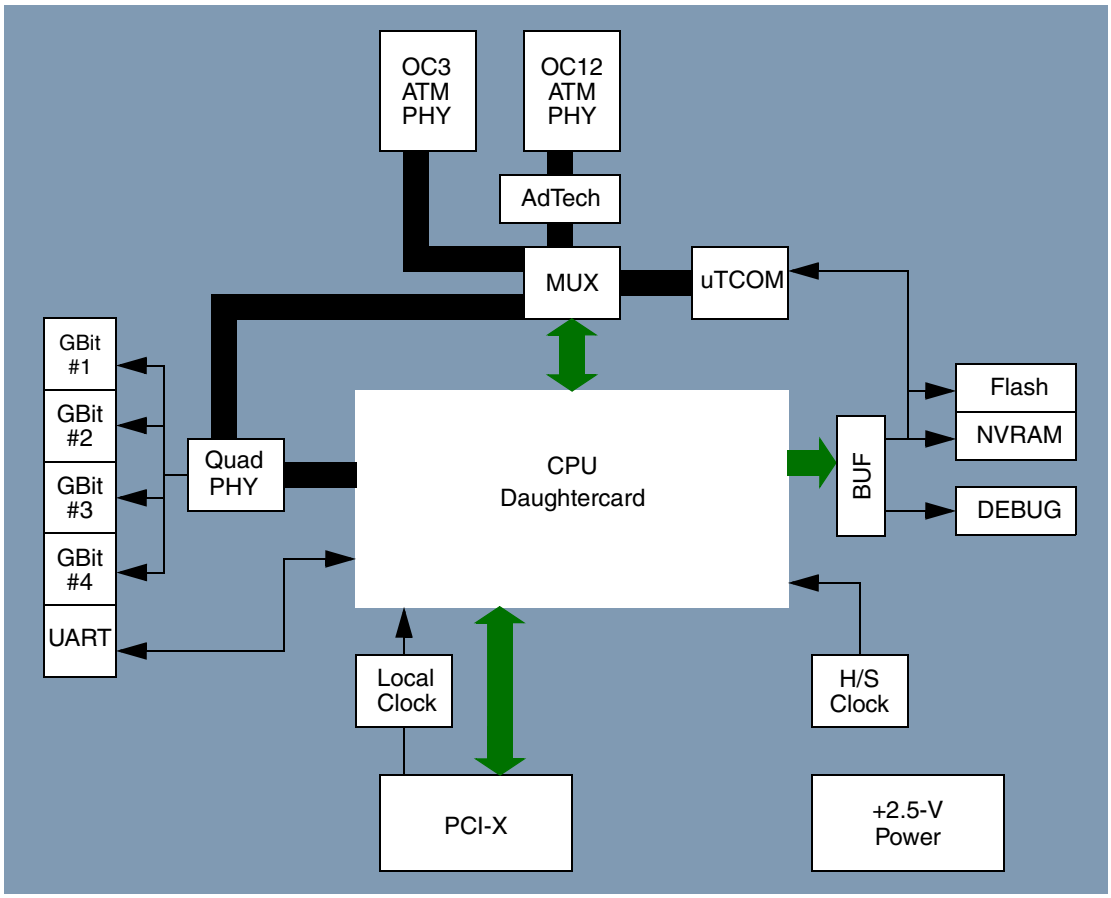


Figure 3-2. Carrier Block Diagram (Configuration 2)

3.3.2, 3-4 In Table 3-2, replace offset rows 0x03 and 0x04 with the following:

0x03	Reserved	—	—
0x04	Reserved	—	—

3.3.2.3, 3-5 In Table 3-5, replace row for bit 1 with the following:

1	PHYRST	This bit allows software to issue a reset to the Ethernet PHY.

3.3.2.4, 3-6 Delete Section 3.3.2.4, Figure 3-6, and Table 3-6.

3.3.2.5, 3-6 Delete Section 3.3.2.5, Figure 3-7, and Table 3-7. Renumber the remaining sections, figures, and tables.

3.5, 3-12 In Figure 3-12, replace the label HFBR-5805 with HFBR-5208M. Replace the label HFBR-58208M with HFBR-5805.

3.5, 3-12 In Table 3-15, replace feature row for optical transceiver with the following:

Optical transceiver	Agilent HFBR-5208M	Agilent HFBR-5805

3.6, 3-12

Replace the first paragraph and note with the following:

In Configuration 1, the CDS carrier card provides four 10/100 1GB-baseT Ethernet ports. Two are located on the basic carrier board and the other two on the IOCard expansion. The four ports are controlled by a Cicada CS8204 quad-PHY, which in turn receives data from three dedicated MII/GMII daughtercard connections.

In Configuration 2, all four Ethernet ports on the carrier card are supported by a Marvell 88E1145. MII/GMII on Ethernet ports #1 and #2. RGMII on Ethernet ports #3 and #4, 10/100 or 1G rates.

NOTE

In Configuration 1, TBI, RTBI, RMII, and RGMII interface modes are not supported.

In Configuration 1, Ethernet port #4 on the I/O card is not functional.

In Configuration 2, RGMII is supported only on Ethernet ports #3 and #4.

3.6, 3-13

Add the following sentence to the paragraph before Table 3-16:

The Ethernet PHY addresses are fixed in Configuration 2.

3.6, 3-13

Change Table 3-16 caption to the following:

Table 3-16. Phy Address Options (Configuration 1)

3.6, 3-13

After Table 3-16, replace the paragraph with the following:

These connections and the interface logic are shown in Figure 3-11 for Configuration 1 and Figure 3-12. for Configuration 2.

3.6, 3-14

Change Figure 3-13 caption to the following:

Figure 3-11. CDS Ethernet Architecture (Configuration 1)

3.6, 3-14 After Figure 3-13, add the following figure:

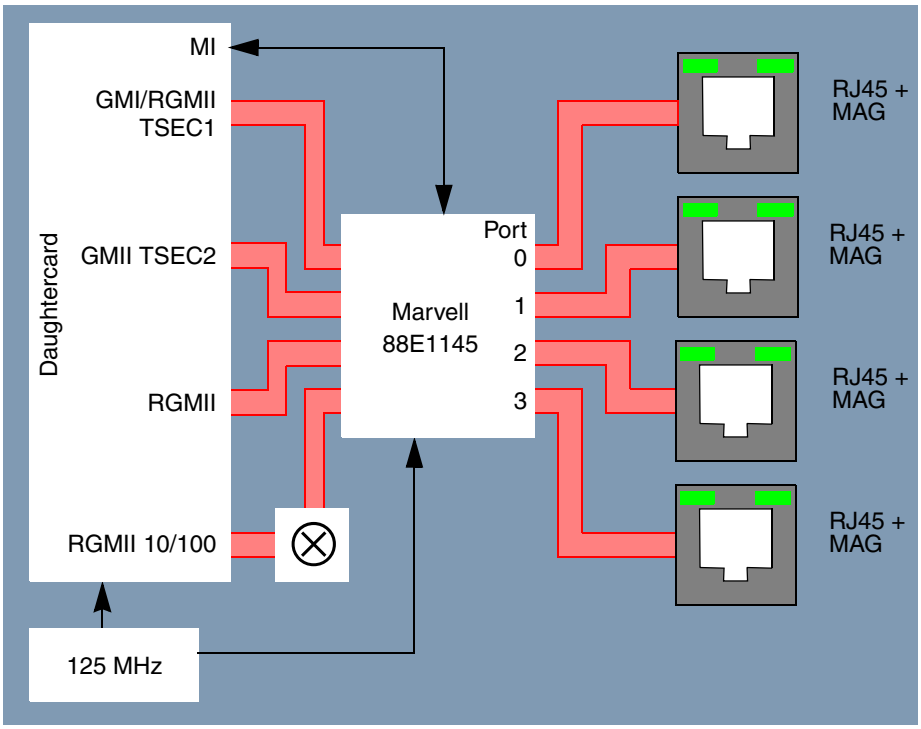


Figure 3-12. CDS Ethernet Architecture (Configuration 2)

3.6, 3-14 In Table 3-17 change the fifth column heading to read: ‘CS8204 PHY or Marvell 88E1145’. Remove the references to note 3 in the table and note 3 at the end of the table.

3.7, 3-16 Table 3-18, replace the Chip selects rows with the following:

Chip selects	$\overline{\text{LB\_CS0}}$	8	Connects to Flash device #1 (carrier card)
	$\overline{\text{LB\_CS1}}$		Connects to Flash device #2 (carrier card)
	$\overline{\text{LB\_CS2}}$		Connects to SRAM/SDRAM port (CPU card)
	$\overline{\text{LB\_CS3}}$		Connects to RTC/NVRAM
	$\overline{\text{LB\_CS4}}$		Connects to uTCOM port
	$\overline{\text{LB\_CS5}}$		Reserved
	$\overline{\text{LB\_CS6}}$		Reserved
	$\overline{\text{LB\_CS7}}$		Reserved

3.8, 3-18 Change the first paragraph to the following:

The CDS carrier board contains four independent clock domains:

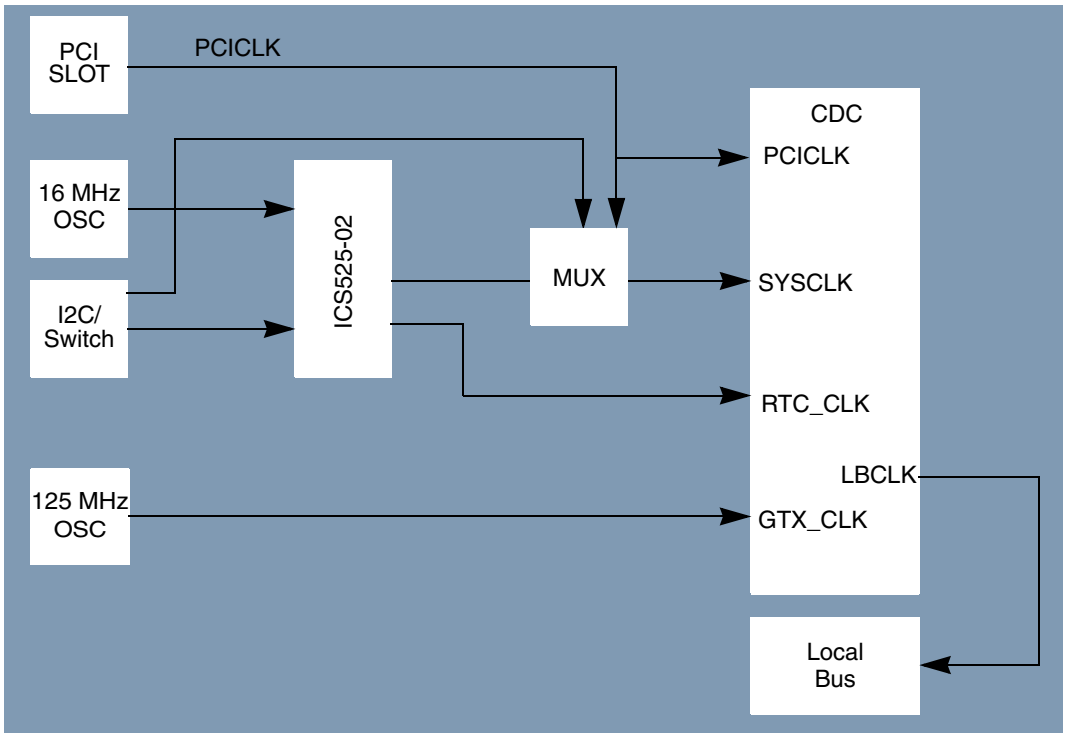
3.8, 3-18 After the first paragraph delete the fourth item.

3.8, 3-19 Table 3-21, change the PCICK row with the following:

PCICLK	33/66 MHz	3.3V LVTTL	PCI interface of daughtercard	

3.8, 3-19 Table 3-21, remove the HS_CLK row and note 1 at the end of the table.

3.8, 3-19 Replace Figure 3-15 with the following:



3.8, 3-21 In the last paragraph, delete the first sentence.

3.8.1, 3-21 Delete Section 3.8.1.

3.13, 3-27 Table 3-27, replace the seventh through eleventh rows with the following:

Uart_Sel		Switch or I2C		6	SW3(2)	1 = Uart_Sel
Reserved		Switch or I2C		7	SW3(1)	1 = Reserved
User-defined	USERMODE(0:1)	Switch or I2C	0x25	1–0	SW2(8:7)	00 = User defined
Reserved		Switch or I2C		2	SW2(6)	1 = Reserved [1]
Reserved		Switch or I2C		3	SW2(5)	1 = Reserved

3.13, 3-28 Table 3-27, replace the fourth from the bottom row with the following:

Reserved		Switch or I2C		5	SW1(3)	1 = Reserved [2]

3.13, 3-28 Table 3-27, add the following notes to the end of the table:

Notes:

1. SW1(3) for Configuration 2 is PCI CLK SEL and must be set to 1.
2. SW2(6) for Configuration 2 is PCI Select PCI = 1 and PCIX = 0.

3.14.1, 3-30 Delete Section 3.14.1 and Table 3-29. Renumber remaining sections and tables.

5.5.4, 5-12 In Table 5-7, for Slots #2, #3, #4, and #5, the Slot 5 information has changed in the ‘Attached Devices by Connection’ column. Replace these rows with the following:

Slot #2	INTA#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	2
	INTB#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	
	INTC#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	
	INTD#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	
Slot #3	INTA#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	2
	INTB#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	
	INTC#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	
	INTD#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	
Slot #4	INTA#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	2
	INTB#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	
	INTC#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	
	INTD#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	
Slot #5	INTA#	$\overline{\text{PCIA1\_INT3}}$	Slot2 INTD# | Slot3 INTC# | Slot4 INTB# | Slot 5 INTD#	2
	INTB#	$\overline{\text{PCIA1\_INT0}}$	Slot2 INTA# | Slot3 INTD# | Slot4 INTC# | Slot 5 INTA#	
	INTC#	$\overline{\text{PCIA1\_INT1}}$	Slot2 INTB# | Slot3 INTA# | Slot4 INTD# | Slot 5 INTB#	
	INTD#	$\overline{\text{PCIA1\_INT2}}$	Slot2 INTC# | Slot3 INTB# | Slot4 INTA# | Slot 5 INTC#	

5.5.6, 5-15 In Table 5-9, replace the last nine rows with the following:

RTK8139 Ethernet	B4	21	
VIA 82C686B	B4	20	
Slot 6	B4	22	
Slot 7	B4	23	
Primary PCI bridge	A	28	
Slot 2	A	20	
Slot 3	A	21	
Slot 4	A	22	
Slot 5	A	24	

5.7, 5-18 In the first paragraph after Table 5-9, replace the second sentence with the following:

The M66EN signal is used to select 33 or 66 MHz, while PCIXCAP is used to select between PCI and PCI-X mode, as well as for 66-MHz operation.

Appendix C, C-1 Replace title and paragraph as follows:

Appendix C
CDS Carrier BOM, Rev. 1.2

This appendix provides CDS Carrier BOM for Rev. 1.2.

Appendix D, D-1 — Replace title and paragraph as follows:

Appendix D
CDS Carrier Schematics, Rev. 1.2

This appendix provides CDS Carrier board schematics for Rev. 1.2.

Appendix E, E-1 — Add new appendices E and F (renumber remaining appendices):

Appendix E
CDS Carrier BOM, Rev. 1.3

This appendix provides CDS Carrier BOM for Rev. 1.3.

Appendix F
CDS Carrier Schematics, Rev. 1.3

This appendix provides CDS Carrier board schematics for Rev. 1.3.

Appendix B
Pinouts

B.1 Carrier/DaughterCard Connectors Pinout

Table B-1. Daughtercard Connector (Left) Definition and Pinout

Pin	A	B	C	D	E	F	G	H	J	K
1	GND		U1_SI	GND	PA0	PA1	GND	PA2	PA3	VCC_2.5
2	U1_TP	VCC_2.5	U1_SO	U2_SI	GND	PA4	PA5	GND	PA6	PA7
3	U1_TN	U1_OC	GND	U2_SO	PA8	GND	PA9	PA10	VCC_2.5	PA11
4	VCC_2.5	U2_OC	U1_RTS	GND	PA12	PA13	GND	PA14	PA15	GND
5	U2_TP	GND	U1_CTS	U2_RTS	GND	PA16	PA17	VCC_2.5	PA18	PA19
6	U2_TN		VCC_2.5	U2_CTS	PA20	GND	PA21	PA22	GND	PA23
7	GND	TS1_0	TS1_1	GND	PA24	PA25	GND	PA26	PA27	VCC_2.5
8	TS1_2	VCC_2.5	TS1_3	TS1_4	GND	PA28	PA29	GND	PA30	PA31
9	TS1_5	TS1_6	GND	TS1_7	PB4	GND	PB5	PB6	VCC_2.5	PB7
10	VCC_2.5	TS1_8	TS1_9	GND	PB8	PB9	GND	PB10	PB11	GND
11	TS1_10	GND	TS1_11	TS1_12	GND	PB12	PB13	VCC_2.5	PB14	PB15
12	TS1_13	TS1_14	VCC_2.5	TS1_15	PB16	GND	PB17	PB18	GND	PB19
13	GND	TS1_16	TS1_17	GND	TS1_18	PB20	GND	PB21	PB22	VCC_2.5
14	TS1_19	VCC_2.5	TS1_20	TS1_21	GND	PB23	PB24	GND	PB25	PB26
15	TS1_22	TS1_23	GND	TS1_24	PB27	GND	PB28	PB29	VCC_2.5	PB30
16	VCC_2.5	TS2_0	TS2_1	GND	TS2_2		GND		PB31	GND
17	TS2_3	GND	TS2_4	TS2_5	GND			VCC_2.5		SLEEP
18	TS2_6	TS2_7	VCC_2.5	TS2_8	TS2_9	GND		MDIO	GND	PCICLK[2]
19	GND	TS2_10	TS2_11	GND	TS2_12		GND	MDC	UDE	VCC_3.3
20	TS2_13	VCC_2.5	TS2_14	TS2_15	GND		GTXCLK	GND		PCICLK2
21	TS2_16	TS2_17	GND	TS2_18	TS2_19	GND			VCC_3.3	AD57
22	VCC_2.5	TS2_20	TS2_21	GND	TS2_22		GND	AD43	AD50	GND
23	TS2_23	GND	TS2_24	TS3_0	GND			VCC_3.3	AD51	AD58
24	TS3_1	TS3_2	GND	TS3_3	TS3_4	GND		AD44	GND	AD59
25	GND	TS3_5	TS3_6	GND	TS3_7	PERR	GND	AD45	AD52	VCC_3.3
26	TS3_8	VCC_2.5	TS3_9	TS3_10	GND	AD32	PAR64	GND	AD53	AD60
27	TS3_11	TS3_12	GND	TS3_13	TS3_14	GND	AD36	AD46	VCC_3.3	AD61
28	VCC_2.5	TS3_15	TS3_16	GND	TS3_17	AD33	GND	AD47	AD54	GND
29	TS3_18	GND	TS3_19	TS3_20	GND	AD34	AD37	VCC_3.3	AD55	AD62
30	TS3_21	TS3_22	VCC_3.3	TS3_23	TS3_24	GND	AD38	AD48	GND	AD63

Table B-1. Daughtercard Connector (Left) Definition and Pinout (continued)

Pin	A	B	C	D	E	F	G	H	J	K
31	GND		AD31	GND	PAR	AD35	GND	AD49	AD56	VCC_3.3
32	GNT#	VCC_3.3	AD30	C_BE0	GND	C_BE3	AD39	GND	AD11	AD5
33	REQ#	GNT64#	GND	C_BE1	C_BE2	GND	AD40	C_BE6	VCC_3.3	AD4
34	VCC_3.3	REQ64#	AD29	GND	AD20	IDSEL	GND	C_BE4	AD10	GND
35	M66EN	GND	AD28	AD24	GND	DEVSEL	AD41	VCC_3.3	AD9	AD3
36	PCIXCAP	SERR#	VCC_3.3	AD23	AD19	GND	AD42	AD15	GND	AD2
37	GND	STOP#	AD27	GND	AD18	TRDY	GND	AD14	AD8	VCC_3.3
38	+12V	VCC_3.3	AD26	AD22	GND	IRDY	C_BE7	GND	AD7	AD1
39	+12V	LOCK#	GND	AD21	AD17	GND	C_BE5	AD13	VCC_3.3	AD0
40	VCC_3.3	SYSCLK[1]	AD25	GND	AD16	FRAME	GND	AD12	AD6	GND

NOTES:

1) Was PCICLK on V1.0 carriers.

2) Was SYSCLK on V1.0 carriers.

Table B-2. Daughtercard Connector (Right) Definition and Pinout

Pin	A	B	C	D	E	F	G	H	J	K
1	GND	PC0	PC1	GND	PC2	PC3	GND	CX0	CX1	VCC_2.5
2	PC4	VCC_2.5	PC5	PC6	GND	PC7	PC8	GND	CX3	CX4
3	PC9	PC10	GND	PC11	PC12	GND	PC13	CX5	VCC_2.5	CX6
4	VCC_2.5	PC14	PC15	GND	PC16	PC17	GND	CX7	CX8	GND
5	PC18	GND	PC19	PC20	GND	PC20	PC21	VCC_2.5	CX9	CX10
6	PC22	PC23	VCC_2.5	PC24	PC25	GND	PC26	CX11	GND	CX12
7	GND	PC27	PC28	GND	PC29	PC30	GND	CX13	CX14	VCC_2.5
8	PC31	VCC_2.5			GND		PD4	GND	CX15	CX16
9	PD5	PD6	GND	PD7	PD8	GND	PD9	CX17	VCC_2.5	CX18
10	VCC_2.5	PD10	PD11	GND	PD12	PD13	GND	CX19	CX20	GND
11	PD14	GND	PD15	PD16	GND	PD17	PD18	VCC_2.5	CX21	CX22
12	PD19	PD20	VCC_2.5	PD21	PD22	GND	PD23	CX23	GND	CX24
13	GND	PD24	PD25	GND	PD26	PD27	GND	CX25	CX26	VCC_2.5
14	PD28	VCC_2.5	PD29	PD30	GND	PD31	CX35	GND	CX27	CX28
15	CX29	CX30	GND	CX31	CX32	GND	CX33	CX34	VCC_2.5	CX35
16	VCC_2.5	CX36	CX37	GND	CX38	CX39	GND	CX40	CX41	GND
17	CX42	GND	CX43	CX44	GND	CX45	CX46	VCC_2.5	CX47	CX48
18	CX49	CX50	VCC_2.5	CX51	CX52	GND	CX53	CX54	GND	CX55
19	GND	CX56	CX57	GND	CX58		GND	CX59		VCC_2.5
20		VCC_3.3		LBCTL	GND	LB_OE	LALE3	GND		LCLK1
21	OVM		GND	LB_GP0	LB_CS7	GND	LALE2	LALE0	VCC_3.3	LCLK0
22	VCC_3.3			GND	LB_CS6	LB_A0	GND	LB_W3	LB_W2	GND
23	SRESET	GND		LB_GP1	GND	LB_A1	LALE1	VCC_3.3	LB_W1	LB_W0
24	HRESET		VCC_3.3	LB_GP2	LB_CS5	GND	LB_A8	LB_A14	GND	LB_A26
25	GND	HR_REQ	DMACK1	GND	LB_CS4	LB_A2	GND	LB_A15	LB_A20	VCC_3.3

Table B-2. Daughtercard Connector (Right) Definition and Pinout (continued)

Pin	A	B	C	D	E	F	G	H	J	K
26	PCIRST#	VCC_3.3	DMACK0	LB_GP3	GND	LB_A3	LB_A9	GND	LB_A21	LB_A27
27	CFGRST	DMADN1	GND	LB_GP4	LB_CS3	GND	LB_A10	LB_A16	VCC_3.3	LB_A28
28	VCC_3.3	DMADN0	DMARQ1	GND	LB_CS2	LB_A4	GND	LB_A17	LB_A22	GND
29	MCP	GND	DMARQ0	LB_GP5	GND	LB_A5	LB_A11	VCC_3.3	LB_A23	LB_A29
30	INT13	INT14	VCC_3.3		LB_CS1	GND	LB_A12	LB_A18	GND	LB_A30
31	GND	INT11	INT15	GND	LB_CS0	LB_A6	GND	LB_A19	LB_A24	VCC_3.3
32	INT10	VCC_3.3	INT12	LB_DP0	GND	LB_A7	LB_A13	GND	LB_A25	LB_A31
33	INT7	INT8	GND	LB_DP1	LB_D0	GND	LB_D11	LB_D16	VCC_3.3	LB_D27
34	VCC_3.3	INT5	INT9	GND	LB_D1	LB_D6	GND	LB_D17	LB_D22	GND
35	INT4	GND	INT6	LB_DP2	GND	LB_D7	LB_D12	VCC_3.3	LB_D23	LB_D28
36	INT0	INT1	VCC_3.3	LB_DP3	LB_D2	GND	LB_D13	LB_D18	GND	LB_D29
37	GND	INT2	INT3	GND	LB_D3	LB_D8	GND	LB_D19	LB_D24	VCC_3.3
38	RTC	VCC_3.3	PCIRED	LB_SIZ0	GND	LB_D9	LB_D14	GND	LB_D25	LB_D30
39	PWRGD	CFGDRV	GND	LB_SIZ1	LB_D4	GND	LB_D15	LB_D20	VCC_3.3	LB_D31
40	VCC_3.3	SDA	SCK	GND	LB_D5	LB_D10	GND	LB_D21	LB_D26	GND

Table B-3. Daughtercard High-Speed Connector Definition and Pinout

	A	B	C
1	HS_A2p	GND	HS_A1p
2	HS_B2n	GND	HS_B1n
3	GND	GND	GND
4	HS_C2p	GND	HS_C1p
5	HS_D2n	GND	HS_D1n
6	GND	GND	GND
7	HS_A4p	GND	HS_A3p
8	HS_B4n	GND	HS_B3n
9	GND	GND	GND
10	HS_C4p	GND	HS_C3p
11	HS_D4n	GND	HS_D3n
12	GND	GND	GND
13	HS_A6p	GND	HS_A5p
14	HS_B6n	GND	HS_B5n
15	GND	GND	GND
16	HS_C6p	GND	HS_C5p
17	HS_D6n	GND	HS_D5n
18	GND	GND	GND
19	HS_A8p	GND	HS_A7p
20	HS_B8n	GND	HS_B7n
21	GND	GND	GND
22	HS_C8p	GND	HS_C7p

Table B-3. Daughtercard High-Speed Connector Definition and Pinout (continued)

	A	B	C
23	HS_D8n	GND	HS_D7n
24	GND	GND	GND
25	HS_A10p	GND	HS_A9p
26	HS_B10n	GND	HS_B9n
27	GND	GND	GND
28	HS_C10p	GND	HS_C9p
29	HS_D10n	GND	HS_D9n
30	GND	GND	GND
31	HS_E2p	GND	HS_E1p
32	HS_F2n	GND	HS_F1n
33	GND	GND	GND
34	HS_G2p	GND	HS_G1p
35	HS_H2n	GND	HS_H1n
36	GND	GND	GND
37	HS_E4p	GND	HS_E3p
38	HS_F4n	GND	HS_F3n
39	GND	GND	GND
40	HS_G4p	GND	HS_G3p
41	HS_H4n	GND	HS_H3n
42	GND	GND	GND
43	HS_E6p	GND	HS_E5p
44	HS_F6n	GND	HS_F5n
45	GND	GND	GND
46	HS_G6p	GND	HS_G5p
47	HS_H6n	GND	HS_H5n
48	GND	GND	GND
49	HS_E8p	GND	HS_E7p
50	HS_F8n	GND	HS_F7n
51	GND	GND	GND
52	HS_G8p	GND	HS_G7p
53	HS_H8n	GND	HS_H7n
54	GND	GND	GND
55	HS_E10p	GND	HS_E9p
56	HS_F10n	GND	HS_F9n
57	GND	GND	GND
58	HS_G10p	GND	HS_G9p
59	HS_H10n	GND	HS_H9n
60	GND	GND	GND
61		GND	
62		GND	

Table B-3. Daughtercard High-Speed Connector Definition and Pinout (continued)

	A	B	C
63	GND	GND	GND
64	HS_X2p	GND	HS_X1p
65	HS_X2n	GND	HS_X1n
66	GND	GND	GND
67	HS_X4p	GND	HS_X3p
68	HS_X4n	GND	HS_X3n
69	GND	GND	GND
70		GND	
71		GND	
72	GND	GND	GND
73		GND	
74		GND	
75	GND	GND	GND
76		GND	
77		GND	
78	GND	GND	GND
79		GND	
80		GND	
81	GND	GND	GND
82		GND	
83		GND	
84	GND	GND	GND
85		GND	
86		GND	
87	GND	GND	GND
88	HSCLKp	GND	
89	HSCLKn	GND	
90	GND	GND	GND

B.2 IOCard Connector Pinout

Table B-4. IOCard Connector Definition and Pinout

Pin	A	B	C	D	E
1	T3_TXIP_A	GND	T3_TXIP_B	VCC_3.3	T3_LED1A
2	T3_TXIN_A	GND	T3_TXIN_B	VCC_3.3	T3_LED1C
3	GND	GND	GND	VCC_3.3	T3_LED2A
4	T3_TXIP_C	GND	T3_TXIP_D	VCC_3.3	T3_LED2C
5	T3_TXIN_C	GND	T3_TXIN_D	VCC_3.3	T3_LED3A
6	GND	GND	GND	VCC_3.3	T3_LED3C

Table B-4. IOCard Connector Definition and Pinout (continued)

Pin	A	B	C	D	E
7		GND	EVENT1	VCC_3.3	T3_LED4A
8		GND	EVENT2	VCC_3.3	T3_LED4C
9	GND	GND	GND	VCC_3.3	GND
10	T4_TXIP_A	GND	T4_TXIP_B	VCC_3.3	T4_LED1A
11	T4_TXIN_A	GND	T4_TXIN_B	VCC_5	T4_LED1C
12	GND	GND	GND	VCC_5	T4_LED2A
13	T4_TXIN_C	GND	T4_TXIP_D	VCC_5	T4_LED2C
14	T4_TXIN_C	GND	T4_TXIN_D	VCC_5	T4_LED3A
15	GND	GND	GND	VCC_5	T4_LED3C
16		GND		VCC_5	T4_LED4A
17		GND		GND	T4_LED4C
18	GND	GND	GND	GND	GND
19	U1_TN	GND	U2_TN	GND	U1_OC
20	U1_TP	GND	U2_TP	GND	U2_OC

B.3 uTCOM Connector Pinout

Table B-5. uTCOM Connector (Right) Definition and Pinout

Pin	A	B	C	D	E	F	G	H	J	K
1	PA0	PA16	GND	PB16	PC0	VCC_5		PD16	GND	CX16
2	PA1	GND		PB17	VCC_3.3	PC16		GND		CX17
3	GND	PA17		VCC_3.3	PC1	PC17	GND	PD17		VCC_5
4	PA2	PA18	VCC_3.3	PB18	PC2	GND		PD18	VCC_5	CX18
5	PA3	VCC_3.3		PB19	GND	PC18		VCC_5		CX19
6	VCC_3.3	PA19		GND	PC3	PC19	VCC_5	PD19		GND
7	PA4	PA20	GND	PB20	PC4	VCC_5	PD4	PD20	GND	CX20
8	PA5	GND	PB4	PB21	VCC_3.3	PC20	PD5	GND	CX4	CX21
9	GND	PA21	PB5	VCC_3.3	PC5	PC21	GND	PD21	CX5	VCC_5
10	PA6	PA22	VCC_3.3	PB22	PC6	GND	PD6	PD22	VCC_5	CX22
11	PA7	VCC_3.3	PB6	PB23	GND	PC22	PD7	VCC_5	CX6	CX23
12	VCC_3.3	PA23	PB7	GND	PC7	PC23	VCC_5	PD23	CX7	GND
13	PA8	PA24	GND	PB24	PC8	VCC_5	PD8	PD24	GND	CX24
14	PA9	GND	PB8	PB25	VCC_3.3	PC24	PD9	GND	CX8	CX25
15	GND	PA25	PB9	VCC_3.3	PC9	PC25	GND	PD25	CX9	VCC_5
16	PA10	PA26	VCC_3.3	PB26	PC10	GND	PD10	PD26	VCC_5	CX26
17	PA11	VCC_3.3	PB10	PB27	GND	PC26	PD11	VCC_5	CX10	CX27
18	VCC_3.3	PA27	PB11	GND	PC11	PC27	VCC_5	PD27	CX11	GND
19	PA12	PA28	GND	PB28	PC12	VCC_5	PD12	PD28	GND	CX28
20	PA13	GND	PB12	PB29	VCC_3.3	PC28	PD13	GND	CX12	CX29

Table B-5. uTCOM Connector (Right) Definition and Pinout (continued)

Pin	A	B	C	D	E	F	G	H	J	K
21	GND	PA29	PB13	VCC_3.3	PC13	PC29	GND	PD29	CX13	VCC_5
22	PA14	PA30	VCC_3.3	PB30	PC14	GND	PD14	PD30	VCC_5	CX30
23	PA15	VCC_3.3	PB14	PB31	GND	PC30	PD15	VCC_5	CX14	CX31
24	VCC_3.3	PA31	PB15	GND	PC15	PC31	VCC_5	PD31	CX15	GND
25	SDA		GND			VCC_5			GND	
26	SCK	GND			VCC_3.3			GND		
27	GND			VCC_3.3			GND			VCC_5
28	MDIO		VCC_3.3			GND			VCC_5	LB_A8
29	MDC	VCC_3.3			GND		LB_D0	VCC_5	LB_A0	LB_A9
30	VCC_3.3			GND			VCC_5	LB_D8	LB_A1	GND
31	LB_GP0		GND			VCC_5	LB_D1	LB_D9	GND	LB_A10
32	LB_GP1	GND	INT6		VCC_3.3		LB_D2	GND	LB_A2	LB_A11
33	GND		INT7	VCC_3.3			GND	LB_D10	LB_A3	VCC_5
34	LB_GP2		VCC_3.3	LB_W3		GND	LB_D3	LB_D11	VCC_5	LB_A12
35	LB_GP3	VCC_3.3		LB_W2	GND		LB_D4	VCC_5	LB_A4	LB_A13
36	VCC_3.3	LB_CS7		GND			VCC_5	LB_D12	LB_A5	GND
37	LB_GP4	LB_CS6	GND	LB_W1		VCC_5	LB_D5	LB_D13	GND	LB_A14
38	LB_GP5	GND		LB_W0	VCC_3.3		LB_D6	GND	LB_A6	LB_A15
39	GND	PWRGD	CFGDRV	VCC_3.3			GND	LB_D14	LB_A7	VCC_5
40	TCMRST	CFGRST	VCC_3.3	LBCTL	LALE0	GND	LB_D7	LB_D15	VCC_5	LCLK0

Appendix C
CDS Carrier BOM, Rev. 1.2

This appendix provides CDS Carrier BOM for Rev. 1.2.

Board Station BOM file
Date : NOV 1 2005
Variant : CDS_Carrier rev 1.2
Line item 68, J12, is now a NO POP component

BOM CDS Carrier rev 1.2a updated 12_MAY_05
BOM CDS Carrier rev 1.2B updated 1_SEP_05
BOM CDS Carrier rev 1.2C updated 1_NOV_05

ITEM_NO	COMPANY PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1		pcb_carrier	1		
2	1-1605458-1	conn_rj45_mag_led	2	conn.rj45_cat5_mag_led.ra, TransPower	J6 J8
3	103167-2	header_ra_2x5	1	header.ra.2x5, AMP	J1
4	103309-1	header_2x5_shrouded	1	header.2x5, AMP	J2
5	105-1089-00		3	Latch_Housing_Tektronix	
6	1210YG106ZAT2A	cc1210	9	cap, 10uF, AVX	C117 C162 C165 C255 C257 C282 C298 C300 C302
7	1469001-1	conn_hmzd40pr_recpt_ra	1	conn.amp.HMZd.40pr.recpt.ra, Tyco	P7
8	218-8LPST	sw_som16	4	sw.8spst.cts, CTS	SW1 SW2 SW3 SW4
9	223961-1	conamp_223961-1	2	conn.pwr.3pos.ra, AMP	P5 P6
10	223986-1	guide_mod	2	guide_module.keyed.ra, AMP	GM1 GM2
11	293D105X9016A2T	cct3216	2	cap_tant, 1uF, SPRAGUE	C2 C96
12	293D106X9016C2T	cct6032	2	cap_tant, 10uF, SPRAGUE	C60 C69
13	293D226X9016C2T	cct6032	5	cap_tant, 22uF, SPRAGUE	C1 C15 C83 C196 C285
14	293D476X9016D2T	cct7343	1	cap_tant, 47uF, SPRAGUE	C132
15	597-5112-40X	led_0603	12	led, Dialight, Red	D1 D2 D3 D4 D5 D6 D7 D8 D11 D12 D13 D14
16	597-5312-40X	led_0603	2	led, Dialight, Green	D9 D10
17	74390-001	connFCI_recp_10x40_sm	3	conn.megarray.10x40.1of5, FCI	J3 J10 J11
18	767054-1	conn_mictor38	3	conn.mictor.38, Amp	J14 J16 J17
19	AM29LV641DH120REI	tsop48w	2	am29lv641d.tsop48w, AMD	U49 U54

20	APA150-FG256	fbga256	1	apa150.1of2.fbga256, ACTEL	U24
21	AT24C64AN-10SI-2.7	so8	1	at24c64a.s08, ATMEL	U1
22	CY7B9950AC	tqfp32	1	cy7b9950ac.tqfp32, CYPRESS	U50
23	DEM9PL	conn_db9_plg_ra	1	conn.db9.plug.rta, ITT Cannon	J15
24	DS1553WP-120	pcm34	1	ds1553wp_120.pcm34, DallasSemi	U51
25	DS1834S	so8	2	ds1834s.so8, DALLAS SEMI.	U34 U37
26	DS9034PCX		1	POWERCAP	
27	E13W1F2C-77.760M	osc_smd_e13j1	1	osc.3_3v.diff.smd, 77.760MHz, ECLIPTEK	U22
28	EEFUE0G221R	cc_7.3x4.3_ue	19	cap_tant, 220uF, PANASONIC	C18 C62 C86 C87 C91 C127 C135 C136 C146 C192 C193 C208 C212 C278 C289 C291 C292 C297 C306
29	EH2645TS-125.000M	osc_smd_5x7mm	1	osc.3_3v.smd, 125.00MHz, ECLIPTEK	Y1
30	EH2645TS-16.000M	osc_smd_5x7mm	1	osc.3_3v.smd, 16.000MHz, ECLIPTEK	U44
31	EH2645TS-19.440M	osc_smd_5x7mm	1	osc.3_3v.smd, 19.440MHz, ECLIPTEK	U27
32	ETQP6F1R1BFA	inductor_12.5x12.5	2	inductor, 1.1uH, Panasonic	L1 L2
33	FTR-125-01-S-D	header_2x25_05sp_smt	1	header_2x25_05sp, Samtec	J13
34	FTSH-113-01-L-DV-K	conn_2x13_050_sma	1	conn.2x13, Samtec	J9
35	G3B15AH-x-XA	sw_sm_spdt_ra	1	sw.1spdt, NKK	SW5
36	HFBR-5208M	1x9mezz	1	hfbr_5xxx.1x9mezz, AGILENT	U12
37	HFBR-5805	1x9mezz	1	hfbr_5xxx.1x9mezz, AGILENT	U13
38	HI1206N101R-00	ferrite_1206	7	ferrite_bead_1206, Steward	FB1 FB2 FB3 FB4 FB5 FB6 FB7
39	ICS525R-02I	ssop28_pit635mm	1	ics525_02.ssop28, ICS	U42
40	IDTQS3VH16233PA	tssop56	6	idtqs3vh16233pa.tssop56, IDT	U7 U8 U17 U18 U20 U21
41	IDTQS3VH257PA	tssop16	2	idtqs3vh257.tssop16, IDT	U19 U41
42	IRF6604	irf6604	1	irf66xx.dirfet, IRF	Q2
43	IRF6607	irf6607	1	irf66xx.dirfet, IRF	Q1
44	LMK107F105ZA	cc0603	9	cap, 1.0uF, TAIYO_YUDEN	C34 C35 C55 C90 C128 C129 C134 C304 C305
45	LT1331CG	ssop28	2	lt1331cg.ssop28, Linear	U16 U47
46	LT1587CM-1.5	ddpak3	1	lt1587-1.5v.ddpak3, Linear Technology	U31
47	LTC4300-1CMS8	ms8	1	ltc4300_1.ms8, Linear Tech	U2

48	MAX4372FEUK-T	sot23_5p	1	max4372f.sot23_5, Maxim	U14
49	MBRS140T3	smb_403a	1	mbrs140t3.smb, MOT	CR1
50	MCCA101K0NRT	cc0402	1	cap, 100pF, SMEC	C54
51	MCCA104K0NRT	cc0402	240	cap, 0.1uF, SMEC	C3 C5 C7 C8 C11 C13 C16 C19 C20 C22 C24 C25 C27 C29 C32 C36 C37 C39 C41 C42 C43 C45 C46 C47 C48 C50 C51 C53 C57 C58 C66 C67 C68 C70 C71 C72 C76 C77 C78 C79 C82 C84 C85 C88 C89 C92 C93 C94 C95 C97 C100 C102 C105 C107 C108 C110 C111 C112 C113 C114 C115 C116 C118 C119 C120 C121 C122 C123 C124 C125 C130 C131 C137 C141 C142 C143 C144 C145 C147 C148 C149 C150 C151 C152 C153 C154 C155 C156 C157 C159 C160 C161 C163 C164 C166 C167 C168 C169 C170 C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 C181 C182 C183 C184 C185 C186 C187

C188 C189 C190
C191 C194 C195
C197 C199 C200
C201 C202 C203
C204 C205 C206
C207 C209 C210
C213 C214 C215
C216 C217 C218
C219 C220 C221
C222 C223 C224
C225 C226 C227
C228 C229 C230
C231 C232 C233
C236 C237 C238
C239 C240 C241
C242 C243 C244
C245 C246 C248
C249 C250 C251
C252 C253 C256
C258 C259 C260
C261 C262 C263
C264 C265 C266
C267 C268 C269
C270 C271 C272
C273 C274 C275
C276 C277 C279
C280 C281 C283
C284 C287 C288
C294 C295 C296
C299 C301 C303
C309 C311 C312
C313 C314 C315
C316 C317 C318
C319 C320 C321
C322 C323 C324
C325 C326 C327
C328 C329 C330

					C331 C333 C334 C335 C336 C337 C338 C339 C340 C341 C342 C343 C345
52	MCCA470K0NRT	cc0402	3	cap, 47pF, SMEC	C211 C235 C307
53	MCCE102KONRT	cc0402	34	cap, 1000pF, SMEC	C4 C6 C9 C10 C12 C14 C17 C21 C23 C26 C28 C30 C31 C33 C38 C40 C44 C49 C56 C59 C63 C64 C65 C73 C74 C75 C80 C81 C98 C99 C101 C103 C104 C106
54	MCCE103KONRT	cc0402	1	cap, 0.01uF, SMEC	C286
55	MCR10-EZHM-J-5R0	rc0805	1	res, 5, Rohm	R176
56	MMSZ6V2T1	sod_123	1	MMSZ6V2T1.sod123, Motorola	CR2
57	MPC9259FA	lqfp32	1	mpc9259fa.lqfp32, MOTOROLA	U29
58	MPC962308DT-1H	tssop16	2	mpc962308, Freescale	U9 U11
59	NOT_A_COMPONENT	tp_pth	31	test.pth, None	TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40 TP41 TP42 TP43 TP44 TP45 TP46
60	Not_a_component	jump_2x1_1mil	1	splice.1, PCB	SP1
61	P6880	conn_banjo	3	conn.banjo, Tektronix	P1 P3 P4
62	PCA9557PW	tssop16	4	pca9557pw.tssop16, PHILIPS	U48 U52 U53 U55
63	PM5357-B1	sbga304_1.27mm	1	pm5357.main.1of3.sbga304, PMC-SIERRA	U23
64	PM5384NI	stpbga196_1mm	1	pm5384.main.1of2.stpbga196, PMC-SIERRA	U25
65	QSE-020-01-L-D-A	qse_2x20_gnd	2	conn.qse.2x20, SAMTEC	J4 J5

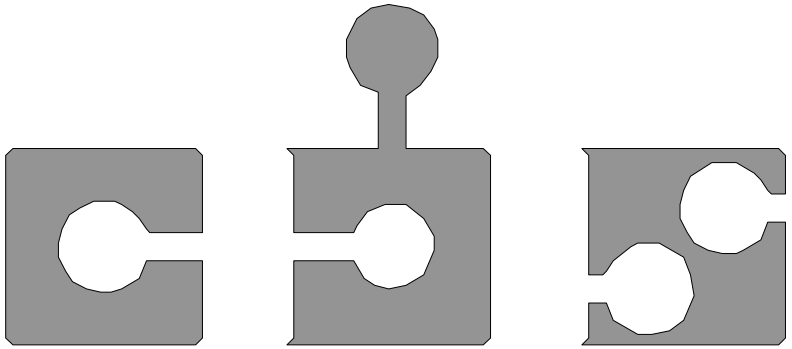
67	RC5051M	sol20	1	rc5051m.so20, Raytheon	U15
68	RC73L2Z000JT	rc0402	29	res, 0, SMEC	R56 R63 R67 R68 R69 R70 R74 R77 R85 R104 R105 R111 R112 R114 R126 R127 R133 R134 R139 R147 R154 R158 R161 R162 R169 R205 R207 R208 R204
69	RC73L2Z100JT	rc0402	5	res, 10, SMEC	R150 R177 R201 R202 R203
70	RC73L2Z101JT	rc0402	17	res, 100, SMEC	R36 R37 R41 R49 R61 R121 R132 R137 R140 R144 R170 R171 R175 R178 R179 R180 R182
71	RC73L2Z102JT	rc0402	3	res, 1K, SMEC	R45 R46 R117
72	RC73L2Z103JT	rc0402	9	res, 10K, SMEC	R75 R119 R122 R123 R124 R125 R128 R129 R130
73	RC73L2Z104JT	rc0402	3	res, 100K, SMEC	R135 R153 R163
74	RC73L2Z181JT	rc0402	4	res, 180, SMEC	R53 R54 R59 R60
75	RC73L2Z202JT	rc0402	1	res, 2K, SMEC	R65
76	RC73L2Z221JT	rc0402	10	res, 220, SMEC	R28 R29 R30 R31 R32 R33 R34 R35 R78 R80
77	RC73L2Z330JT	rc0402	11	res, 33, SMEC	R146 R148 R164 R165 R166 R167 R173 R174 R186 R197 R198
78	RC73L2Z331JT	rc0402	2	res, 330, SMEC	R79 R81
79	RC73L2Z470JT	rc0402	1	res, 47, SMEC	R91
80	RC73L2Z472JT	rc0402	40	res, 4.7K, SMEC	R47 R48 R51 R52 R57 R58 R82 R83 R84 R92 R93 R94

					R95 R96 R103 R115 R118 R136 R141 R142 R143 R151 R152 R155 R156 R157 R168 R183 R184 R185 R189 R190 R191 R192 R193 R194 R195 R196 R199 R200
81	RK73H1ETTP1500F	rc0402	3	res, 150, KOA	R100 R101 R102
82	RK73H1ETTP1580F	rc0402	4	res, 158, KOA	R106 R107 R108 R109
83	RK73H1ETTP15R0F	rc0402	3	res, 15, KOA	R145 R159 R160
84	RK73H1ETTP2001F	rc0402	1	res, 2.00K, KOA	R131
85	RK73H1ETTP2R70F	rc0402	2	res, 2.7, KOA	R116 R138
86	RK73H1ETTP3010F	rc0402	5	res, 301, KOA	R97 R98 R110 R113 R120
87	RK73H1ETTP47R5F	rc0402	35	res, 47.5, KOA	R1 R2 R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 R26 R27 R38 R39 R40 R42 R43 R50 R55 R62
88	RK73H1ETTP49R9F	rc0402	4	res, 49.9, KOA	R86 R87 R88 R89
89	RK73H1ETTP4R70F	rc0402	2	res, 4.7, KOA	R99 R149
90	RNA4A8E102JT	rna4a	4	rnet8.bussed.rna4a, 1K, AVX	RN1 RN5 RN6 RN7
91	RNA4A8E472JT	rna4a	4	rnet8.bussed.rna4a, 4.7K, AVX	RN2 RN3 RN4 RN8
92	SN74CBTLV1G125DBVR	sop5	2	74cbtlv1g125dbv.so5, TI	U56 U57
93	SN74LVC16244ADGG	tssop48	2	74lvc16244adgg.tssop48, TI	U40 U46
94	SN74LVC1G125DCKR	sc70	13	74lvc1g125.sc70, TI	U3 U4 U26 U28 U30 U32 U33 U35 U36 U38 U39 U43 U45
95	SN74LVTH273PW	tssop20	2	74lvth273, TI	U5 U10
96	T510X337M010AS	cct_casee	14	cap_tant, 330uF, Kemet	C52 C61 C126 C133 C138 C139 C140

					C198 C254 C290 C308 C332 C344 C346
97	T510X477M006AS	cct_casee	1	cap_tant, 470uF, Kemet	C310
98	TPSE227K010R0100	cct_casee	3	cap_tant, 220uF, AVX	C234 C247 C293
99	VSC8204VX	pbga388_35x35	1	cis8204.ports.1of3.pbga388, CICADA	U6
100	WSL2512R010F	rc2512	1	res, 0.010, DALE	R44
101	YFS-20-03-H-05-SB-K	header_array_5x20	1	header.5x20.1of3, Samtec	J7
102	pcix_econ_64b_3.3v	econ_pcix64b_3.3v_Signal8_	1	pcix_edgeconn_64bit, MOT	P8
103	screw		2	screw	
		NO POP Components			
	QTH-090-02-F-D-A	qth_2x90_gnd	0	conn.qsh.2x90.1of3, SAMTEC	J12
	RC73L2Z000JT	rc0402	0	res, 0, SMEC	R205,R206
	RC73L2Z330JT	rc0402	0	res, 33, SMEC	R198

Appendix D
CDS Carrier Schematics, Rev. 1.2

This appendix provides CDS carrier board schematics for Rev. 1.2.



Carrier

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:25:20 am	Title: Cover Story	Page: 01

Schematic Notes

1. Unless otherwise specified:
   All resistors are SMD0402, in ohms, 0.08W, +/-5%
   All capacitors are SMD0402, in microfarads (uF), +/-20%.
   All inductances are in microhenries (uH).
   All ferrites are Z=50 ohms at 100 MHz.
   All fuses are self-resetting polyswitch (PTC) devices.
   Board impedance is 55 +/- 5 ohms.

2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:

VCC_3.3	VCC_2.5	GND
VCC_5	VCC_1.2	VCORE

3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.

4.

5. The sheet-to-sheet cross reference format is:
   Sheet VertZoneLetter HorizZoneNumber

6. Components with the label "No_Stuff" are not to be installed by default; they are for test or manufacturing purposes only.

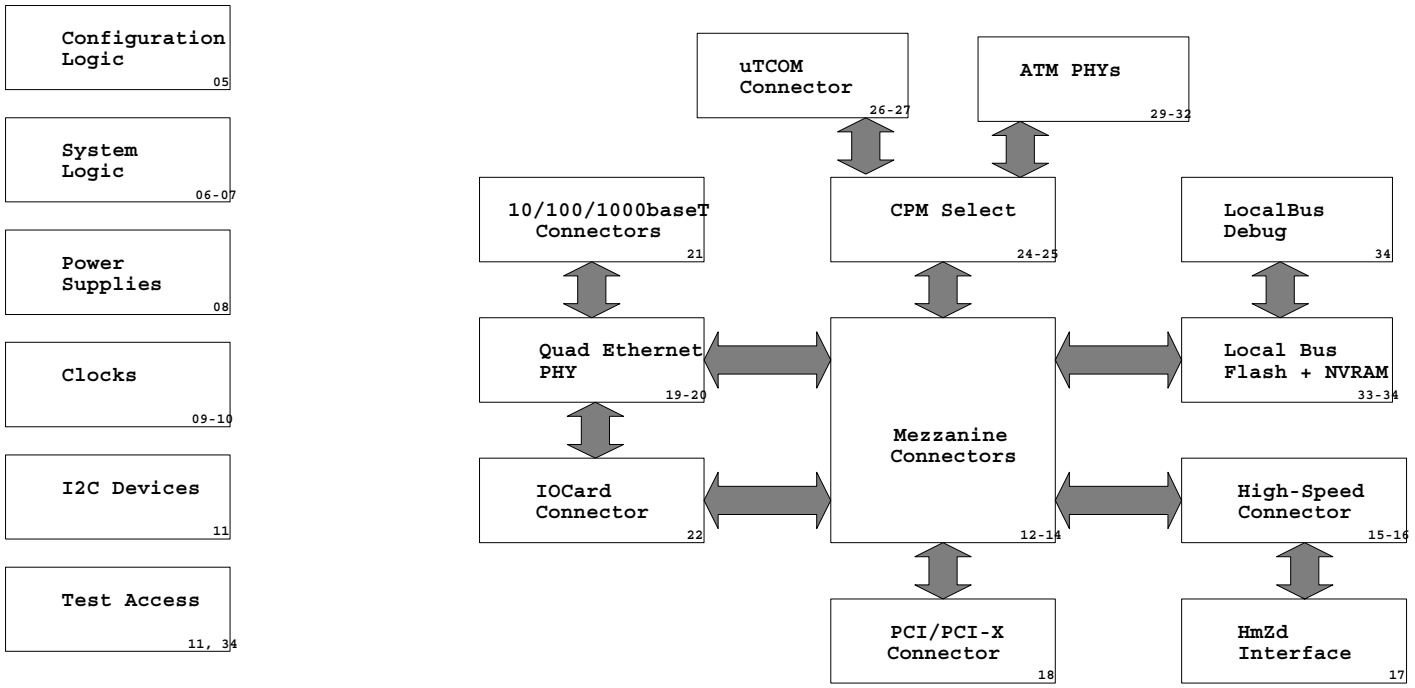
7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

Carrier

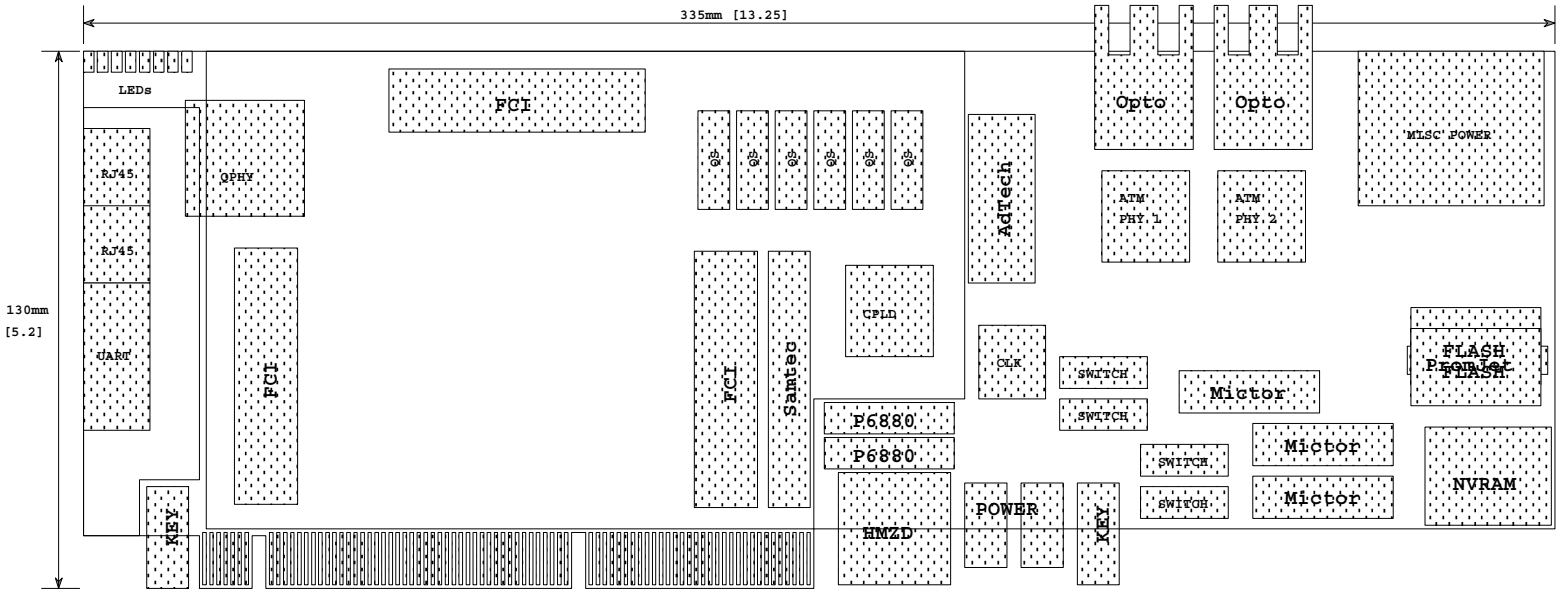
REV	DATE	CHANGES
V1.0	03Nov03	Initial version
V1.1	04Apr08	Errata fix; see errata.
V1.2	04Oct04	Errata fix; see errata.

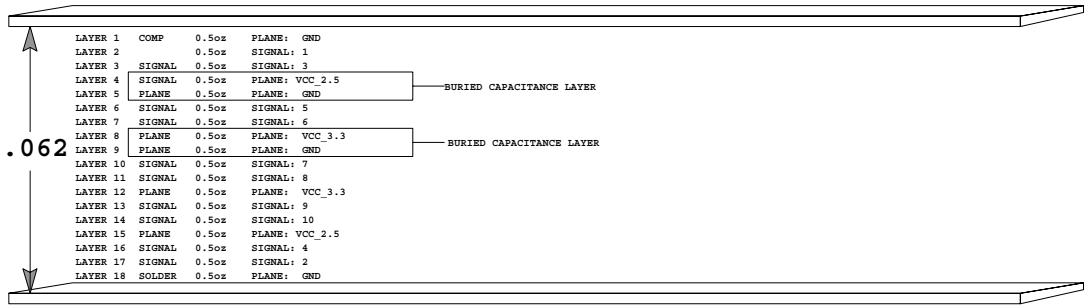
freescale semiconductor
Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

Project: CDS_Carrier
Revision: 1.2
Engineer: Gary Milliorn
Date Changed: 11/8/2005
Time Changed: 10:25:33 am
Title: Information, please

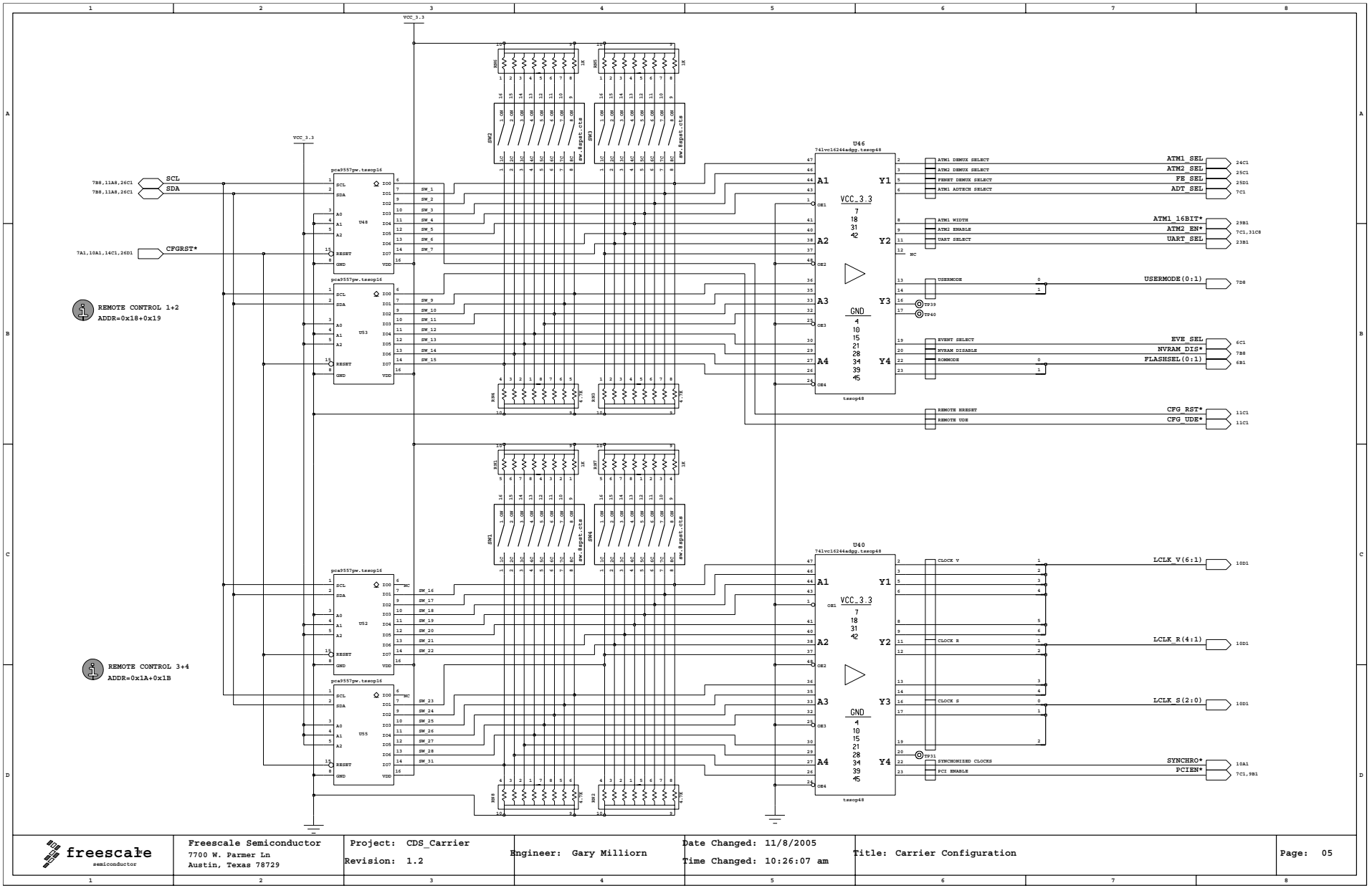


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:25:43 am	Title: Block Diagram	Page: 03

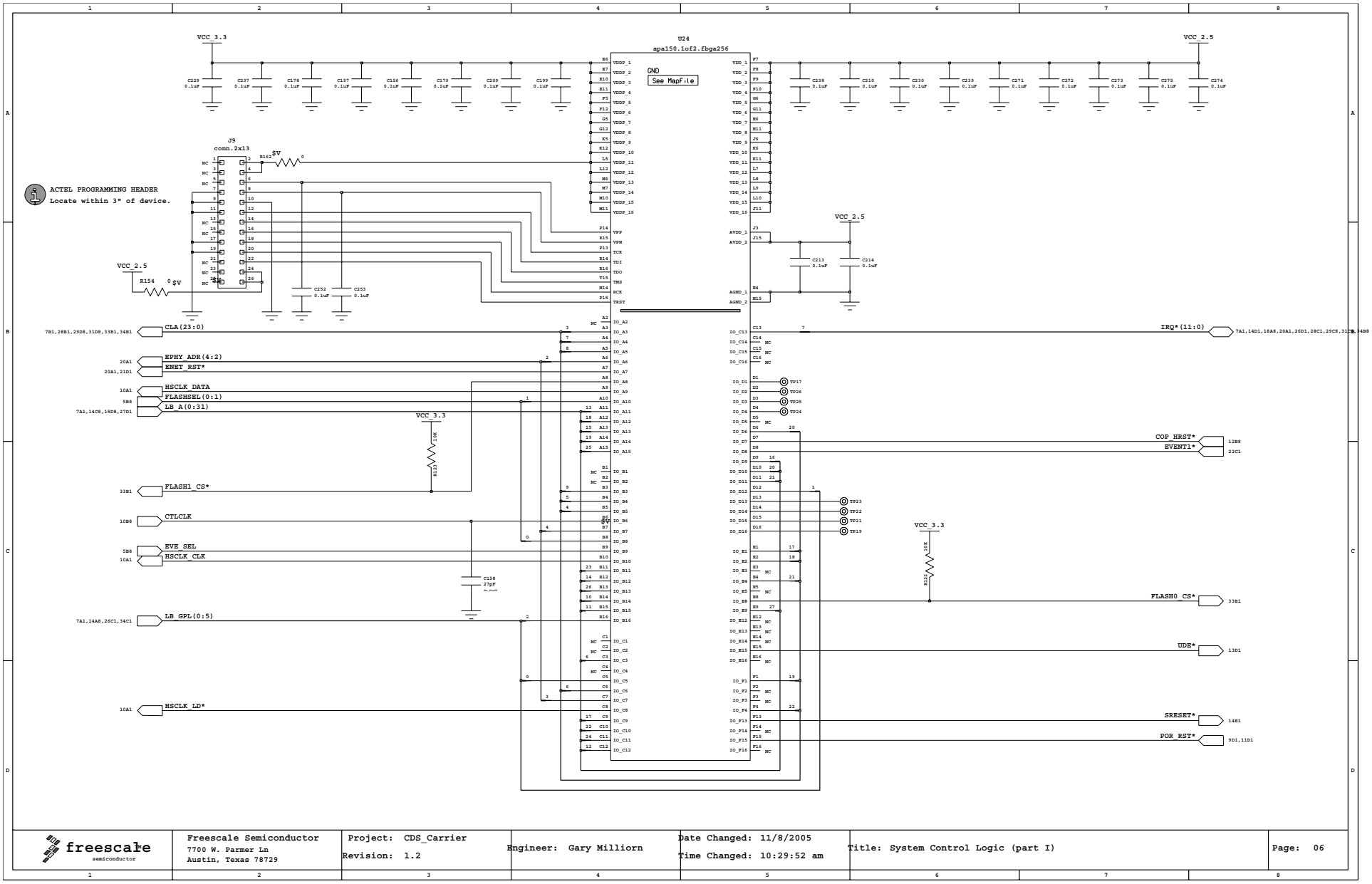




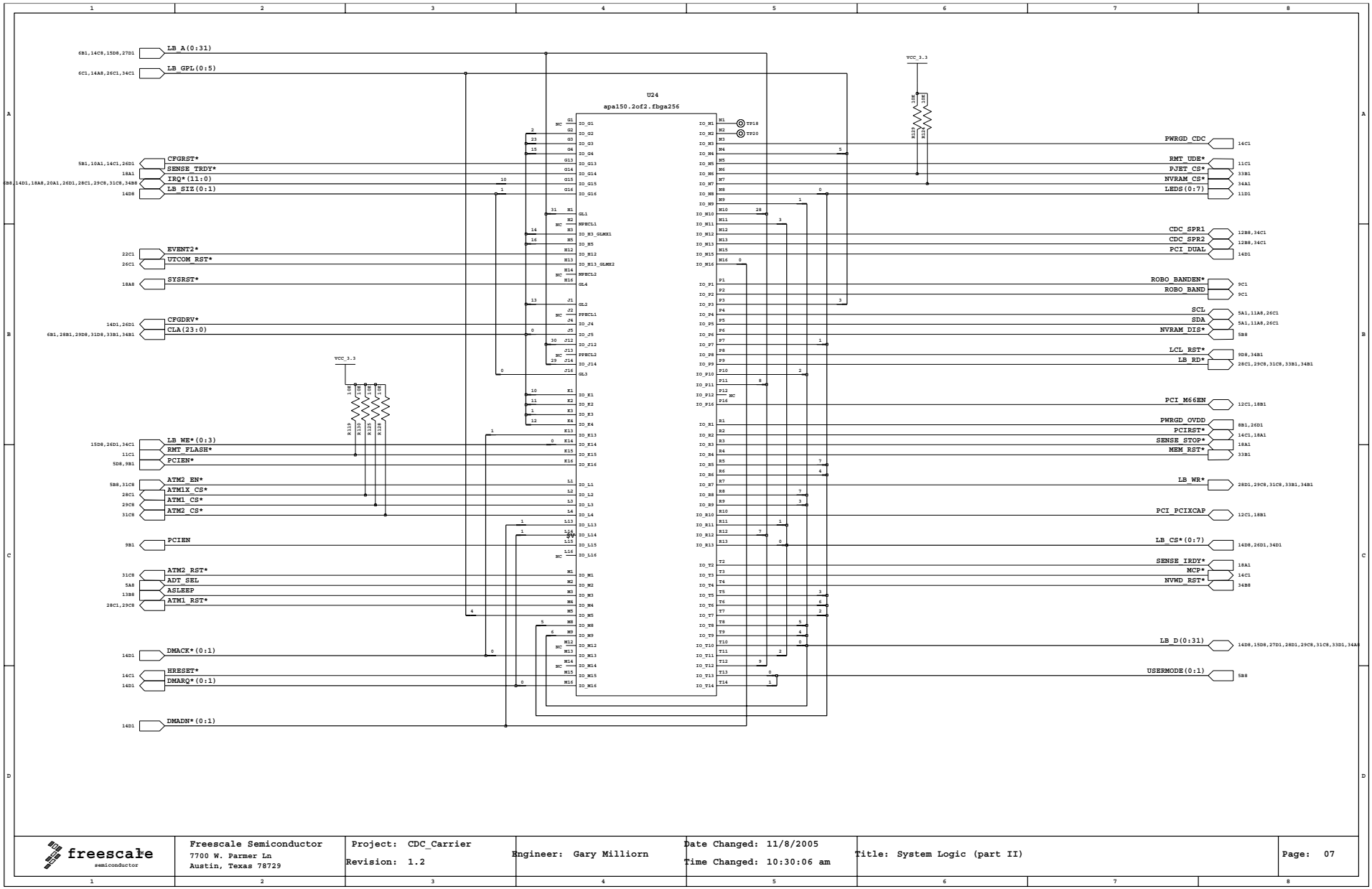
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:25:53 am	Title: Placement (approximate) and PCB Stackup	Page: 04



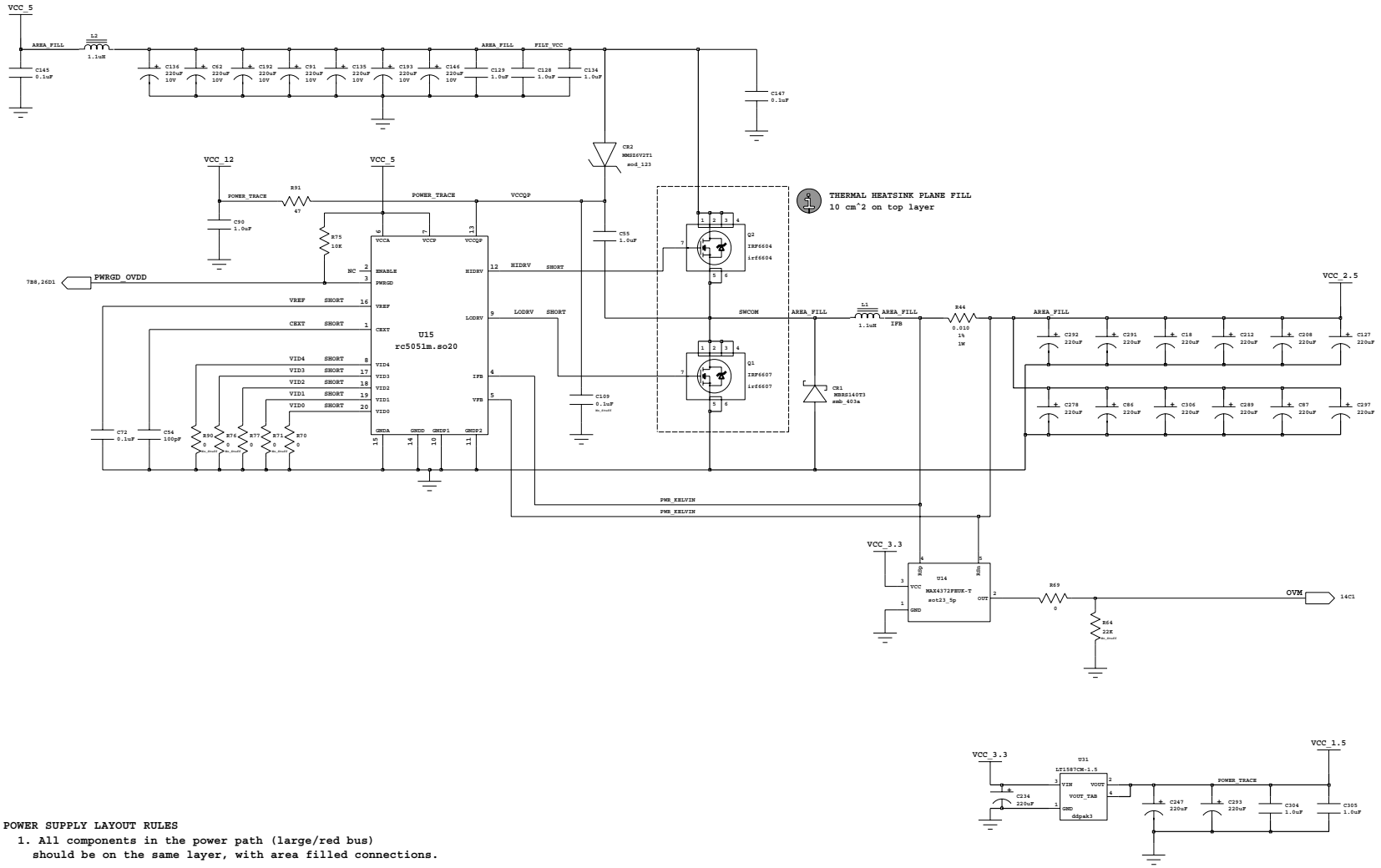
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:26:07 am	Title: Carrier Configuration	Page: 05



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:29:52 am	Title: System Control Logic (part I)	Page: 06



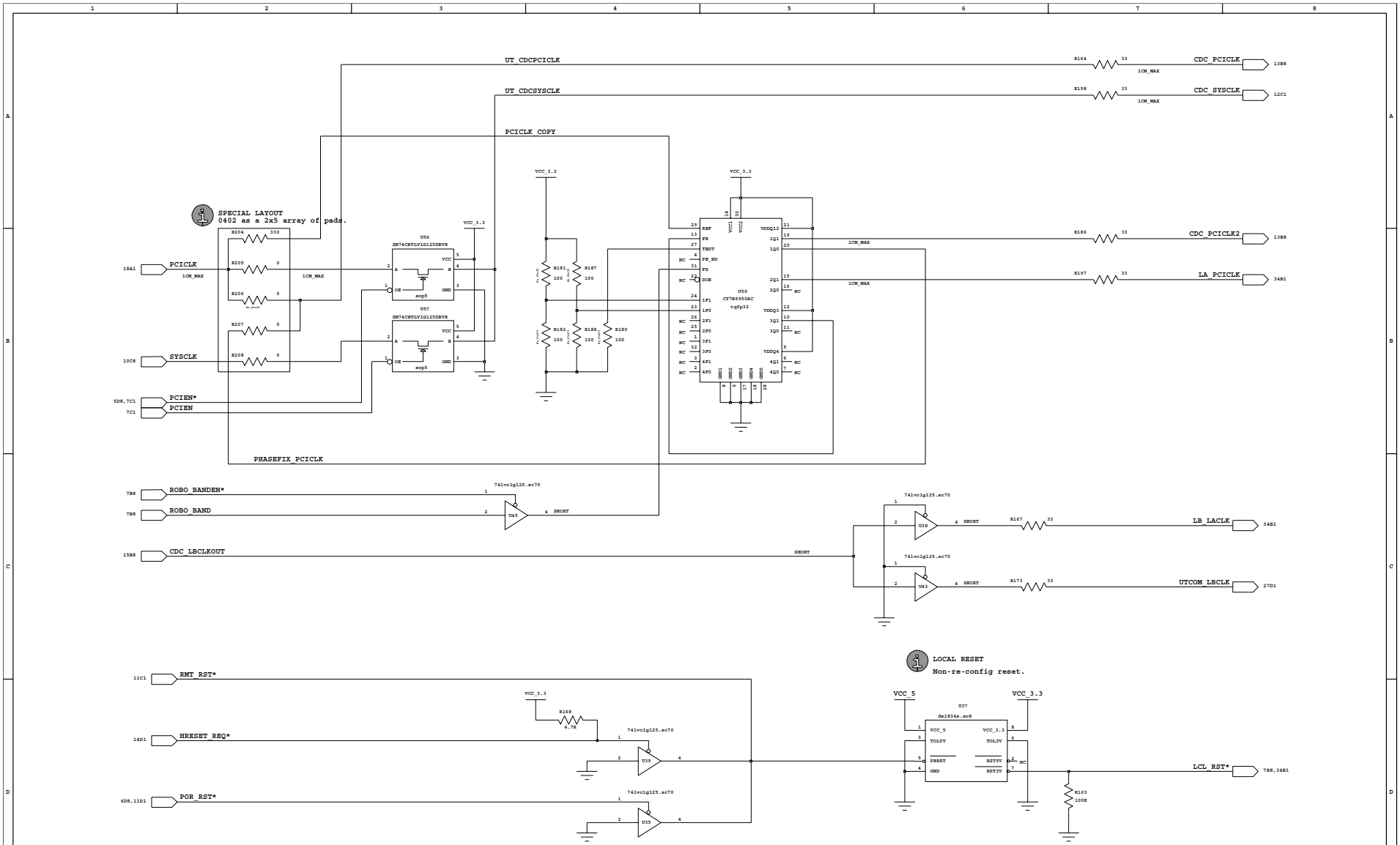
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:30:06 am	Title: System Logic (part II)	Page: 07



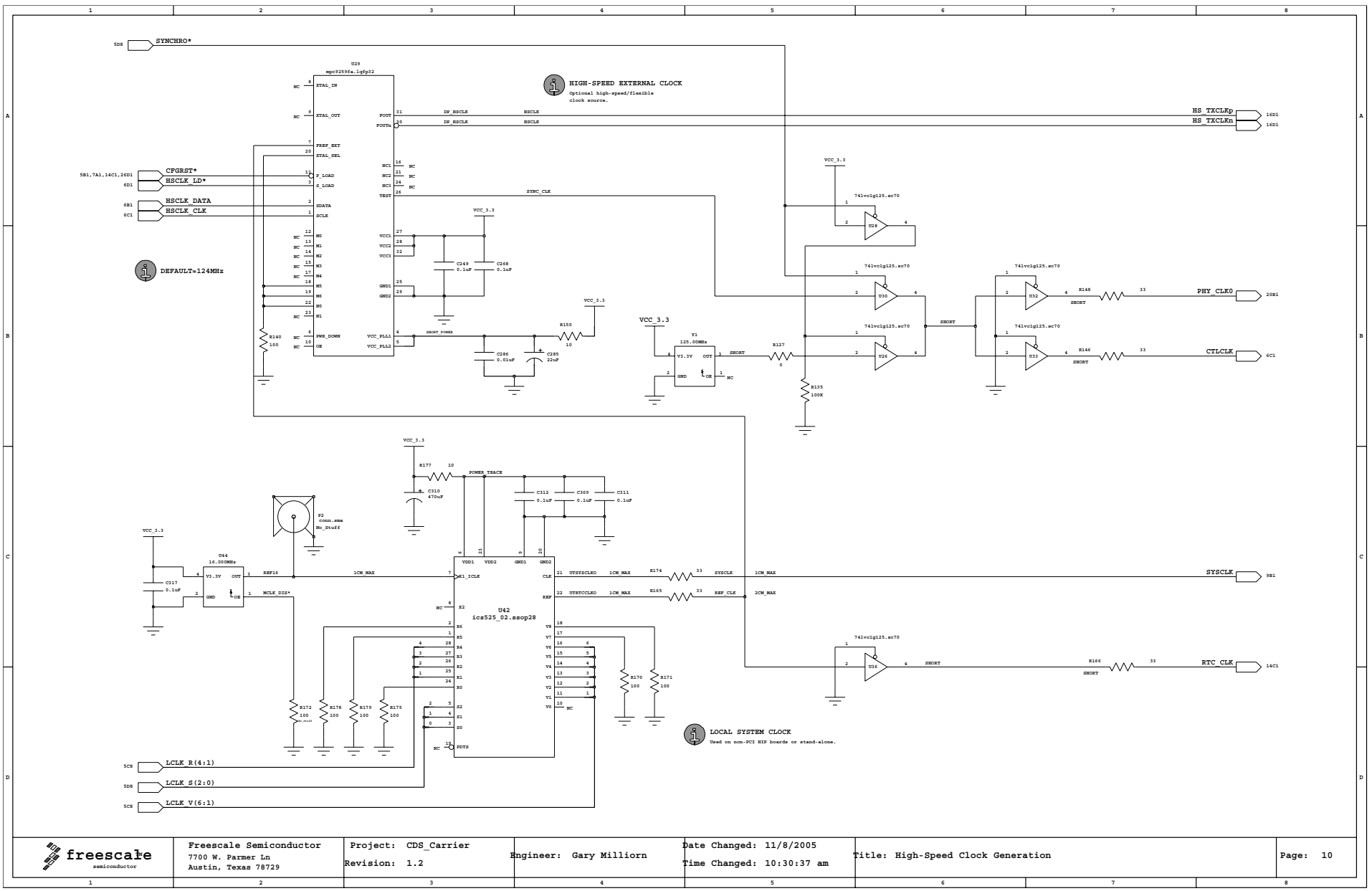
POWER SUPPLY LAYOUT RULES

1. All components in the power path (large/red bus) should be on the same layer, with area filled connections.
2. No vias or thermal reliefs allowed on power path components.
3. Ground plane connections should be made with two vias close to the component.

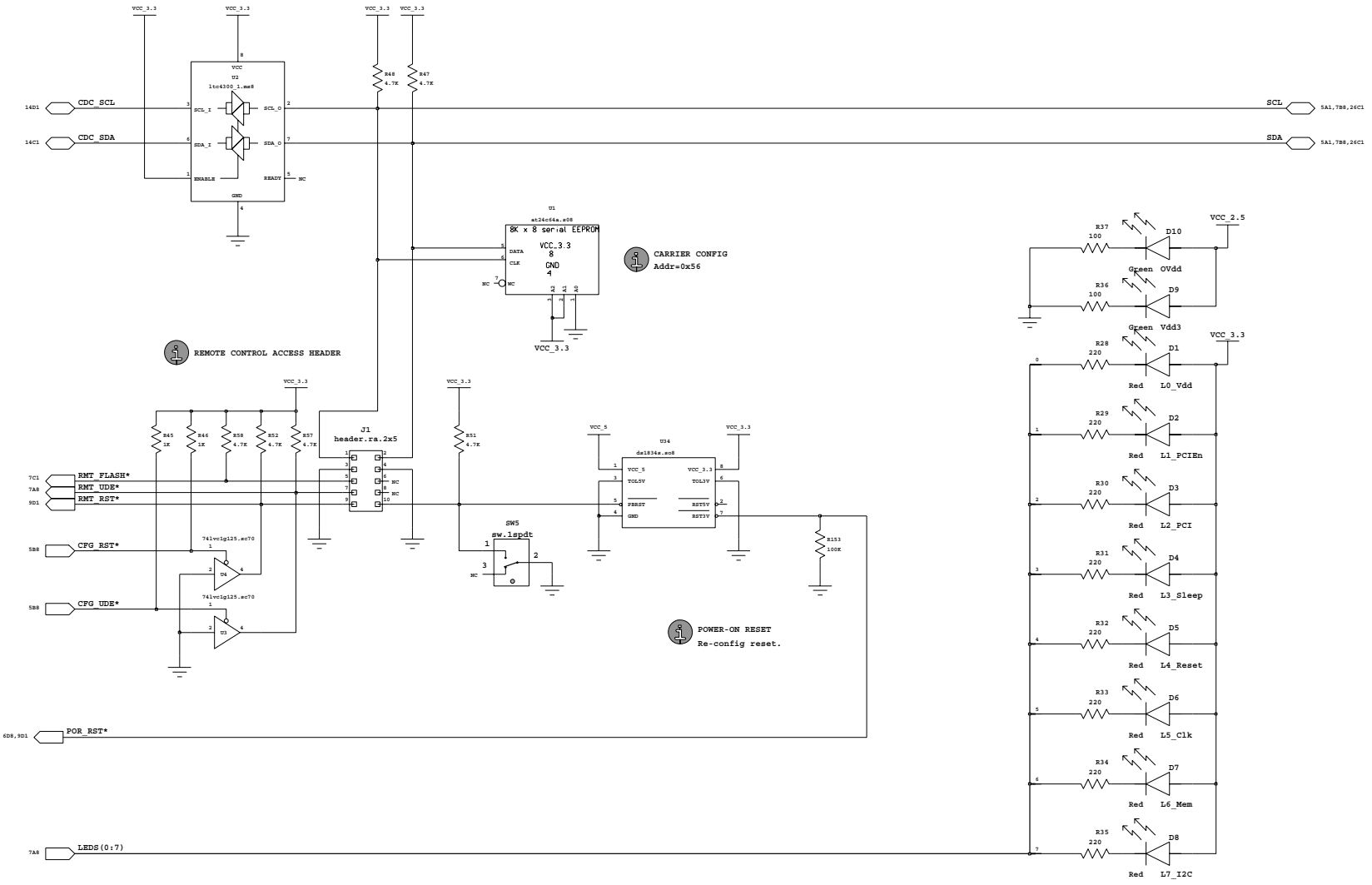
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:28:43 am	Title: System +2.5V Power Supply	Page: 08



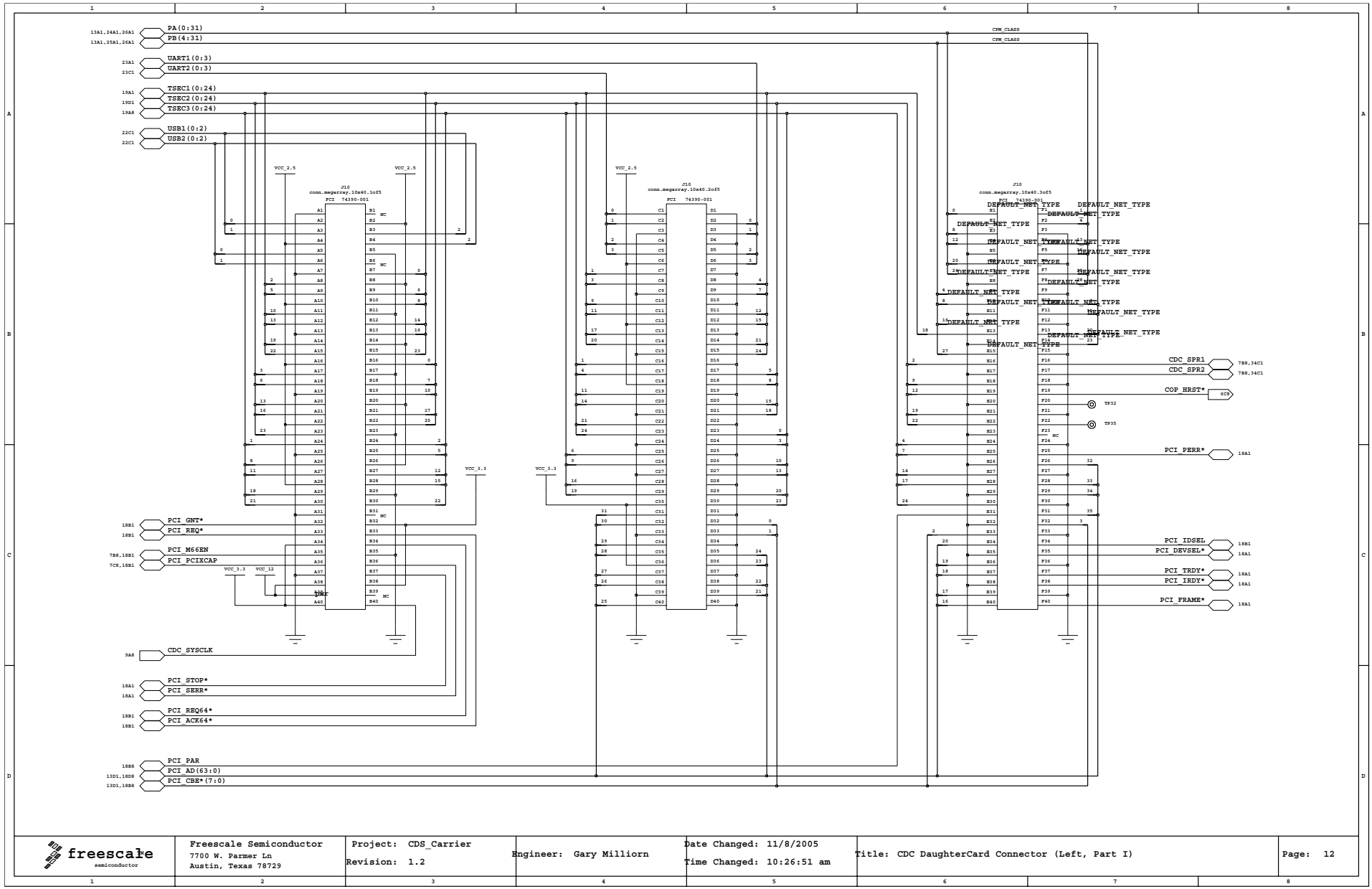
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:30:22 am	Title: Local (non-PCI) Resources: System Clock, System Reset	Page: 09



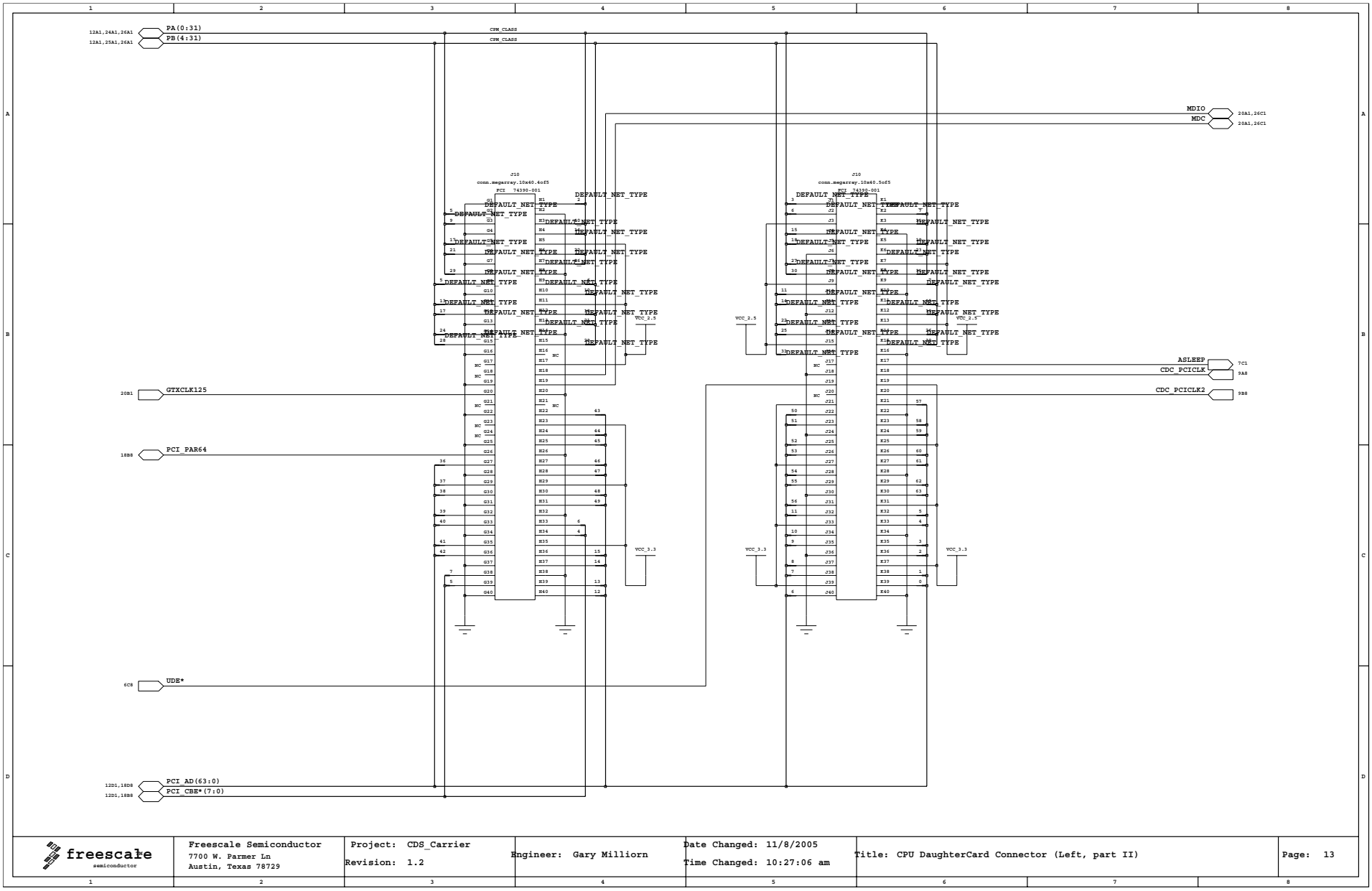
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:30:37 am	Title: High-Speed Clock Generation	Page: 10



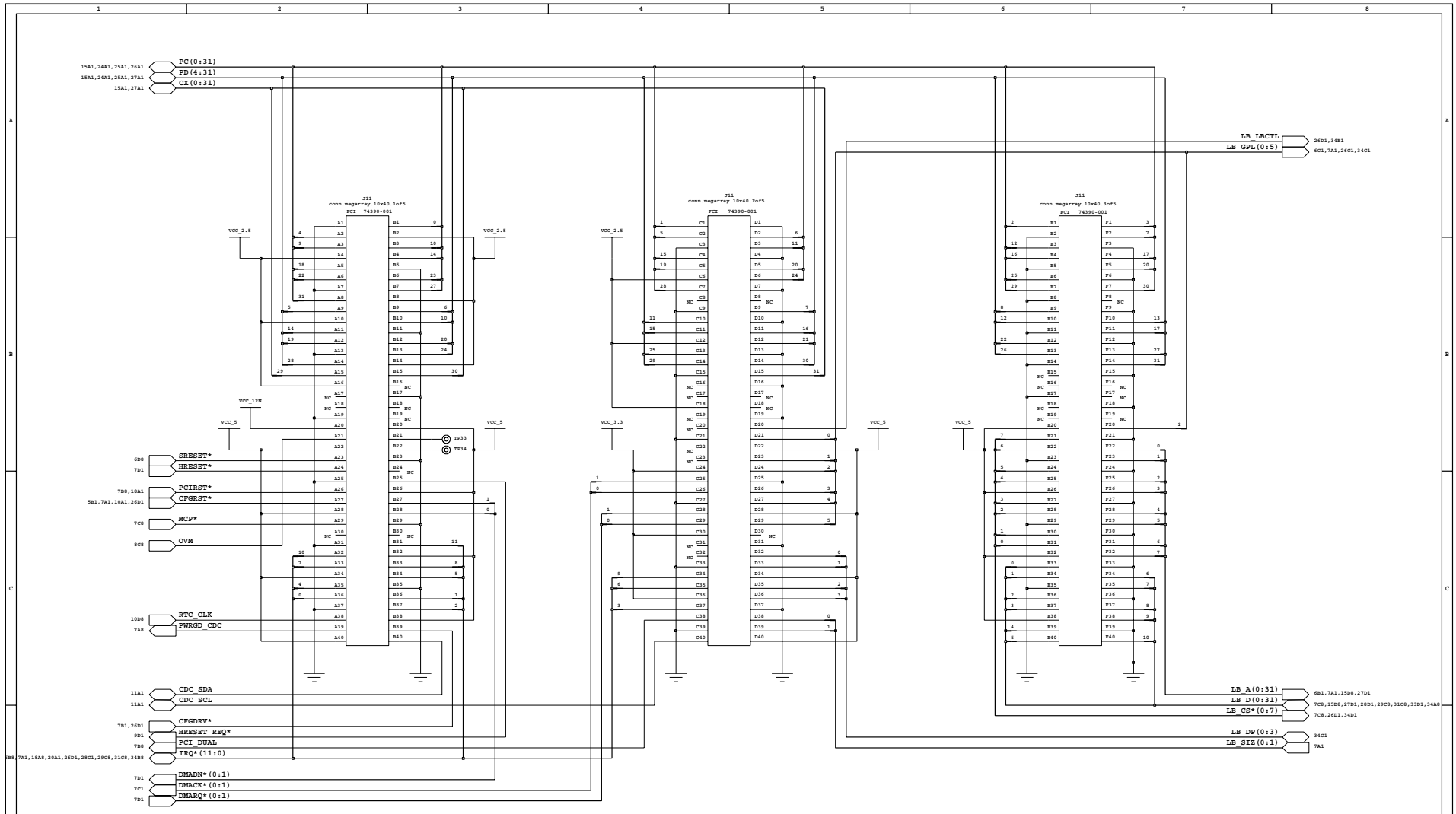
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:30:52 am	Title: Miscellaneous: LEDs, Debug Port and I2C Devices	Page: 11



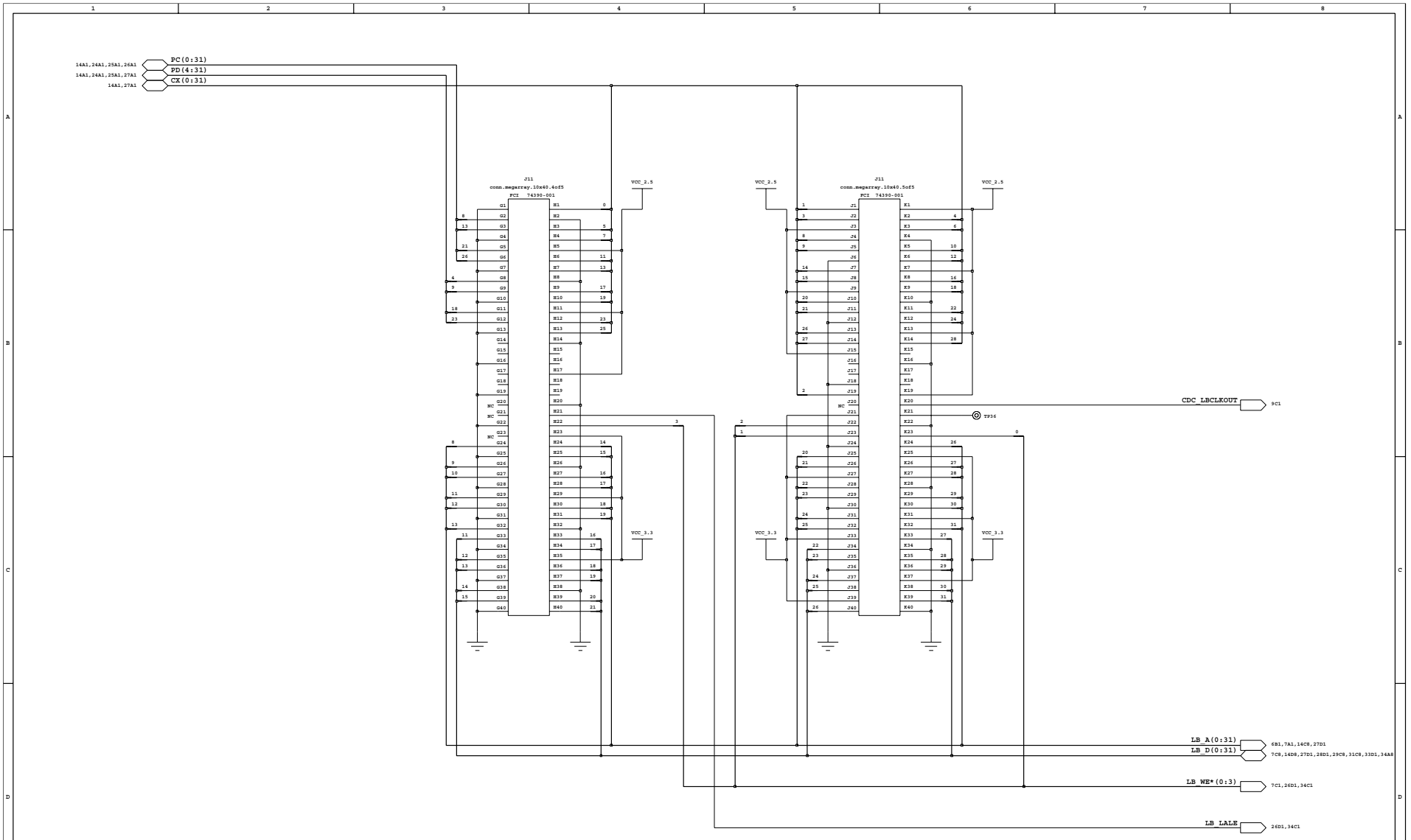
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:26:51 am	Title: CDC DaughterCard Connector (Left, Part I)	Page: 12



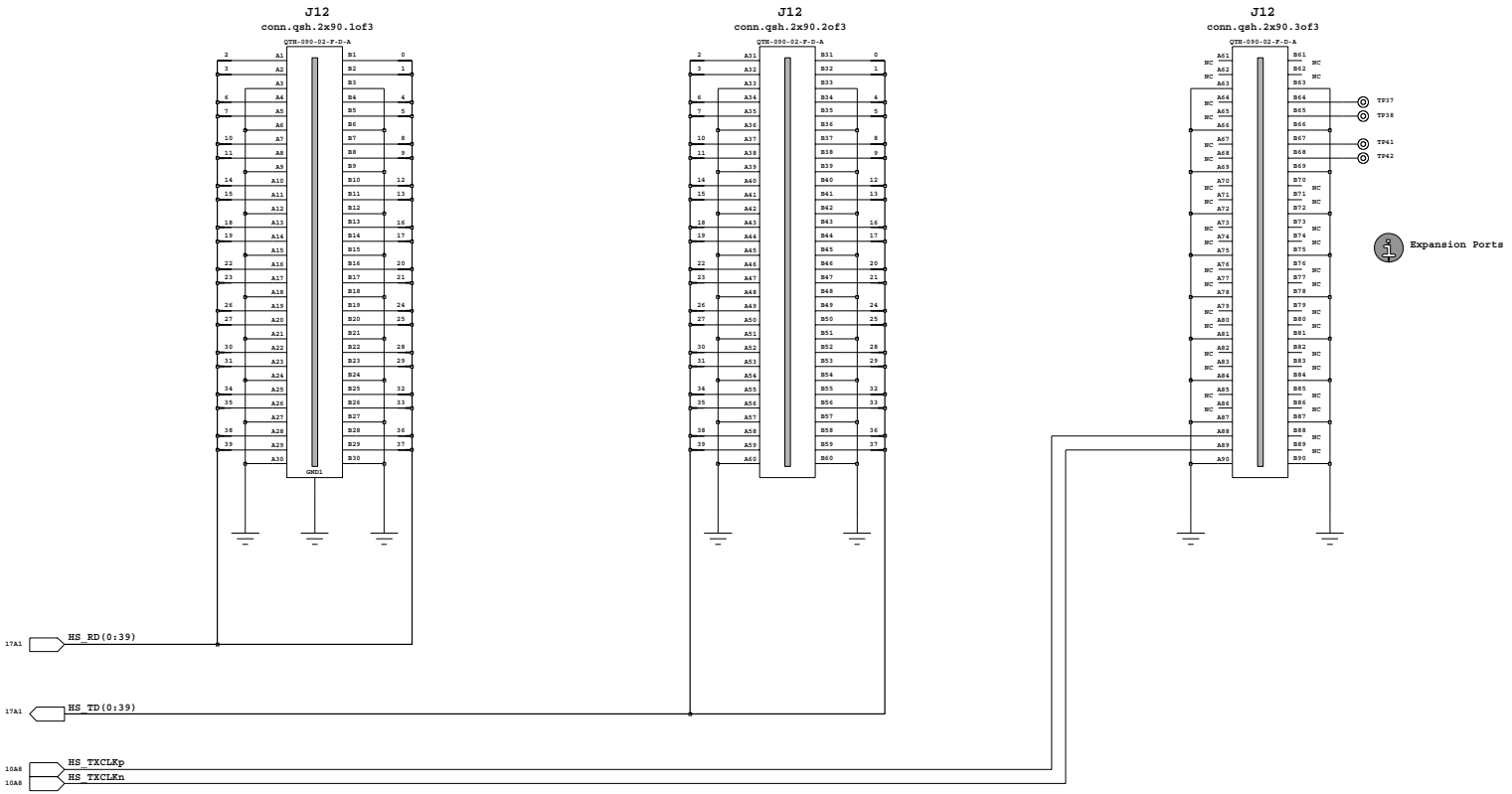
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:27:06 am	Title: CPU DaughterCard Connector (Left, part II)	Page: 13



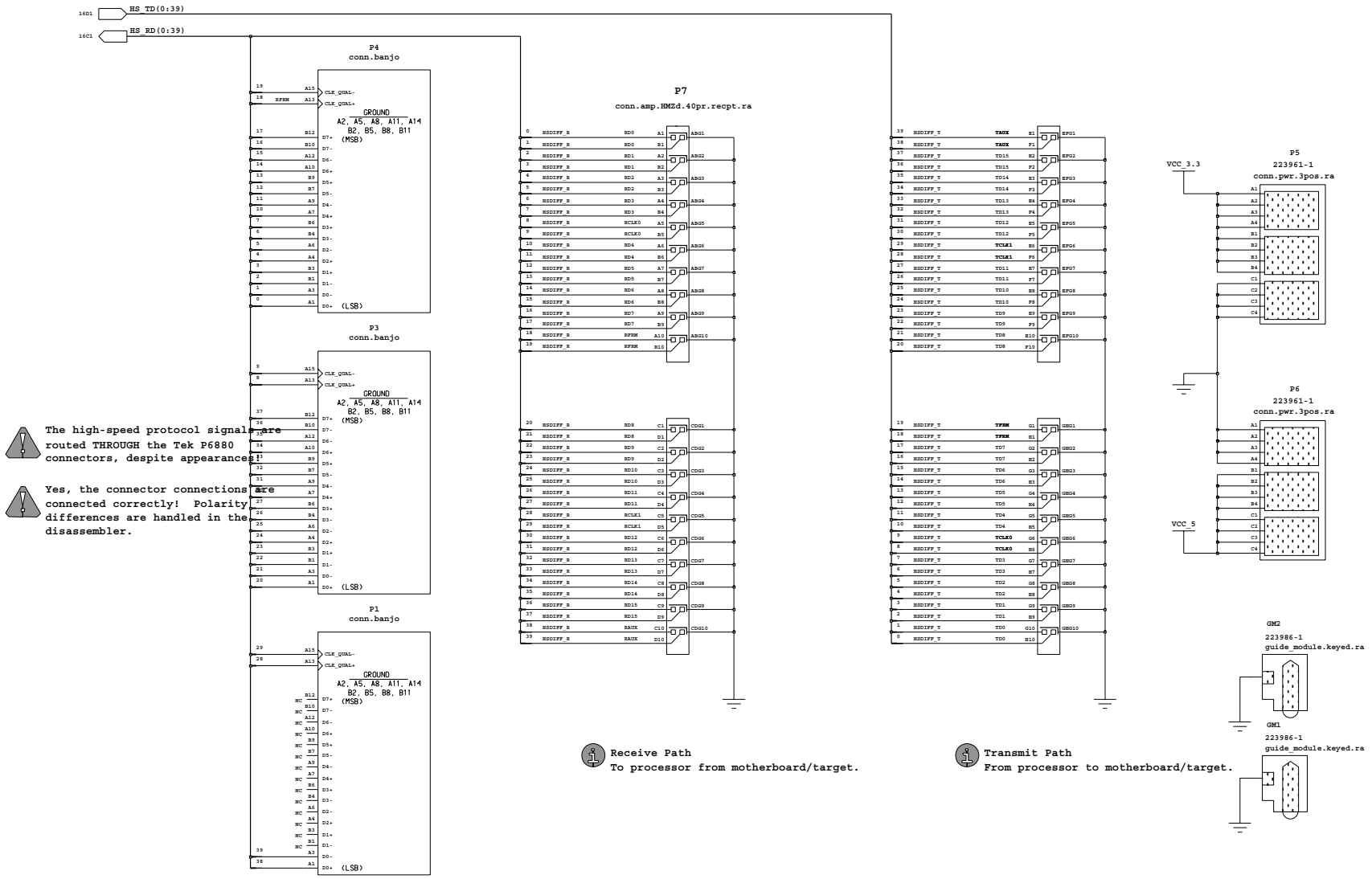
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:27:20 am	Title: CDC DaughterCard Connector (Right, Part I)	Page: 14



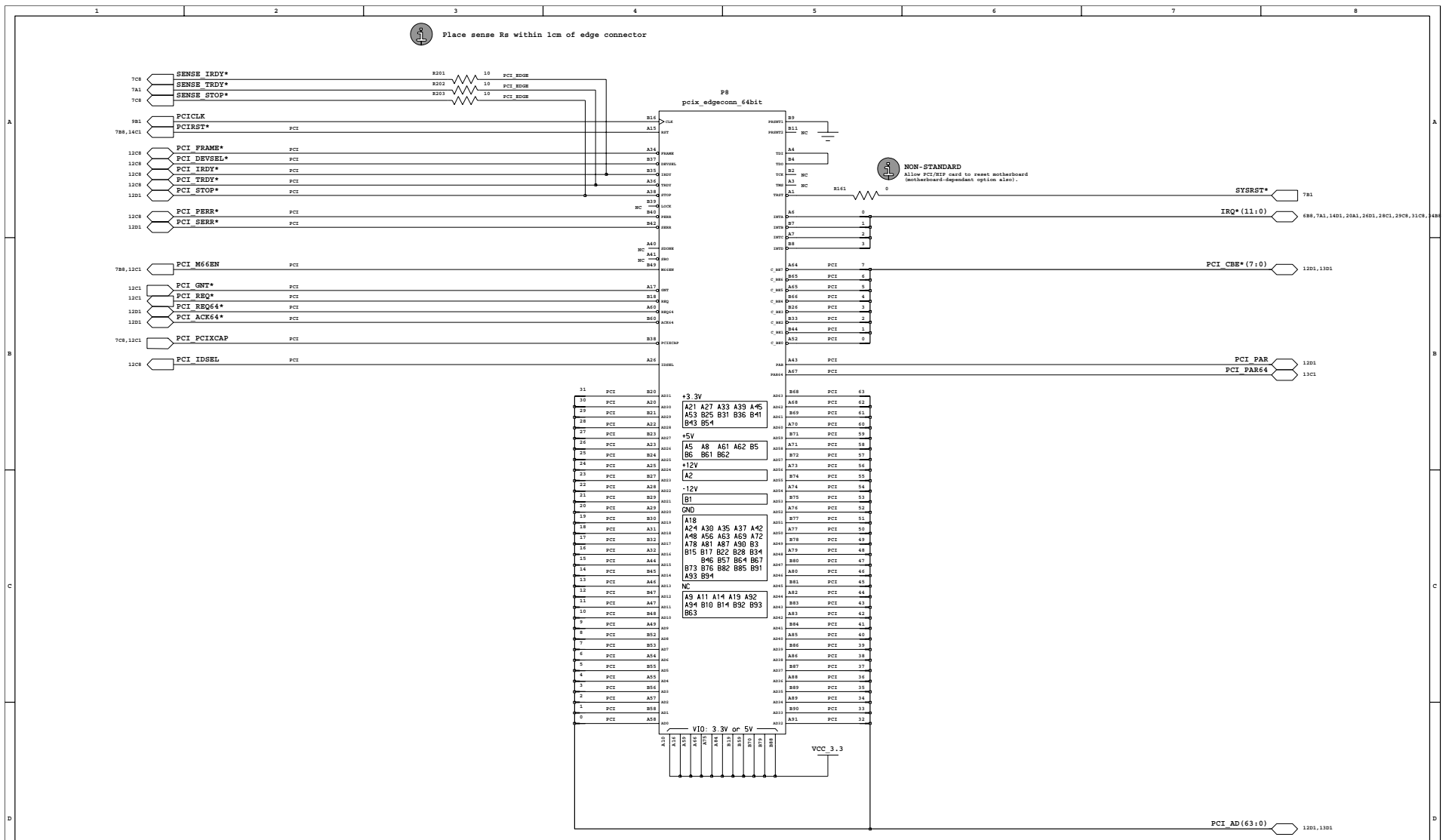
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:27:33 am	Title: CDC DaughterCard Connector (Right, Part II)	Page: 15



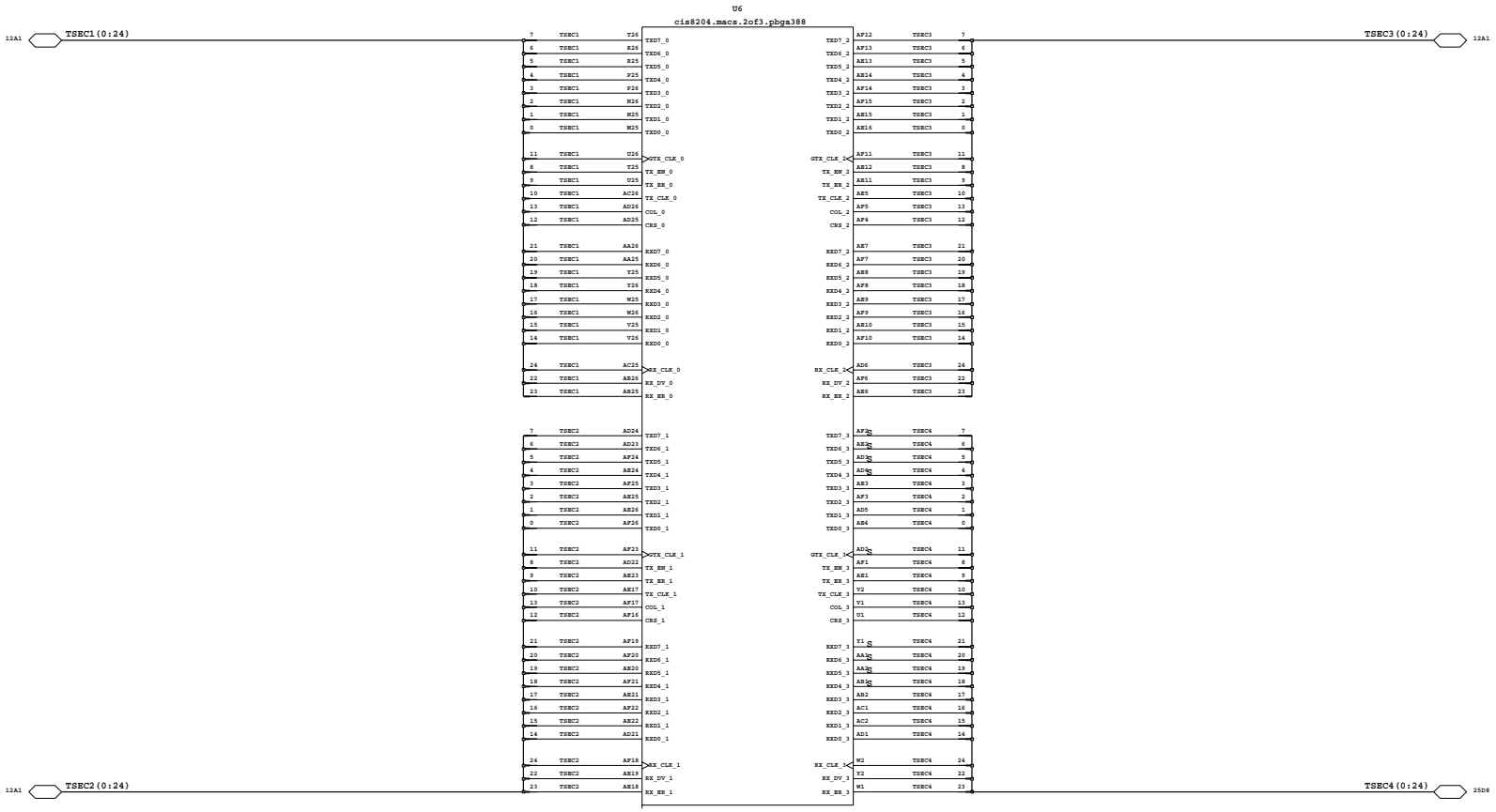
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:27:47 am	Title: High-Speed IO Daughtercard Connector	Page: 16



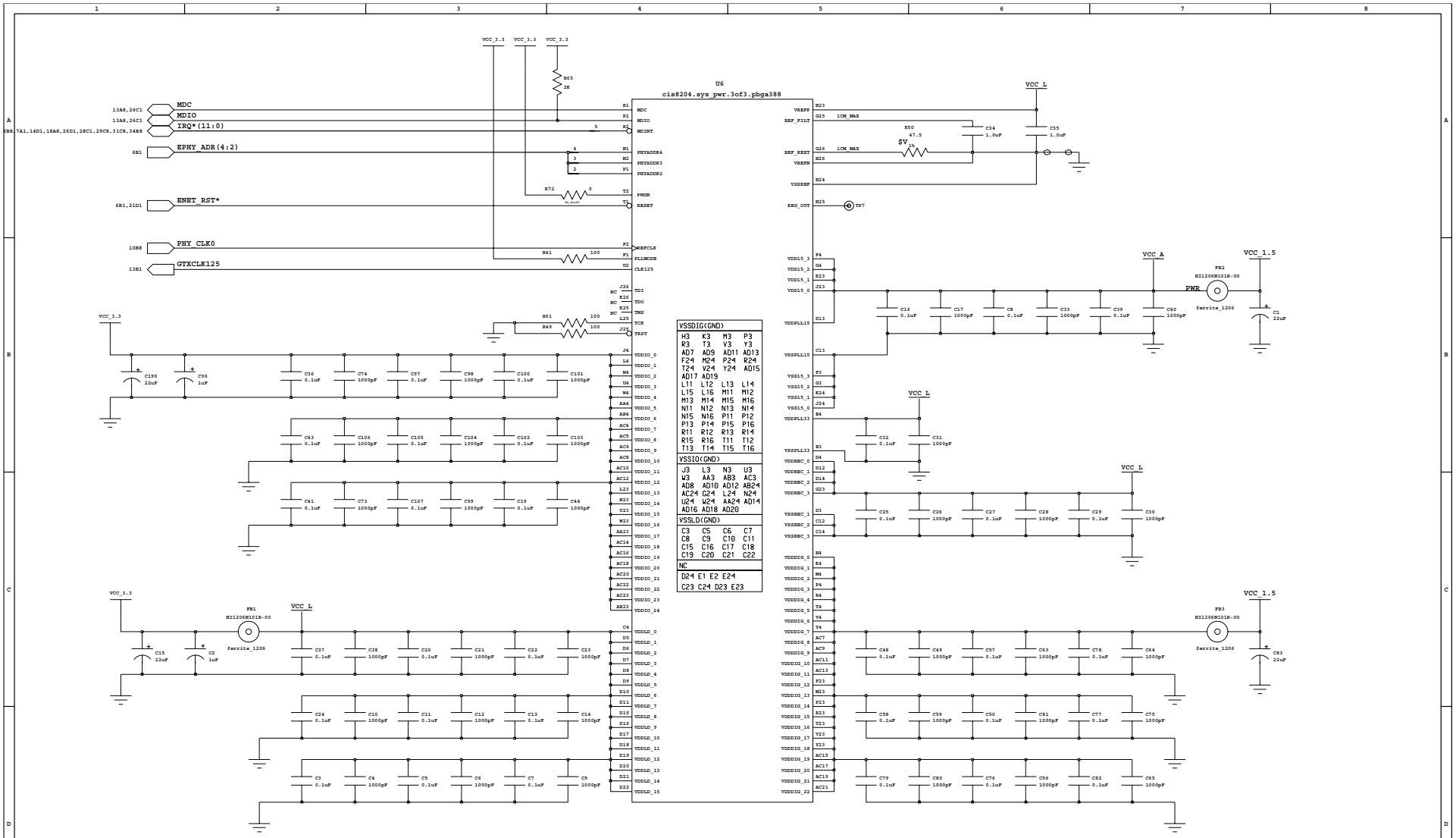
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:28:00 am	Title: High-Speed Differential IO, HMZD/HIP Interface and P6880 "Banjo" Re...



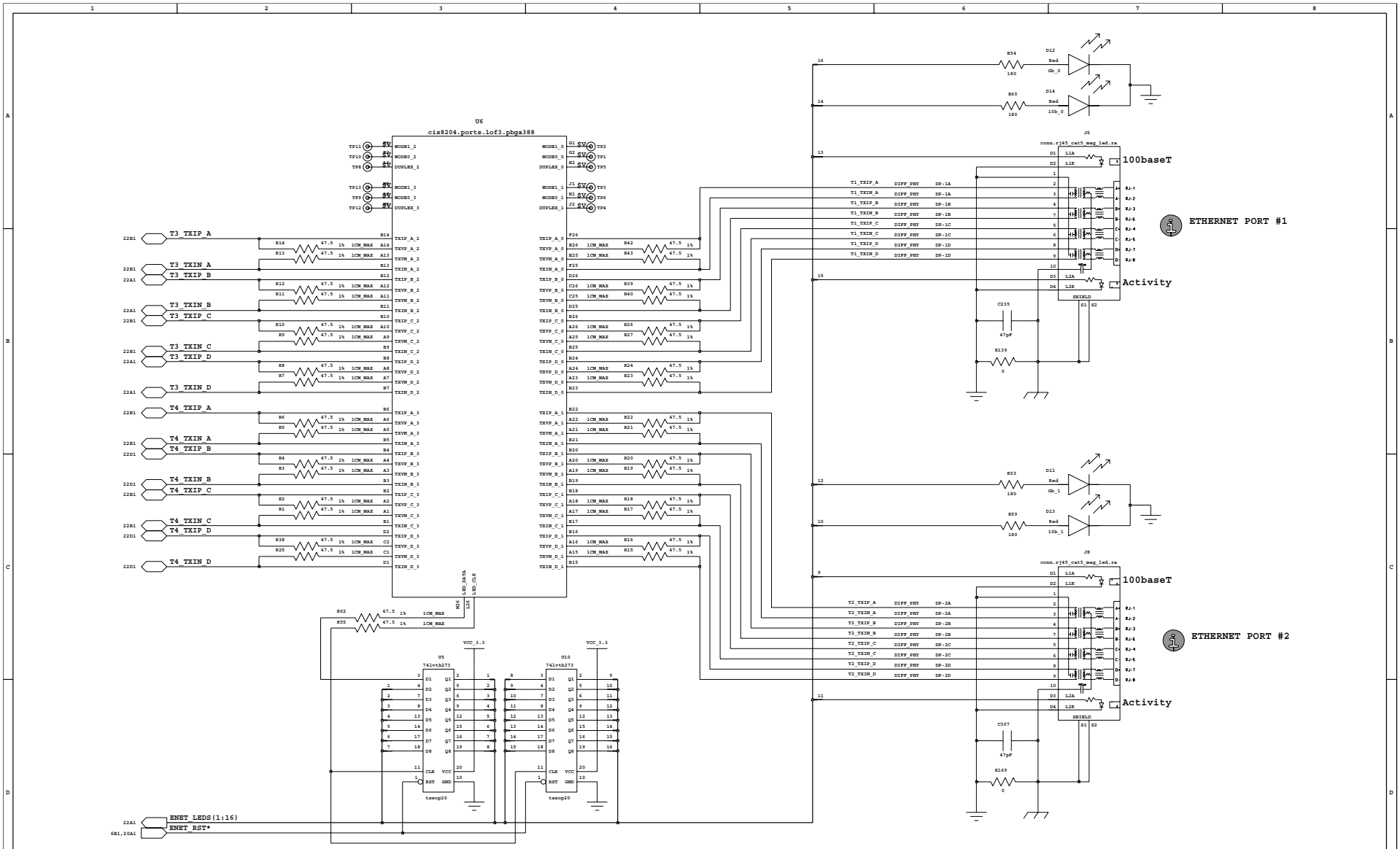
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:28:15 am	Title: Primary PCI/PCI-X Edge Connector	Page: 18



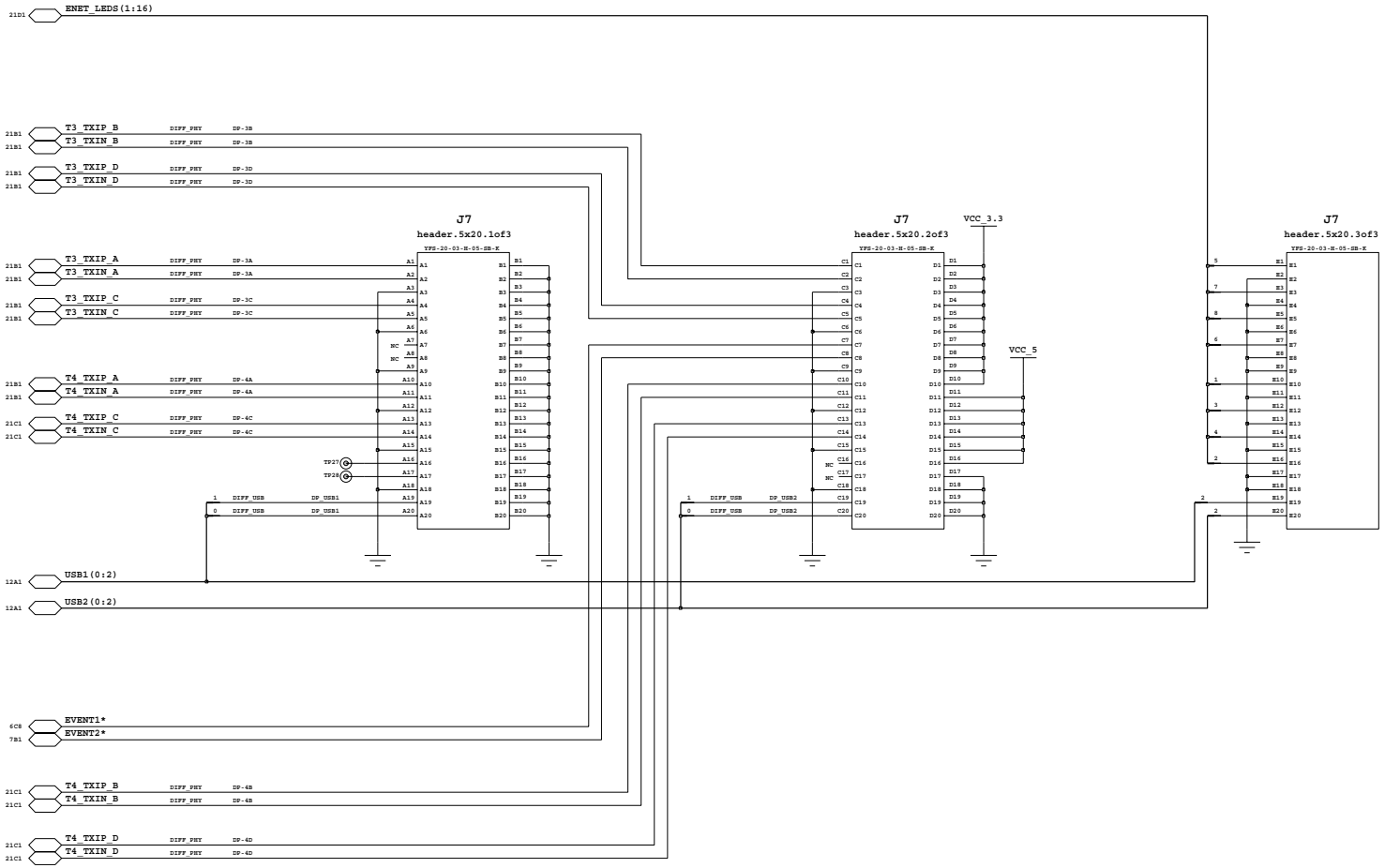
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:31:05 am	Title: Quad 10/100/GB PHY MAC Interfaces	Page: 19



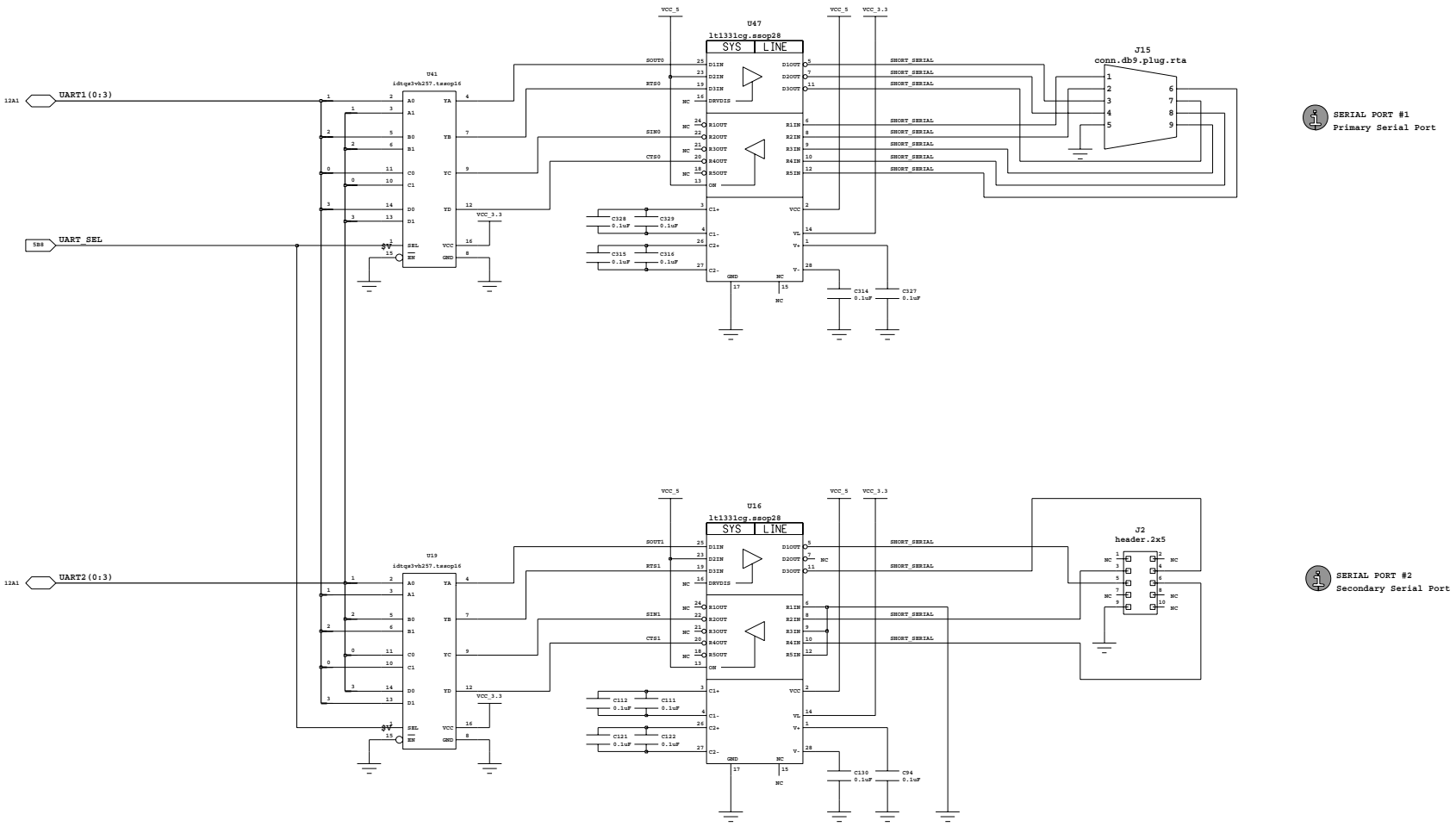
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:31:19 am	Title: Quad 10/100/Gb PHY Power/System Interface	Page: 20



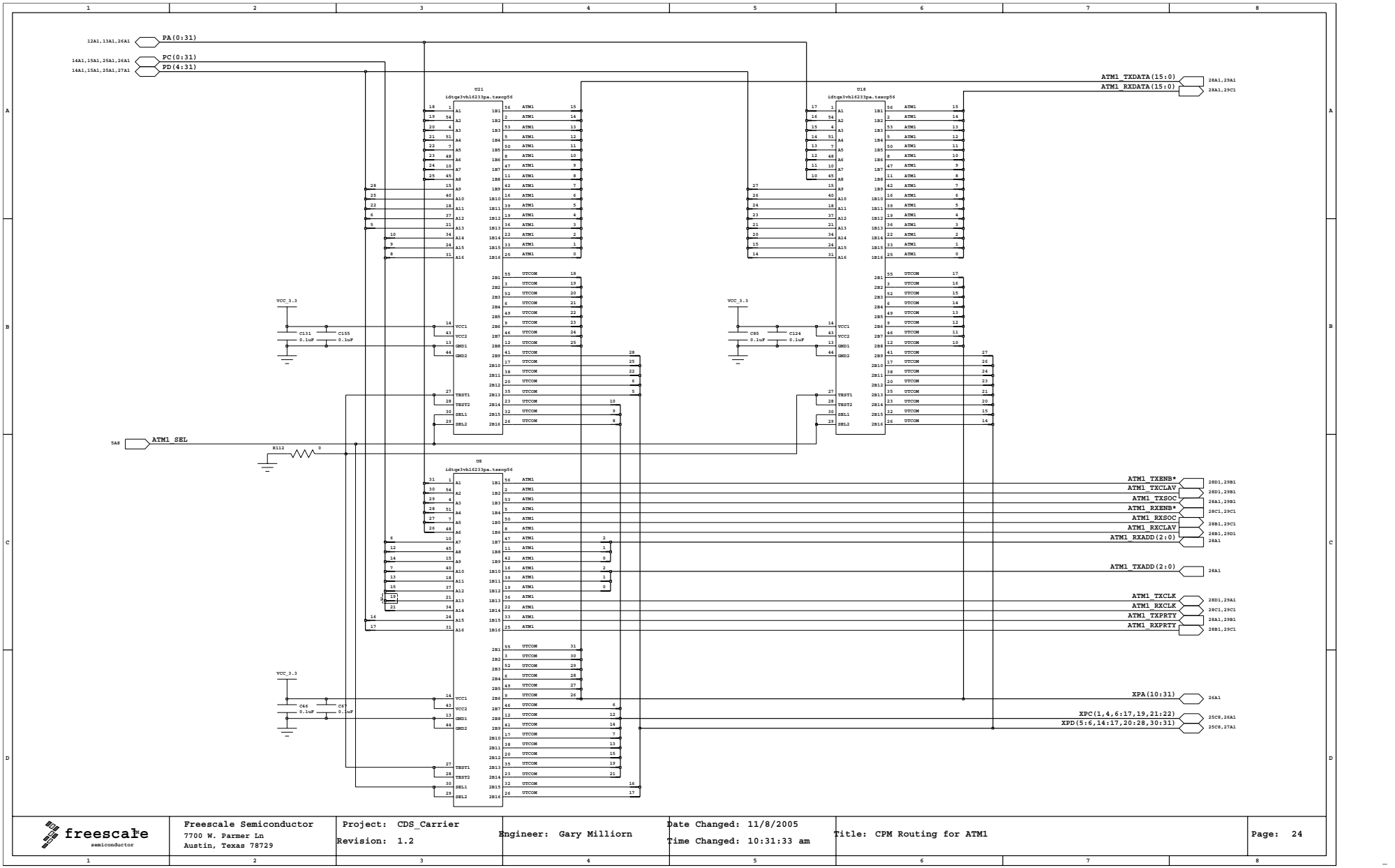
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:26:36 am	Title: Ethernet Ports #1 and #2	Page: 21



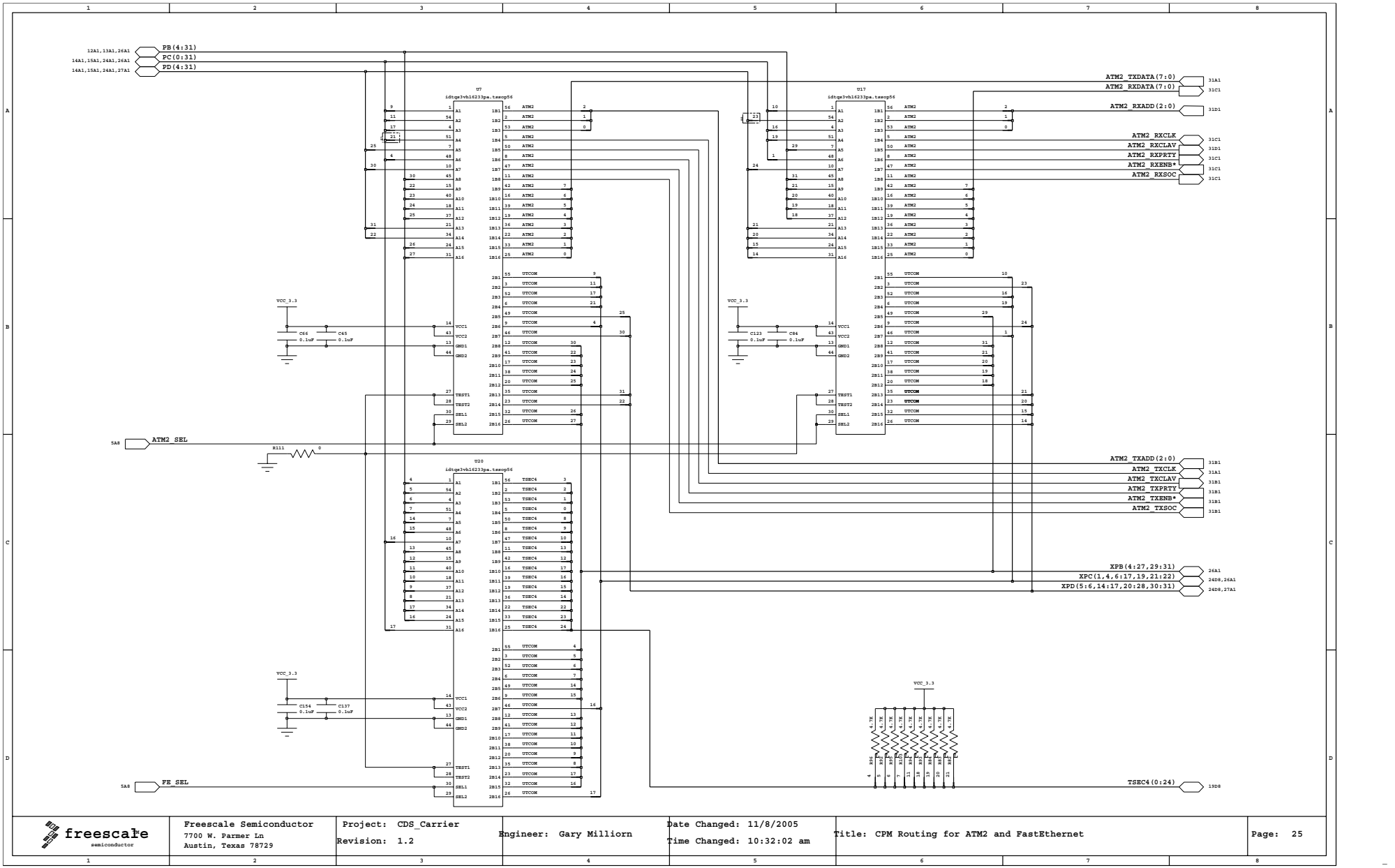
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:26:22 am	Title: Carrier-to-IOCard Connector	Page: 22



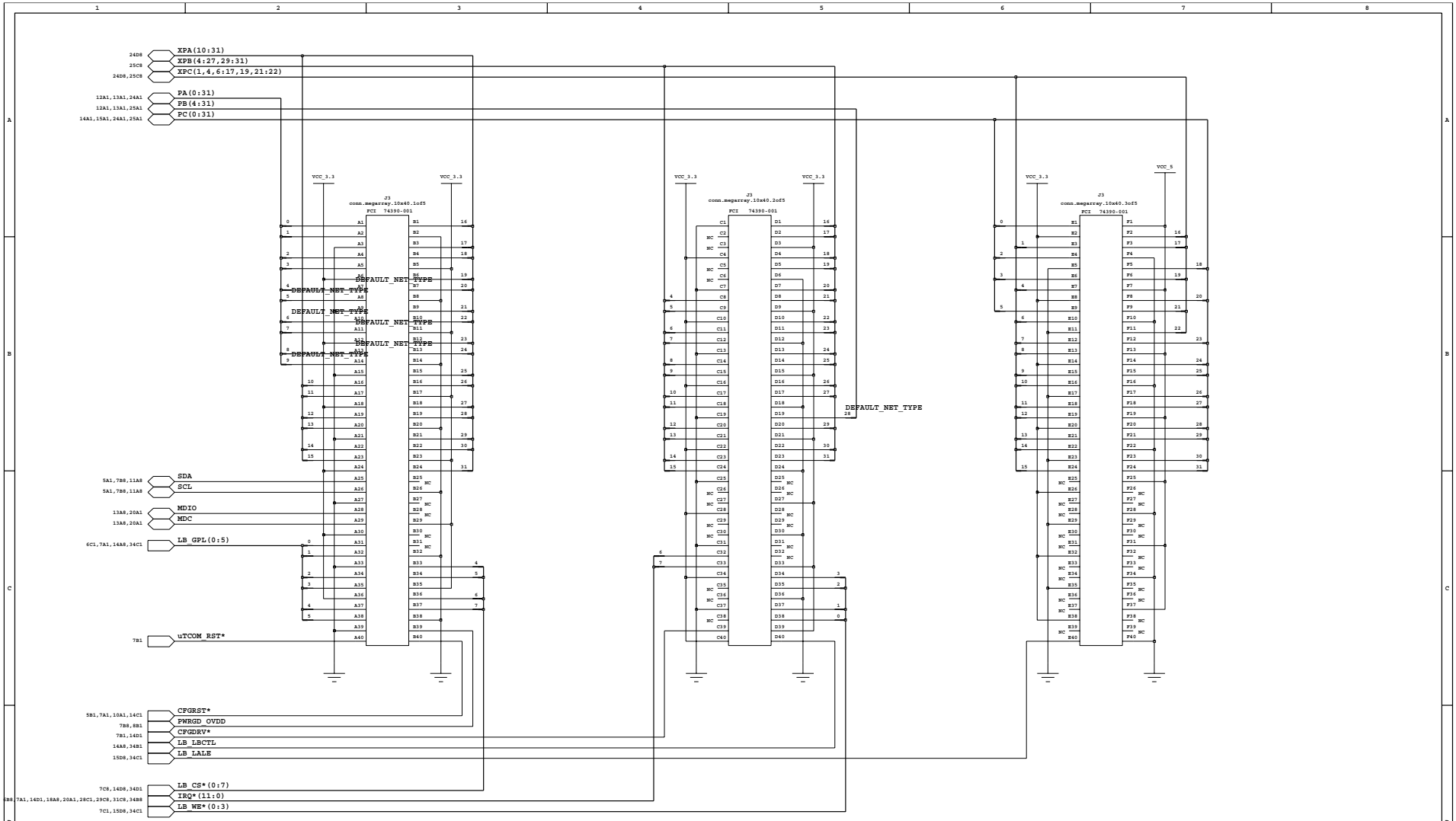
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:28:29 am	Title: Serial Ports	Page: 23



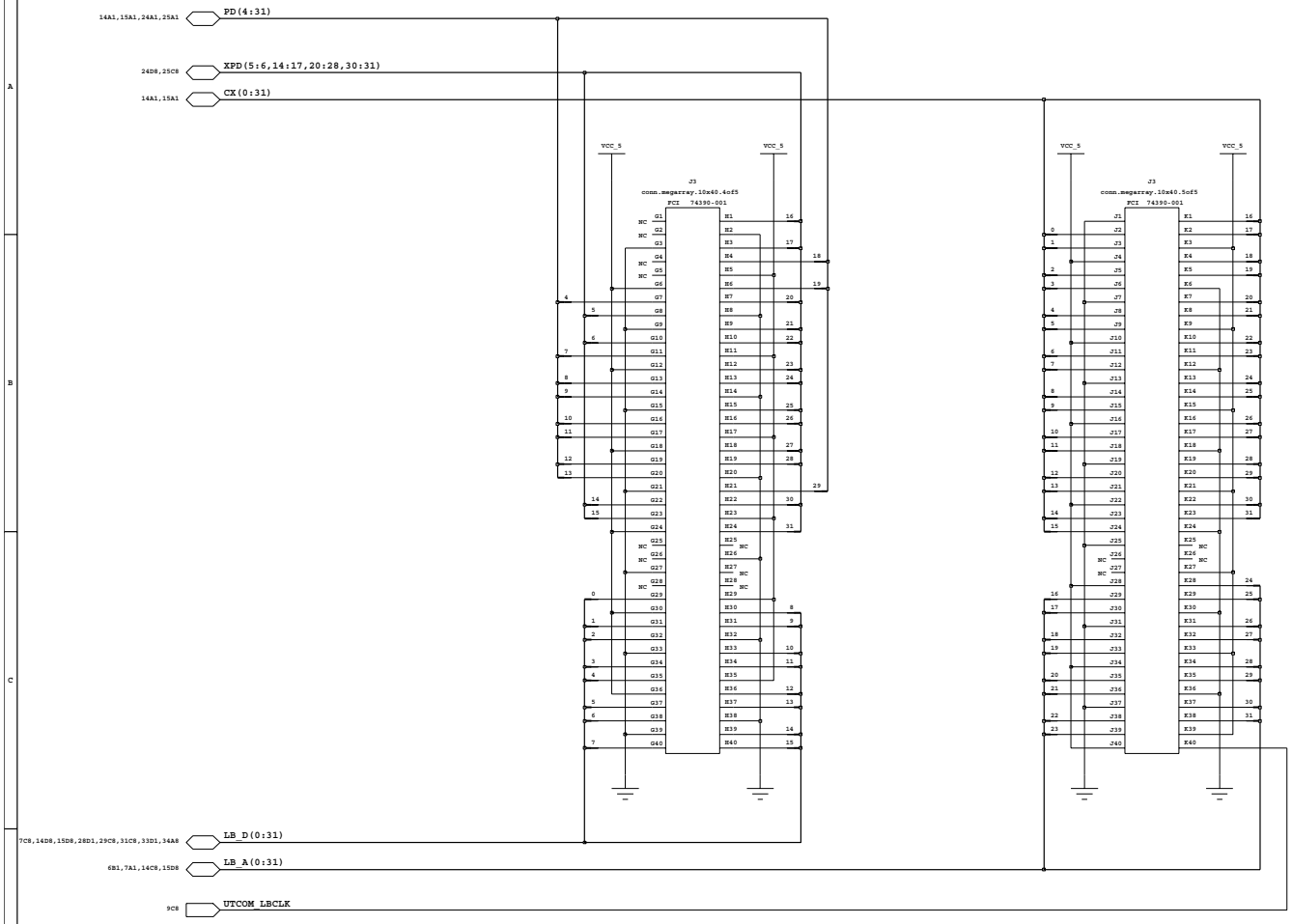
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:31:33 am	Title: CPM Routing for ATM1	Page: 24



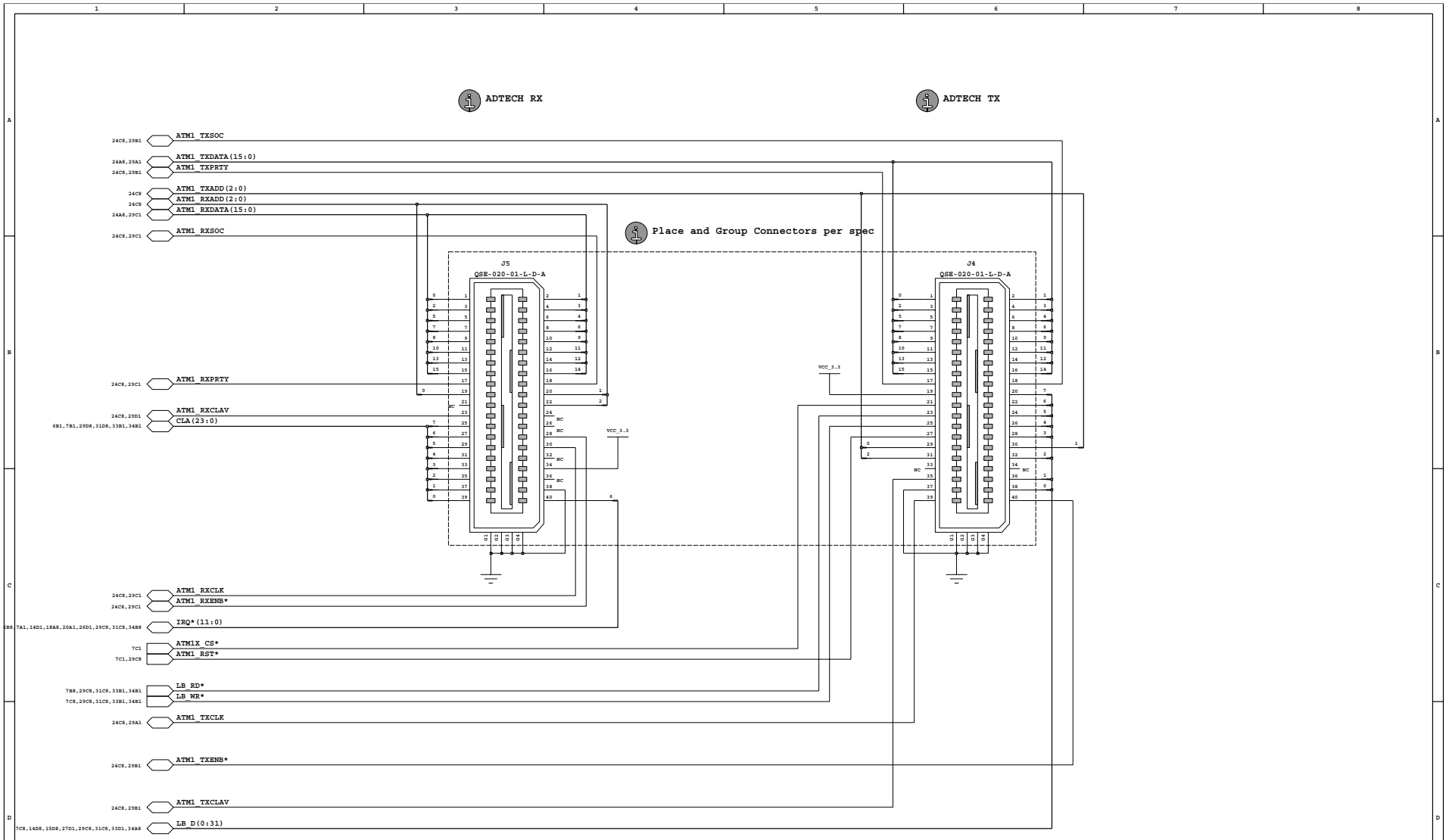
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:32:02 am	Title: CPM Routing for ATM2 and FastEthernet	Page: 25



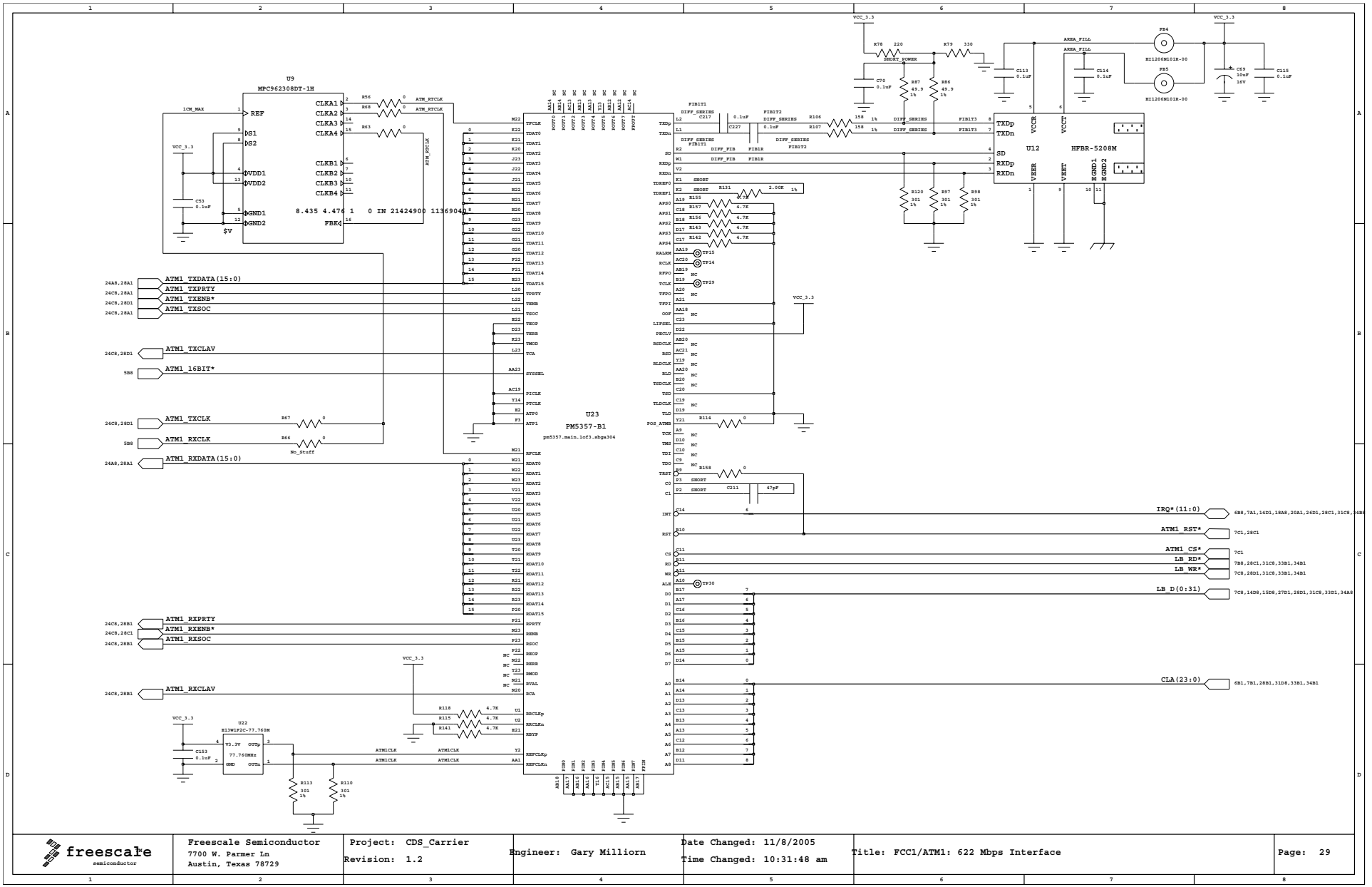
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:32:45 am	Title: uTCOM Connector (part I)	Page: 26



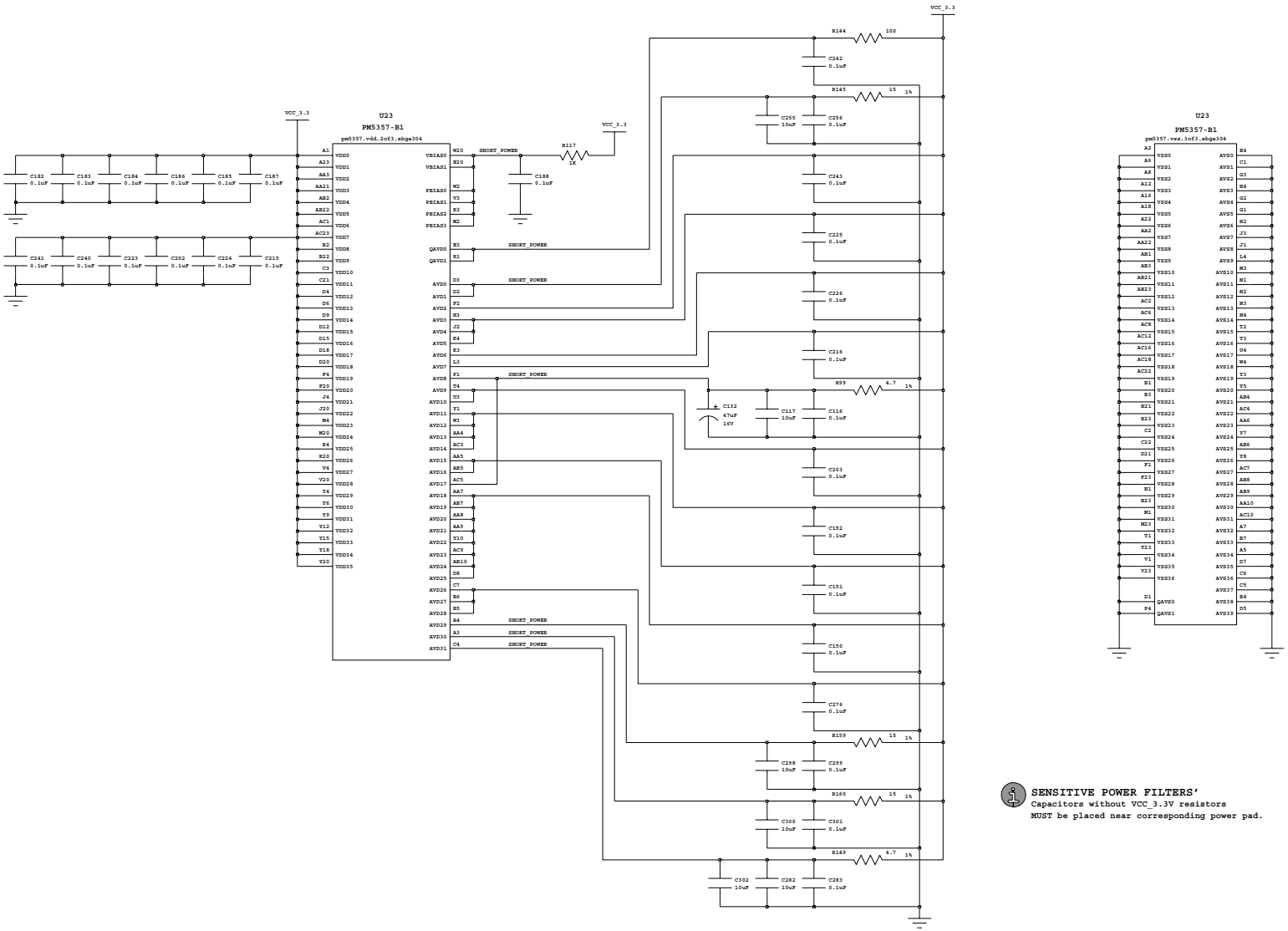
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:32:59 am	Title: uTCOM Connector (part II)	Page: 27



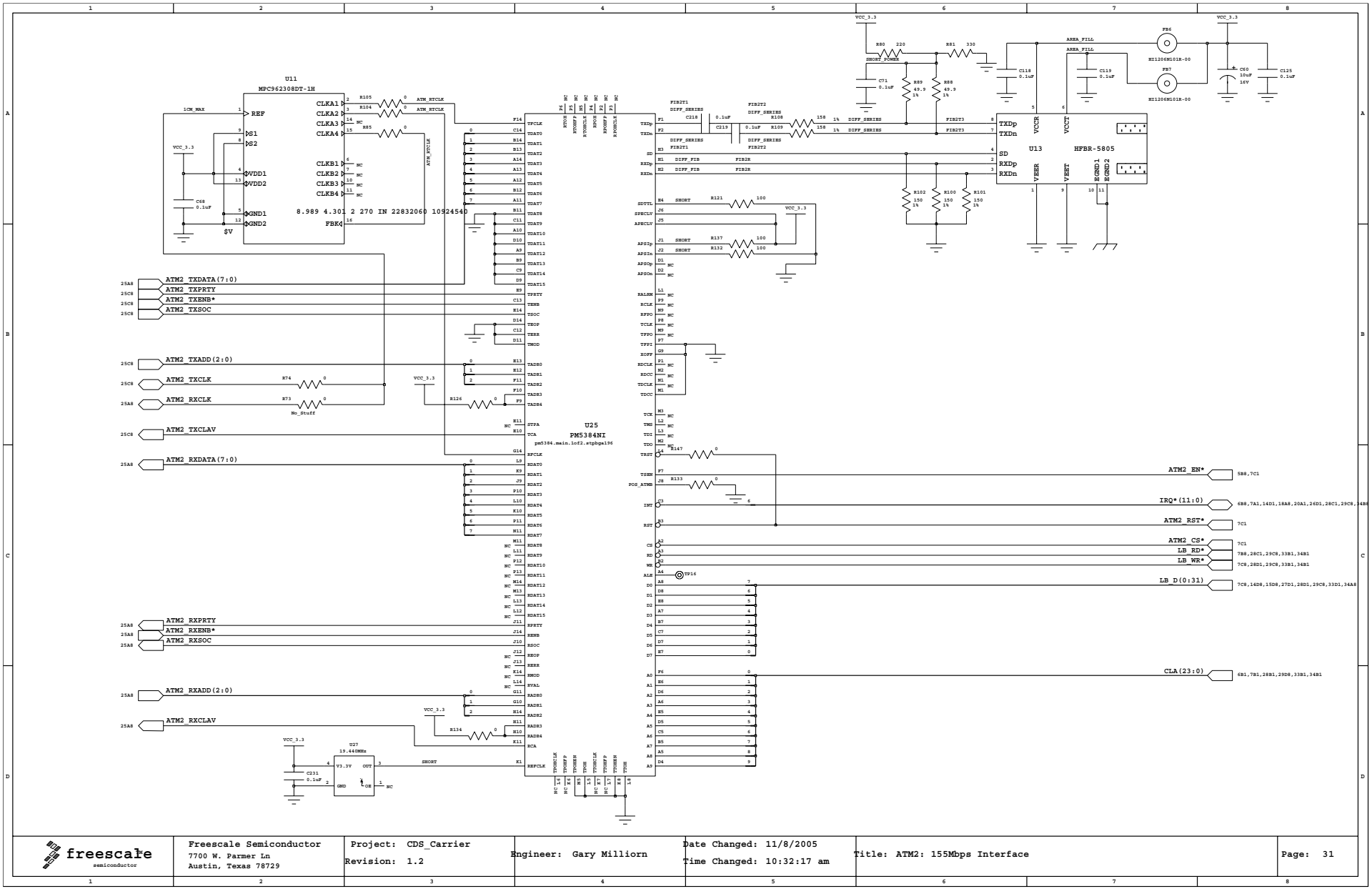
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:33:28 am	Title: FCC1/ATM1: AdTech Adapter Connector	Page: 28



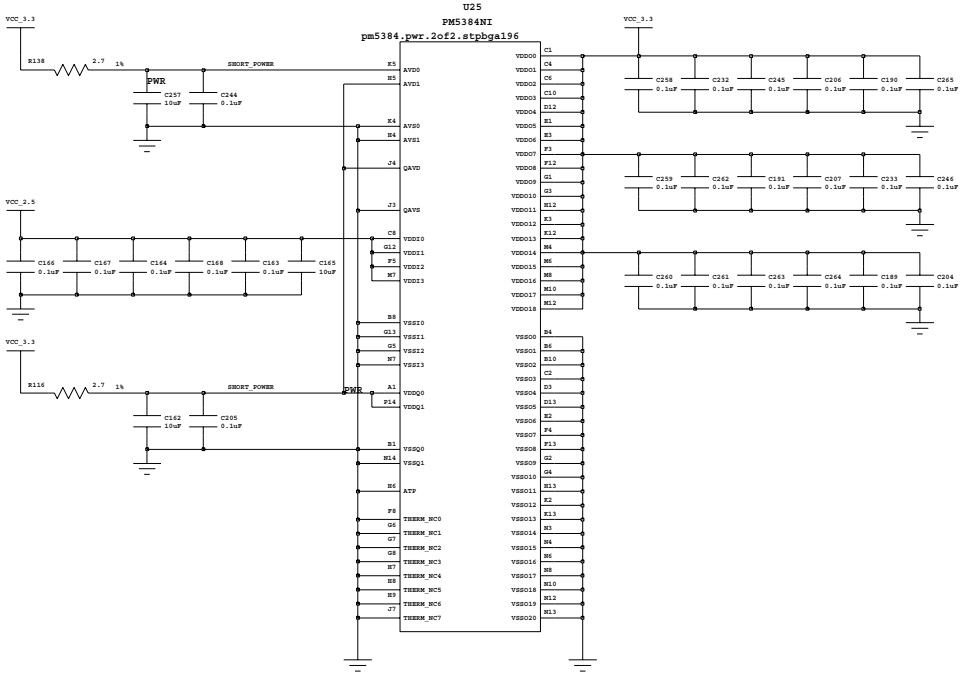
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:31:48 am	Title: FCC1/ATM1: 622 Mbps Interface	Page: 29



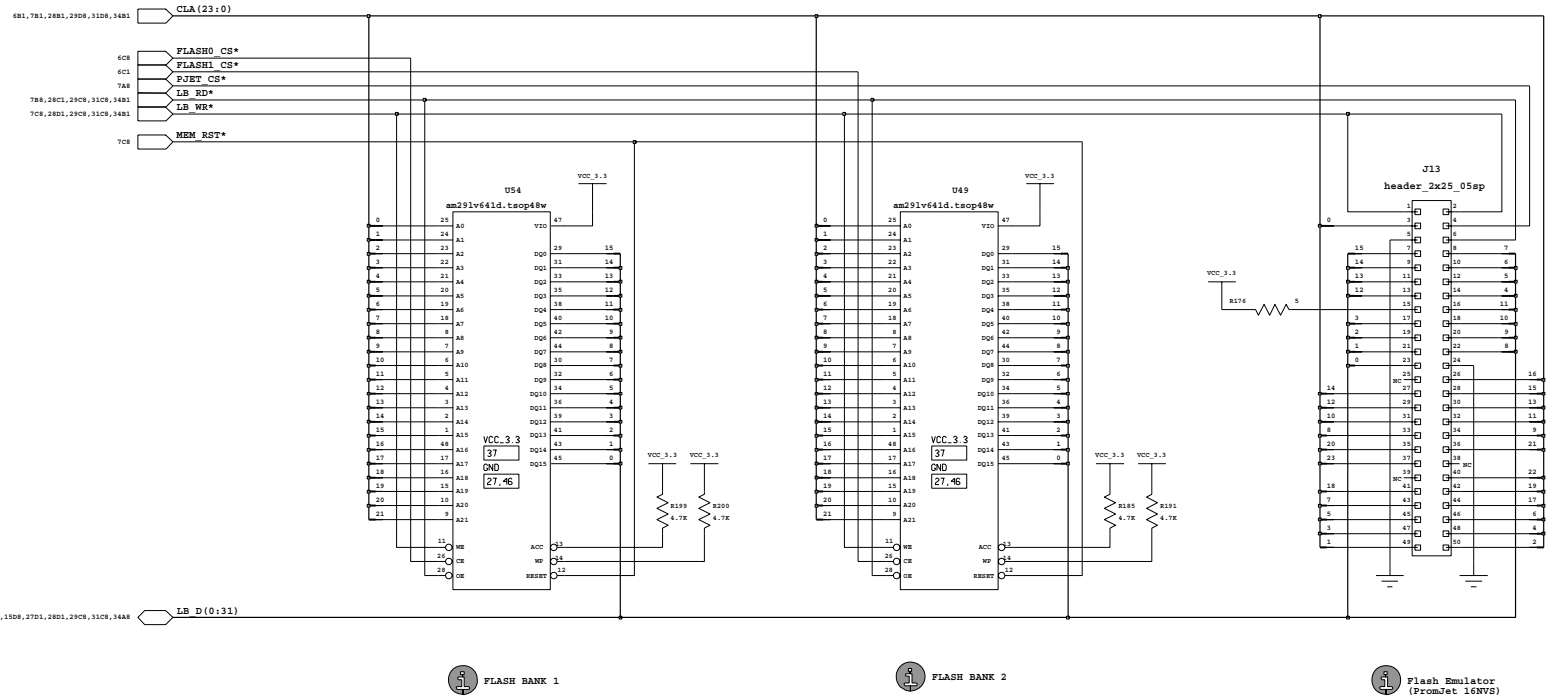
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:33:14 am	Title: FCC1/ATM1:PHY Power	Page: 30



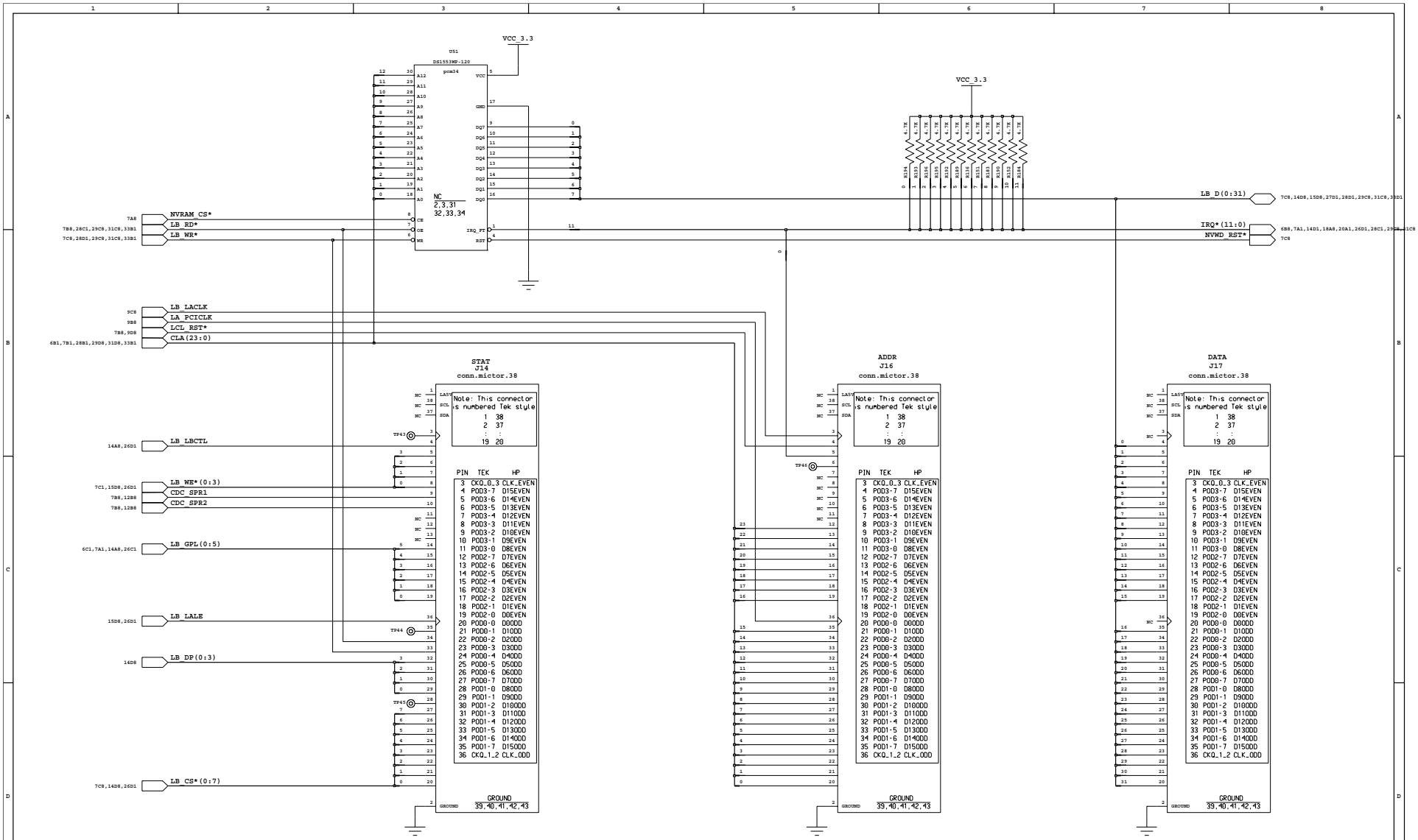
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:32:17 am	Title: ATM2: 155Mbps Interface Page: 31



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:32:32 am	Title: FCC2/ATM2: PHY Power	Page: 32



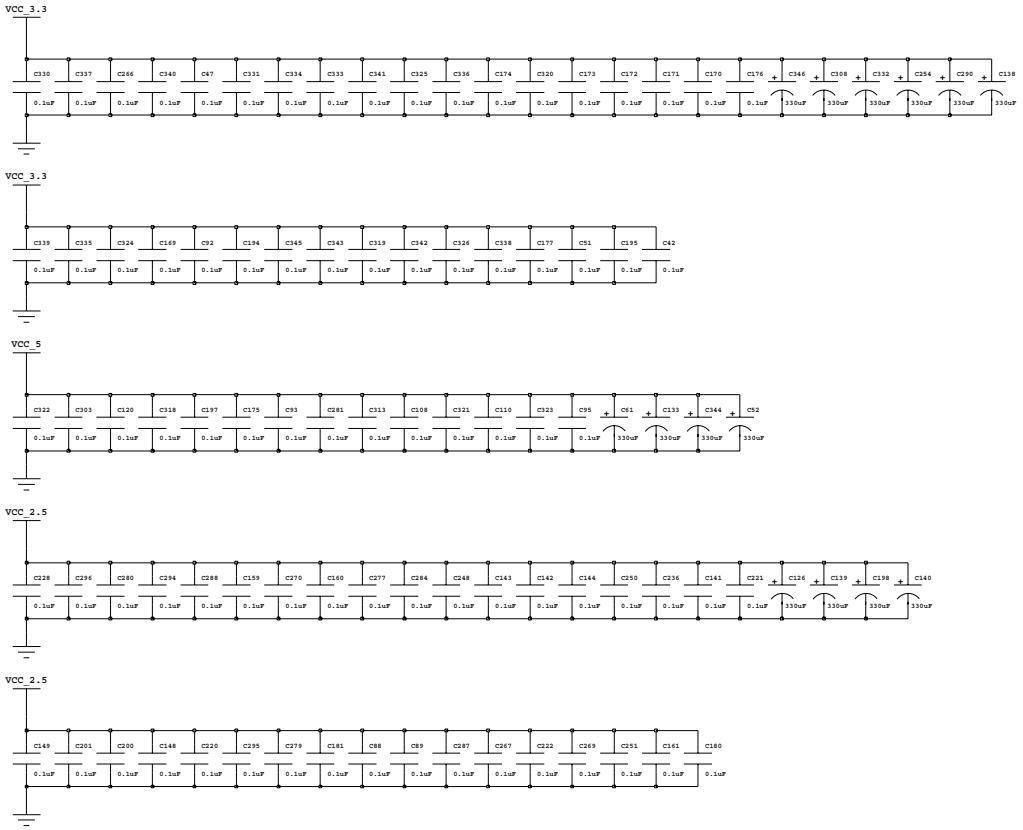
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:28:57 am	Title: Flash Memory + Flash Emulator	Page: 33



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:29:11 am	Title: Local Bus NVRAM/Debug Connectors	Page: 34

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:29:23 am	Title: --reserved--		Page: 35

GLOBAL BYPASS CAPS.
Add or subtract based on density.



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 11/8/2005 Time Changed: 10:29:37 am	Title: Bypass Capacitors	Page: 36

Appendix E
CDS Carrier BOM, Rev. 1.3

This appendix provides CDS Carrier BOM for Rev. 1.3.

Item Number: 750-21600
Description: SUB ASSEMBLY, SCHEMATIC PARTS,700-21600. CARRIER 1.3
Item Revision: C ECO13129

Item	Description	Qty	Ref Des	Notes
1	SUB ASSEMBLY, SCHEMATIC PARTS,700-21600. CARRIER 1.3			
2	CAP CER 0.01UF 50V 10% X7R 0402	38	C286,C360-C396	
3	CAP TANT ESR=0.035 OHMS 330UF 10V 20% -- 7343-43	13	C52,C133,C138-C140,C198,C254,C290,C308,C310,C332,C344,C346	
4	CAP TANT 10UF 16V 10% -- 6032-28	2	C60,C69	
5	CAP CER 10UF 16V +80%/-20% Y5V 1210	9	C117,C162,C165,C255,C257,C282,C298,C300,C302	
6	CAP TANT 22UF 16V 10% -- 6032-28	1	C285	
7	CAP TANT 47UF 16V 10% -- 7343-31	1	C132	
8	CAP CER 47PF 50V 5% C0G 0402	1	C211	
9	CAP CER 0.10UF 16V 10% X7R 0402	238	C8,C16,C25,C27,C36,C39,C41-C43,C45-C48,C50,C51,C53,C57,C58,C66-C68,C70-C72,C77,C78,C84,C85,C92-C95,C97,C100,C102,C105,C108,C110-C116,C118-C125,C130,C131,C137,C141-C145,C147-C157,C159-C161,C163,C164,C166-C191,C194,C195,C197,C199-C207,C209,C210,C213-C233,C236-C246,C248-C253,C256,C258-C277,C279-C281,C283,C284,C287,C288,C294-C296,C299,C301,C303,C309,C311-C331,C333-C343,C345,C401-C414,C418,C419	
10	CAP CER 1000PF 50V 10% X7R 0402	21	C17,C26,C33,C40,C49,C59,C63,C64,C74,C75,C81,C98,C101,C103,C104,C106,C415-C417,C420,C421	
11	CAP CER 10UF 16V 10% X5R 0805	7	C353-C359	
12	CAP CER 1.0UF 10V +80%/-20% Y5V 0603	5	C34,C35,C128,C129,C134	
13	CAP ALEL 220UF 4.0V 20% -- 7343	14	C62,C86,C87,C127,C136,C146,C192,C212,C278,C289,C291,C292,C297,C306	

14	CAP TANT LOW ESR 22UF 6.3V 10% 0805	7	C83,C196,C347-C351	
15	CAP TANT LOW ESR 68UF 25V CASE D	2	C352,C422	
16	IND FER BEAD 330OHM@100MHZ 2.5A 25%	8	FB8-FB15	
17	IND FER BEAD 100 OHM@100MHZ 3A -- 1206	4	FB4-FB7	
18	IND PWR CHK 1.06UH@100KHZ 16A 20% 0505	1	L2	
19	CON 8X10 RA SHLD SKT TH 2.5MM SP AU	1	P7	
20	CON 3 PWR PLUG RA SHRD TH -- AU	2	P5,P6	
21	CON 1X2 GIG MAG-JACK TAB-UP WITH LEDS	2	J18,J19	
22	HDR 2X5 TH 100 MIL CTR .100H AU	2	J1,J2	
23	CON DSUB 9POS PLUG RA	1	J15	
24	CON 2X20 SHRD SKT SMT 50MIL SP AU	2	J4,J5	
25	CON 2X13 SMT .05 IN CTR WITH KEY	1	J9	
26	CON 38 SKT 25MIL CTR AU	3	J14,J16,J17	
27	CON 10X40 SKT SMT 50MIL CTR AU	3	J3,J10,J11	
28	HDR 2 X 25 .050 CTR AU SMT	1	J13	
29	OSC 125.000MHZ VCO 3.3V SMT	1	Y1	
30	OSC 16.000MHZ VCO 3.3V SMT	1	U44	
31	OSC 19.440MHZ VCO 3.3V SMT	1	U27	
32	OSC 77.760MHZ FIXED 3.3V 7.0MM X 5.0MM	1	U22	
33	CON 1 PWR SKT TH -- --	2	GM1,GM2	
34	IC ATM-SONET AND POS SGL CHNL 155.52MBS --	1	U25	
35	IC MUX CLK 200MHZ 3-5.5V TSSOP 16	2	U56,U57	
36	IC VSUP 2 1.2-5.5V SOIC 8	4	U34,U37,U63,U64	
37	IC CTLR 8BIT 400KHZ 2.3-5.5V TSSOP 16	4	U48,U52,U53,U55	
38	IC BUF TS 1.65-5.5V SC-70	13	U3,U4,U26,U28,U30,U32,U33,U35,U36,U38,U39,U43,U45	
39	IC BUF 200MHZ 2.5/3.3V TQFP 32	1	U50	
40	IC XCVR SONET 4.75-5.25V SIP 1X9	1	U12	
41	IC BUF 400KHZ 2.7-5.5V MSOP 8	1	U2	
42	IC XCVR -- 5/3.3V SOIC 28	2	U16,U47	
43	IC LIN SW 32BIT:16BIT 500MHZ 2.3-3.6V TSSOP 56	6	U7,U8,U17,U18,U20,U21	Unsolder and lift up the IC lead of U7, pin 4 away from the pad on the PCB. Please make sure pins 3 and pin 5 of U7 is not shorted
44	IC LIN SW 2BIT:1BIT 500MHZ 2.3-3.6V TSSOP 16	2	U19,U41	
45	IC BUF DRV 16BIT TS 1.65-3.6V TSSOP 48	2	U40,U46	
46	IC VREG LDO ADJ VOLTAGE 3A S-PAK-5	1	U67	
47	IC BUF 0.25NS 3-3.6V TSSOP 16	2	U9,U11	
48	IC XCVR MULTIMODE LOW COST 1 X 9 PKG	1	U13	
49	IC CLOCK GEN 200MHZ 3-5.5V SSOP 28	1	U42	
50	IC BUS SWITCH LOW VOLTAGE QSOP20	3	U58,U59,U62	
51	IC VREG LDO 2IN ADJ 1.5A 1.4-6.5V S-PAK 5	1	U66	
52	IC LIN COMP 2 2-36V SOIC 8	1	U68	
53	IC MEM SRAM 8KX8 3.3V POWERCAP 34	1	U51	
54	POWER CAP MODULE WITH CRYSTAL SM, ROHS COMPLIANT	1	U51A	

55	IC XCVR QUAD GIG E HSLBGA364 ROHS COMPLIANT	1	U65
56	IC LIN AMP HIGH SIDE CURRENT SENSING SOT-23	1	U14
57	IC LIN NON ISOLATED DC/DC CONVERTER DIP 12	1	U80
58	IC ATM-SONET PHY -- 3.3V SBGA 304	1	U23
59	IC FPGA 150K GATE 3.3V BGA-256	1	U24
60	IC,EEPROM,NOR FLASH,4MX16,CMOS,TSSOP,48PIN,PLASTIC, ROHS COMPLIANT	2	U49,U54
61	IC MEM EEPROM 8192X8 400KHZ 2.7-5.5V SOIC 8	1	U1
62	LED GRN SGL 2.2V 20MA 0603	2	D9,D10
63	LED RED SGL 1.8V 25MA 0603	20	D1-D8,D11-D22
64	RES MF 22.1 OHM 1/16W 1% 0402	34	R250-R283
65	RES MF 100 OHM 1/16W 0.1% 0402	12	R36,R37,R121,R132,R137,R140,R144,R170,R171,R175,R178,R179
66	RNET BUS 8 1.0K 1/16W 5% 1608	4	RN1,RN5-RN7
67	RNET BUS 8 4.7K 1/16W 5% 1608	4	RN2-RN4,RN8
68	RES MF 5.6K 1/16W 5% 0402	1	R216
69	RES MF 150 OHM 1/16W 1% 0402	4	R100-R102,R249
70	RES MF 158 OHM 1/16W 1% 0402	4	R106-R109
71	RES MF 15.0 OHM 1/16W 1% 0402	3	R145,R159,R160
72	RES MF 2.00K 1/16W 1% 0402	1	R131
73	RES MF 2.70 OHM 1/16W 1% 0402	2	R116,R138
74	RES MF 301 OHM 1/16W 1% 0402	5	R97,R98,R110,R113,R120
75	RES MF 49.9 OHM 1/16W 1% 0402	36	R86-R89,R217-R248
76	RES MF 4.70 OHM 1/16W 1% 0402	2	R99,R149
77	RES MF ZERO OHM 1/16W -- 0402	37	R56,R63,R67,R68,R74,R85,R104,R105,R111,R112,R114,R126,R127,R133,R134,R147,R154,R158,R161,R162,R284-R289,R304,R306-R311,R352,R383,R384,R387
78	RES MF ZERO OHM 1/8W -- 0805	3	R208-R210
79	RES MF 10K 1/16W 5% 0402	12	R75,R119,R122-R125,R128-R130,R296-R298
80	RES MF 100K 1/16W 5% 0402	5	R135,R153,R163,R294,R295
81	RES MF 220 OHM 1/16W 5% 0402	10	R28-R35,R78,R80
82	RES MF 330 OHM 1/16W 5% 0402	14	R53,R54,R59,R60,R79,R81,R373-R380
83	RES MF 4.7K 1/16W 5% 0402	65	R47,R48,R51,R52,R57,R58,R82-R84,R92-R96,R103,R115,R118,R136,R141-R143,R151,R152,R155-R157,R168,R183-R185,R189-R196,R199,R200,R314-R320,R355-R372
84	RES MF 47 OHM 1/16W 5% 0402	8	R343-R350
85	RES MF 33 OHM 1/16W 5% 0402	12	R146,R148,R164-R167,R173,R174,R186,R197,R198,R351
86	RES MF 2.2K 1/16W 5% 0402	16	R321-R328,R332,R336-R342
87	RES MS 0.01 OHM 1.0W 1% 1206	3	R44,R313,R386
88	RES MF 10.0 OHM 1/8W 1% 0805	2	R150,R207

89	RES MF 2.7K 1/16W 5% 0402	2	R211,R212
90	RES MF 10.0 OHM 1/16W 1% 0402	3	R201-R203
91	RES MF 1.0K 1/16W 5% 0402	7	R25,R45,R46,R90,R117,R299,R385
92	RES MF 5.11K 1/16W 1% 0402	4	R290-R293
93	RES MF 511 OHM 1/16W 1% 0402	1	R215
94	RES MF 5.0 OHM 1/8W 5% 0805	1	R176
95	RES MF 4.75K 1/16W 1% 0402	1	R214
96	RES MF 147 1/16W 1% 0402	1	R213
97	SW SPST DIP 50V 100MA SMT	4	SW1-SW4
98	SW SPDT ULTRA-MIN PUSHBUTTOM GULL R ANGLE	3	SW5-SW7

Created By:
Create Time:

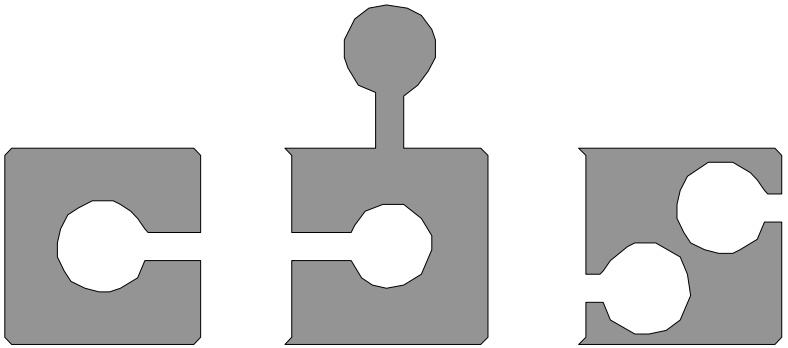
Appendix F
CDS Carrier Schematics, Rev. 1.3

This appendix provides CDS carrier board schematics for Rev. 1.3.

Table F-1 lists the hardware differences between carrier card Rev. 1.2 and Rev. 1.3.

Table F-1. Differences Between Carrier Card Rev. 1.2 and Rev. 1.3

Item No.	What is Changed on CDS Carrier Card Rev. 1.3	Schematic Sheet No.
1	Replace Cicada Quad PHY with MARVELL Quad PHY. Also added level shifters. All four Ethernet ports are connected with the PHY.	19–22
2	Moved all the IO card functionality except the USB port to the carrier. The USB port was not connected to anything on Rev. 1.2.	22
3	Replace the obsolete RC5051M DC-DC converter to Belfuse SRDB-30B1AH. It will convert 5 V to 2.5 V.	8
4	Update the existing clock structure to support MPC8555E SYSCLK and PCICLK signals.	9
5	Power pin filtering for clock drivers and oscillator.	9, 10
6	Remove IO card connector J7 (see schematic ver. 1.2a) since there is no RoHS compliant replacement from Samtec.	22
7	Replaced obsolete 77.76 MHz oscillator (U22) with a different package that has multiple source.	29
8	Convert BOM to use RoHS compliant part number (lead free)	All
9	Allow I2C communication with the Arcadia to gather information such as FPGA version from the Arcadia.	7, 18
10	Connect unused DIP switch pin to the FPGA for future use.	5, 6



Carrier

freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:00:46 pm	Title: Cover Story	Page: 01

Schematic Notes

1. Unless otherwise specified:
   All resistors are SMD0402, in ohms, 0.08W, +/-5%
   All capacitors are SMD0402, in microfarads (uF), +/-20%.
   All inductances are in microhenries (uH).
   All ferrites are Z=50 ohms at 100 MHz.
   All fuses are self-resetting polyswitch (PTC) devices.
   Board impedance is 55 +/- 5 ohms.

2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:

VCC_3.3	VCC_2.5	GND
VCC_5	VCC_1.2	VCORE

3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.

4. Freescale and the Freescale logo are registered trademarks of Freescale Semiconductor. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. For Kristi, with love.

5. The sheet-to-sheet cross reference format is:
   Sheet VertZoneLetter HorizZoneNumber

6. Components with the label "No_Stuff" are not to be installed by default; they are for test or manufacturing purposes only.

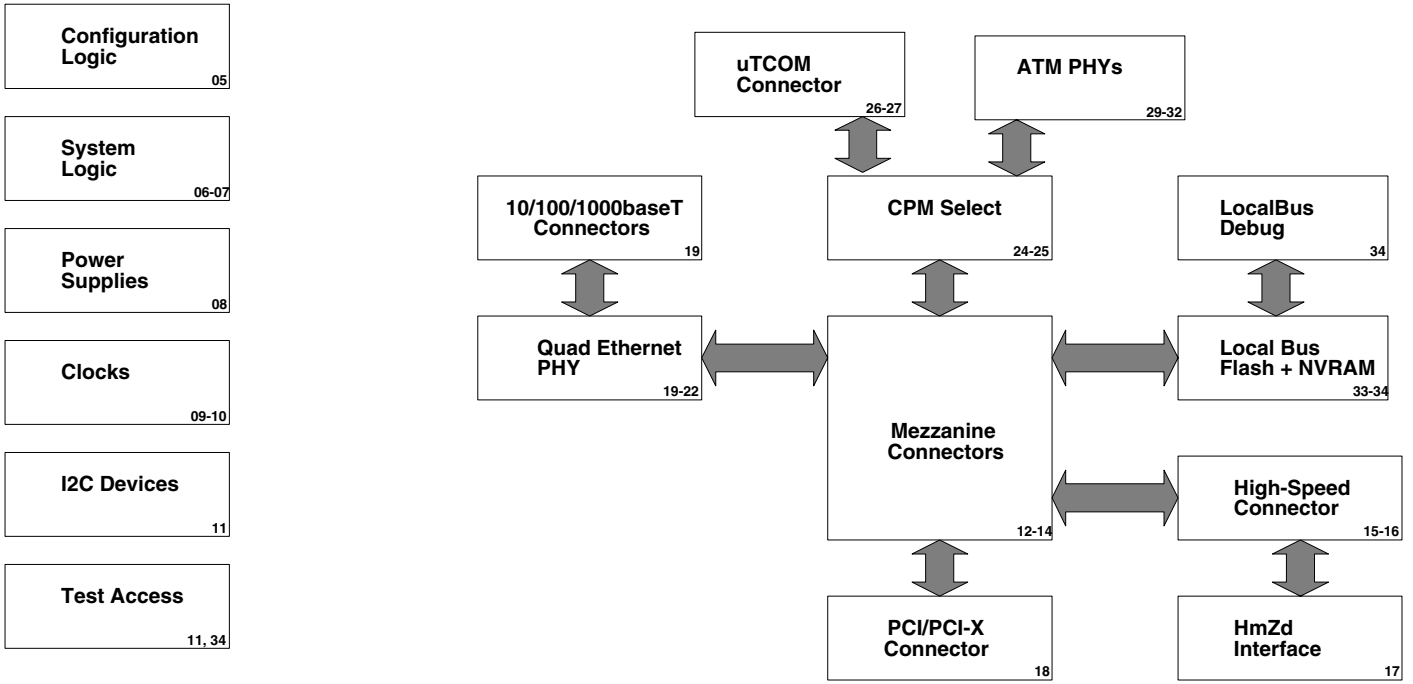
7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

Carrier

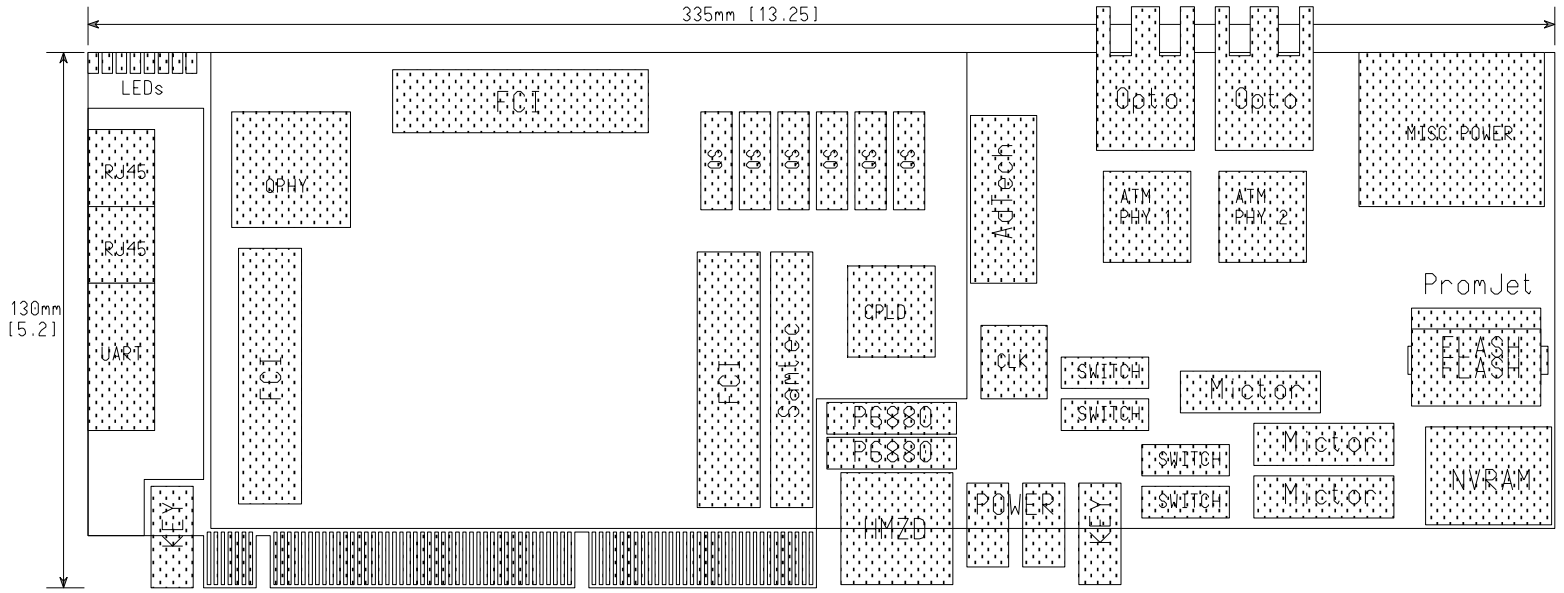
REV	DATE	CHANGES
V1.0	03Nov03	Initial version
V1.1	04Apr08	Errata fix; see errata.
V1.2	04Oct04	Errata fix; see errata.
V1.3	27Jan06	Replace Ethernet PHY, RoHS

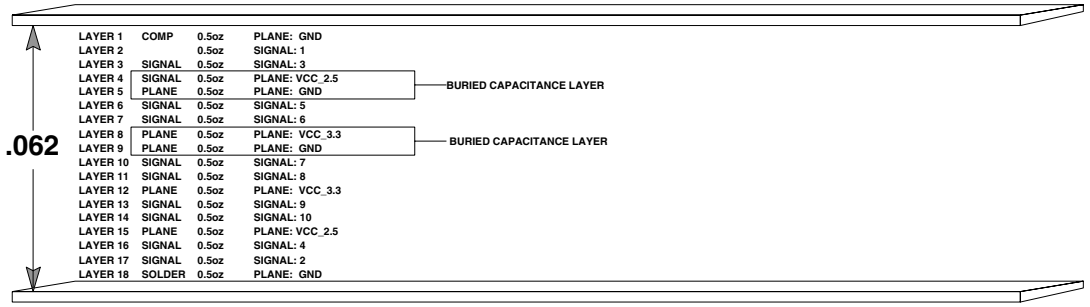
freescale™ semiconductor
Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

Project: CDS_Carrier
Revision: 1.3
Engineer: Gary Milliorn
Date Changed: 2/23/2006
Time Changed: 1:01:30 pm
Title: Information, please
Page: 02

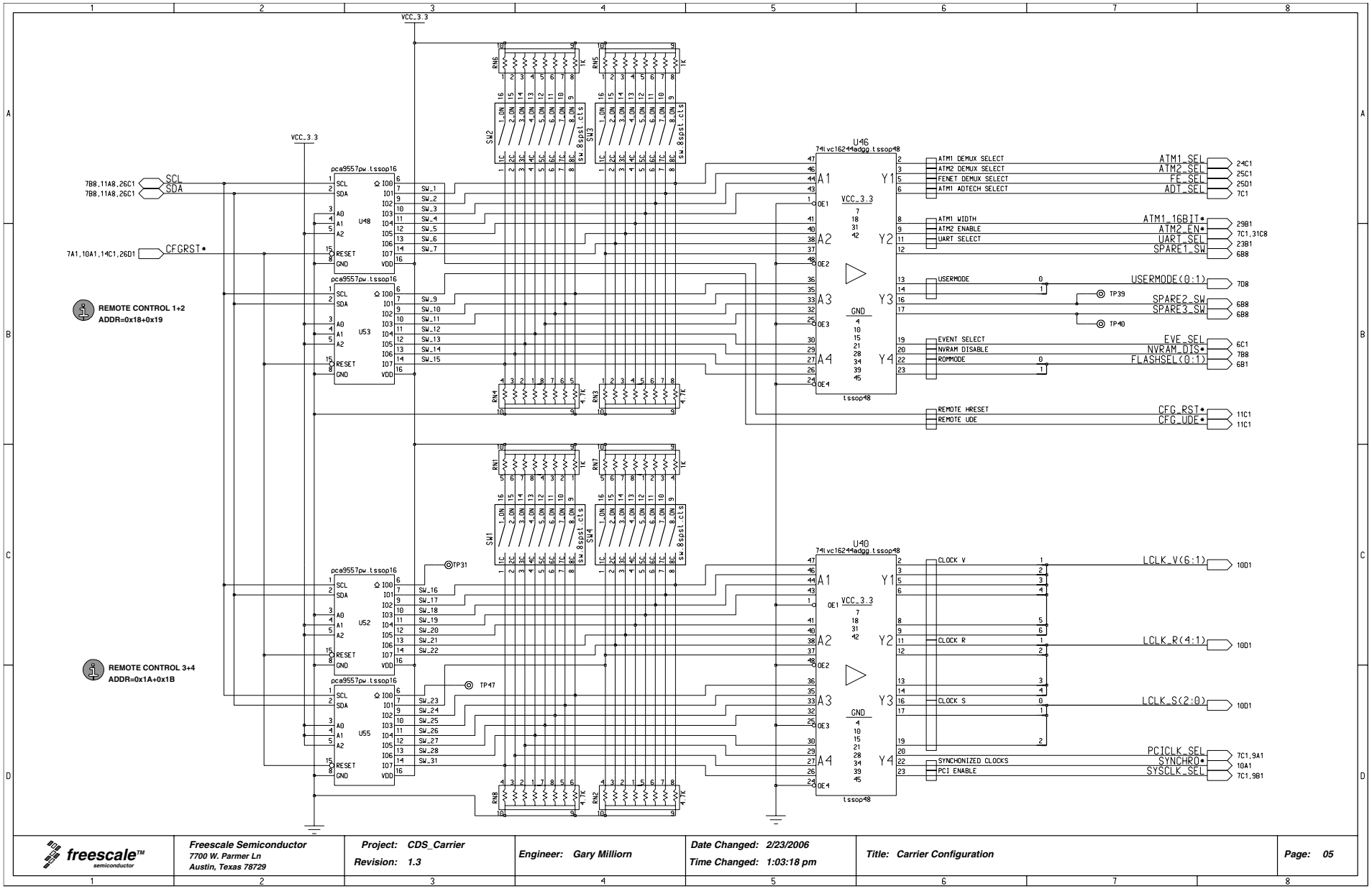


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:02:04 pm	Title: Block Diagram	Page: 03

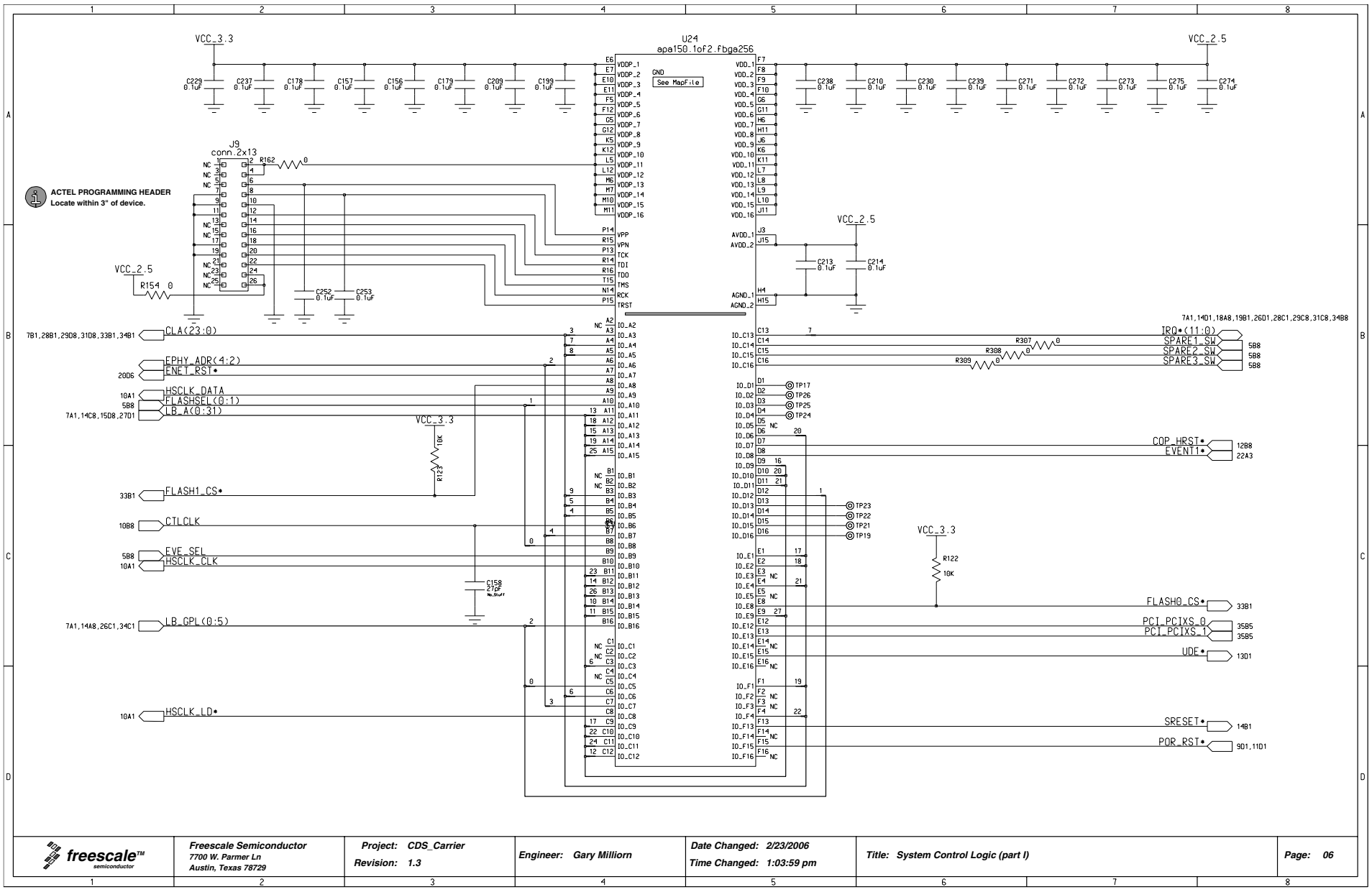




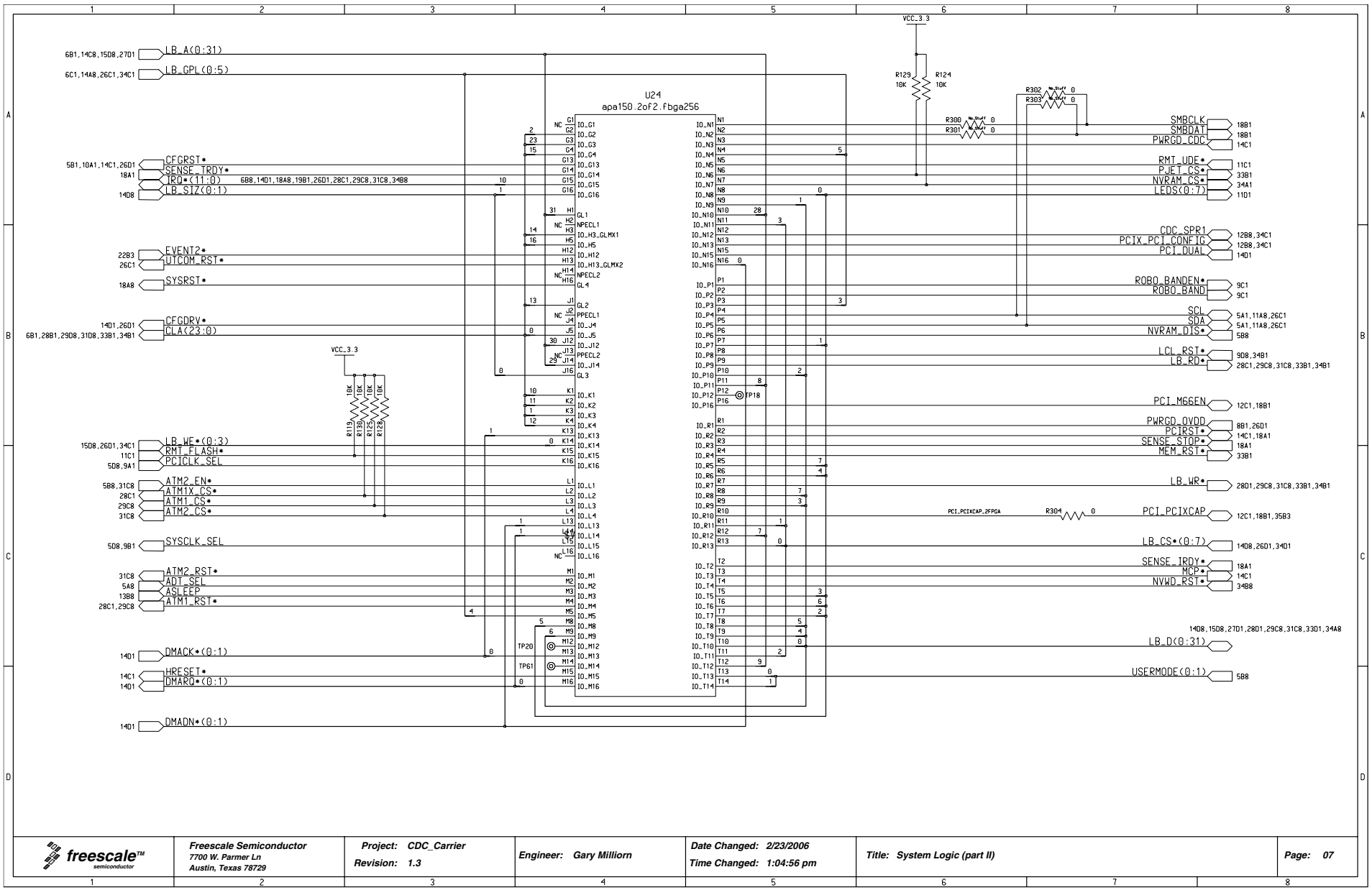
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:02:42 pm	Title: Placement (approximate) and PCB Stackup	Page: 04



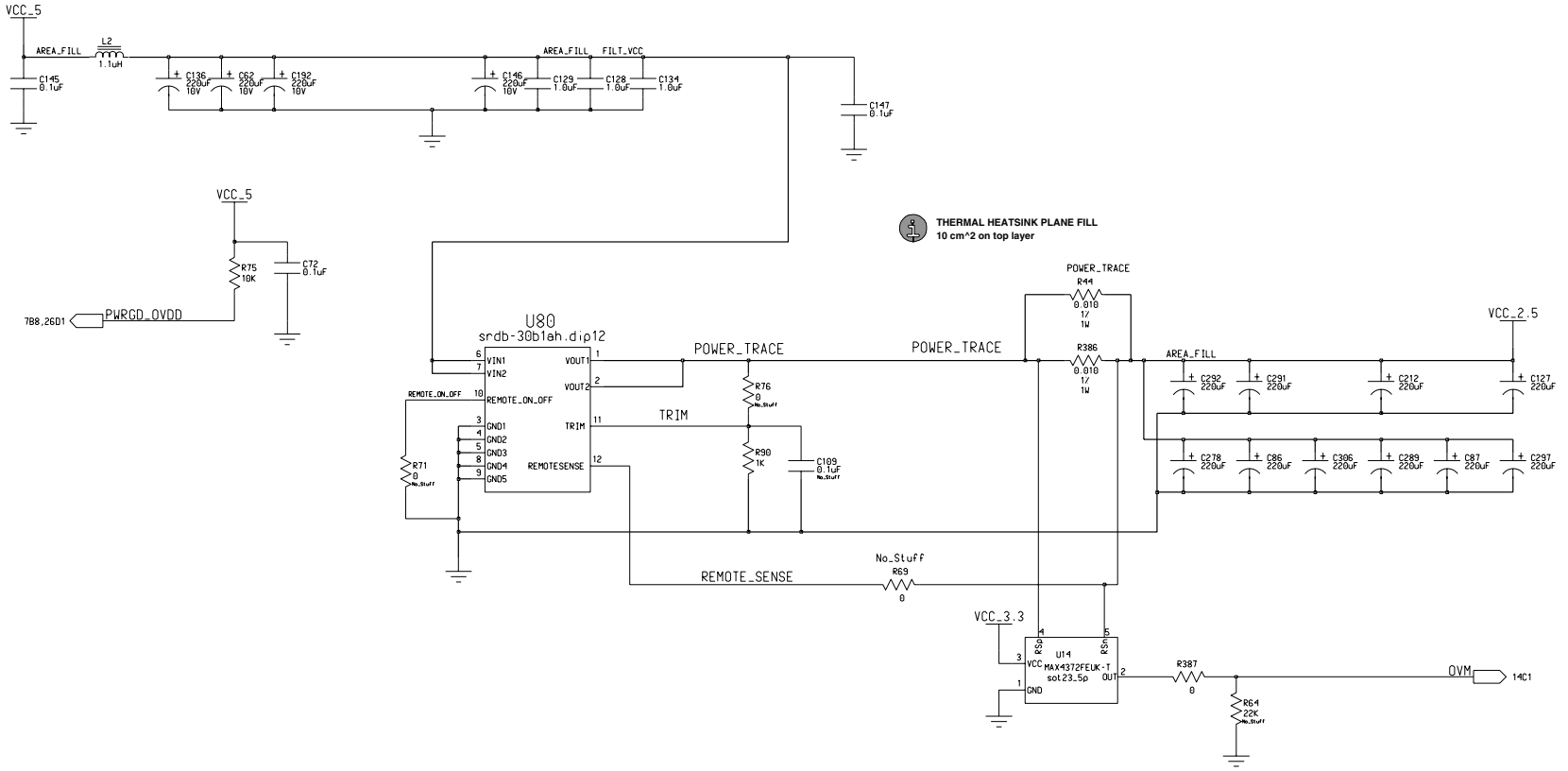
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:03:18 pm	Title: Carrier Configuration	Page: 05



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:03:59 pm	Title: System Control Logic (part I)	Page: 06



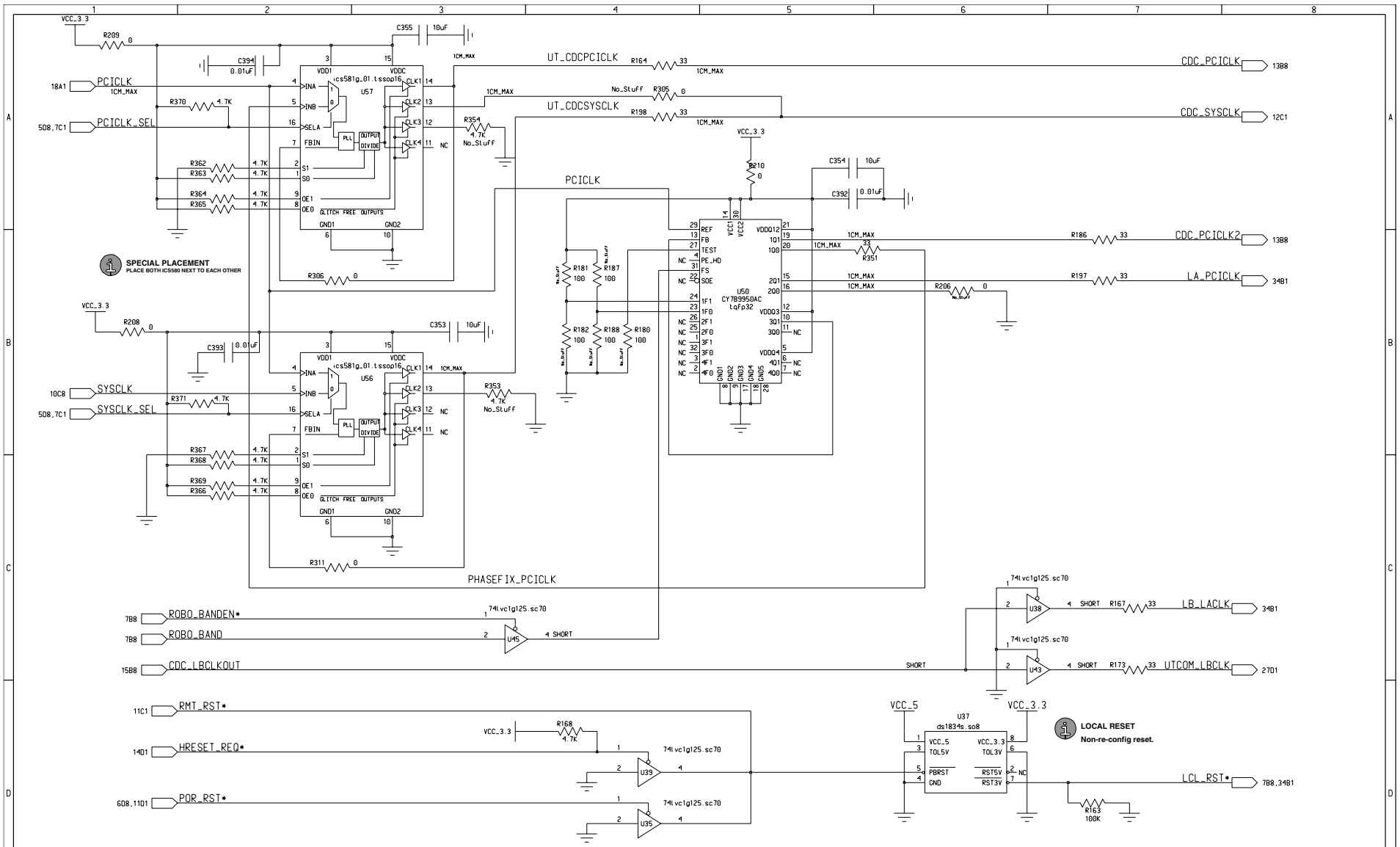
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:04:56 pm	Title: System Logic (part II)	Page: 07



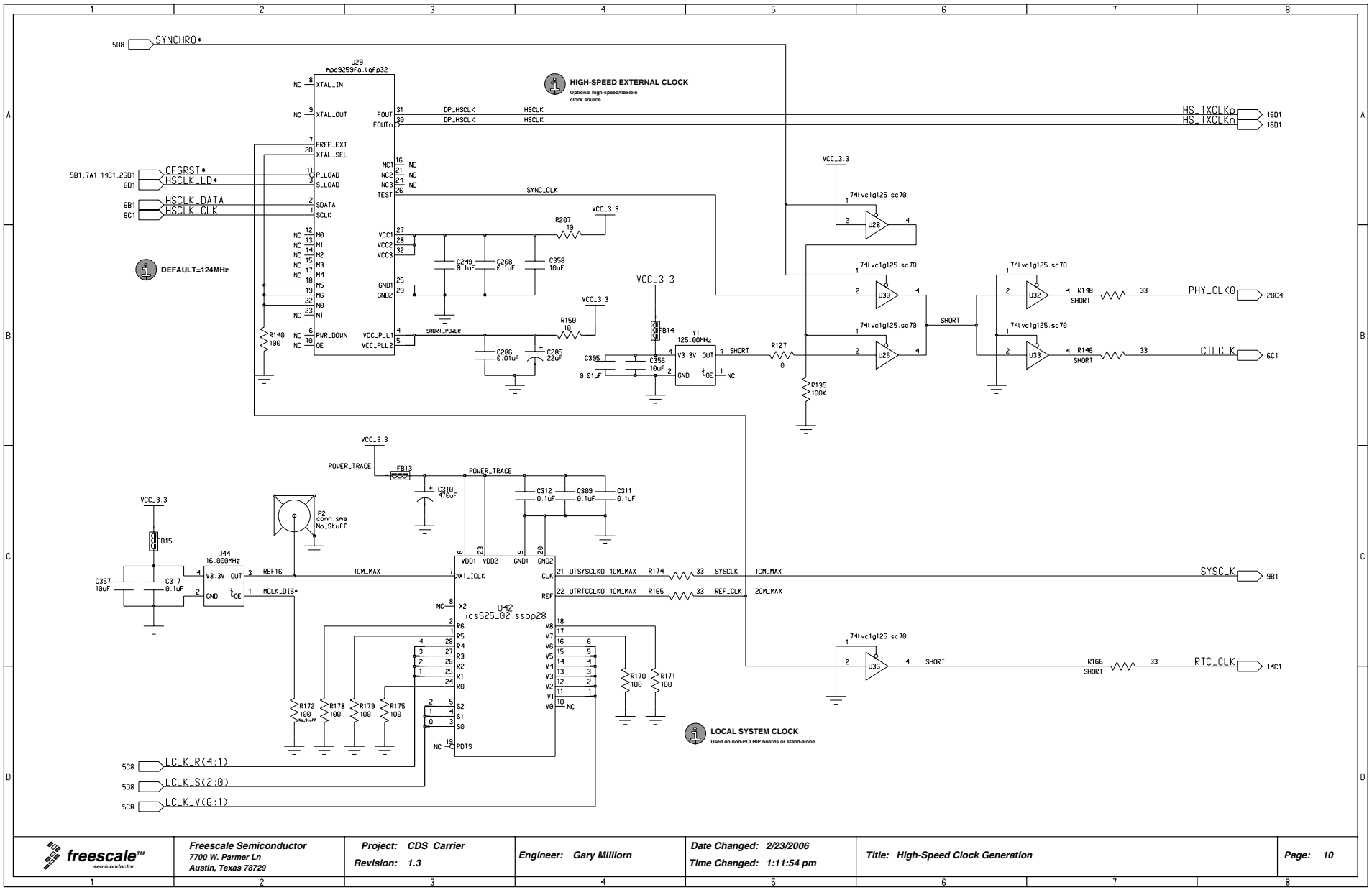
POWER SUPPLY LAYOUT RULES

1. All components in the power path (large/red bus) should be on the same layer, with area filled connections.
2. No vias or thermal reliefs allowed on power path components.
3. Ground plane connections should be made with two vias close to the component.

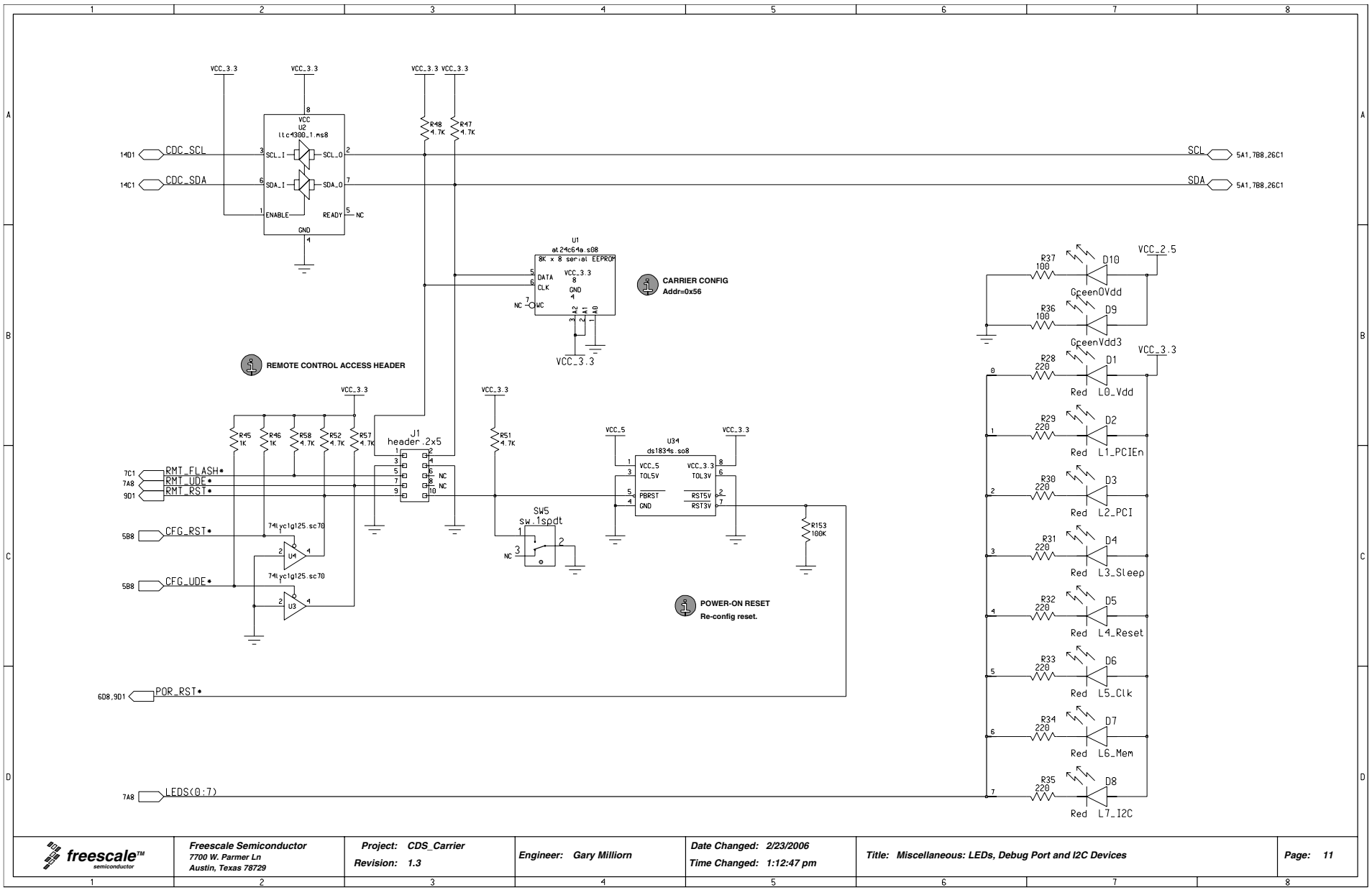
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:07:50 pm	Title: System +2.5V Power Supply	Page: 08



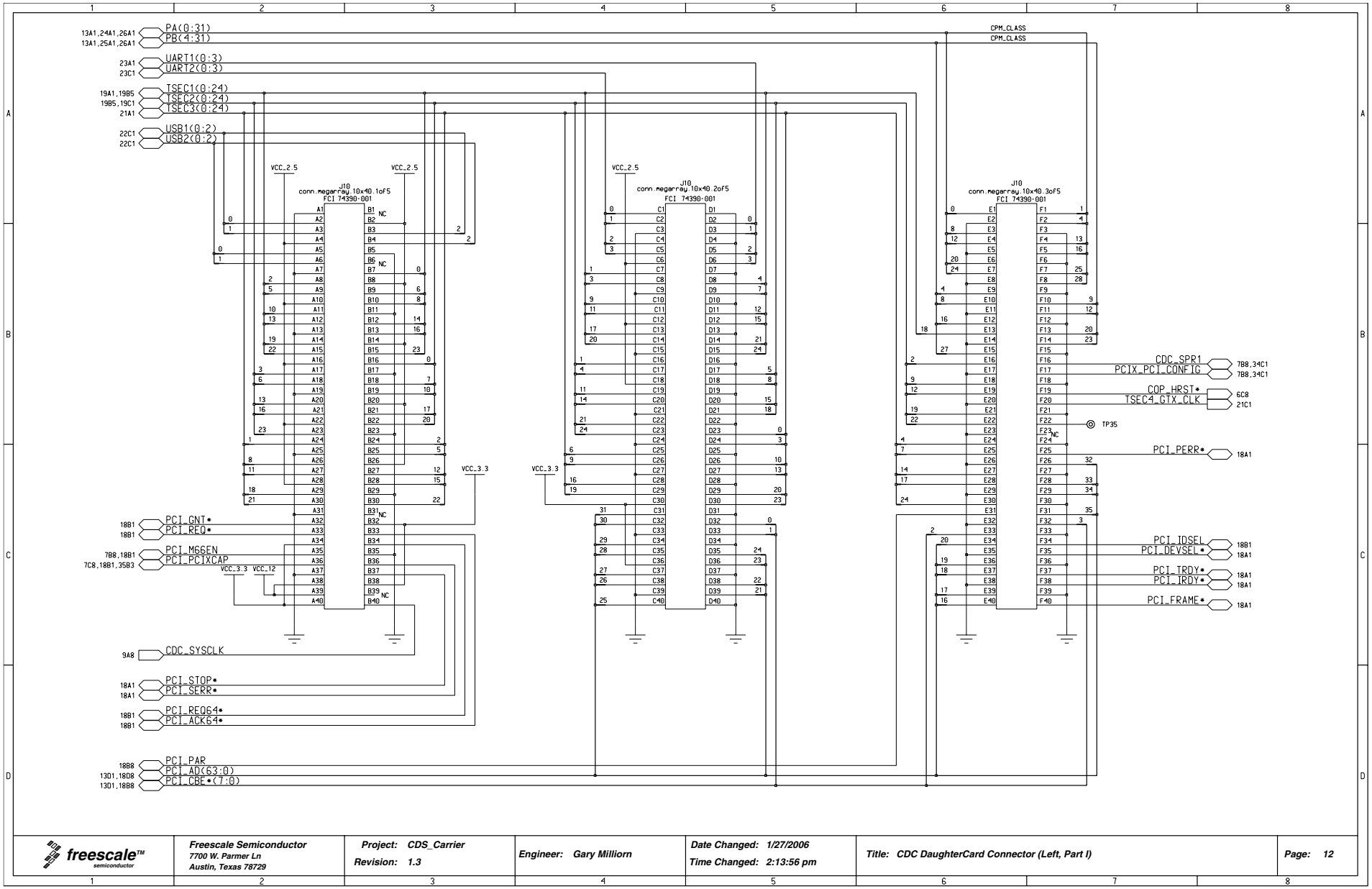
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:04:26 pm	Title: Local (non-PCI) Resources: System Clock, System Reset	Page: 09



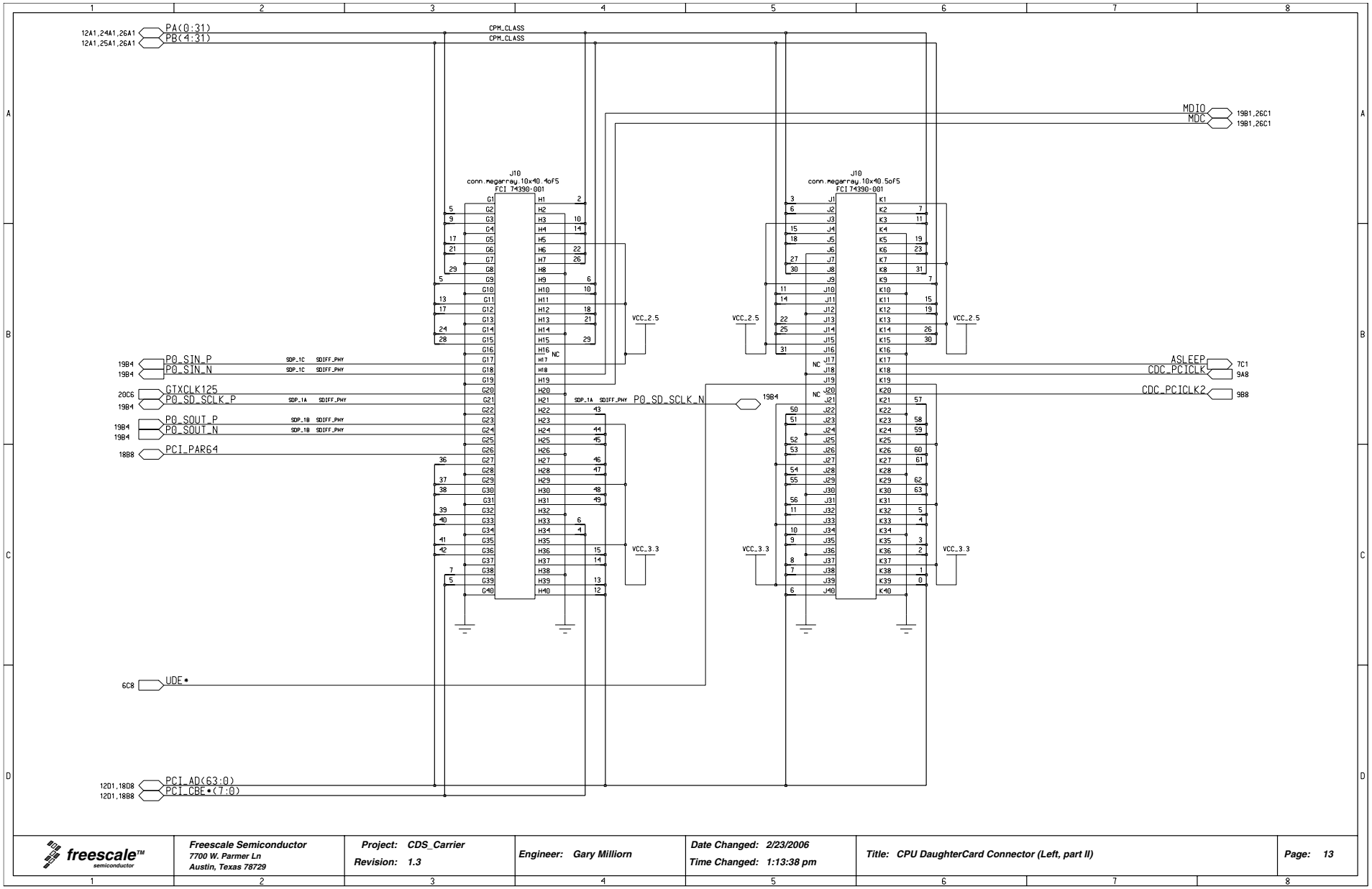
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:11:54 pm	Title: High-Speed Clock Generation	Page: 10



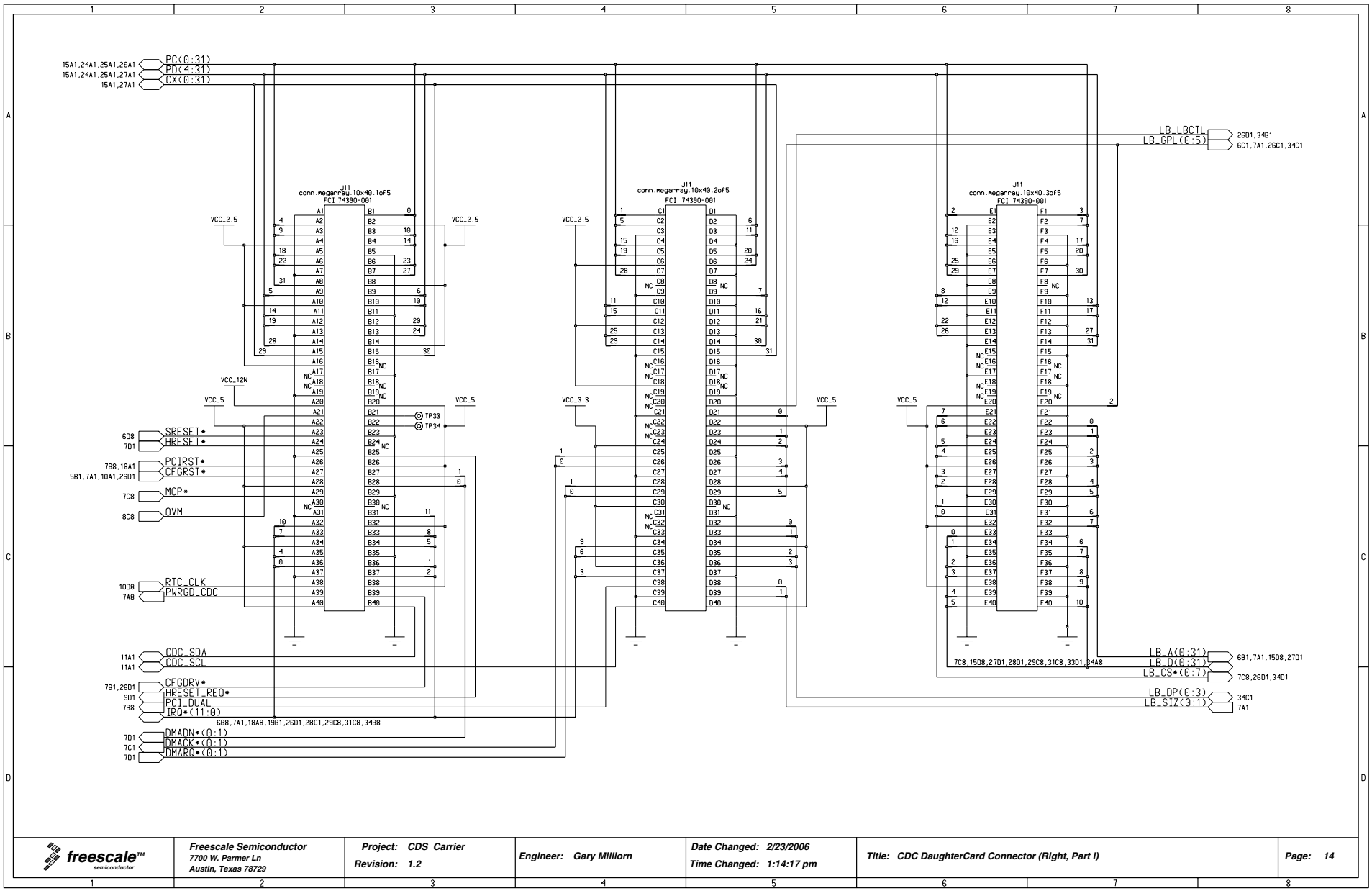
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:12:47 pm	Title: Miscellaneous: LEDs, Debug Port and I2C Devices	Page: 11



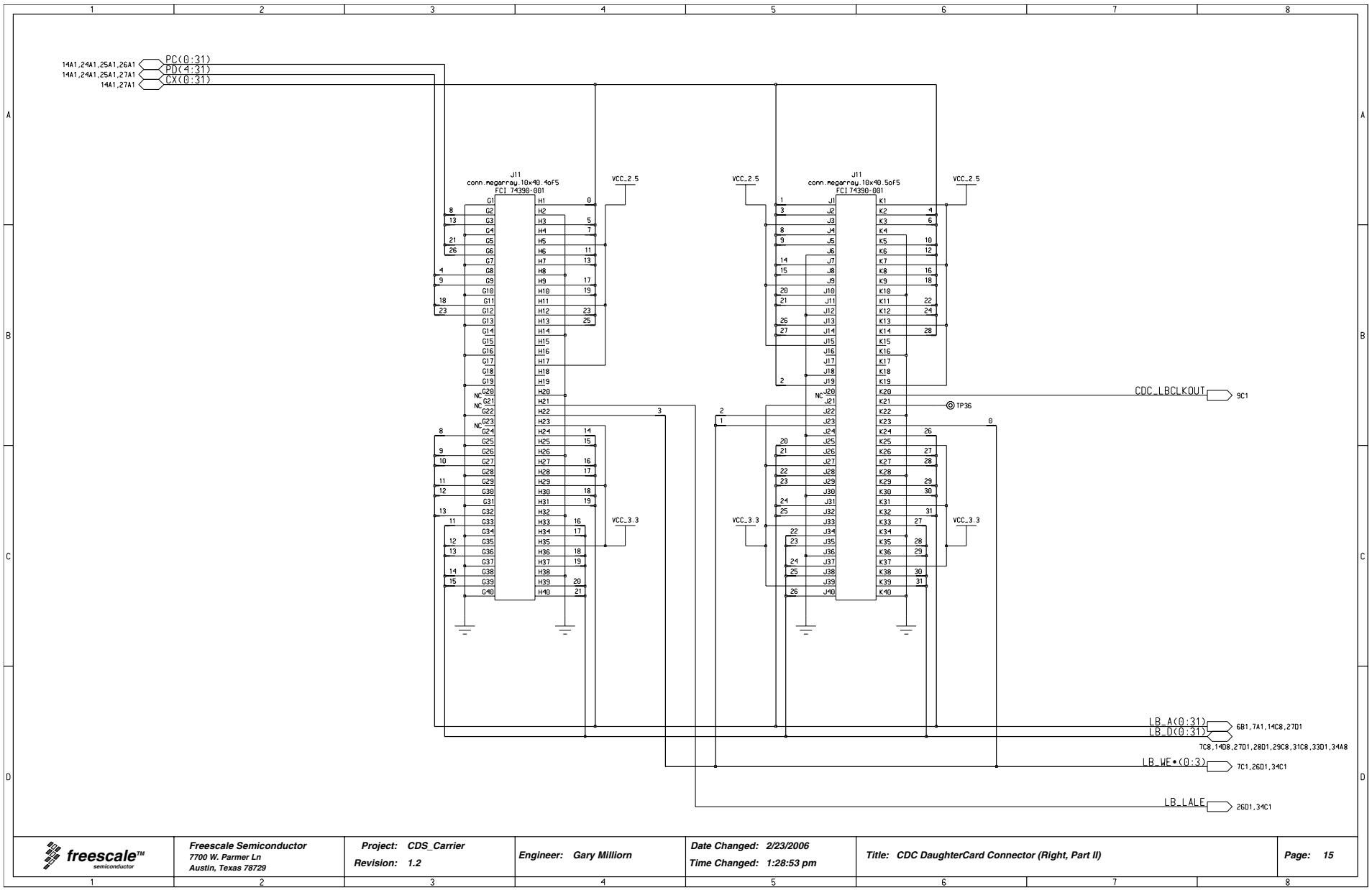
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 1/27/2006 Time Changed: 2:13:56 pm	Title: CDC DaughterCard Connector (Left, Part I)	Page: 12



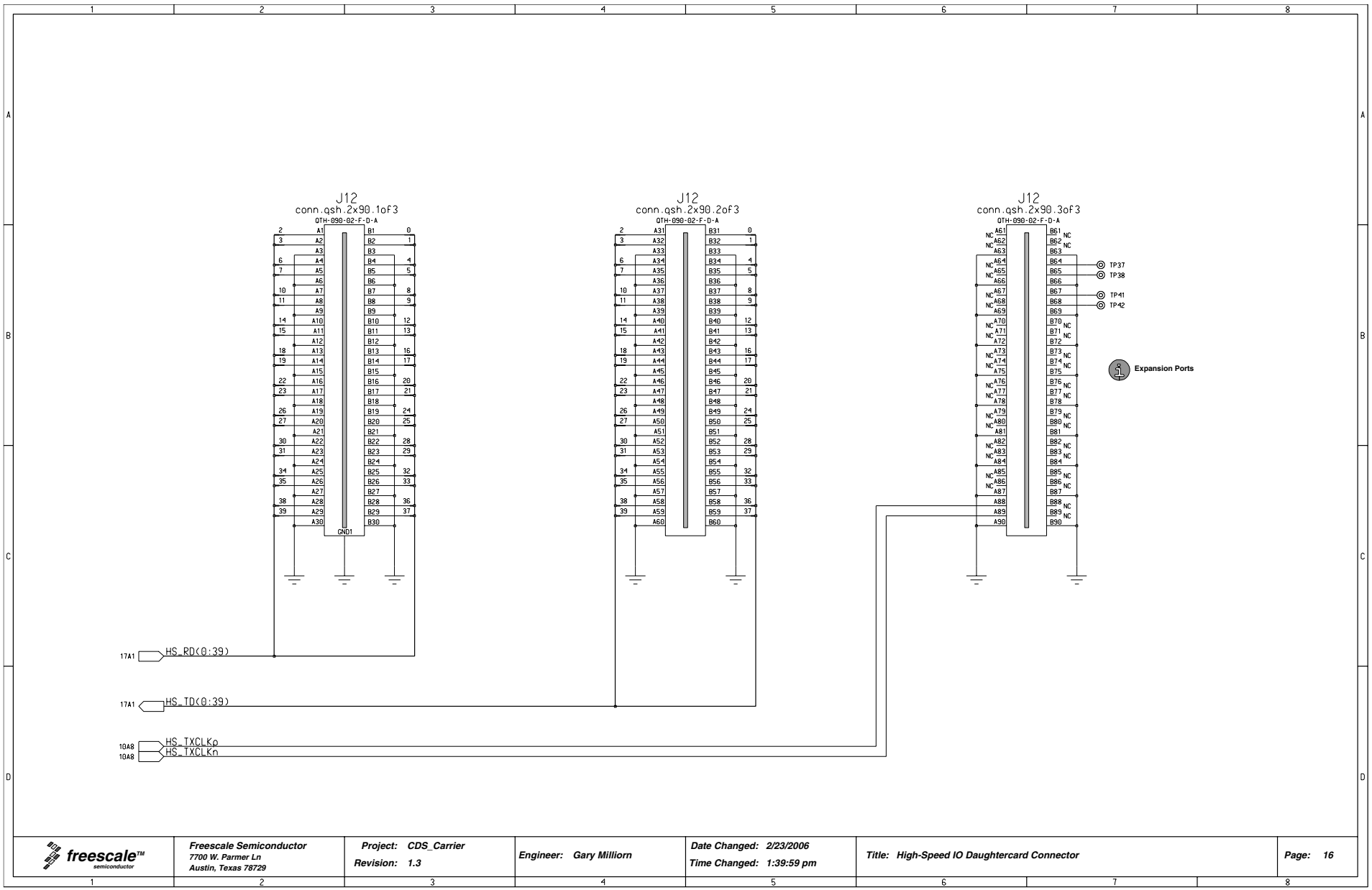
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:13:38 pm	Title: CPU DaughterCard Connector (Left, part II)	Page: 13



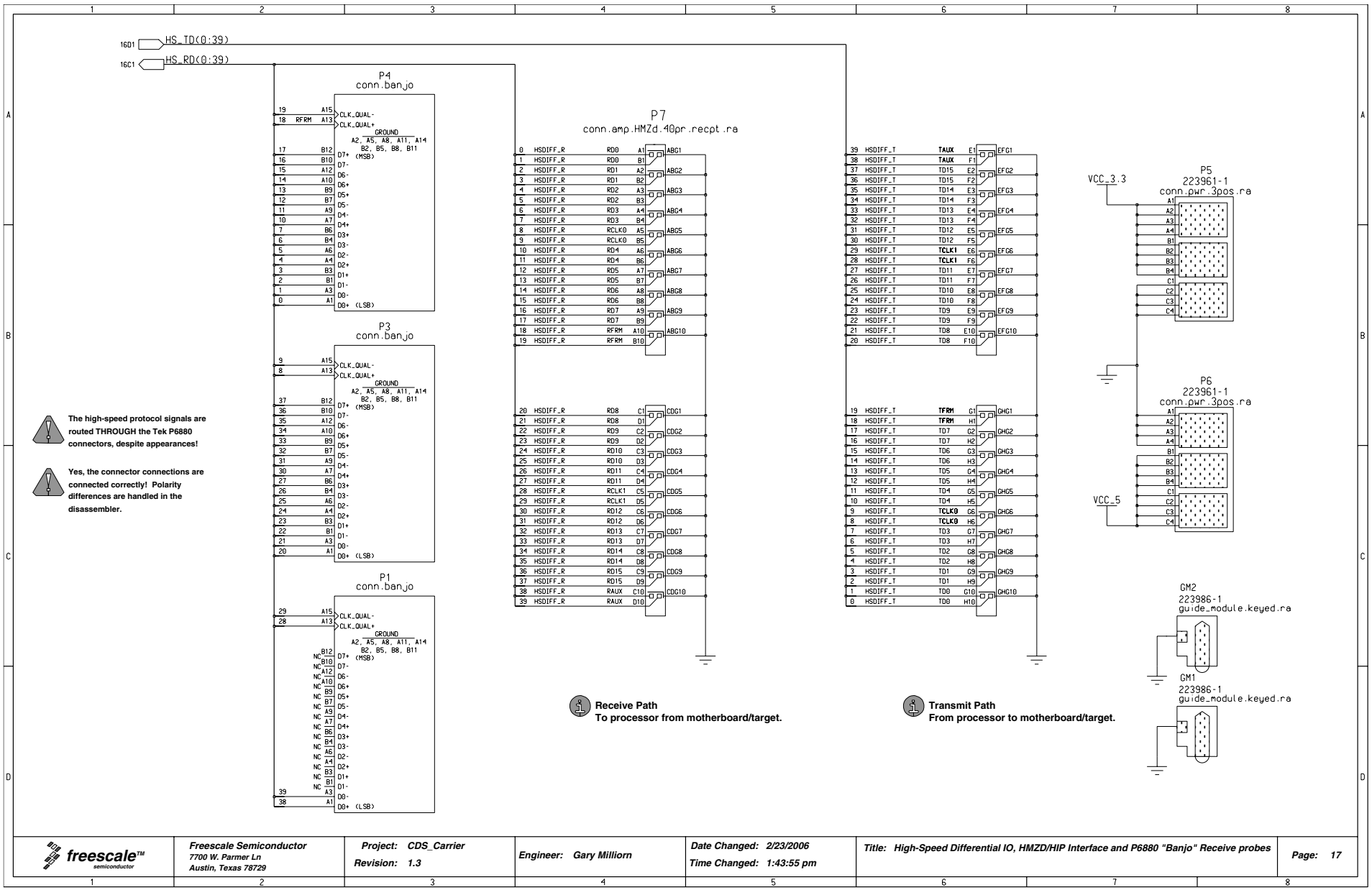
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:14:17 pm	Title: CDC DaughterCard Connector (Right, Part I)	Page: 14



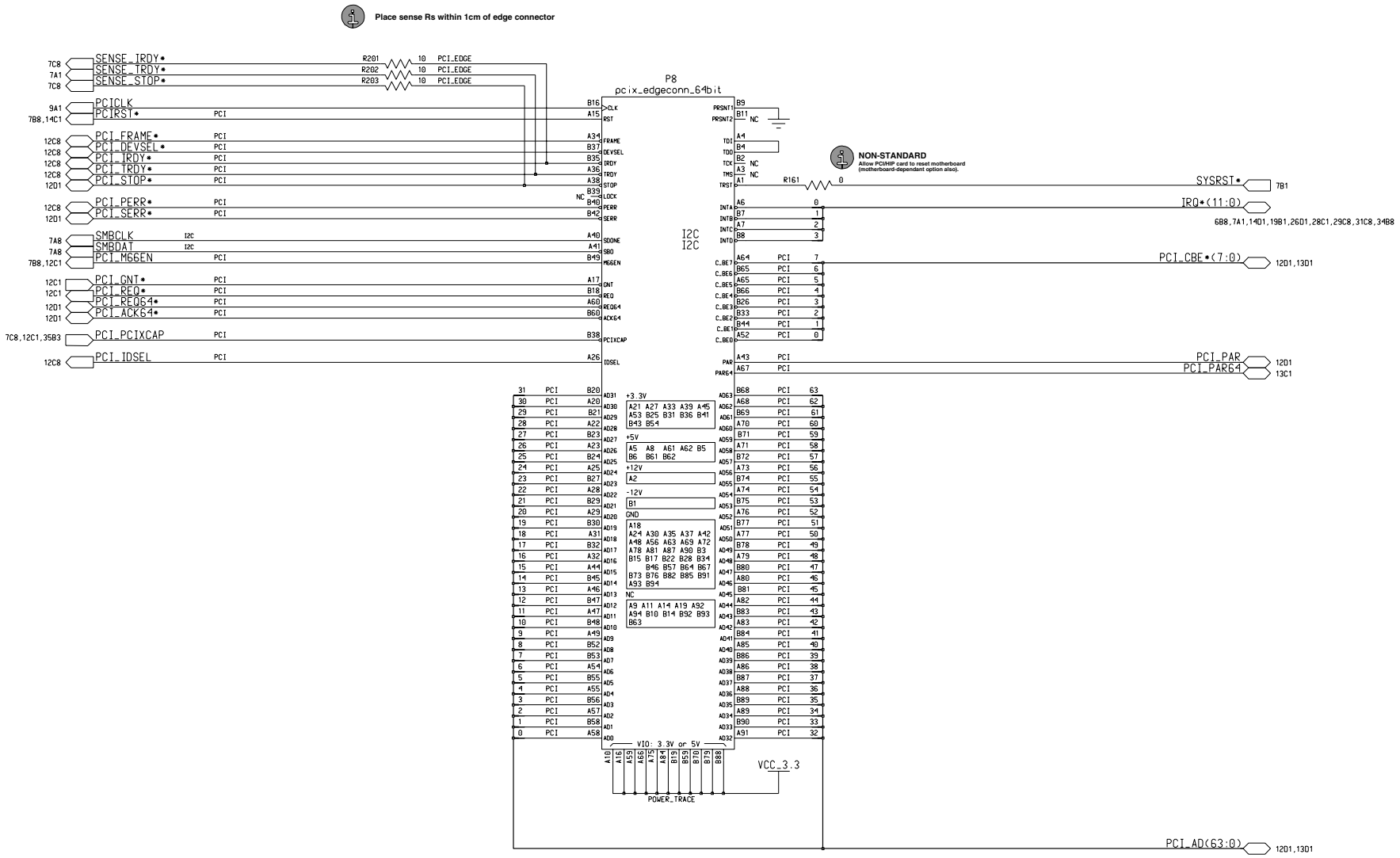
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:28:53 pm	Title: CDC DaughterCard Connector (Right, Part II)	Page: 15



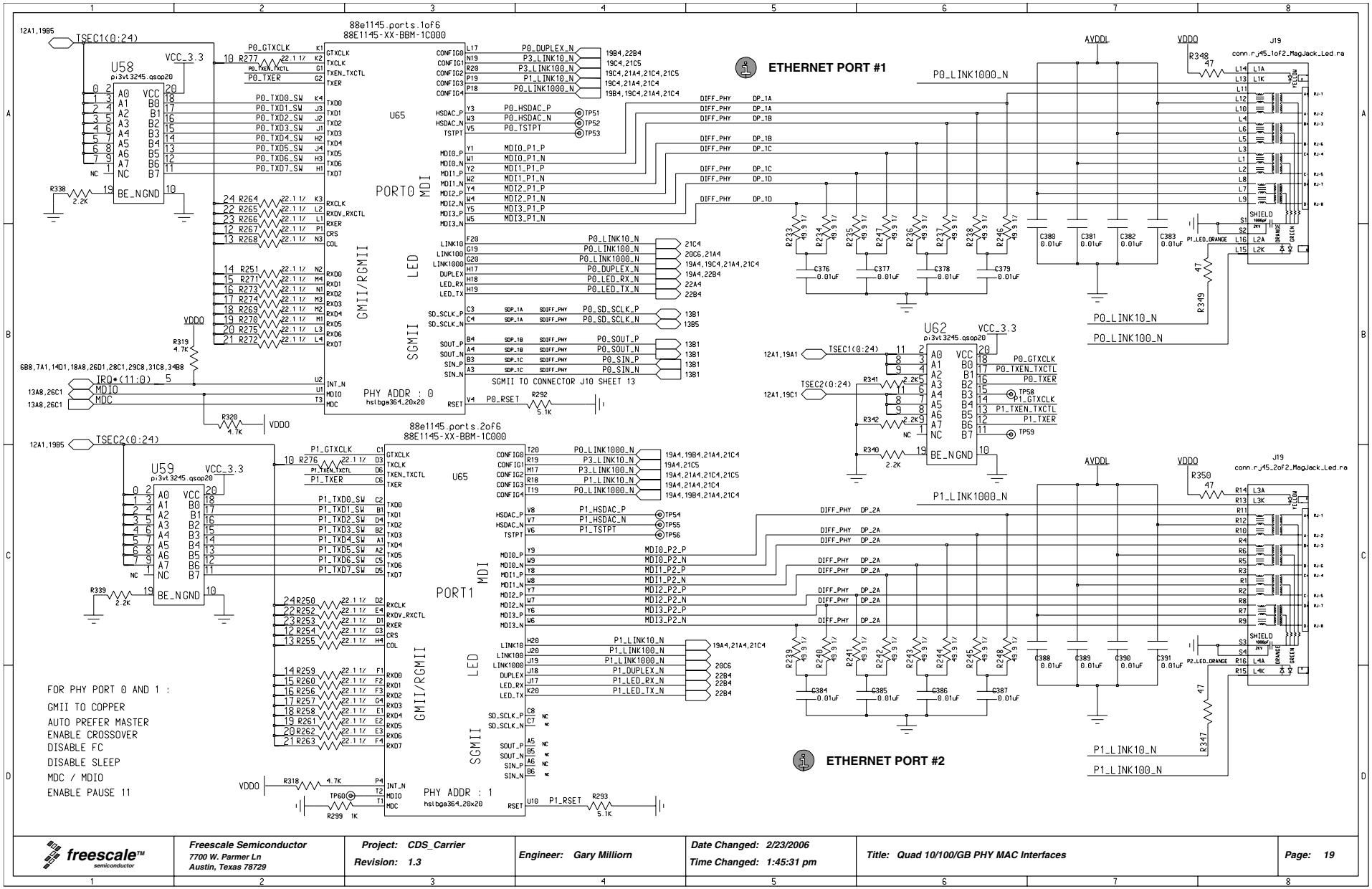
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:39:59 pm	Title: High-Speed IO Daughtercard Connector	Page: 16



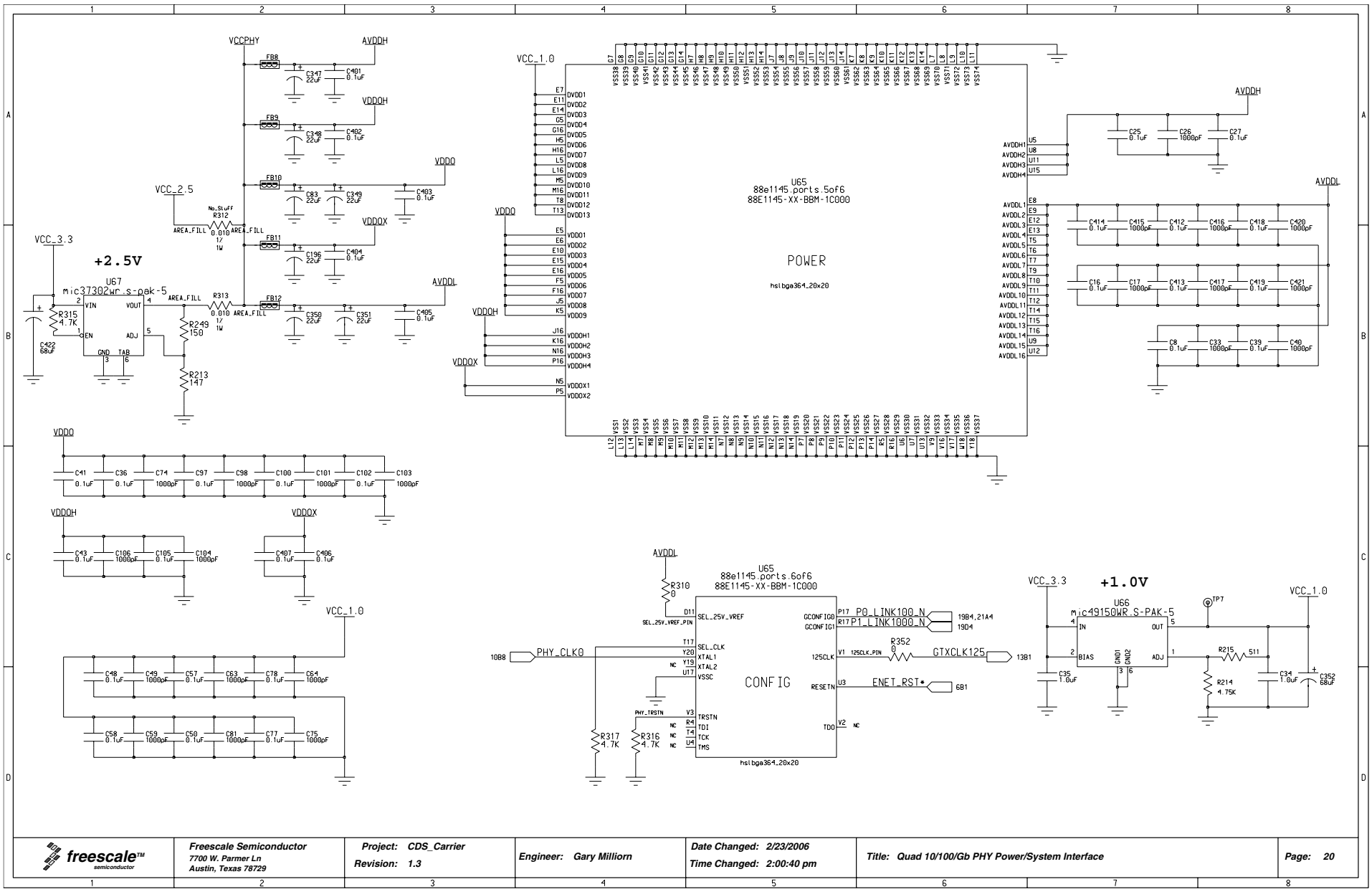
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:43:55 pm	Title: High-Speed Differential IO, HMZD/HIP Interface and P6880 "Banjo" Receive probes	Page: 17



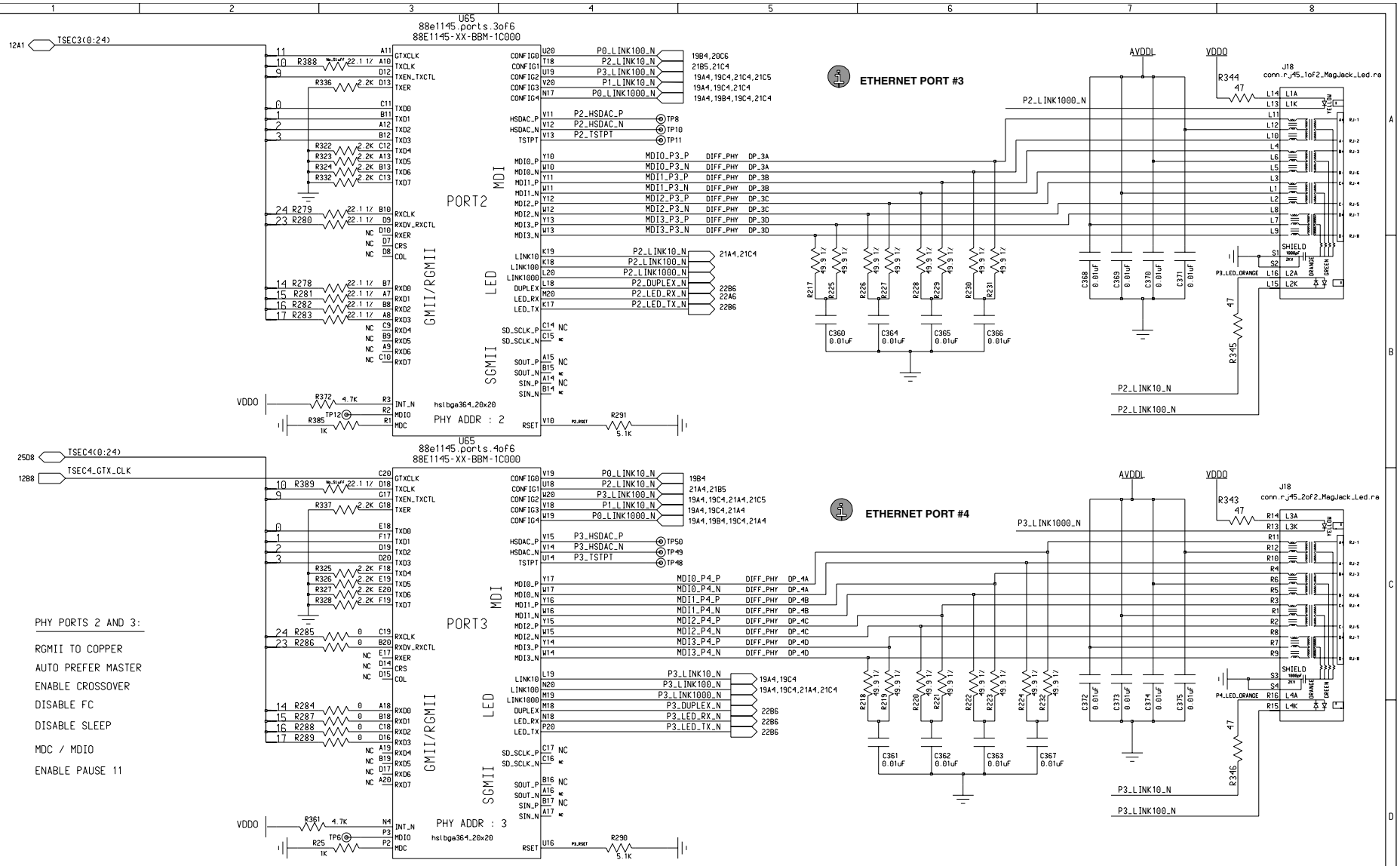
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:44:34 pm	Title: Primary PCI/PCI-X Edge Connector	Page: 18



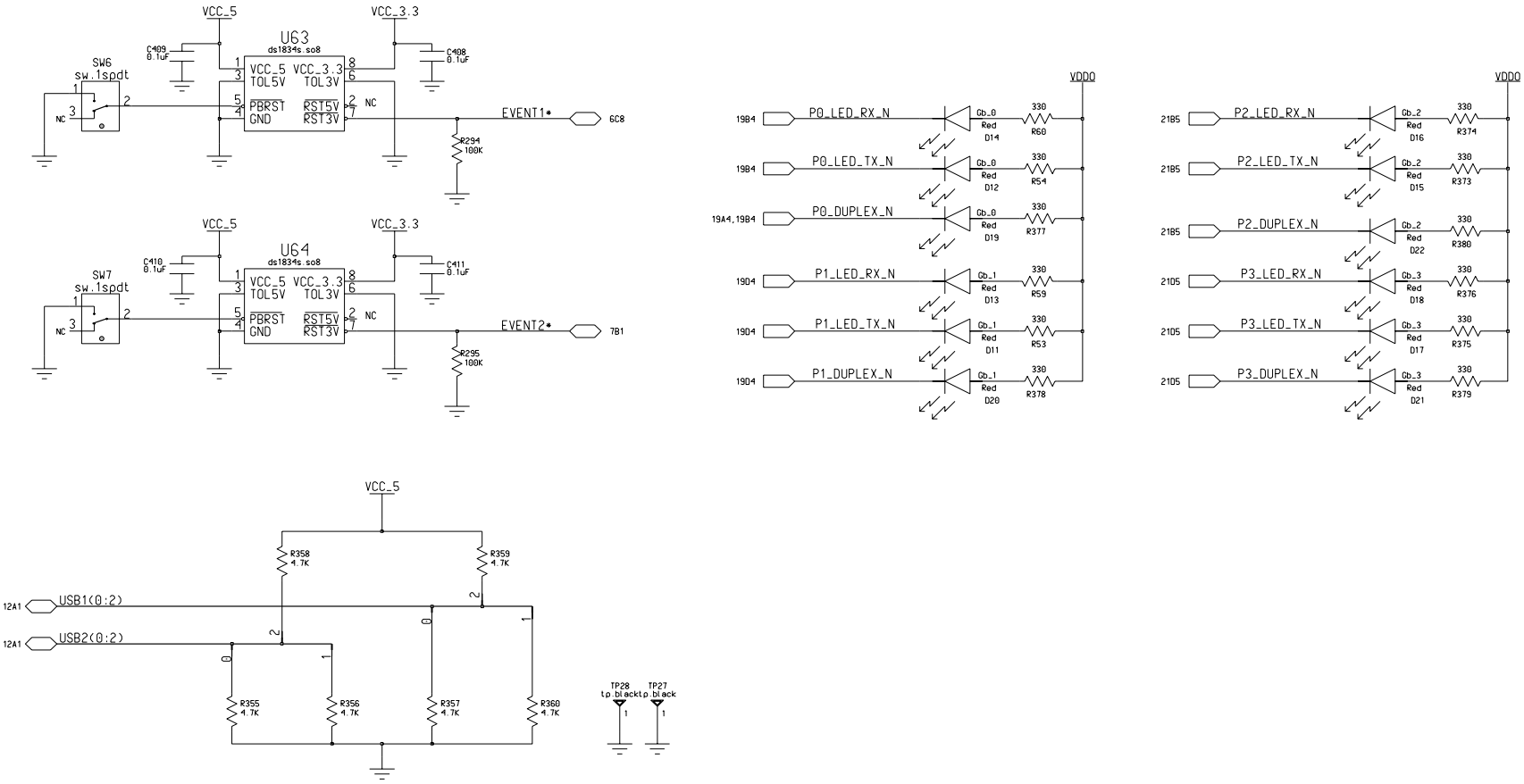
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 1:45:31 pm	Title: Quad 10/100/GB PHY MAC Interfaces	Page: 19



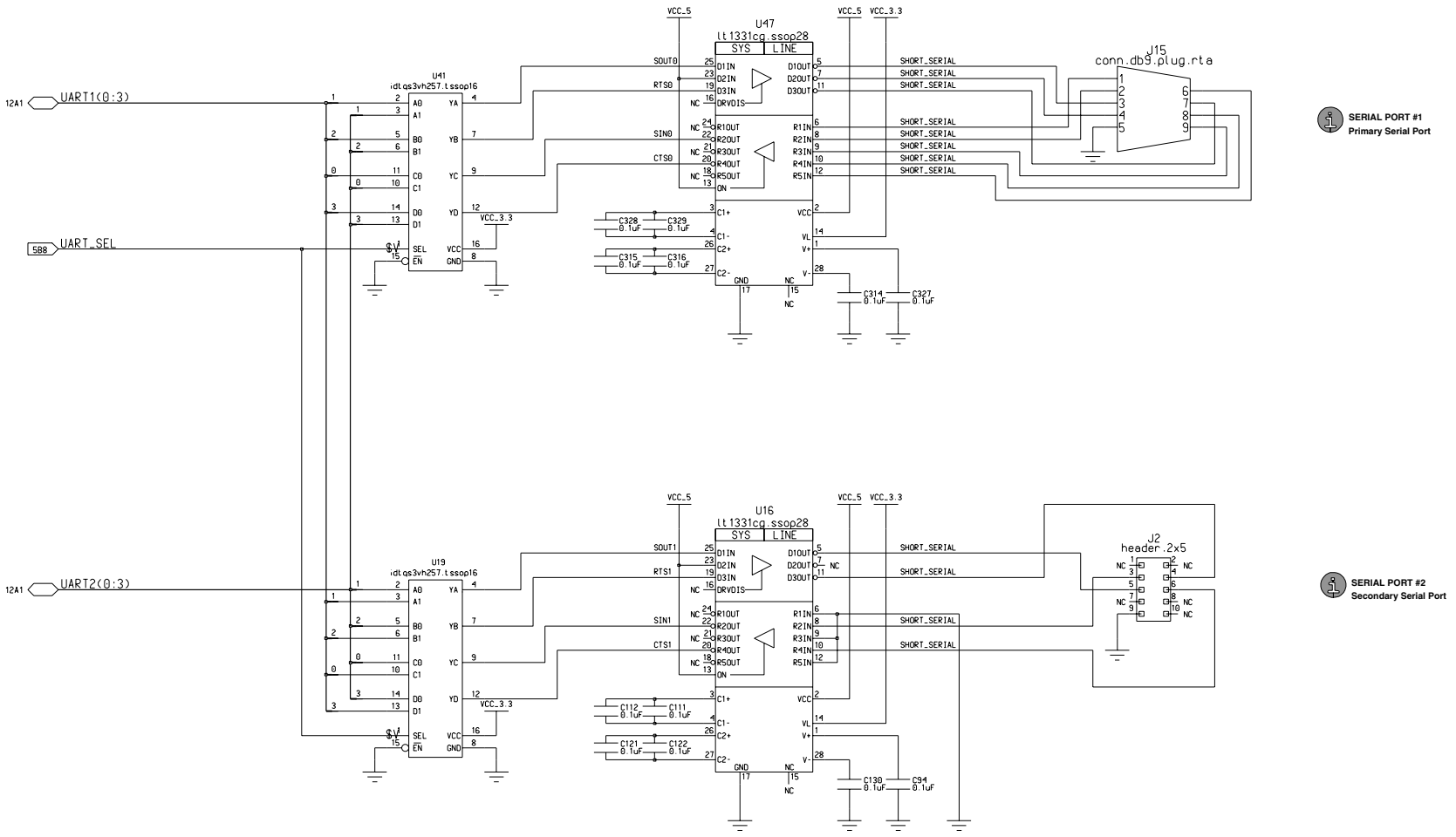
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:00:40 pm	Title: Quad 10/100/Gb PHY Power/System Interface	Page: 20



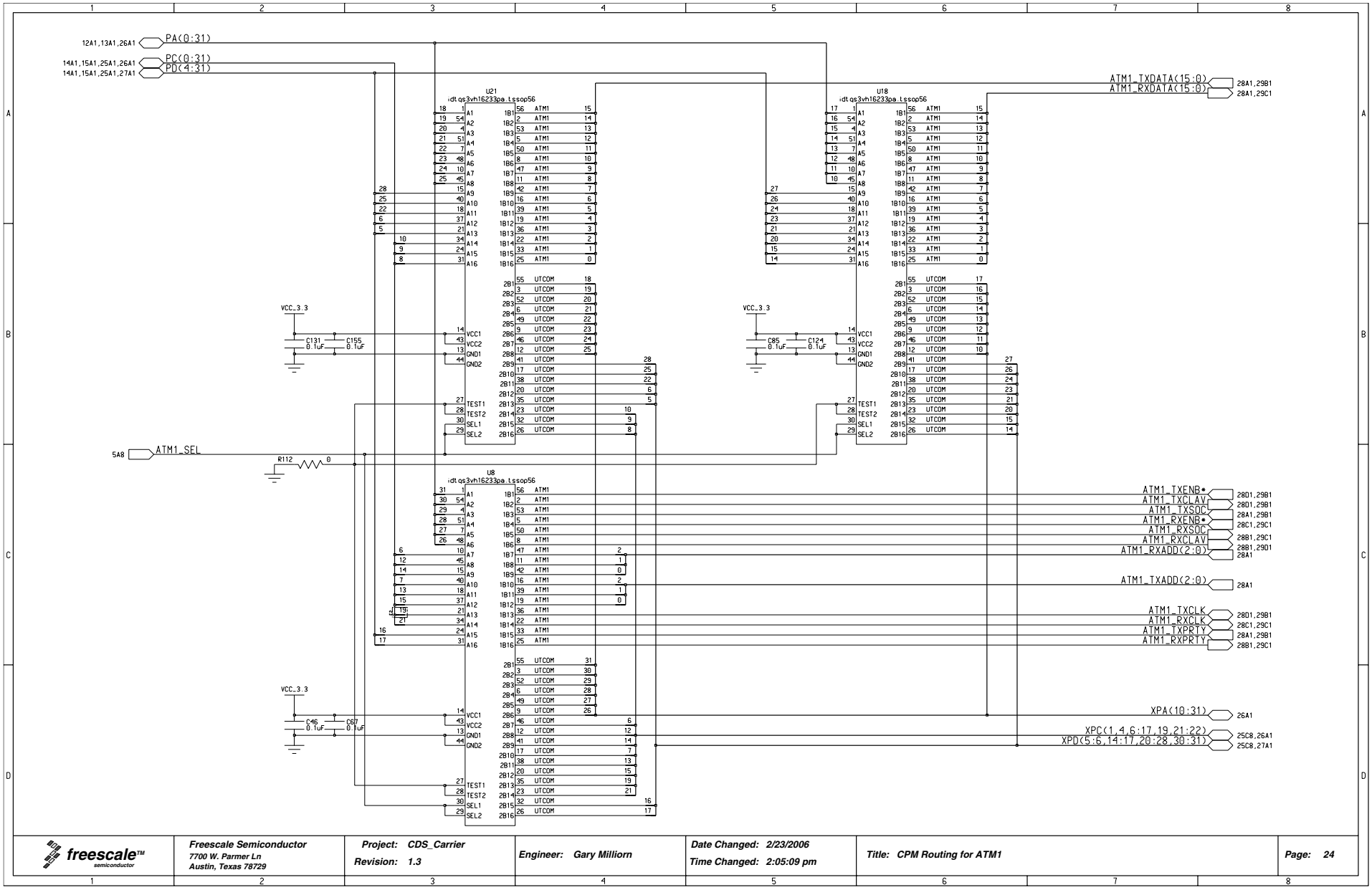
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:02:03 pm	Title: Ethernet Ports #3 and #4	Page: 21



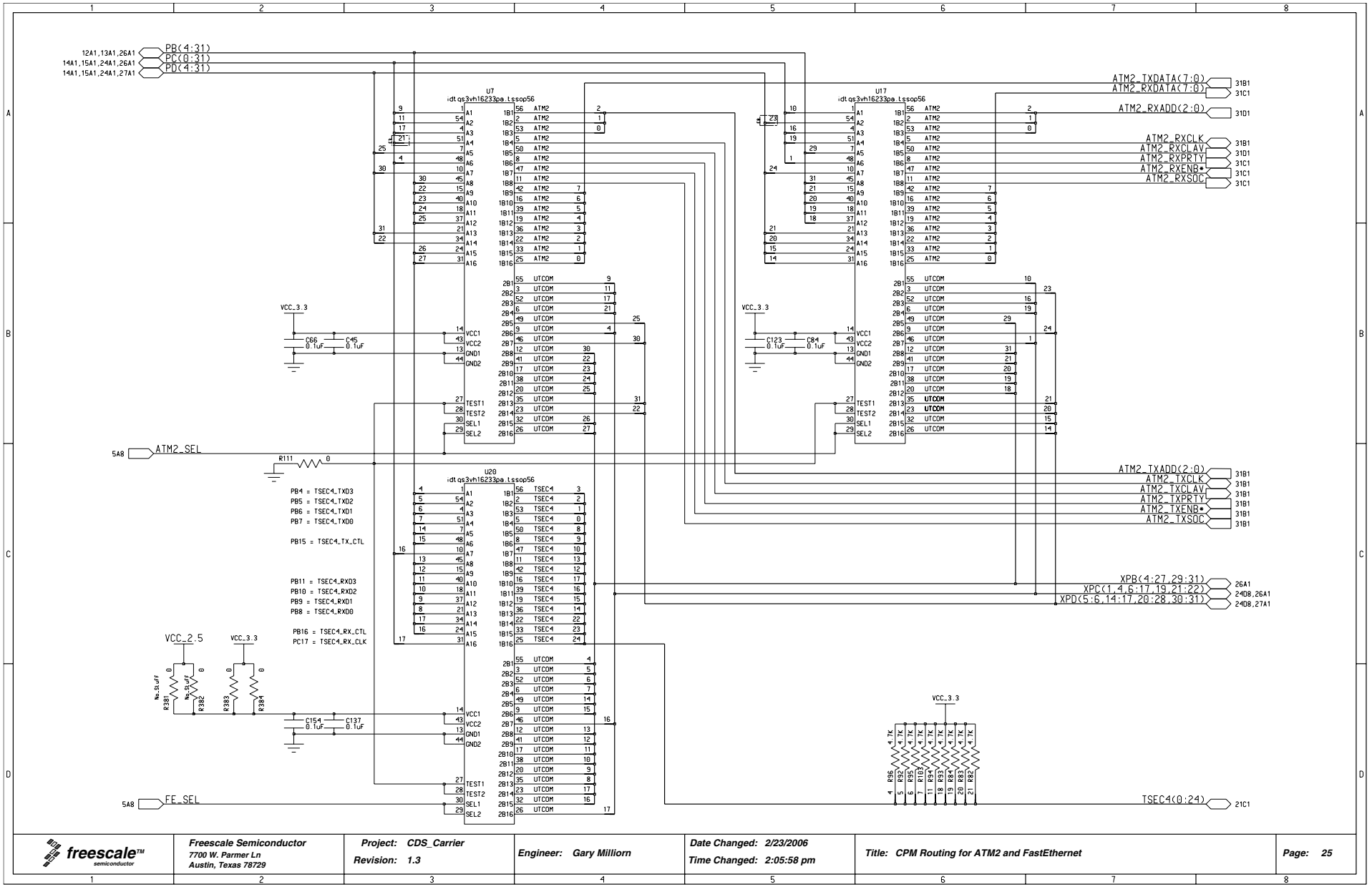
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 1/27/2006 Time Changed: 2:11:35 pm	Title: Carrier-to-IOCard Connector	Page: 22



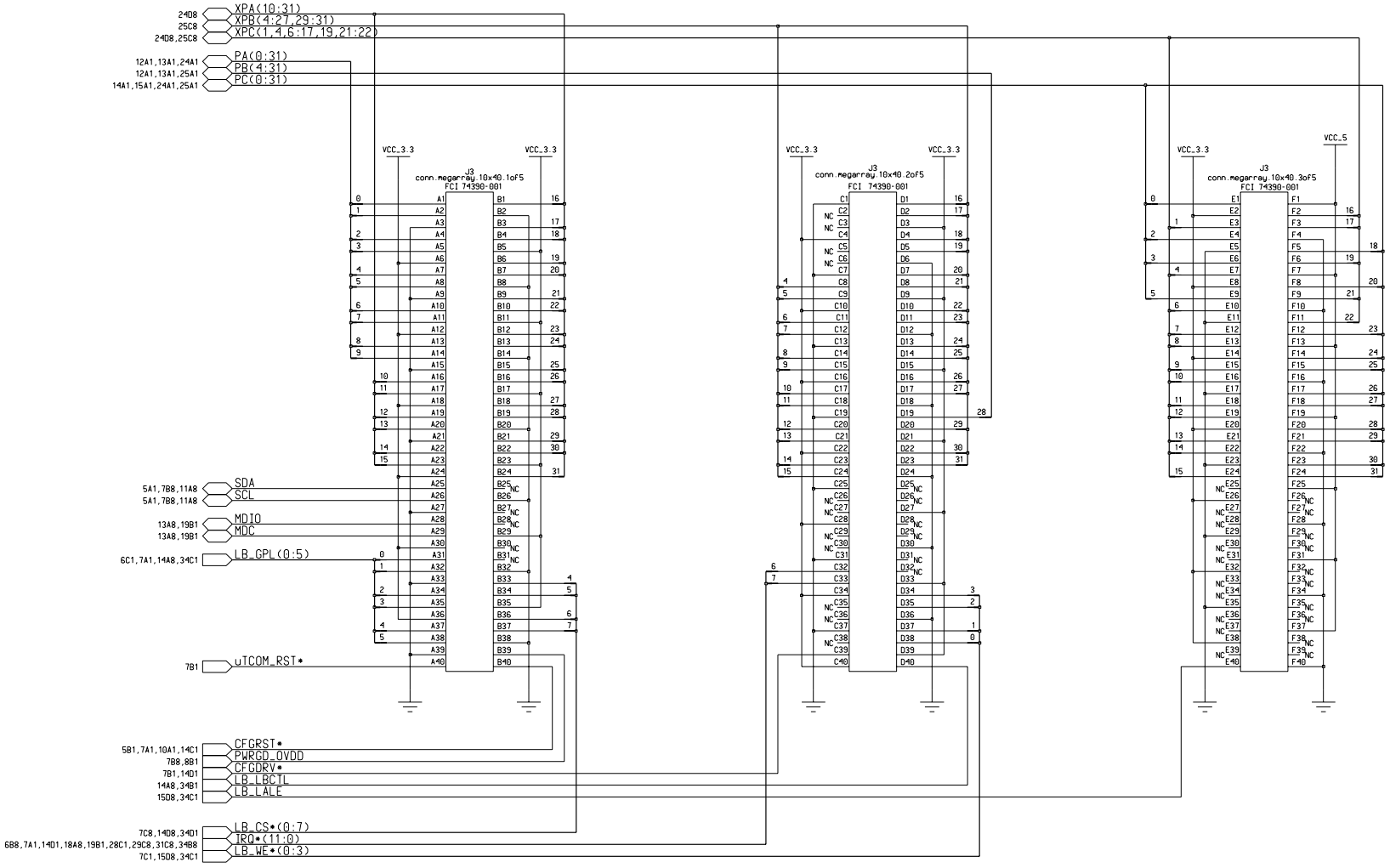
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:03:23 pm	Title: Serial Ports	Page: 23



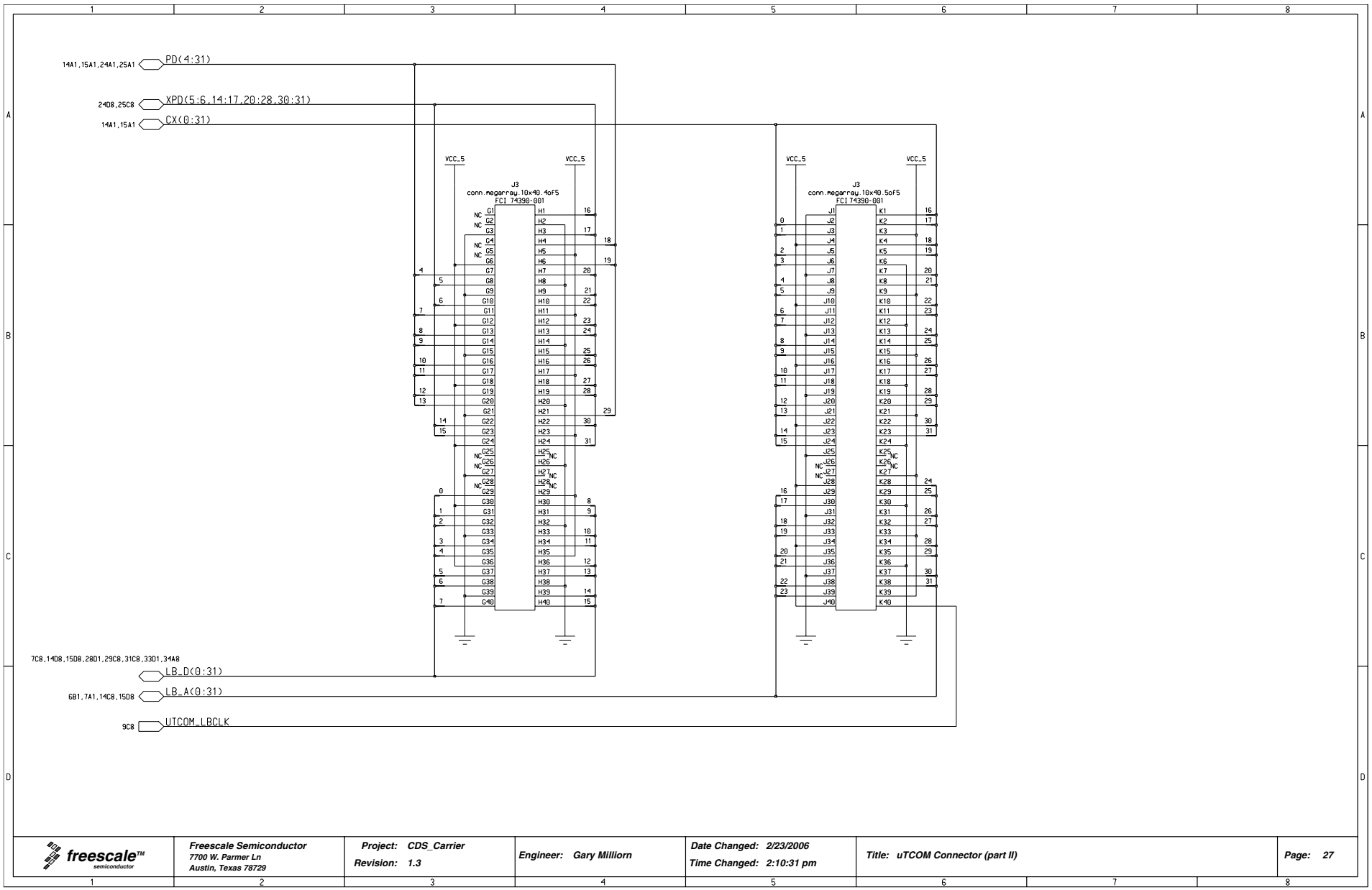
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:05:09 pm	Title: CPM Routing for ATM1	Page: 24



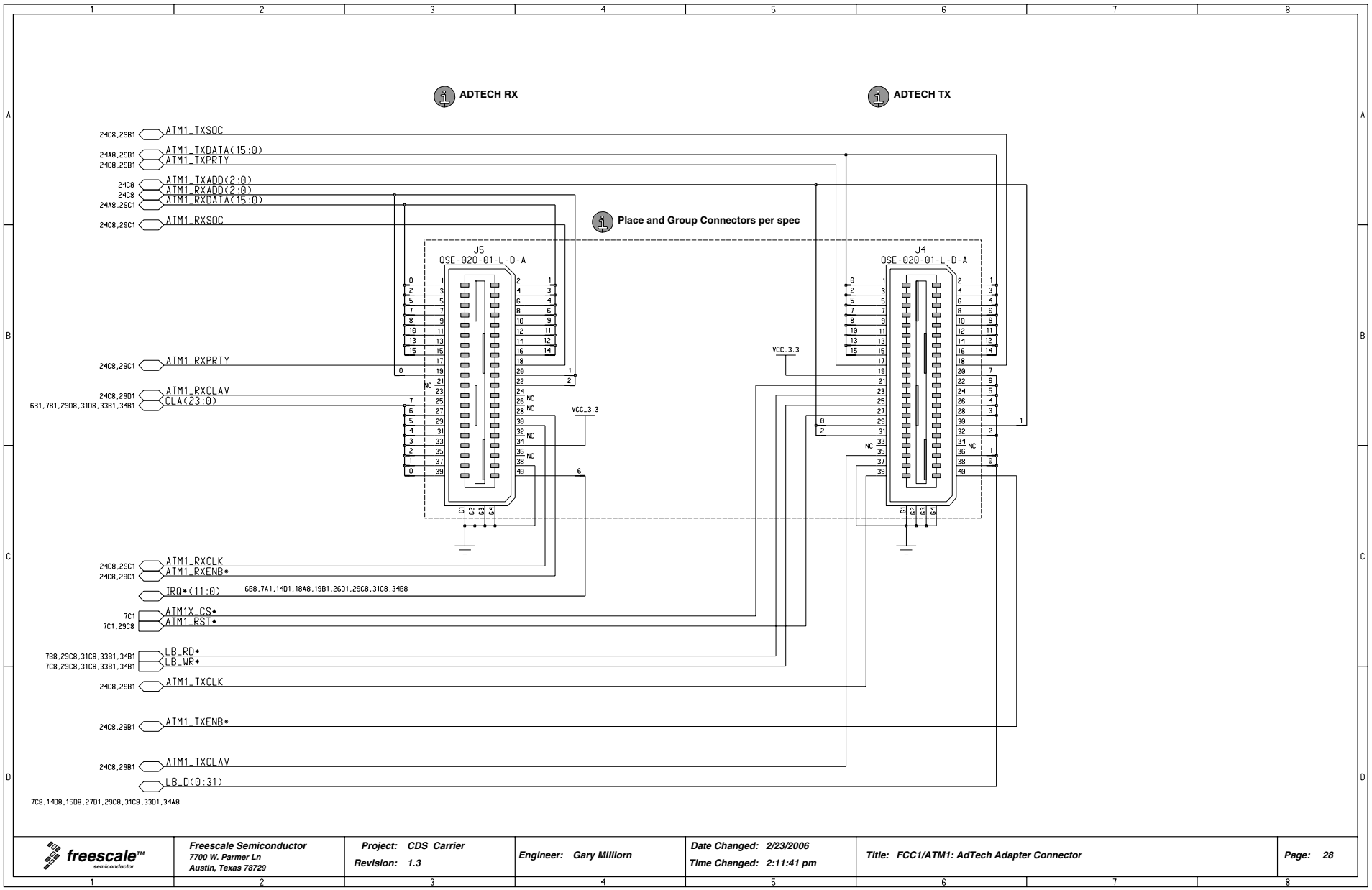
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:05:58 pm	Title: CPM Routing for ATM2 and FastEthernet	Page: 25



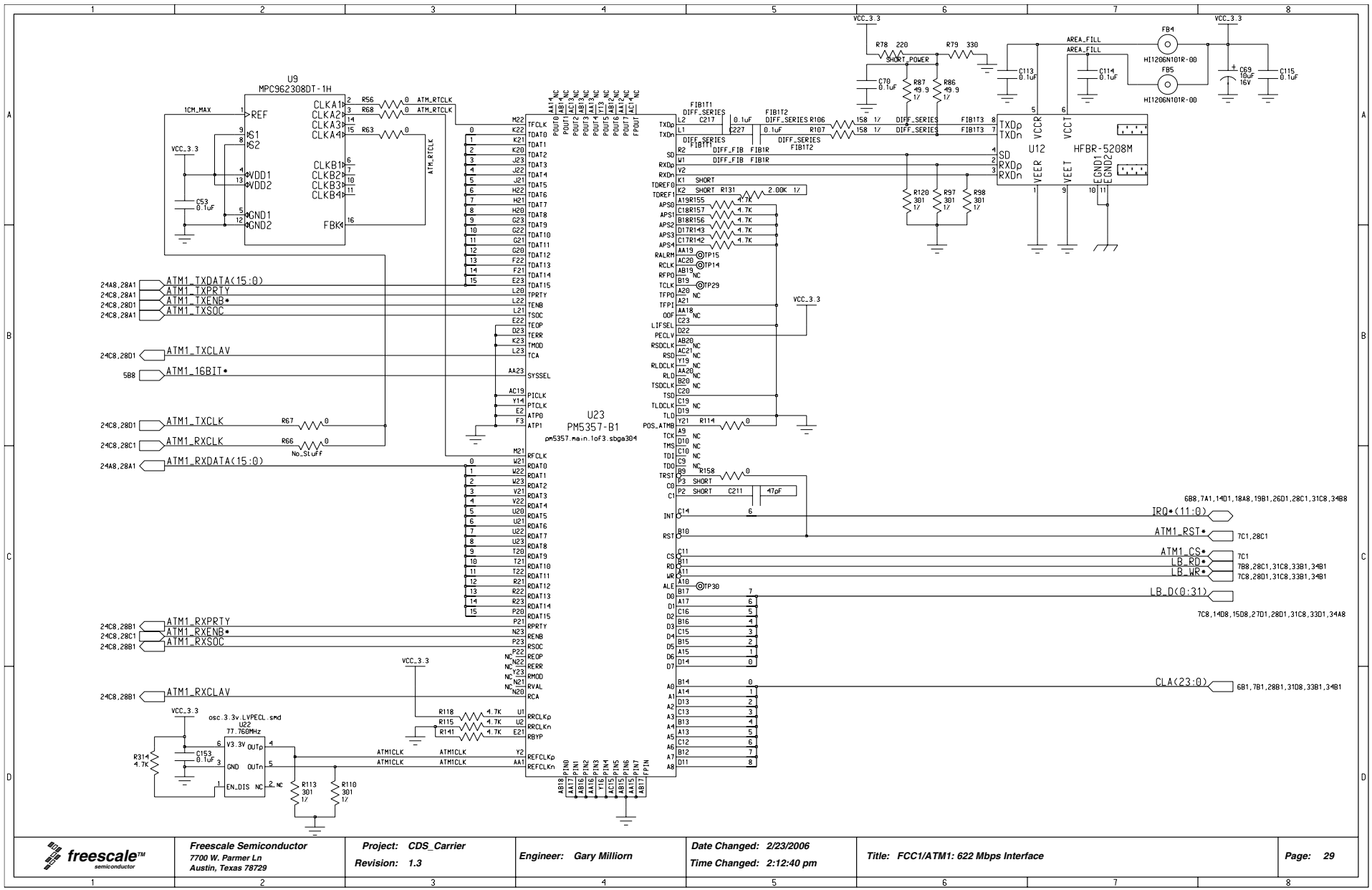
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:09:47 pm	Title: uTCOM Connector (part I)	Page: 26



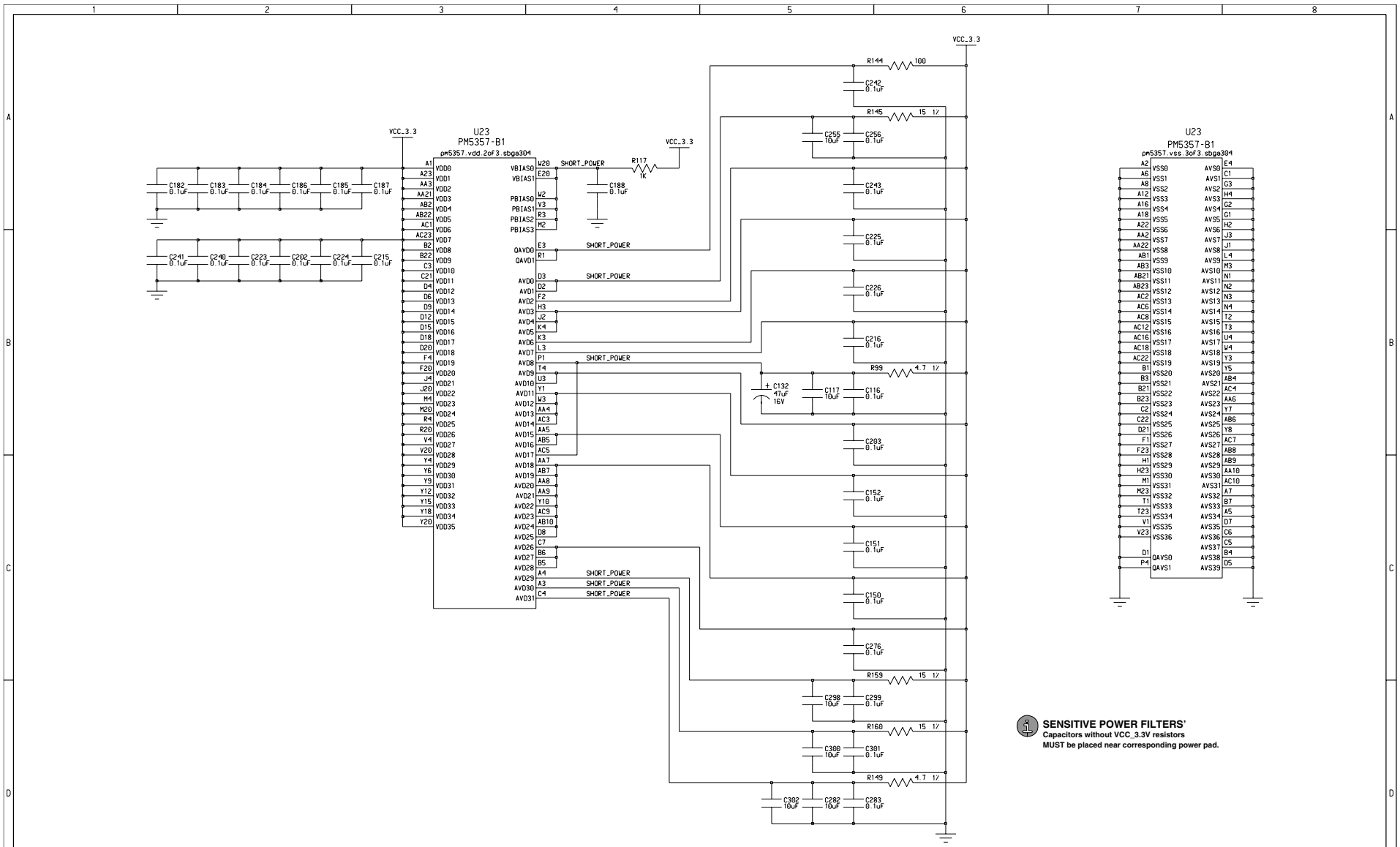
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:10:31 pm	Title: uTCOM Connector (part II)		Page: 27



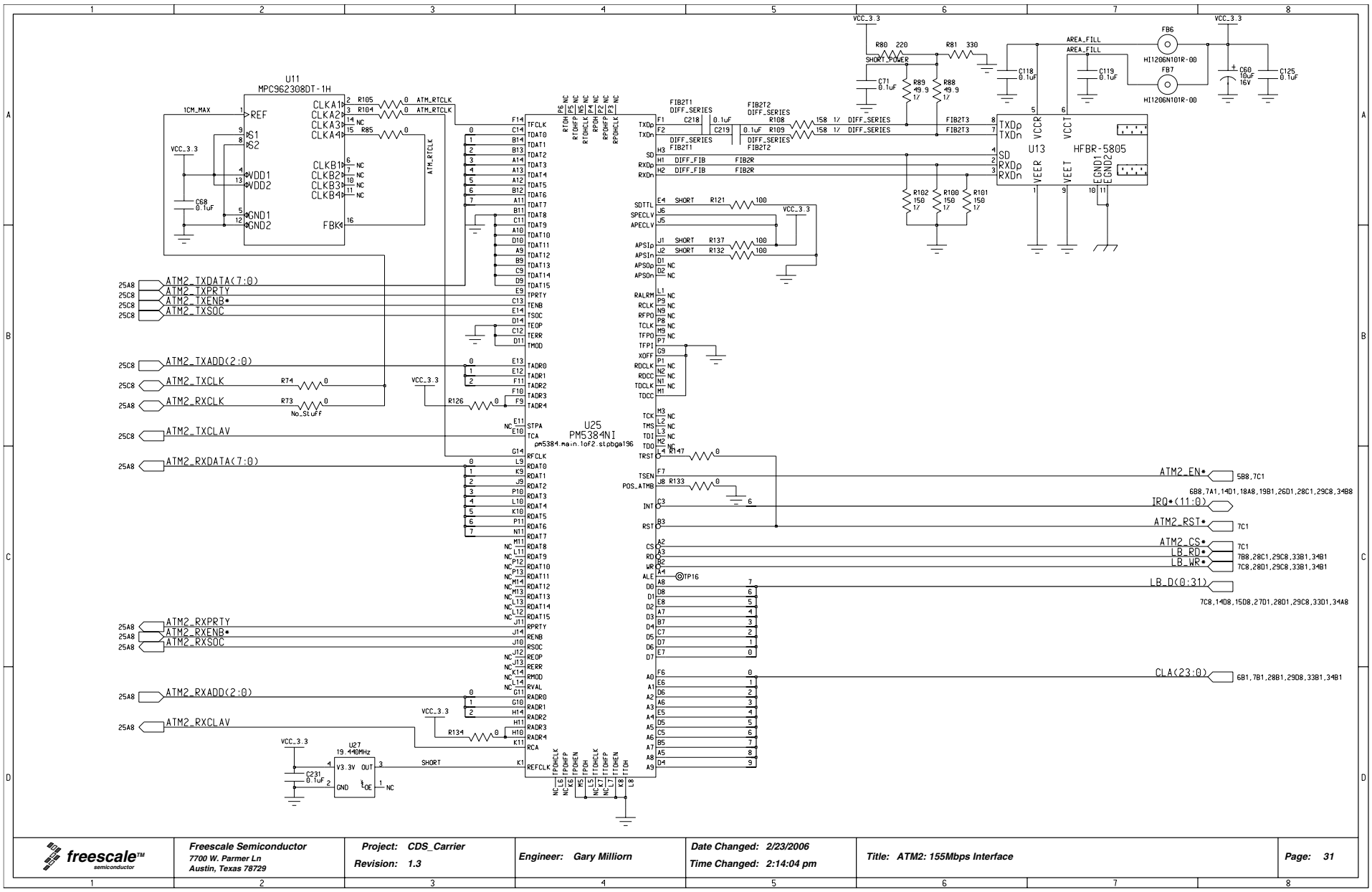
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:11:41 pm	Title: FCC1/ATM1: AdTech Adapter Connector	Page: 28



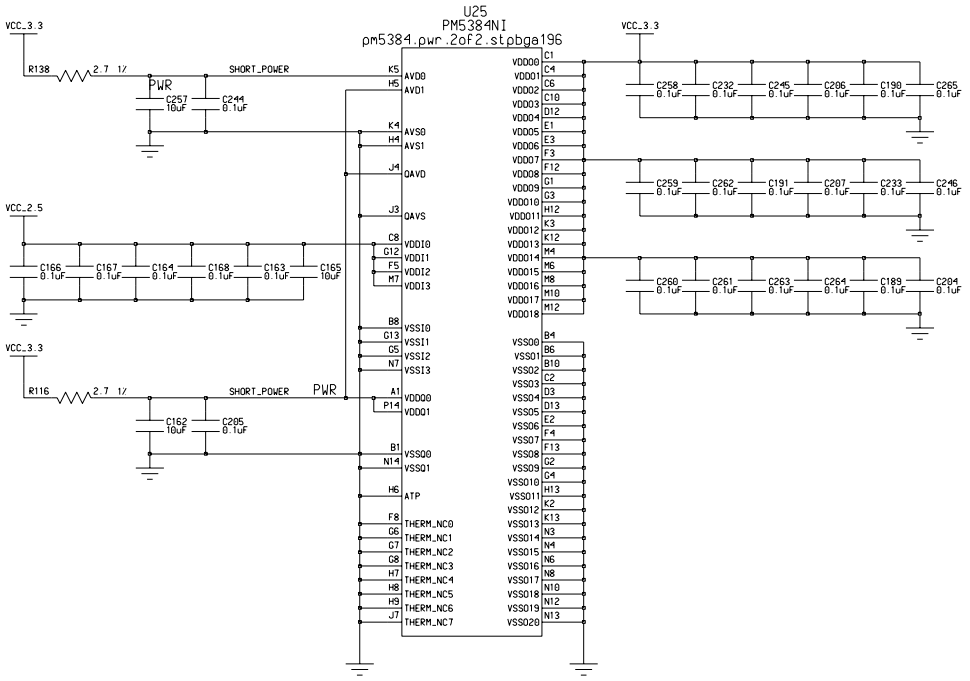
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:12:40 pm	Title: FCC1/ATM1: 622 Mbps Interface	Page: 29



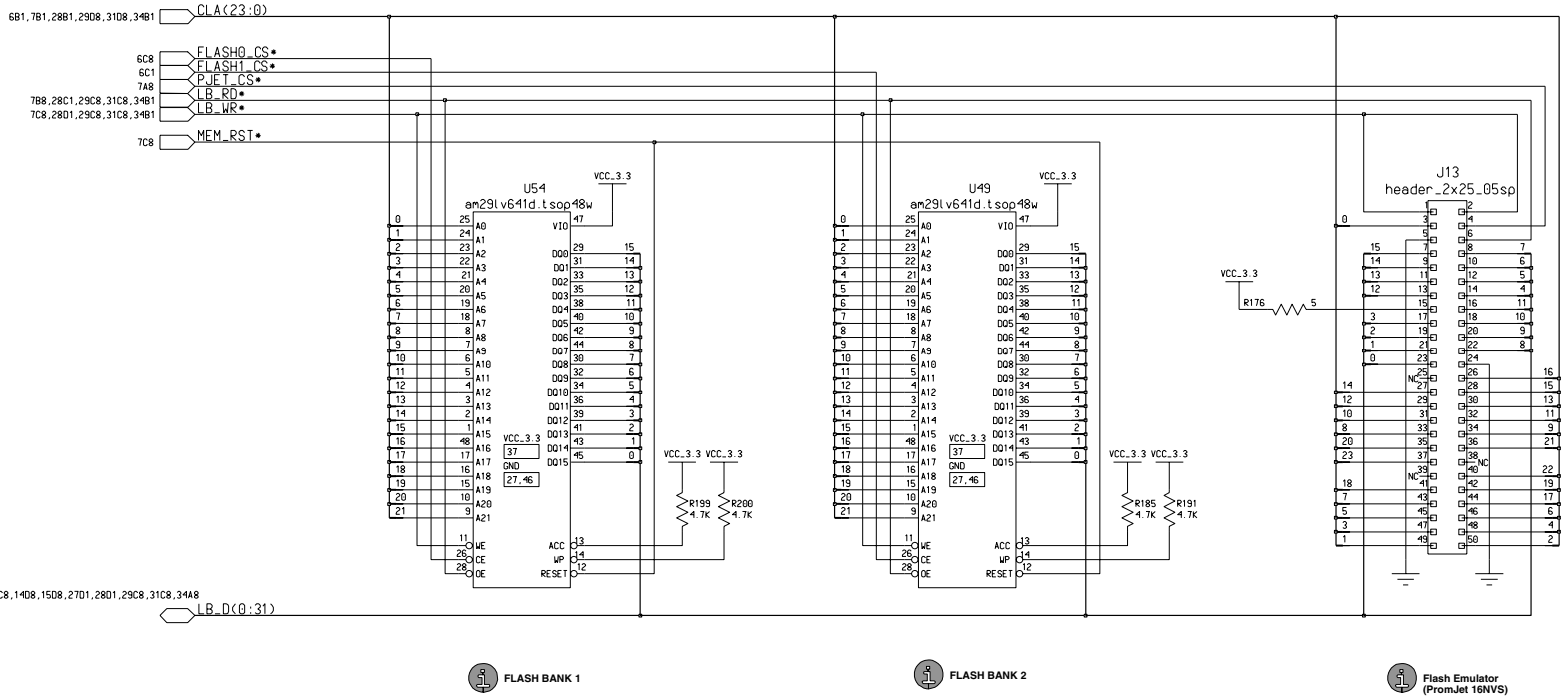
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:13:27 pm	Title: FCC1/ATM1:PHY Power	Page: 30



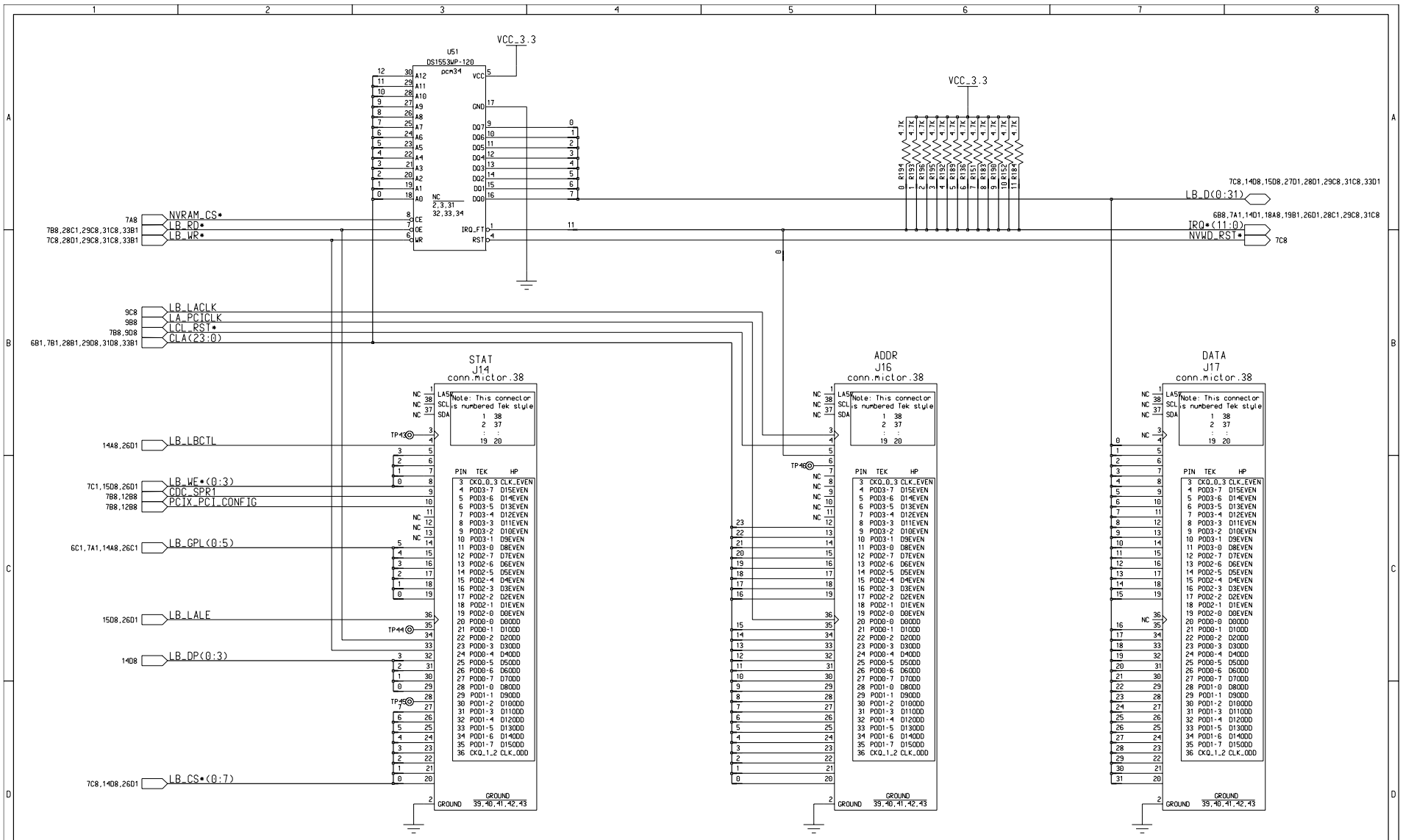
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:14:04 pm	Title: ATM2: 155Mbps Interface	Page: 31



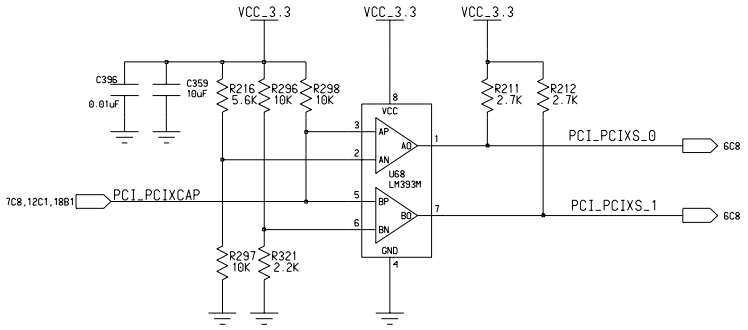
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 1/27/2006 Time Changed: 2:12:39 pm	Title: FCC2/ATM2: PHY Power	Page: 32



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:14:39 pm	Title: Flash Memory + Flash Emulator	Page: 33

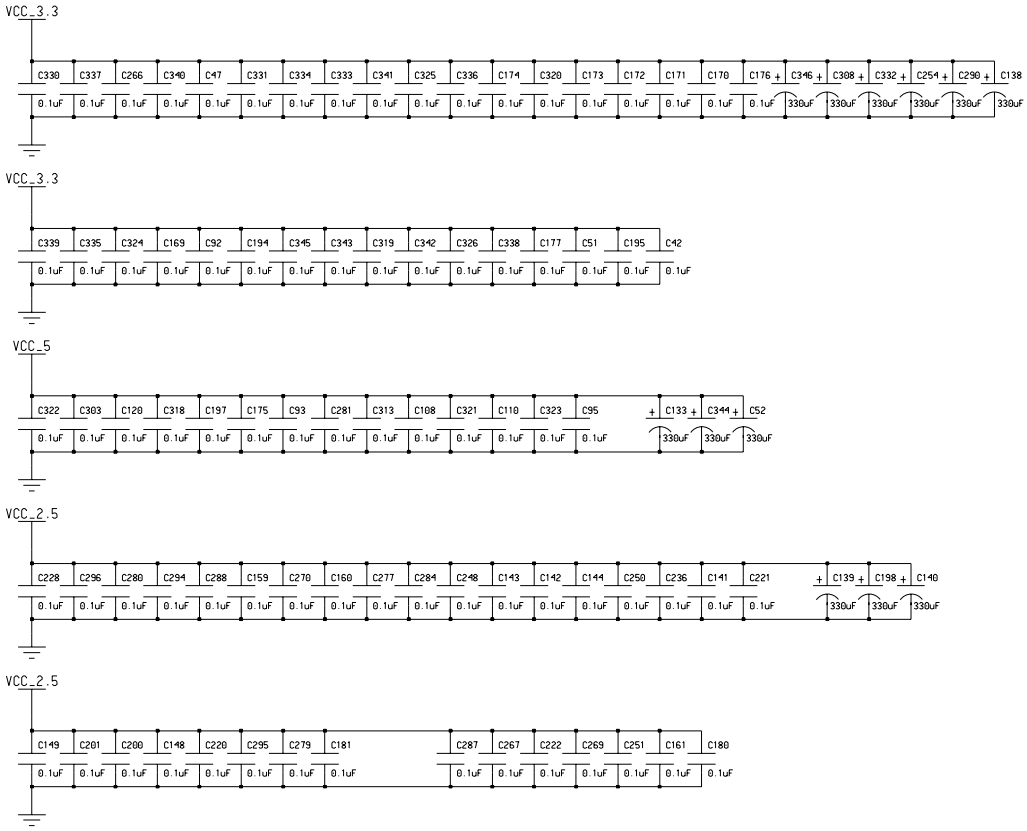


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.3	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:15:30 pm	Title: Local Bus NVRAM/Debug Connectors	Page: 34



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_Carrier Revision: 1.2	Engineer: Gary Milliorn	Date Changed: 2/23/2006 Time Changed: 2:16:14 pm	Title: --reserved--		Page: 35

GLOBAL BYPASS CAPS.
Add or subtract based on density.



Appendix G
CDS CDC BOM

This appendix provides CDC BOM for Rev. 1.1.

Board Station BOM file
date : Tuesday July 6, 2004; 12:09:48
Variant : No_Stuff

CDS MPC85XX V 1.1 BOM
Updated on 8/18/04

ITEM_NO	COMPANY PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1		PCB	1		
2	0603YC104JAT2A	cc0603	1	cap, 0.1uF, AVX	C47
3	102972-3	header_1x3	1	header.1x3, AMP	J3
4	103309-3	header_riscwatch	1	header.2x8	J1
5	218-8LPST	sw_som16	4	sw.8spst.cts, CTS	SW1 SW2 SW3 SW4
6	293D476X9016D2T	cct7343	1	cap_tant, 47uF, SPRAGUE	C8
7	33-40111-1		1	pbga_28x28_socket_tecknit	
8	597-5112-40X	led_0603	12	led, Dialight, Red	D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12
9	71243-3002	conn_184ddr_Molexdimm_vert	1	conn_184_ddr_dimm_2.5v_angled_1of2, AMP	P3
10	SN74LVC74APW sub SN74LV74APW	so14	1	sn74lvc74a.sso14, TI	U2
11	74lv08d	so14	1	74lv08d.so14, TI	U5
12	84740-002	connFCI_array_10x40_sm	2	conn.megarray.10x40.1of5, FCI	J4 J5
13	981131-120-2MCF	pciconn_3.3v_ra_32bit	1	pciconn_3.3V_ra_32bit_block, MERITEC	J2
14	AT24C64AN-10SI-2.7	so8	2	at24c64a.s08, ATMEL	U25 U31
15	EEFUE0E221R	cc_7.3x4.3_ue	6	cap_tant, 220uF, PANSONIC	C79 C80 C94 C179 C209 C210
16	EH2645TS-66.000M	osc_smd_5x7mm	1	osc.3_3v.smd, 66.666MHz, ECLIPTEK	U3
17	EMK107F224ZA	cc0603	1	cap, .22uF, TAIYO_YUDEN	C15
18	ERJM1WTJ1M5U	rc2512	2	res, 1.5mohm, PANASONIC	R149 R266
19	EXCCL4532U1	induct_4532	1	exccl4532.smd, PANASONIC	L2
20	IDTQS3VH257PA	tssop16	2	idtqs3vh257.tssop16, IDT	U10 U11
21	IRF6604	irf6604	2	irf66xx.dirfet, IRF	Q1 Q2
22	IRF6607	irf6607	2	irf66xx.dirfet, IRF	Q3 Q4
23	JMK107F225ZA	cc0603	10	cap, 2.2uF, TAIYO_YUDEN	C169 C170 C171 C172 C173 C174 C175 C185 C186 C187

24	K4S561632E-TC75	tsop54	2	sdram.sdr.jedec.tsop54, VAR	U15 U17
25	LM358D	so8	1	lm358d.so8, NATSEMI	U27
26	LMK107F105ZA	cc0603	3	cap, 1.0uF, TAIYO_YUDEN	C13 C14 C46
27	LP2995M	so8	1	lp2995m.so8, National Semi	U8
28	MAX1037EKA-T	sot23_8p	1	max1037eka_t.sot23_8, Maxim	U26
29	MAX1813EEI	ssop28_pit635mm	1	max1813eei.qsop28, MAXIM	U9
30	MAX4372FEUK-T	sot23_5p	1	max4372f.sot23_5, Maxim	U13
31	MBRS140T3	smb_403a	1	mbrs140t3.smb, MOT	CR1
32	MBRS340T3	smb_403	1	mbrs340t3.smb, MOT	CR2
33	MCCA104K0NRT	cc0402	140	cap, 0.1uF, SMEC	C1 C2 C3 C4 C5 C6 C9 C10 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C52 C81 C82 C83 C87 C88 C89 C90 C91 C92 C95 C96 C97 C98 C99 C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 C111 C112 C113 C114 C115 C116 C117 C119 C120 C121 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135 C136 C137 C138 C139 C140 C141 C142 C143 C144 C145 C146 C147 C148 C149 C150 C151

					C152 C153 C154 C155 C156 C160 C161 C162 C163 C164 C165 C166 C168 C176 C177 C178 C180 C181 C182 C183 C184 C188 C189 C190 C191 C192 C193 C194 C195 C196 C197 C198 C199 C200 C201 C202 C203 C204 C206 C207 C208
34	MCCA470K0NRT	cc0402	1	cap, 47pF, SMEC	C50
35	MCCE102KONRT	cc0402	2	cap, 1000pF, muRATA	C48 C49
36	MNR14-EOAB-J-390	rnet1632	4	rnet, 39, Rohm	RN4 RN5 RN6 RN7
37	MPC8555	pbga_28x28_1mm_skt	1	dracomLITE.1of9.ddr.pbga783, Motorola	U19
38	Not_a_component	jump_2x1_1mil	1	splice.1, PCB	SP1
39	P6880	conn_banjo	1	conn.banjo_alt, Tektronix	P2
40	PCA9557PW	tssop16	4	pca9557pw.tssop16, PHILIPS	U23 U24 U28 U30
41	RC73L2Z000JT	rc0402	11	res, 0, KOA	R145 R222 R223 R302 R303 R307 R317 R320 R322 R334 R346
42	RC73L2Z100JT	rc0402	6	res, 10, KOA	R87 R319 R327 R329 R332 R336
43	RC73L2Z101JT	rc0402	6	res, 100, KOA	R8 R146 R148 R295 R296 R341
44	RC73L2Z102JT	rc0402	13	res, 1K, KOA	R19 R26 R284 R288 R293 R294 R304 R305 R306 R315 R337 R339
45	RC73L2Z103JT	rc0402	3	res, 10K, KOA	R25 R344 R345
46	RC73L2Z104JT	rc0402	11	res, 100K, KOA	R22 R283 R291 R292 R297 R310 R311 R312 R313 R314

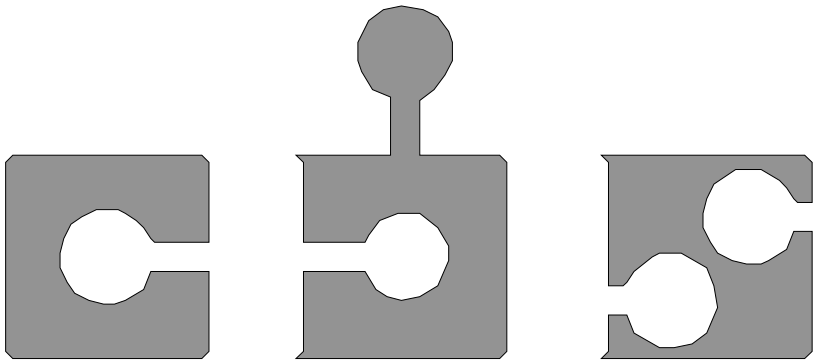
					R324
47	RC73L2Z124JT	rc0402	1	res, 120K, KOA	R147
48	RC73L2Z154JT	rc0402	1	res, 150K, KOA	R24
49	RC73L2Z200JT	rc0402	2	res, 20, KOA	R20 R318
50	RC73L2Z220JT	rc0402	129	res, 22, KOA	R3 R4 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 R167 R168 R169 R170 R171 R172 R173 R174 R175 R176 R177 R178 R179 R180 R181 R182 R183 R184 R185 R186 R187 R188 R189 R190 R191 R192 R193 R194 R195 R196 R197 R198 R199 R200 R201 R202 R203 R204 R205 R206 R207 R208 R209 R210 R211 R212 R213 R214 R215 R216 R217 R218 R219 R220 R221 R224 R225 R226 R227 R228 R229 R230 R231 R232 R233 R234 R235 R236 R237 R238 R239 R240 R241 R242 R243 R244 R245 R246 R247 R248 R249

					R250 R251 R252 R253 R254 R255 R256 R257 R258 R259 R260 R261 R262 R263 R264 R265 R269 R270 R271 R272 R273 R274 R275 R276 R277 R290 R298 R300 R301
51	RC73L2Z221JT	rc0402	12	res, 220, KOA	R6 R7 R9 R10 R11 R12 R13 R14 R15 R16 R17 R18
52	RC73L2Z223JT	rc0402	2	res, 22K, KOA	R279 R343
53	RC73L2Z270JT	rc0402	116	res, 27, KOA	R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R38 R39 R40 R41 R42 R43 R44 R45 R46 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 R85 R86 R88 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99 R100 R101 R102 R103 R104 R105 R106 R107 R108 R109 R110 R111 R112 R113 R114 R115

					R116 R117 R118 R119 R120 R121 R122 R123 R124 R125 R126 R127 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R144
54	RC73L2Z331JT	rc0402	1	res, 330, KOA	R5
55	RC73L2Z333JT	rc0402	1	res, 33K, KOA	R280
56	RC73L2Z390JT	rc0402	2	res, 39, KOA	R281 R282
57	RC73L2Z391JT	rc0402	1	res, 390, KOA	R299
58	RC73L2Z472JT	rc0402	1	res, 4.7K, KOA	R47
59	RC73L2Z563JT	rc0402	1	res, 56K, KOA	R342
60	RC73L2Z862JT	rc0402	1	res, 8.6K, KOA	R340
61	RNA4A8E102JT	rna4a	4	rnet8.bussed.rna4a, 1K, AVX	RN12 RN15 RN17 RN18
62	RNA4A8E472JT	rna4a	4	rnet8.bussed.rna4a, 4.7K, AVX	RN13 RN14 RN16 RN19
63	RNA4A8E472JT	rna4a	7	rnpullup_3.3v.rna4a, 4.7K, AVX	RN1 RN2 RN3 RN8 RN9 RN10 RN11
64	SN74ALVCH32973KR	lfbga96	2	74alvch32973kr.lfbga96, TI	U16 U20
65	SN74CBT16211ADGGR	ssop56_20mil	2	74cbt16211dggr.ssop56, TI	U14 U18
66	SN74LVC04APW	tssop14	1	74lvc04a.tssop14, TI	U7
67	SN74LVC16244ADGG	tssop48	2	74lvc16244adgg.tssop48, TI	U22 U29
68	SN74LVC1G04DCKR	sot_5p	1	sn74lvc1g04.sot_5p, TI	U6
69	SN74LVC1G125DCKR	sc70	3	74lvc1g125.sc70, TI	U1 U4 U21
70	SN74LVCH32244GKER	lfbga96	1	sn74lvch32244gker.lfbga96, TI	U12
71	T510X337M010AS	cct_casee	6	cap_tant, 330uF, Kemet	C84 C85 C86 C122 C167 C205
72	TMK432BJ106MM	cc1812	7	cap, 10uF, TAIYO_YUDEN	C11 C12 C43 C44 C45 C93 C118
73	TPSE227K010R0100	cct_casee	3	cap_tant, 220uF, AVX	C7 C32 C51
74	RC73L2Z000JT	rc0402	1	res, 0 ohm, KOA	R21 R23
75	ETQP6F0R6BFA	induct_12.5x12.5	1	indutor, 0.6IH	L1

Appendix H
CDS CPU Schematics (CDC)

This appendix provides CPU board schematics for Rev. 1.1.



CDC_MPC85xx

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:36:16 pm	Title: Cover Story	Page: 01 of 35

Schematic Notes

1. Unless otherwise specified:
   All resistors are SMD0402, in ohms, 0.08W, +/-5%
   All capacitors are SMD0402, in microfarads (uF), +/-20%.
   All inductances are in microhenries (uH).
   All ferrites are Z=50 ohms at 100 MHz.
   All fuses are self-resetting polyswitch (PTC) devices.
   Board impedance is 55 +/- 5 ohms.

2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:
   GND
   VCC_3.3 VCC_2.5 OVDD
   VCC_5 VCORE VCC_12

3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.

4. Freescale Semiconductor and the Freescale logo are registered trademarks of Motorola. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. Don't wait for tomorrow. All rights reserved. No warranty is made, express or implied.

5. The sheet-to-sheet cross reference format is:
   Sheet VertZoneLetter HorizZoneNumber

6. Components with the visible property "NO STUFF" are not to be installed by default; they are for test or manufacturing purposes only.

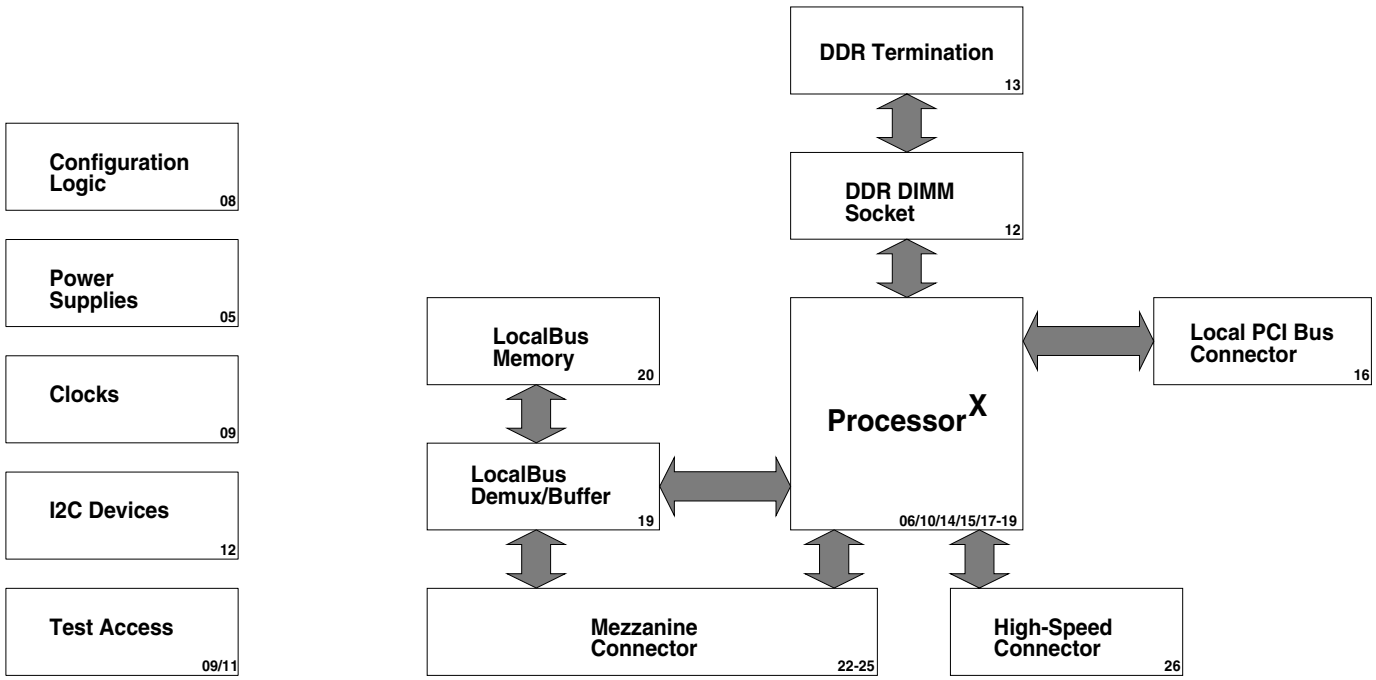
7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

8. Team CDS is:
   Jon Burnett.....Simulation/Program Management
   Cindy Callis.....CAD/Layout
   Gary Milliorn.....Hardware Design
   Tony Saucedo.....Purchasing
   Margarito Trevino.....Tech/Debug
   Alex Milliorn.....Best Buddy

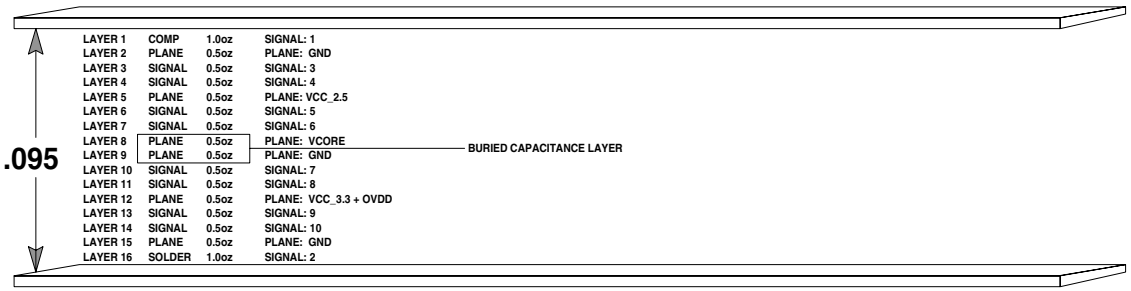
CDC_MPC85xx

New P/S ---->

REV	DATE	CHANGES
V1.0	03SEP25	Initial version
V1.1	04APR04	Errata fixes



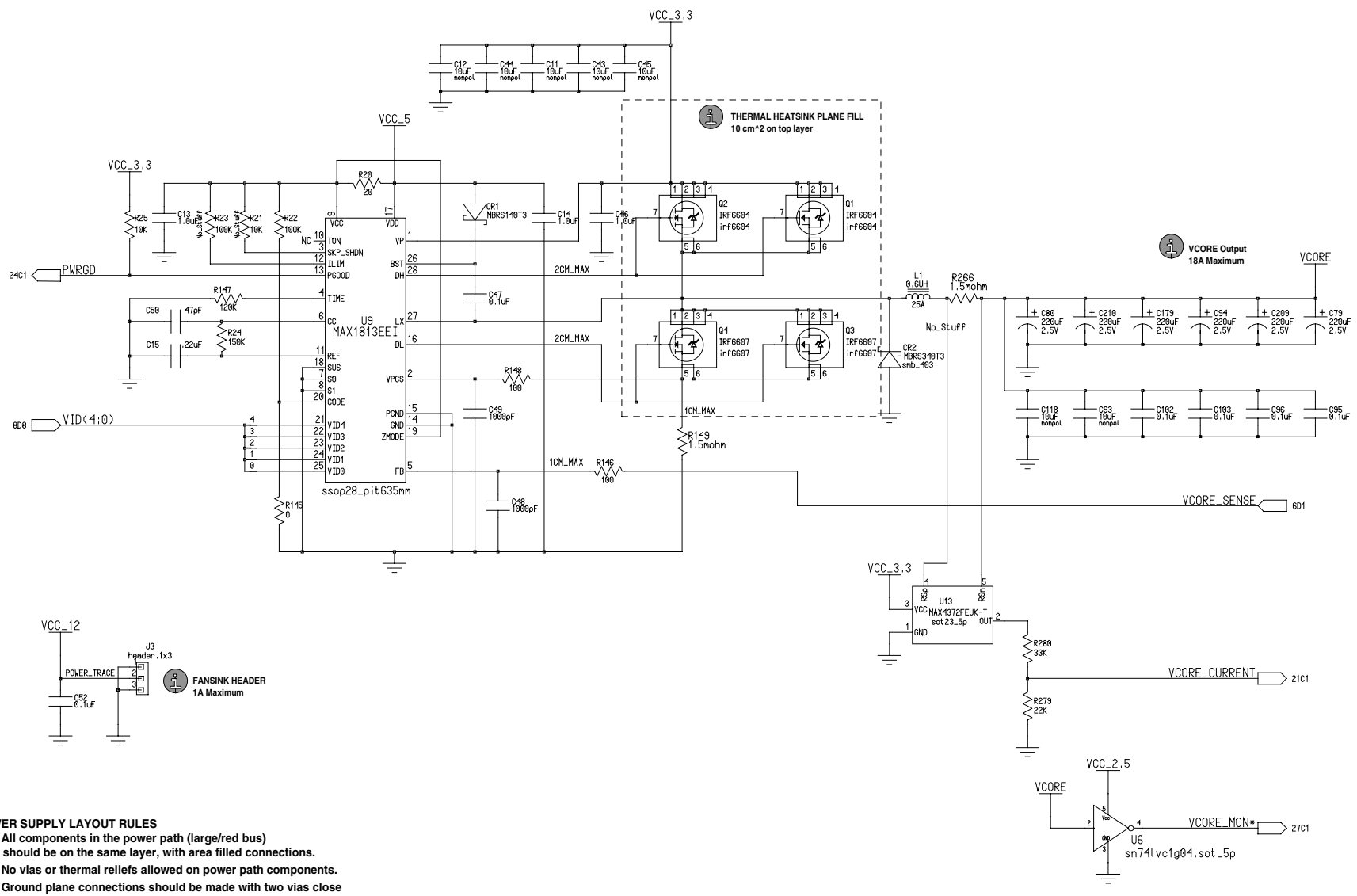
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85x_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 1:20:22 pm	Title: Block Diagram	Page: 03



LAYER 1	COMP	1.0oz	SIGNAL: 1
LAYER 2	PLANE	0.5oz	PLANE: GND
LAYER 3	SIGNAL	0.5oz	SIGNAL: 3
LAYER 4	SIGNAL	0.5oz	SIGNAL: 4
LAYER 5	PLANE	0.5oz	PLANE: VCC_2.5
LAYER 6	SIGNAL	0.5oz	SIGNAL: 5
LAYER 7	SIGNAL	0.5oz	SIGNAL: 6
LAYER 8	PLANE	0.5oz	PLANE: VCORE
LAYER 9	PLANE	0.5oz	PLANE: GND
LAYER 10	SIGNAL	0.5oz	SIGNAL: 7
LAYER 11	SIGNAL	0.5oz	SIGNAL: 8
LAYER 12	PLANE	0.5oz	PLANE: VCC_3.3 + OVDD
LAYER 13	SIGNAL	0.5oz	SIGNAL: 9
LAYER 14	SIGNAL	0.5oz	SIGNAL: 10
LAYER 15	PLANE	0.5oz	PLANE: GND
LAYER 16	SOLDER	1.0oz	SIGNAL: 2

BURIED CAPACITANCE LAYER

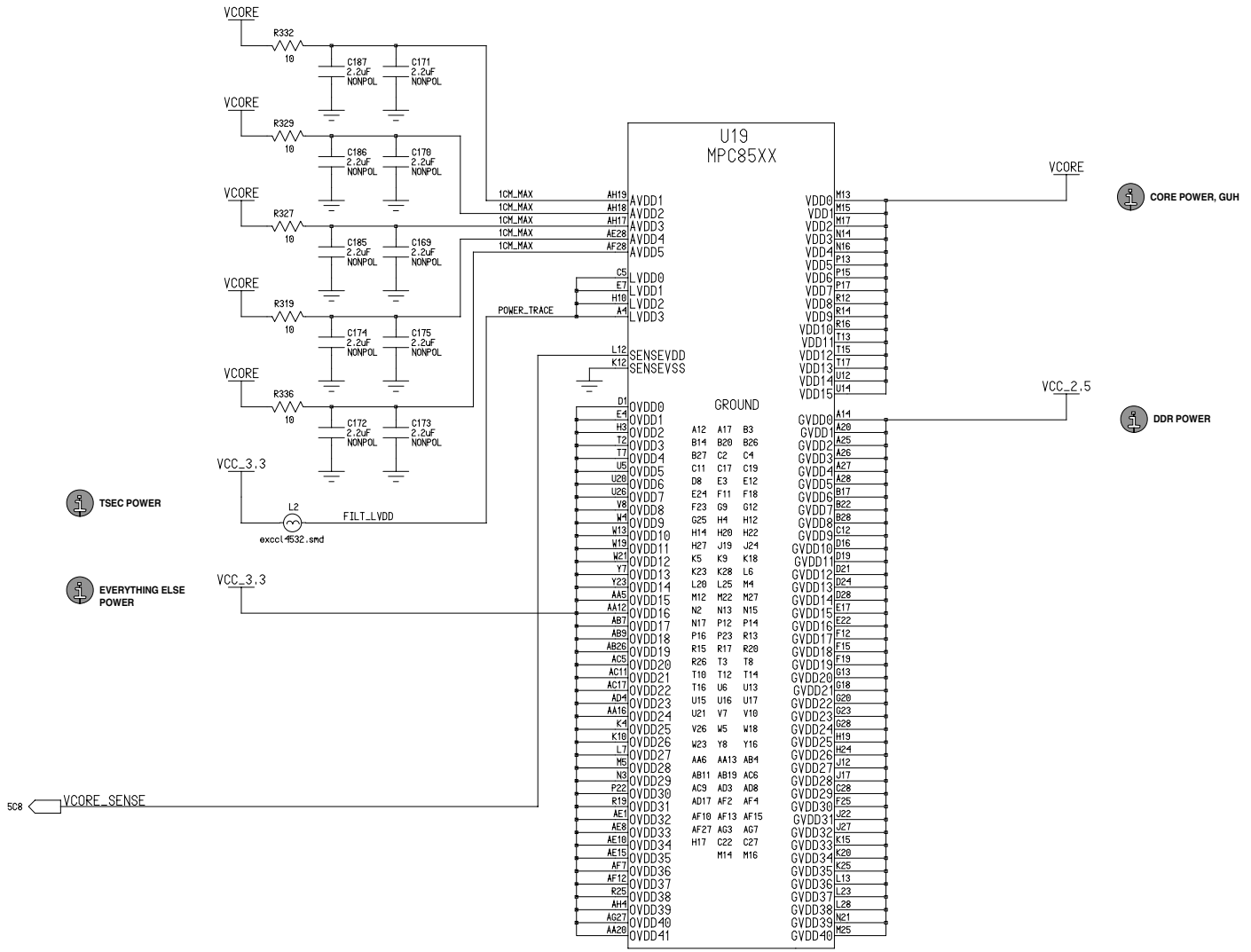
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 12:20:26 pm	Title: Cover Story	Page: 04



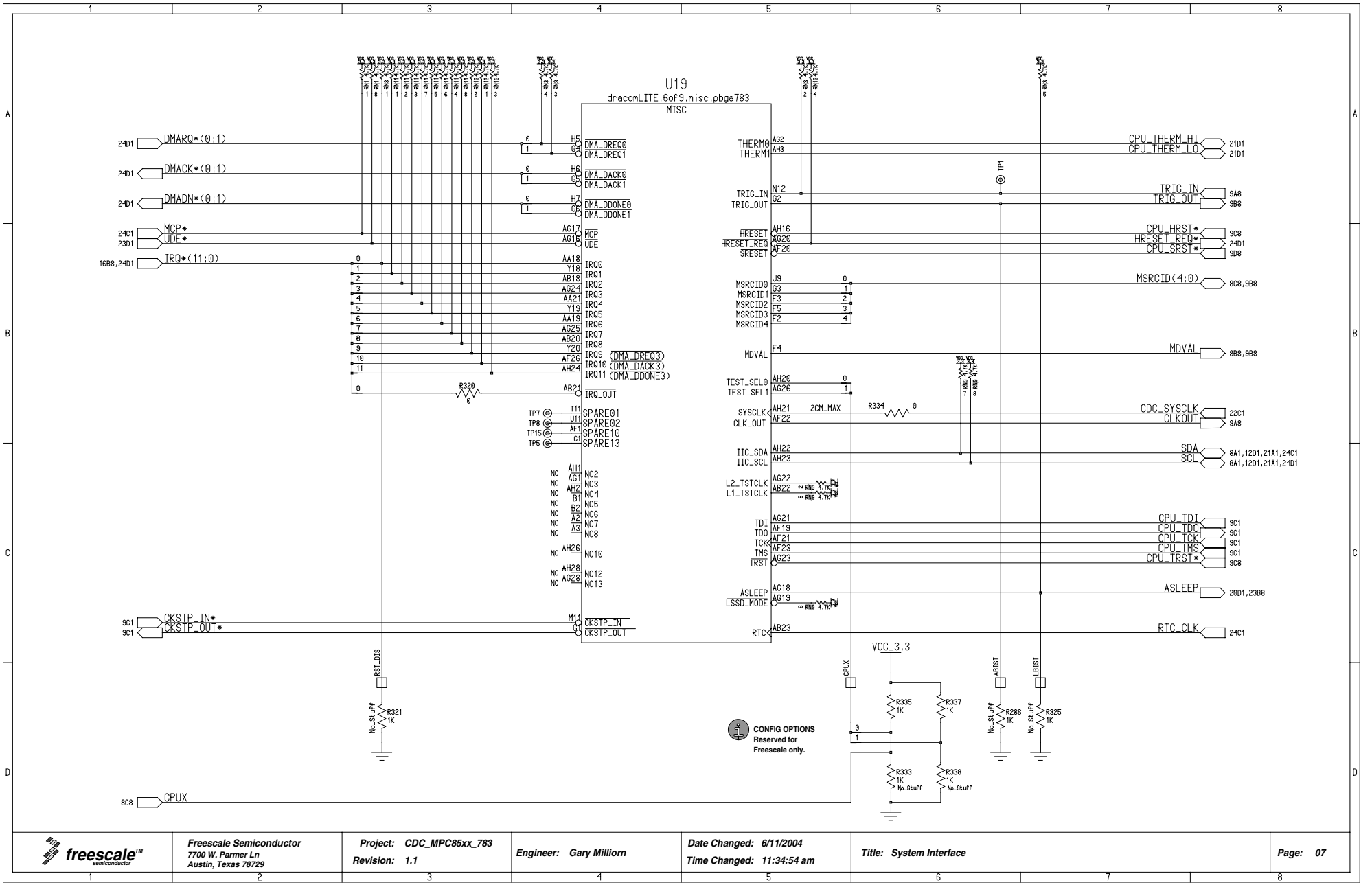
POWER SUPPLY LAYOUT RULES

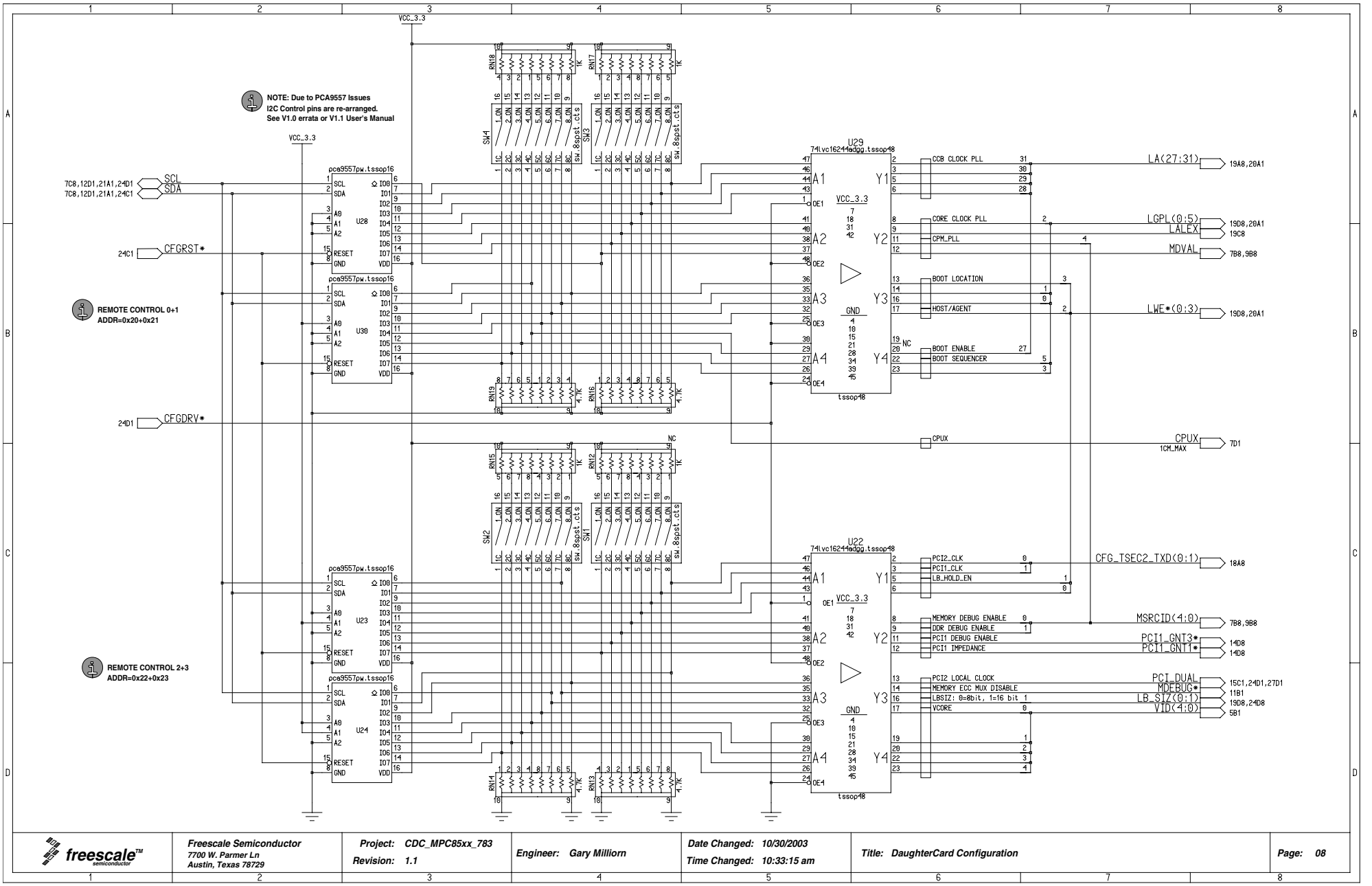
1. All components in the power path (large/red bus) should be on the same layer, with area filled connections.
2. No vias or thermal reliefs allowed on power path components.
3. Ground plane connections should be made with two vias close to the component.

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:52:16 pm	Title: Processor Core Power Supply	Page: 05

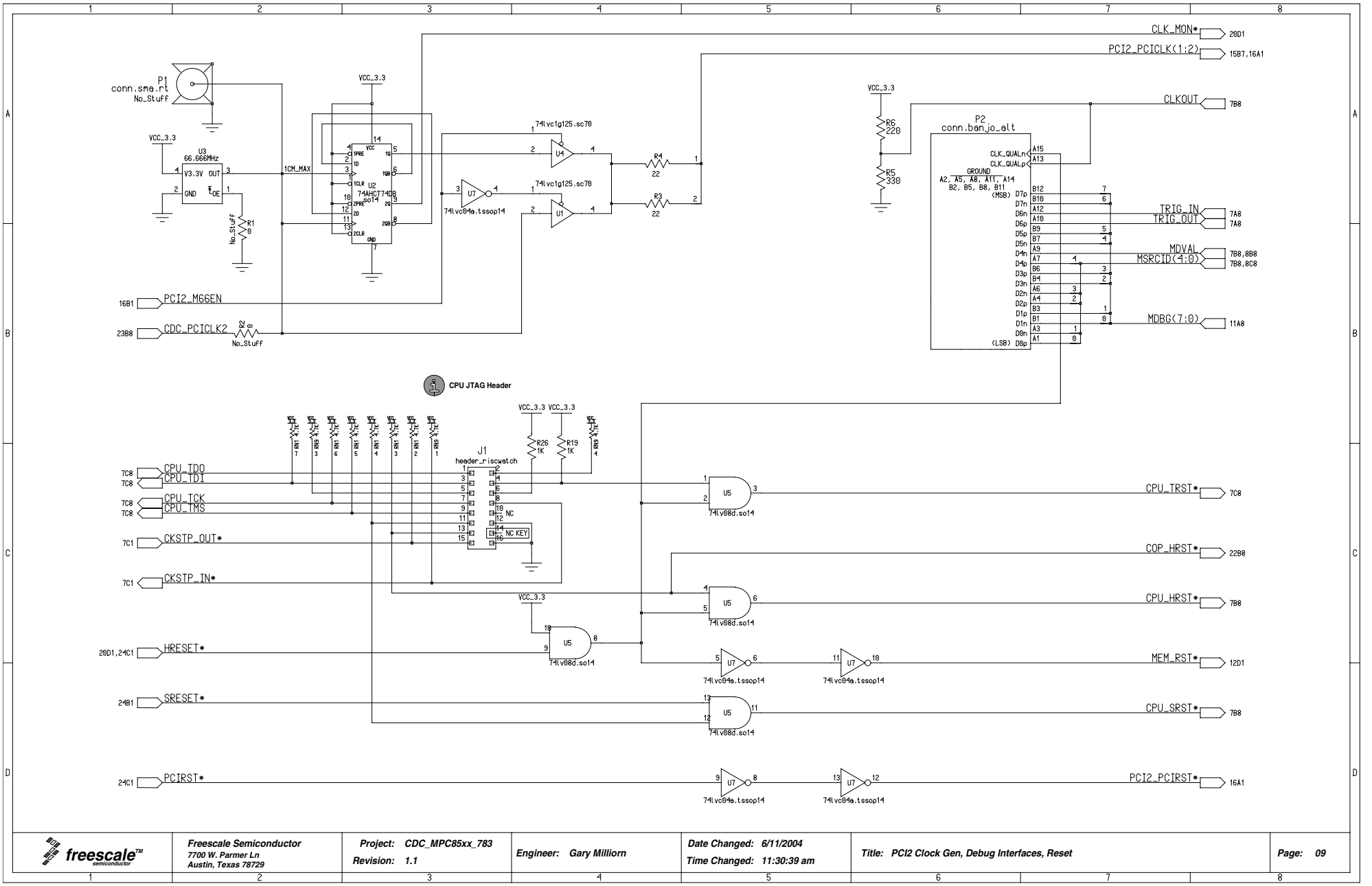


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:51:02 pm	Title: Processor Power Connections	Page: 06

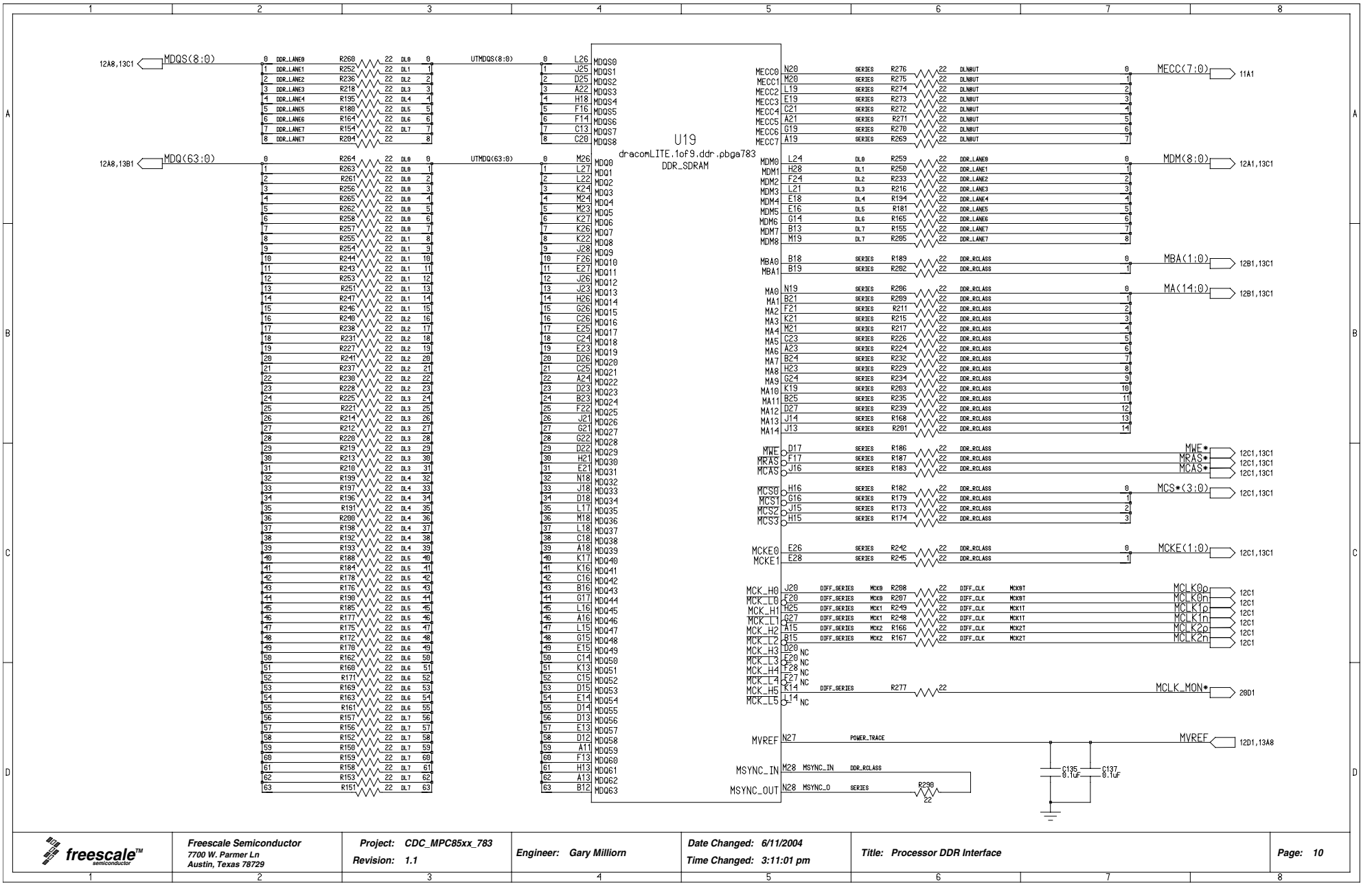

U19
dracomLITE,6of9,misc,pbga783
MISC
DMARQ*(0:1)
DMACK*(0:1)
DMADN*(0:1)
MCP*
UDE*
IRQ*(11:0)
DMA_DREQ0
DMA_DREQ1
DMA_DACK0
DMA_DACK1
DMA_DDONE0
DMA_DDONE1
MCP
UDE
IRQ0
IRQ1
IRQ2
IRQ3
IRQ4
IRQ5
IRQ6
IRQ7
IRQ8
IRQ9 (DMA_DREQ3)
IRQ10 (DMA_DACK3)
IRQ11 (DMA_DDONE3)
IRQ_OUT
R320
0
SPARE01
SPARE02
SPARE10
SPARE13
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC10
NC12
NC13
CKSTP_IN*
CKSTP_OUT*
CKSTP_IN
CKSTP_OUT
RST_DIS
R321
1K
No_Stuff
CPUX
THERM0
THERM1
CPU_THERM_HI
CPU_THERM_LO
TRIG_IN
TRIG_OUT
TP1
HRESET
HRESET_REQ
SRESET
CPU_HRST*
HRESET_REQ*
CPU_SRST*
MSRCID0
MSRCID1
MSRCID2
MSRCID3
MSRCID4
MSRCID(4:0)
MDVAL
TEST_SEL0
TEST_SEL1
SYSCLK
CLK_OUT
2CM_MAX
R334
CDC_SYSCLK
CLKOUT
IIC_SDA
IIC_SCL
SDA
SCL
L2_TSTCLK
L1_TSTCLK
TDI
TDO
TCK
TMS
TRST
CPU_TDI
CPU_TDO
CPU_TCK
CPU_TMS
CPU_TRST*
ASLEEP
LSSD_MODE
RTC
RTC_CLK
VCC_3.3
CONFIG OPTIONS
Reserved for
Freescale only.
R335
R337
R333
R338
R286
R325
ABIST
LBIST
freescale
Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729
Project: CDC_MPC85xx_783
Revision: 1.1
Engineer: Gary Milliorn
Date Changed: 6/11/2004
Time Changed: 11:34:54 am
Title: System Interface
Page: 07



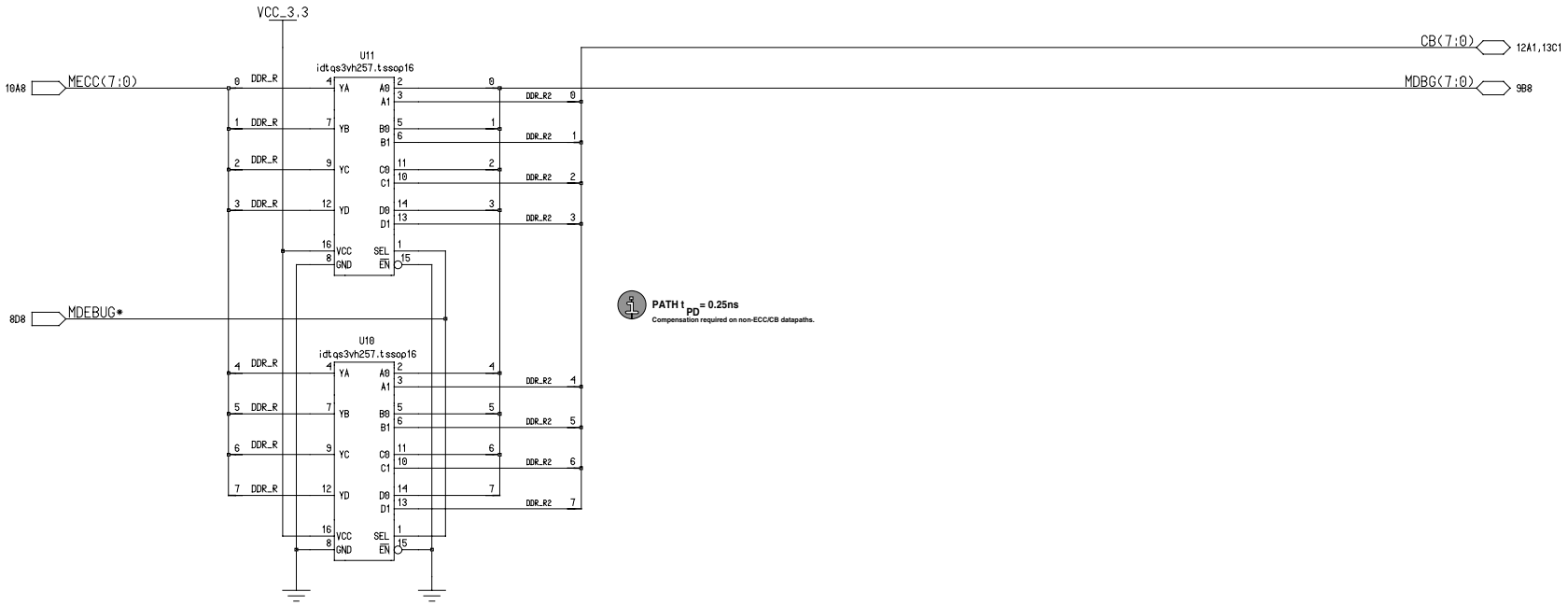
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 10/30/2003 Time Changed: 10:33:15 am	Title: DaughterCard Configuration	Page: 08



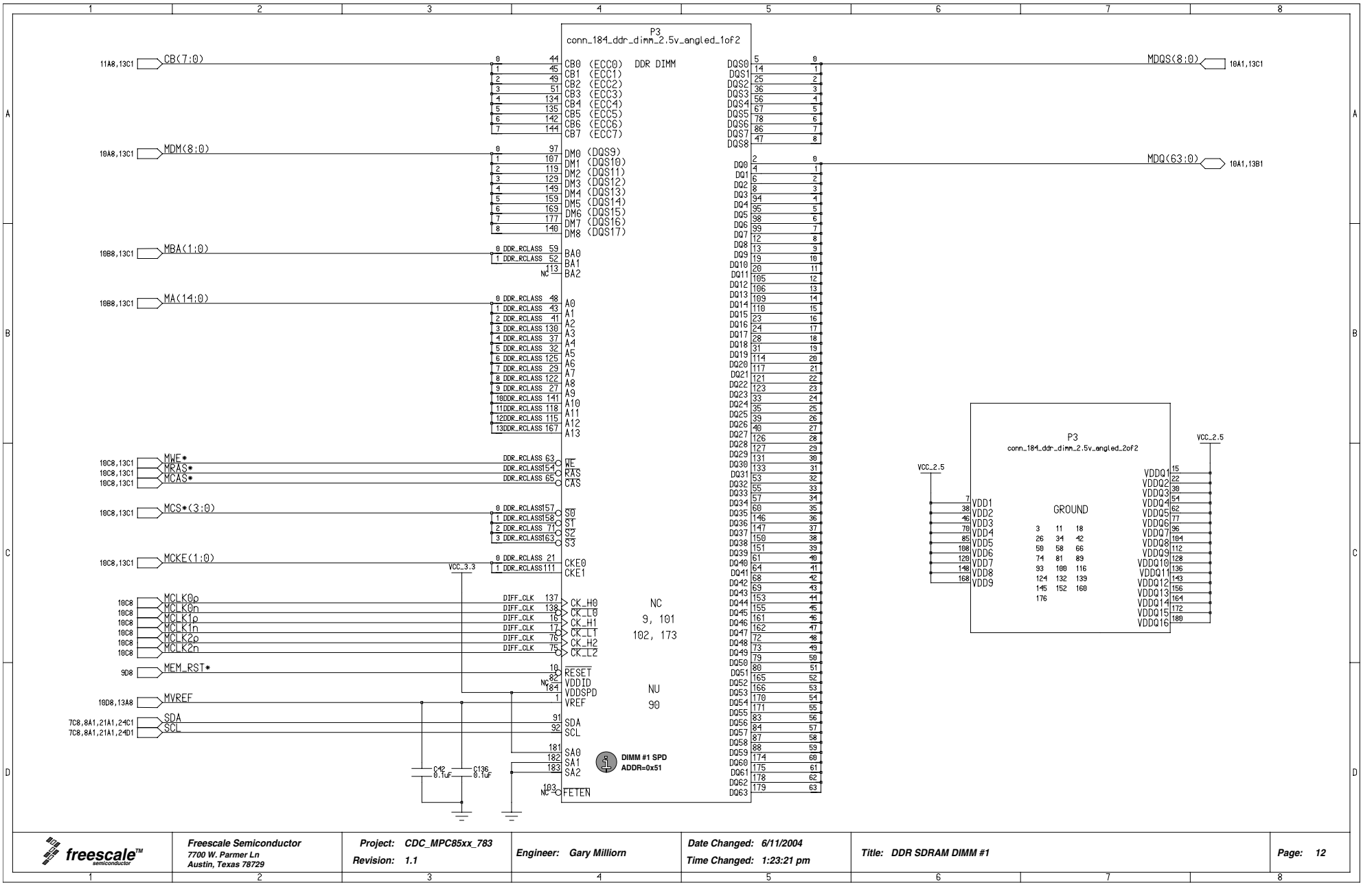
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 11:30:39 am	Title: PCI2 Clock Gen, Debug Interfaces, Reset	Page: 09



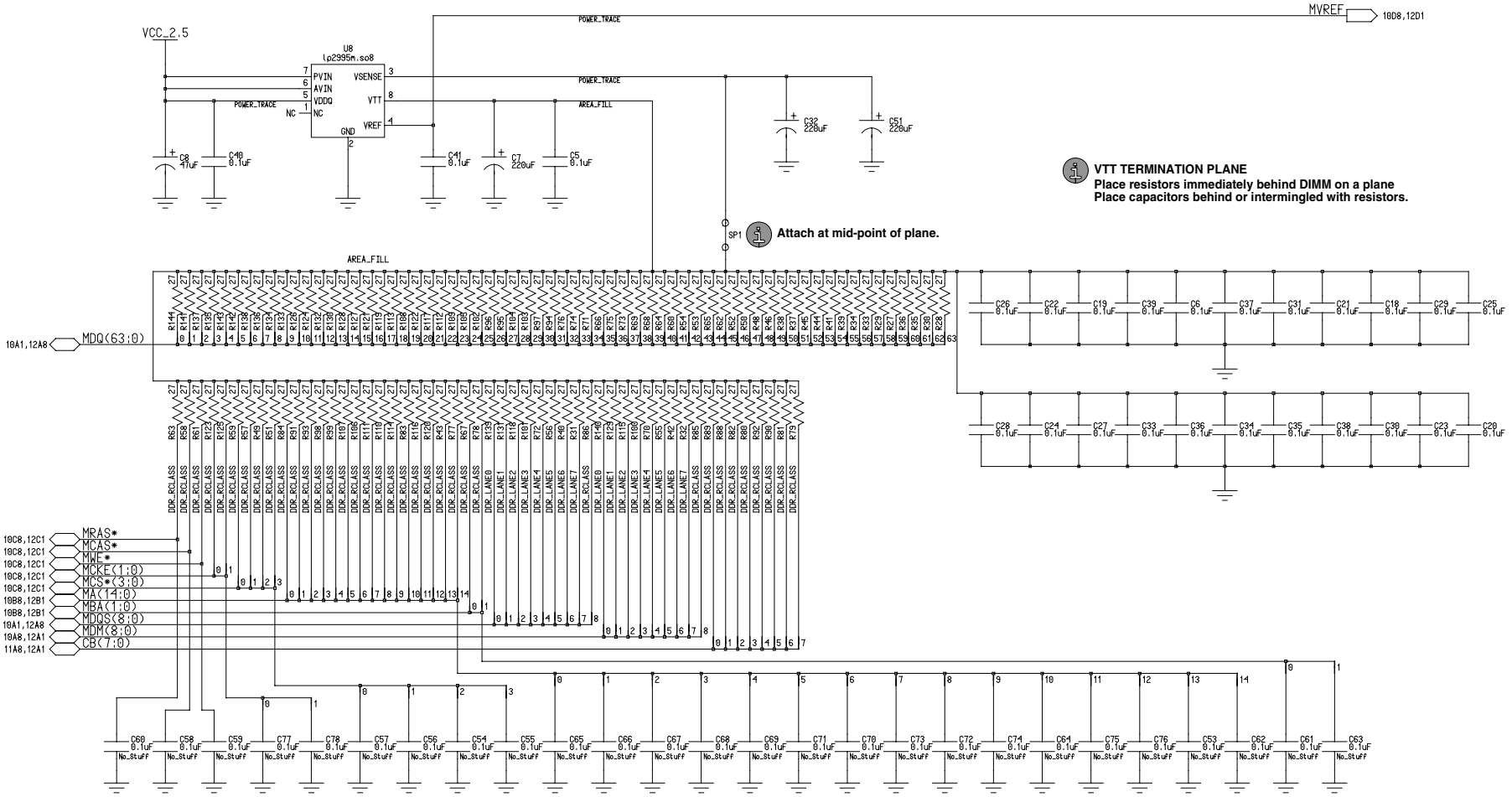
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 3:11:01 pm	Title: Processor DDR Interface	Page: 10



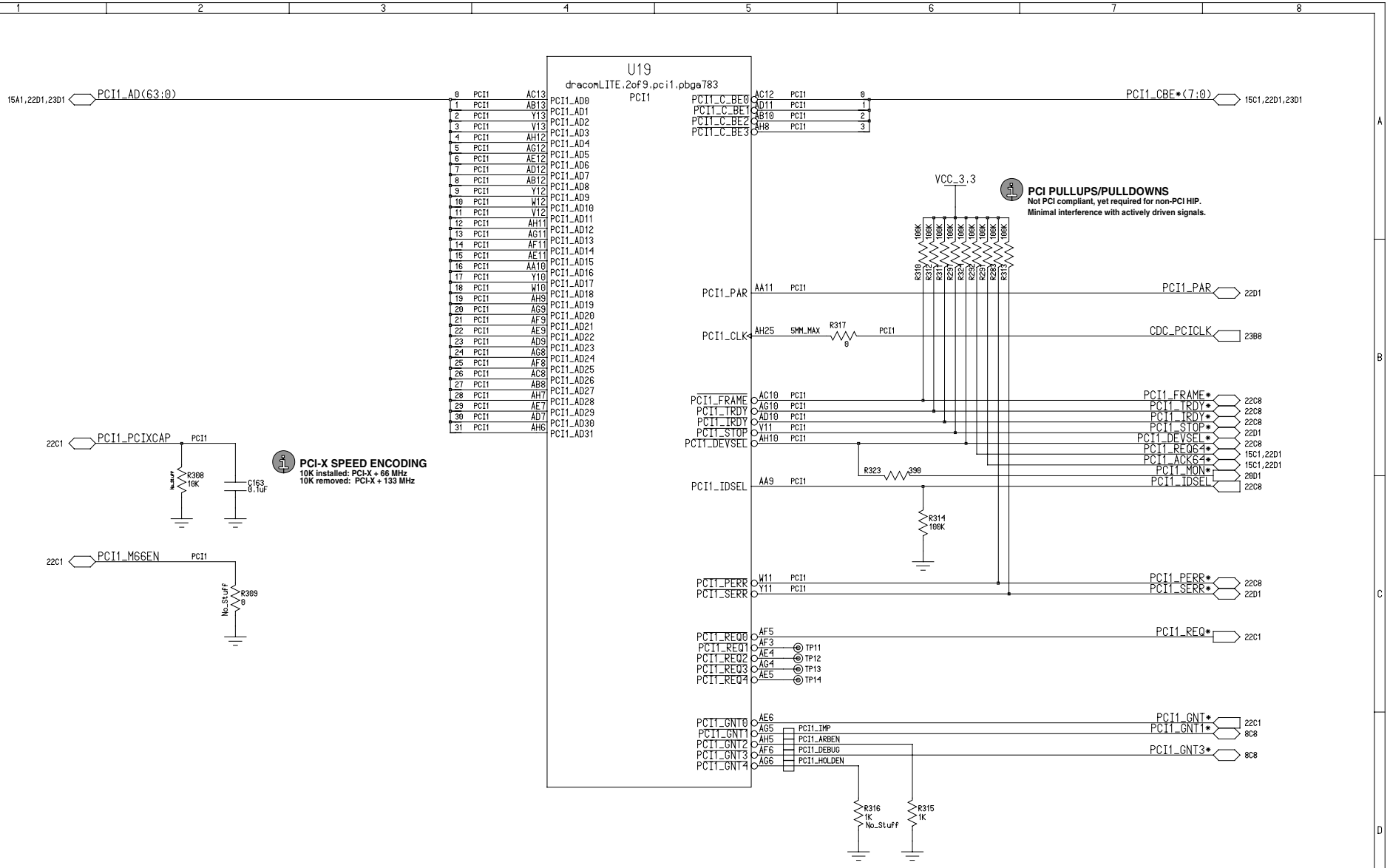
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 7/27/2004 Time Changed: 3:18:28 pm	Title: ECC Debug Access Breakout	Page: 11



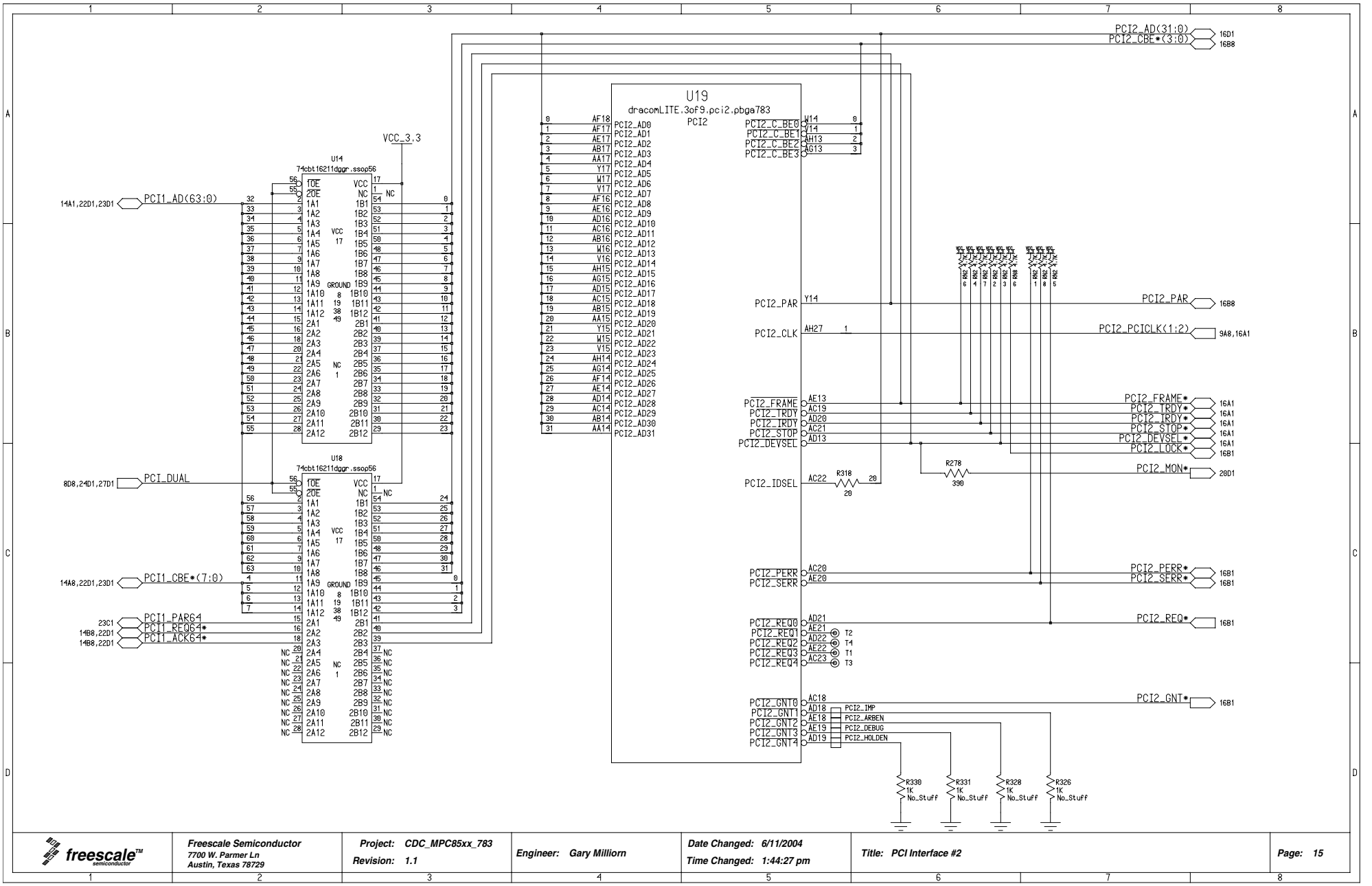
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 1:23:21 pm	Title: DDR SDRAM DIMM #1	Page: 12



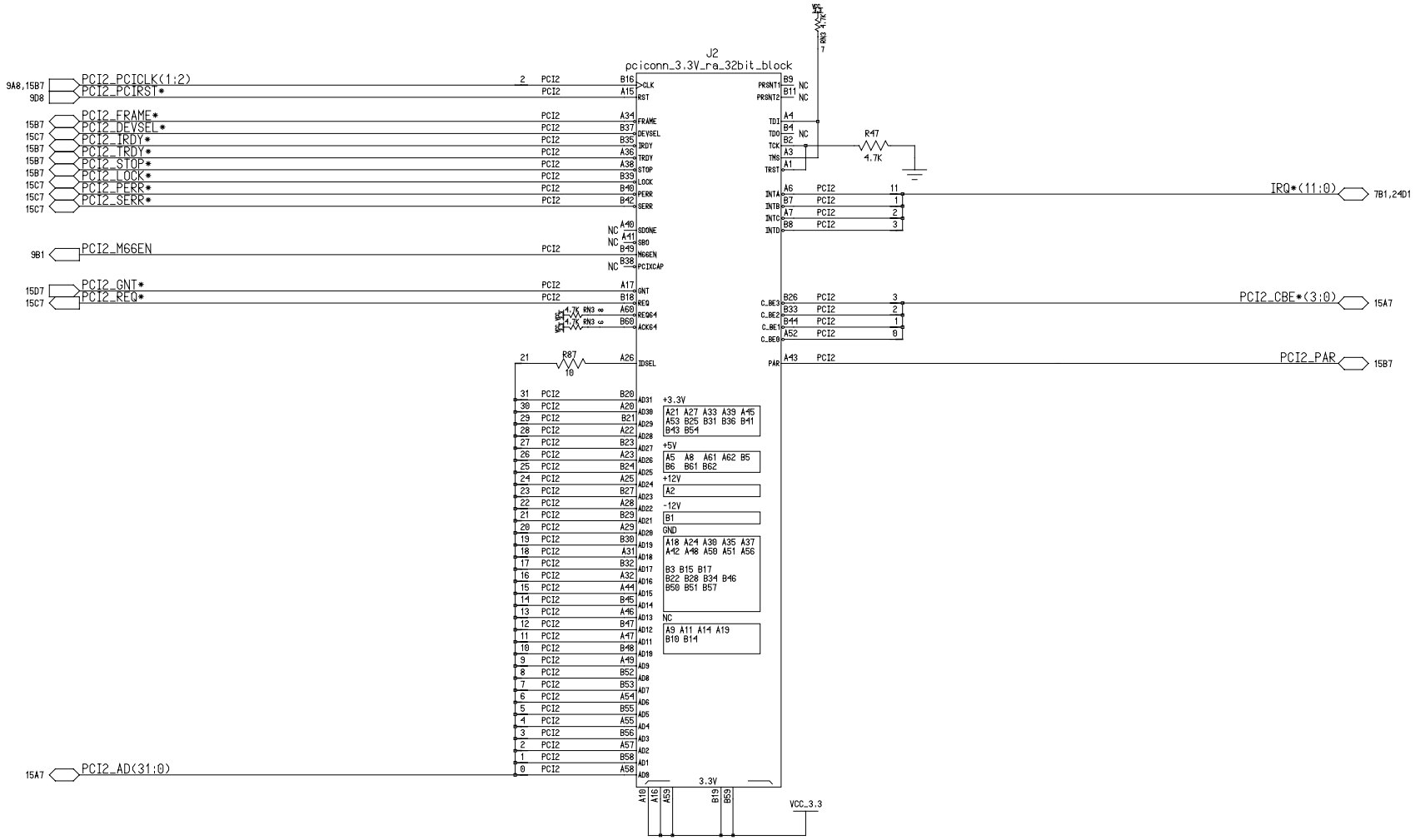
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 1:24:27 pm	Title: VTT+Termination Power and Termination Array	Page: 13



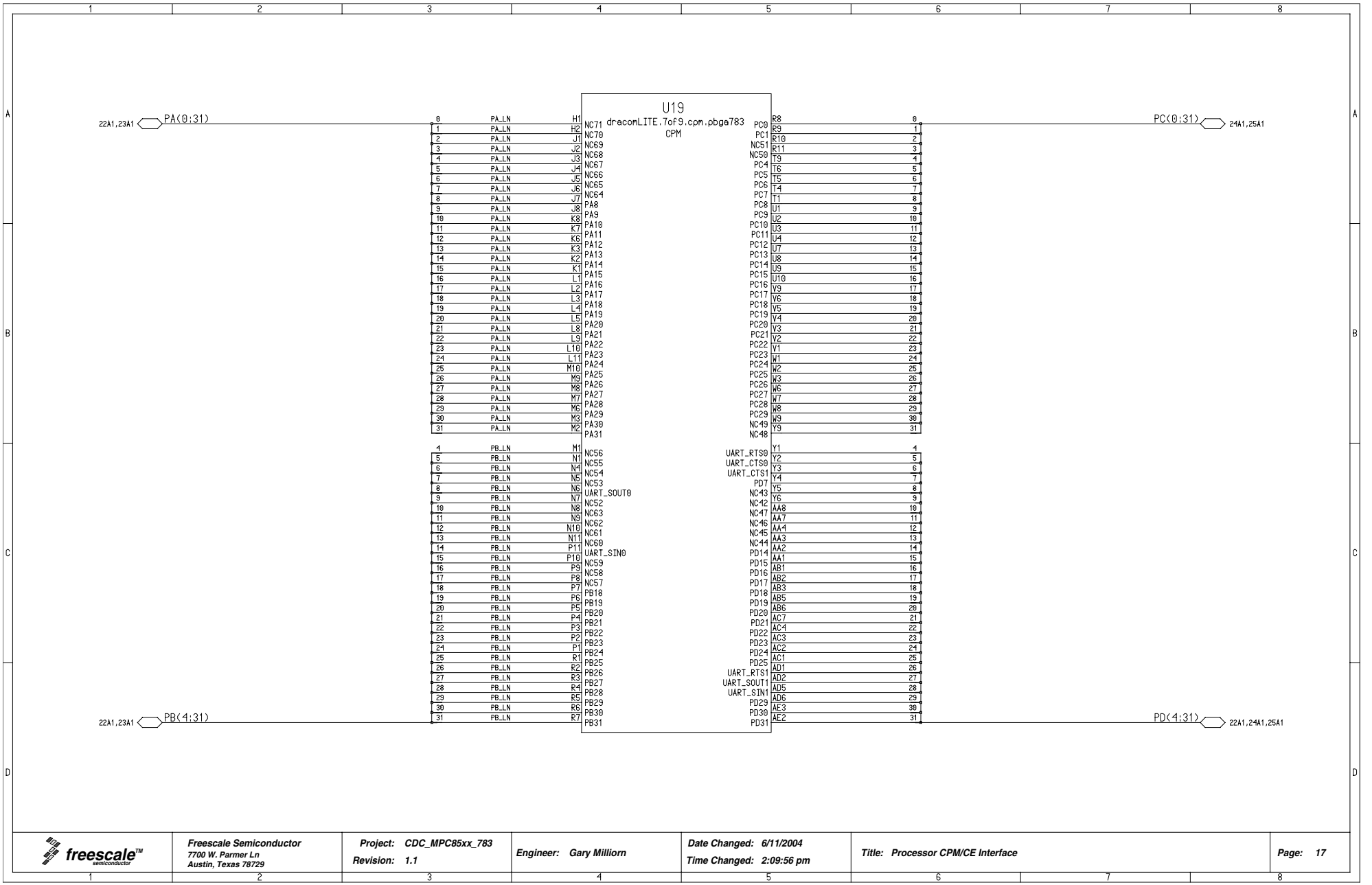
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 3:17:32 pm	Title: PCI Interface #1	Page: 14 of 35



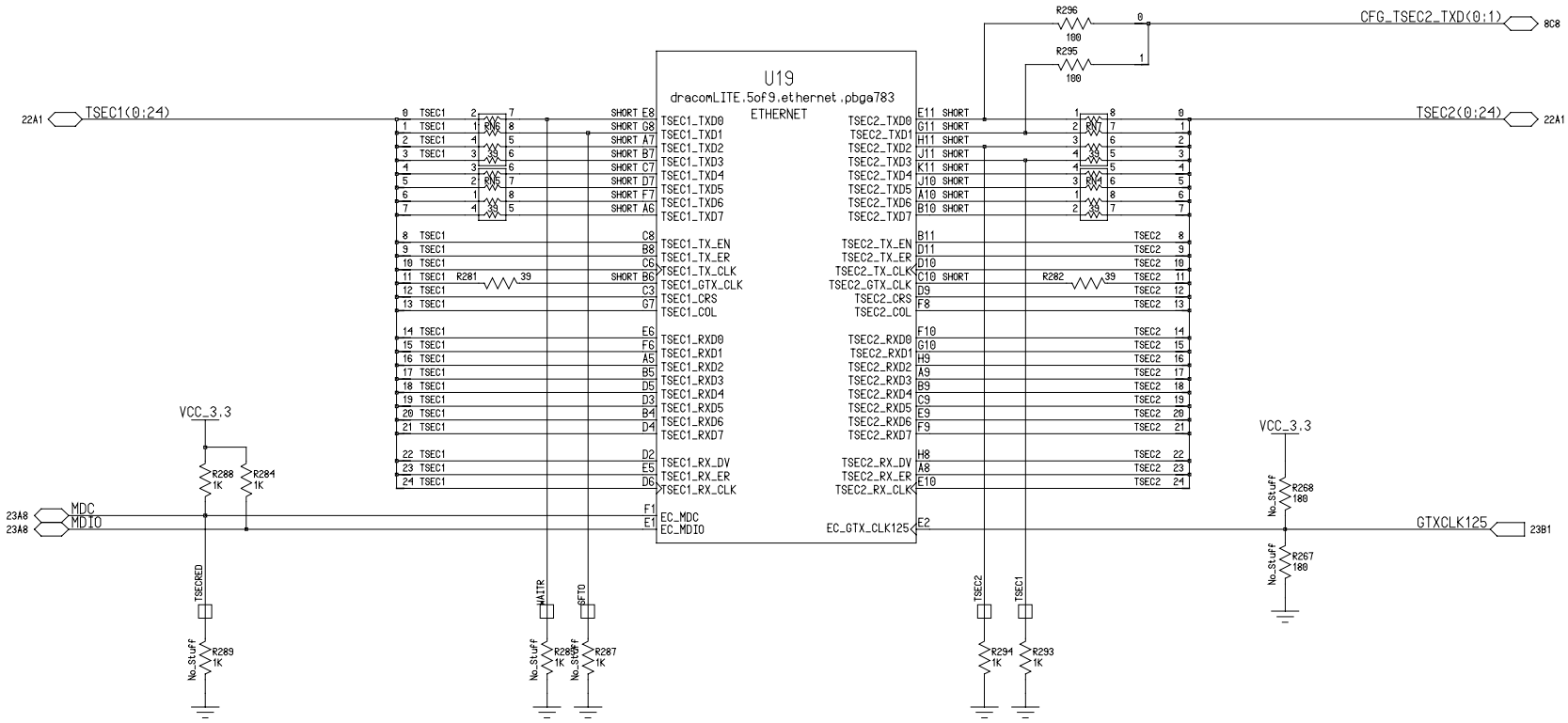
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 1:44:27 pm	Title: PCI Interface #2	Page: 15



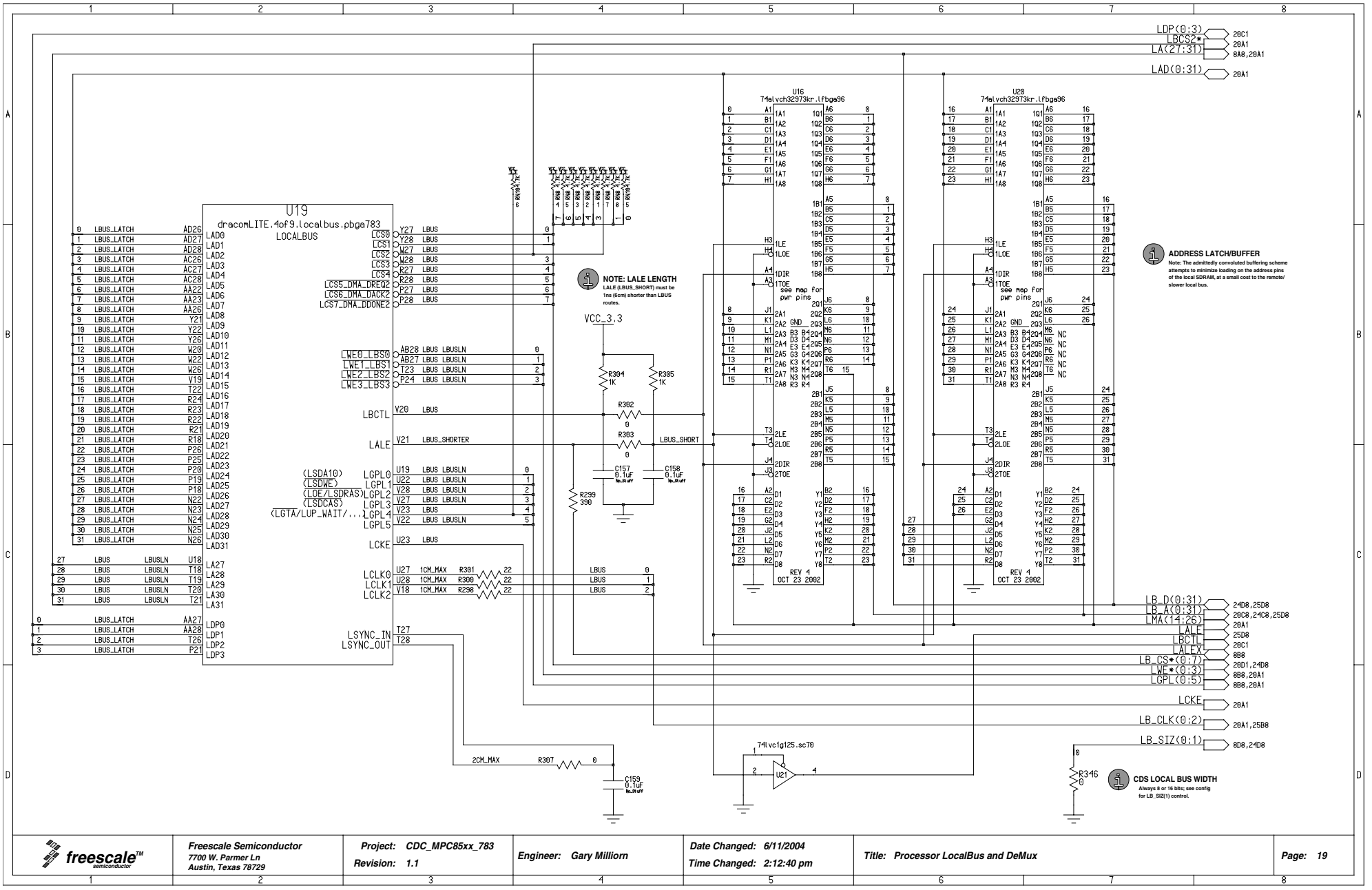
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:08:26 pm	Title: Secondary PCI Slot	Page: 16



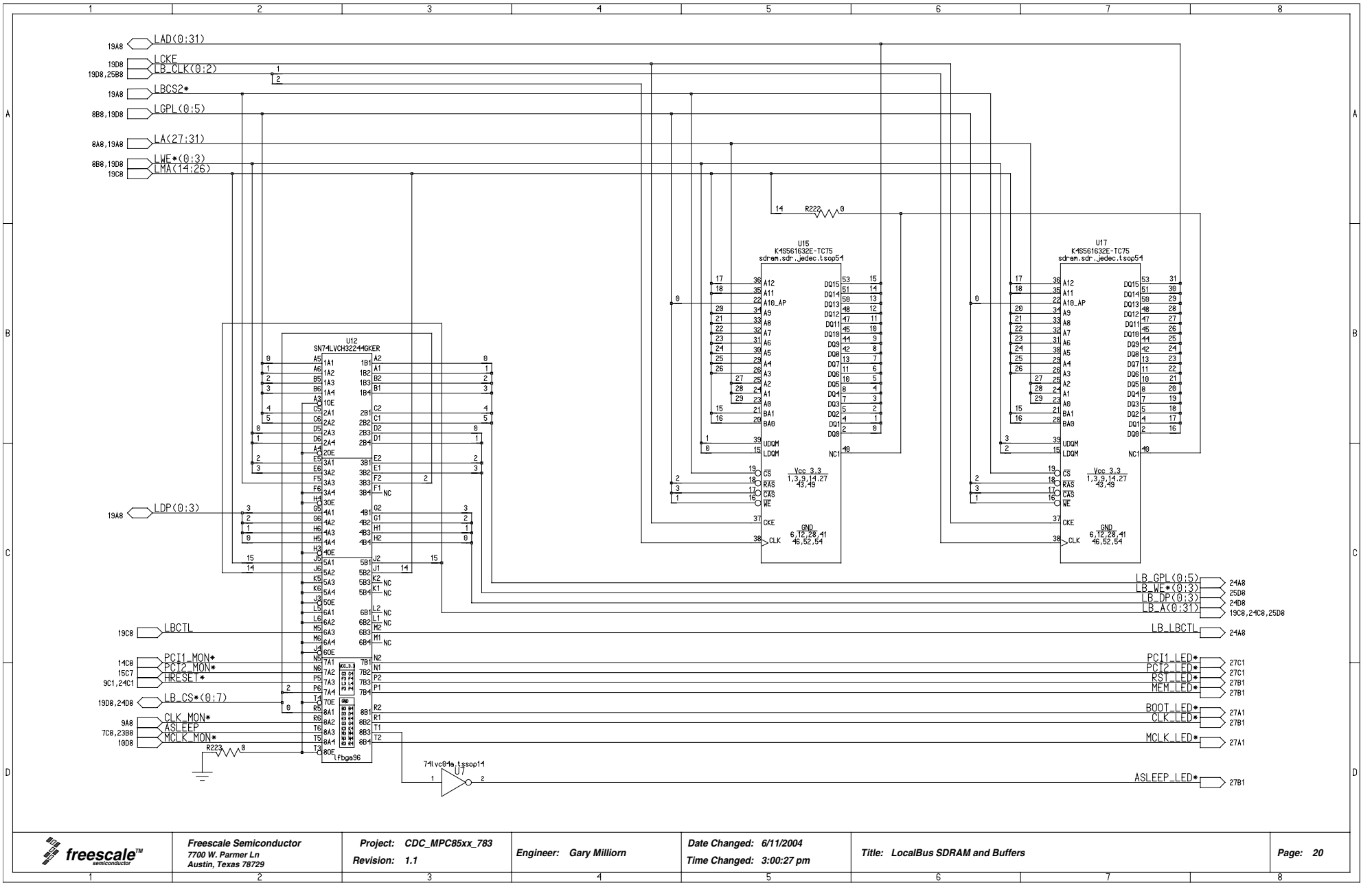
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:09:56 pm	Title: Processor CPM/CE Interface	Page: 17



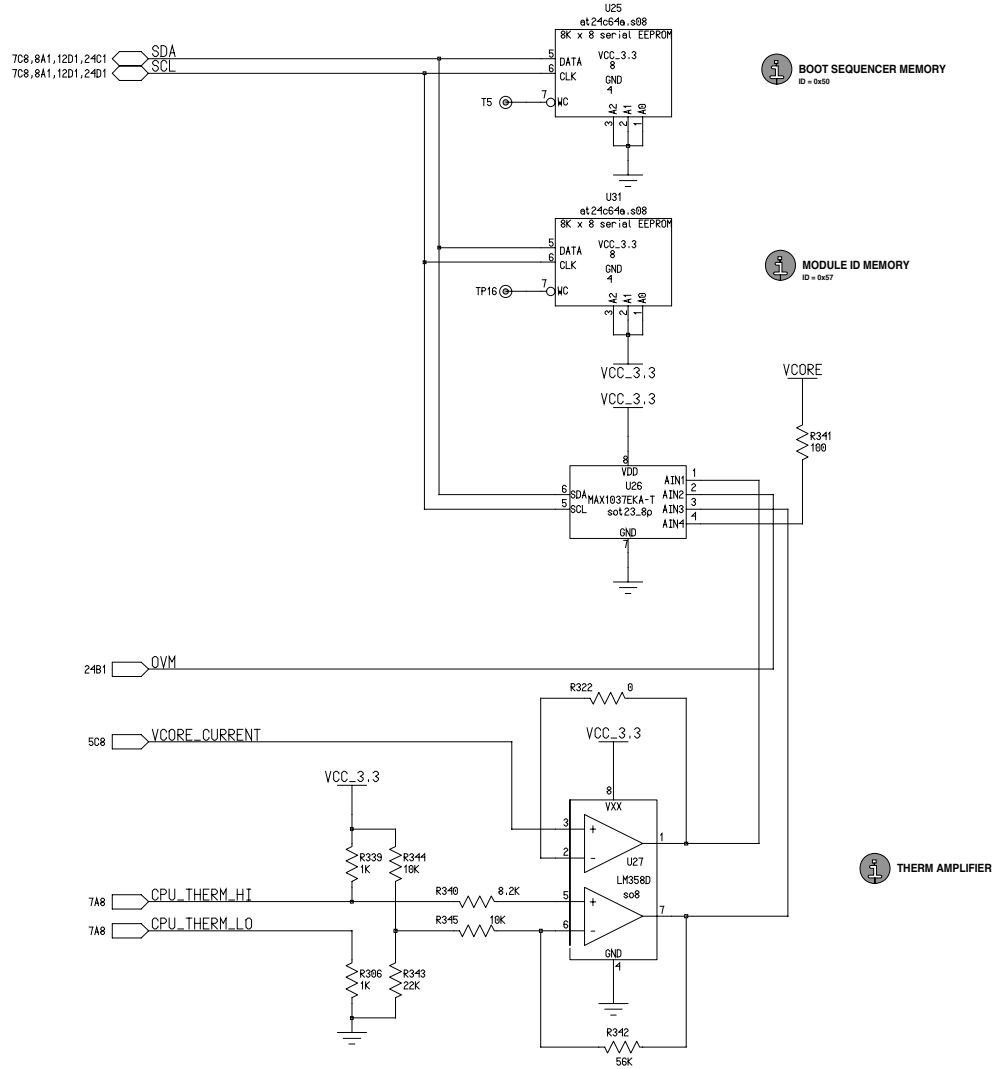
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:11:21 pm	Title: TSEC Ethernet Interface	Page: 18



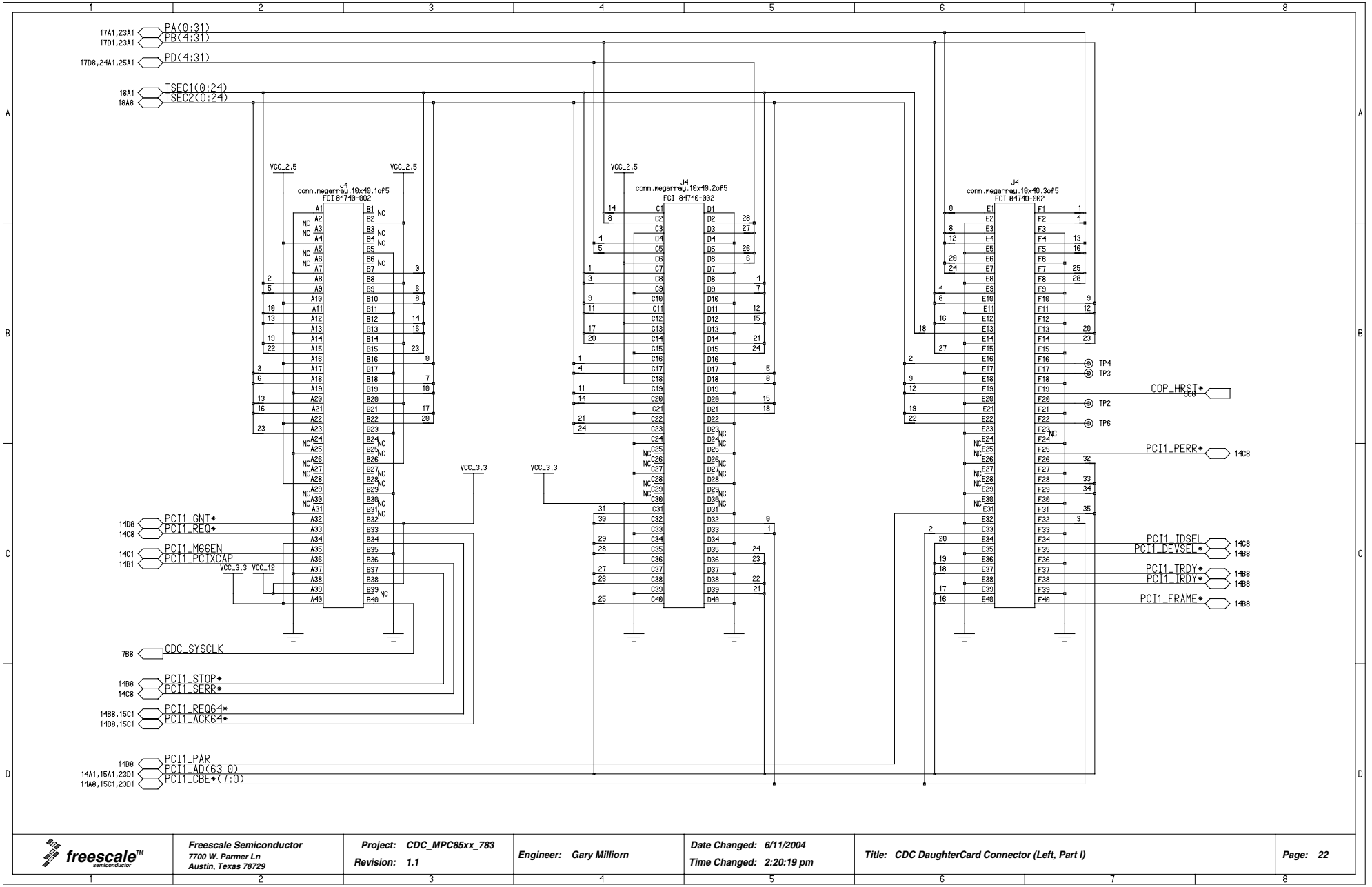
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:12:40 pm	Title: Processor LocalBus and DeMux	Page: 19



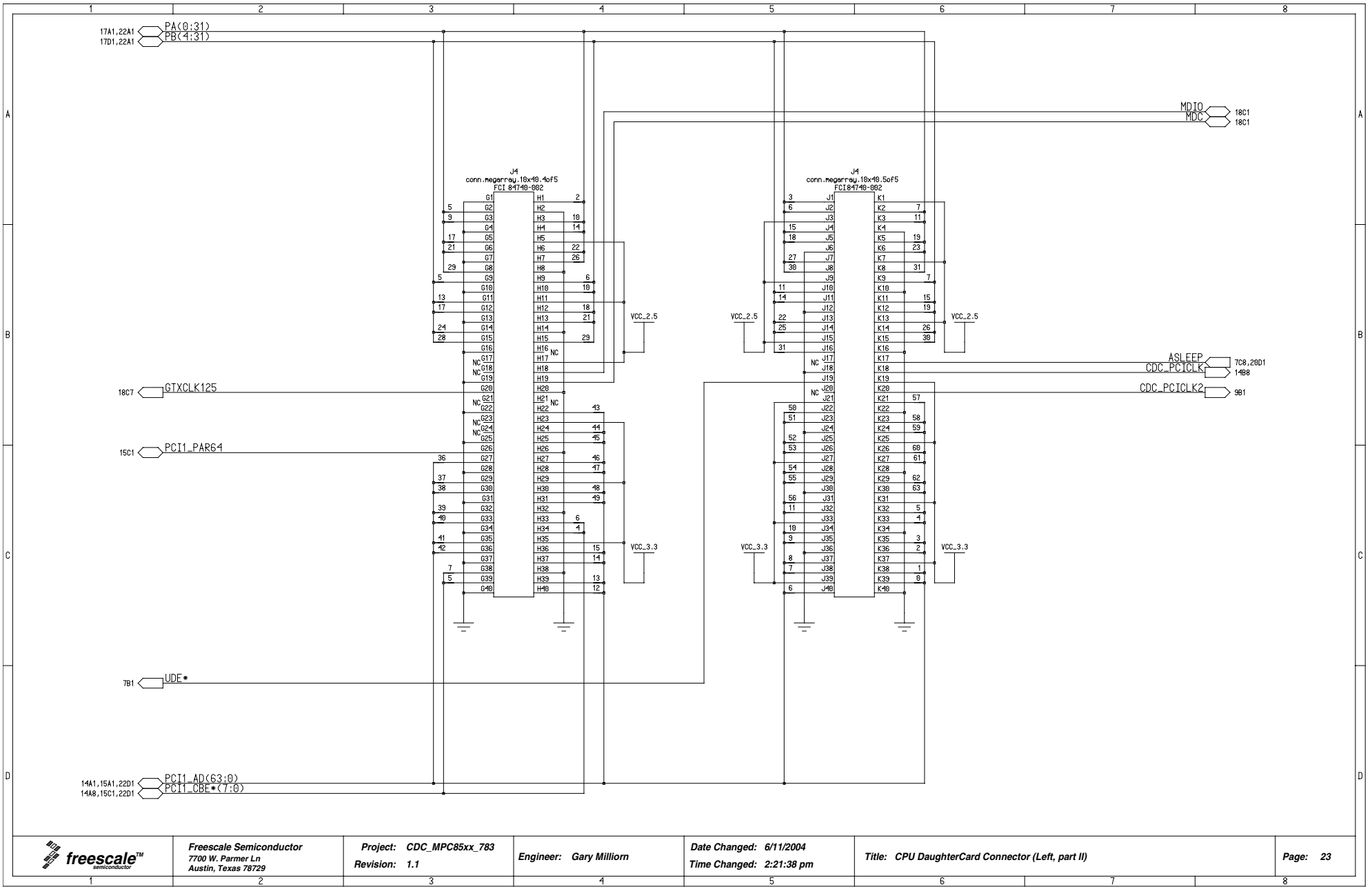
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 3:00:27 pm	Title: LocalBus SDRAM and Buffers	Page: 20



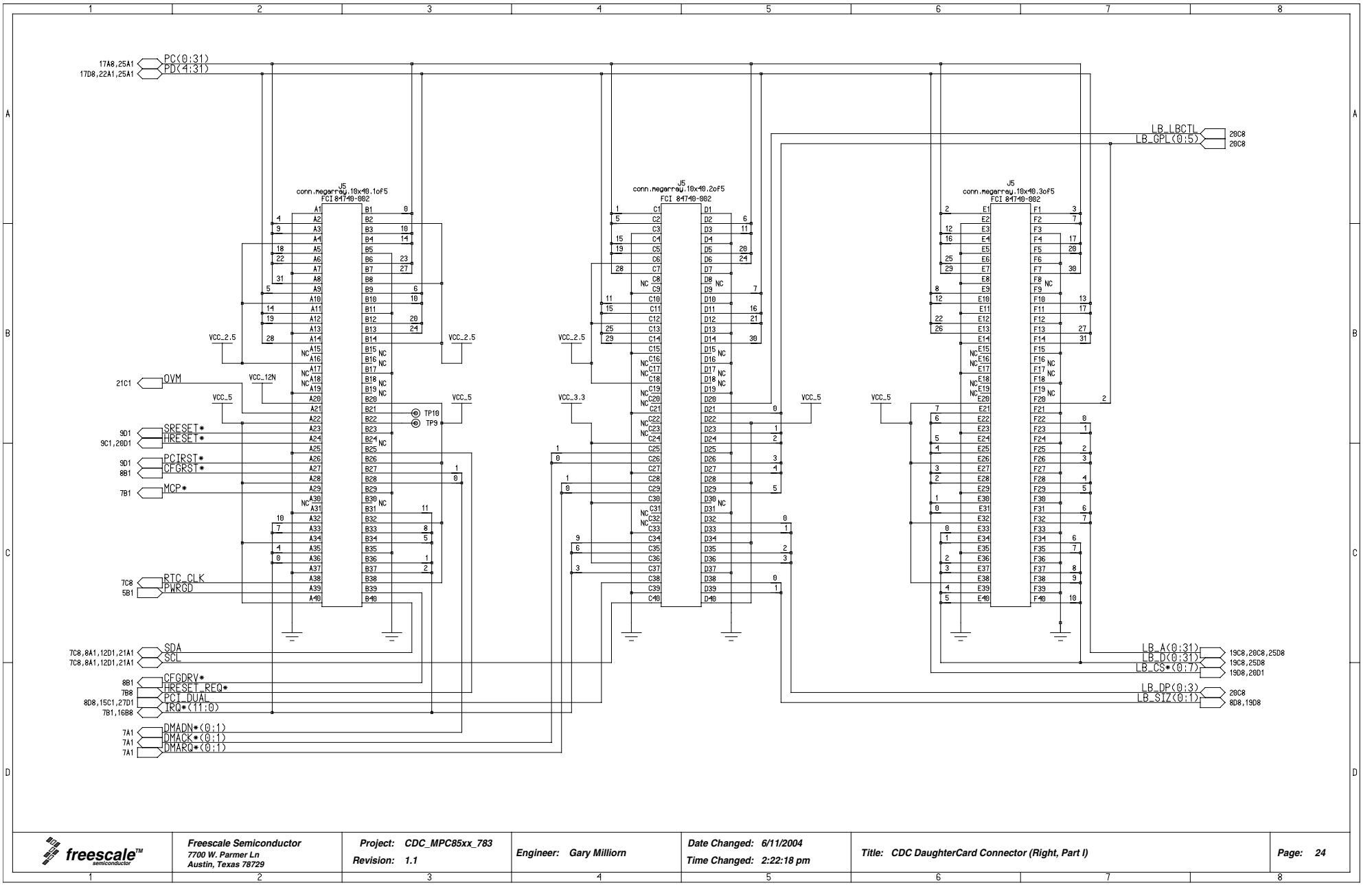
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:16:23 pm	Title: I2C Bus and Components	Page: 21



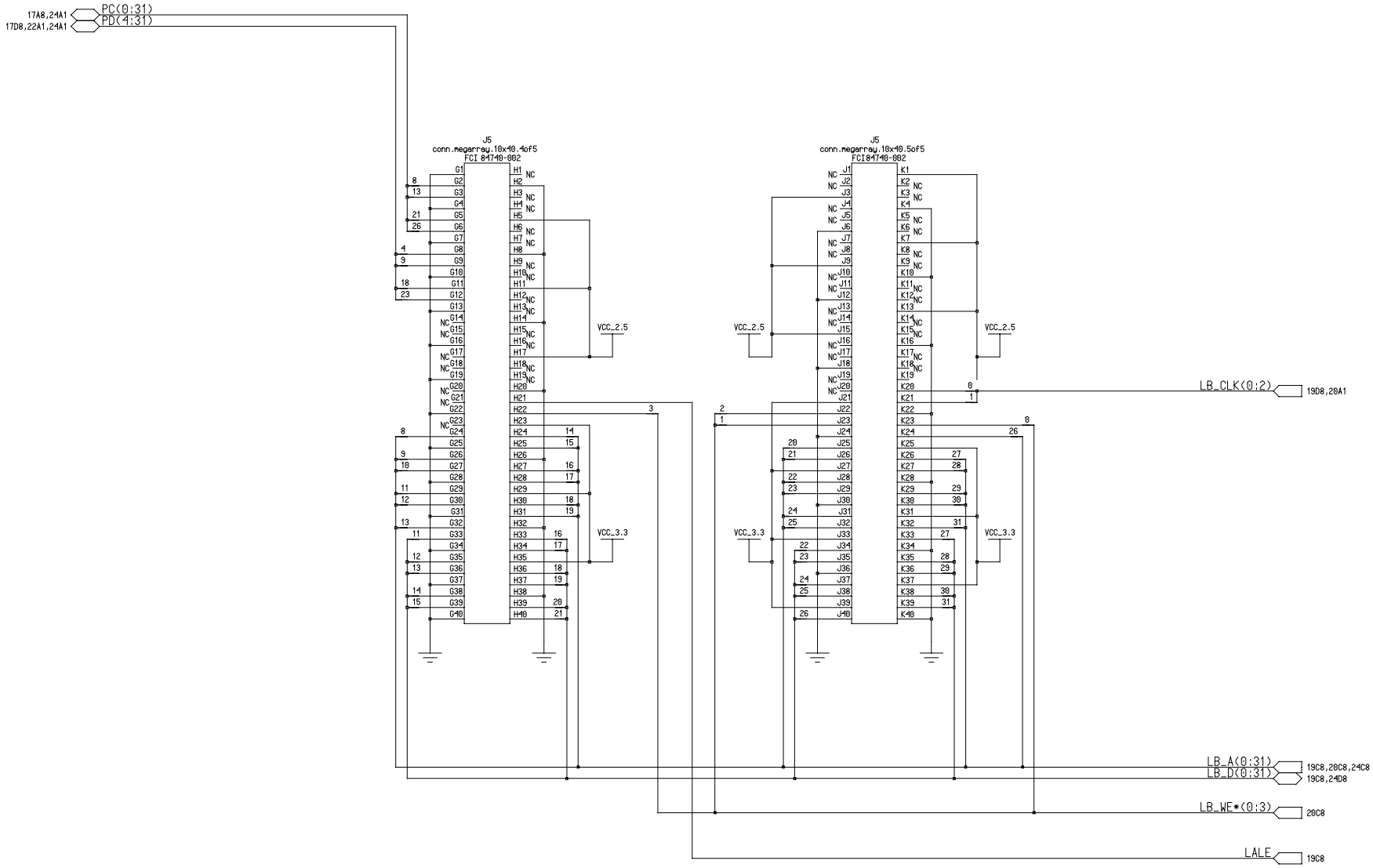
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:20:19 pm	Title: CDC DaughterCard Connector (Left, Part I)	Page: 22



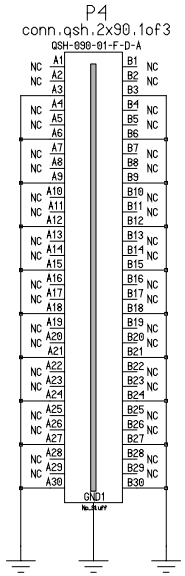
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:21:38 pm	Title: CPU DaughterCard Connector (Left, part II)	Page: 23

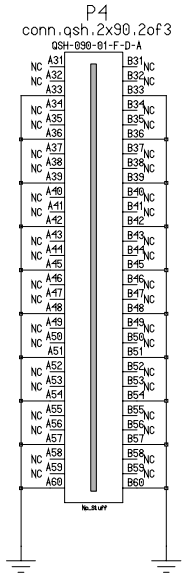


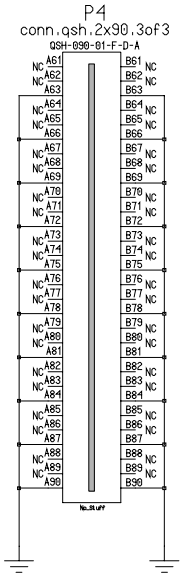
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:22:18 pm	Title: CDC DaughterCard Connector (Right, Part I)	Page: 24



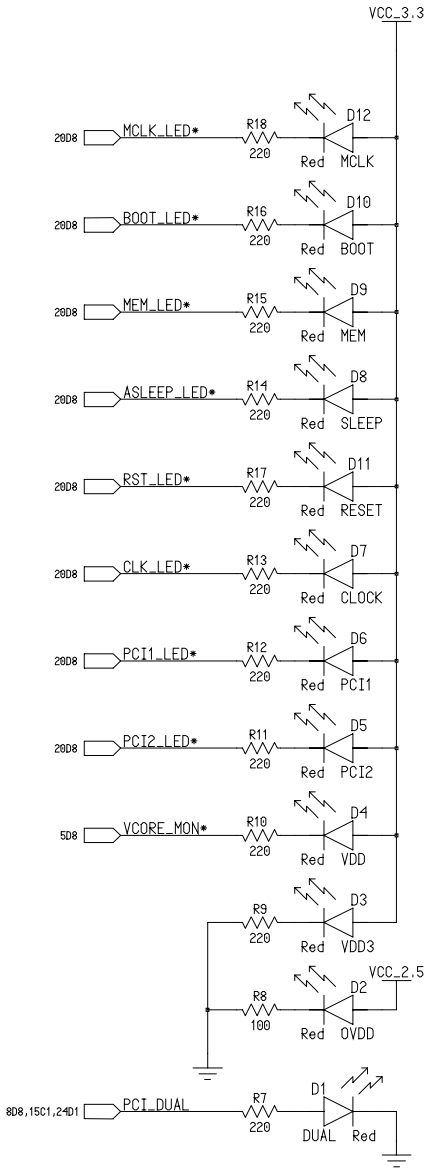
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:24:22 pm	Title: CDC DaughterCard Connector (Right, Part II)	Page: 25



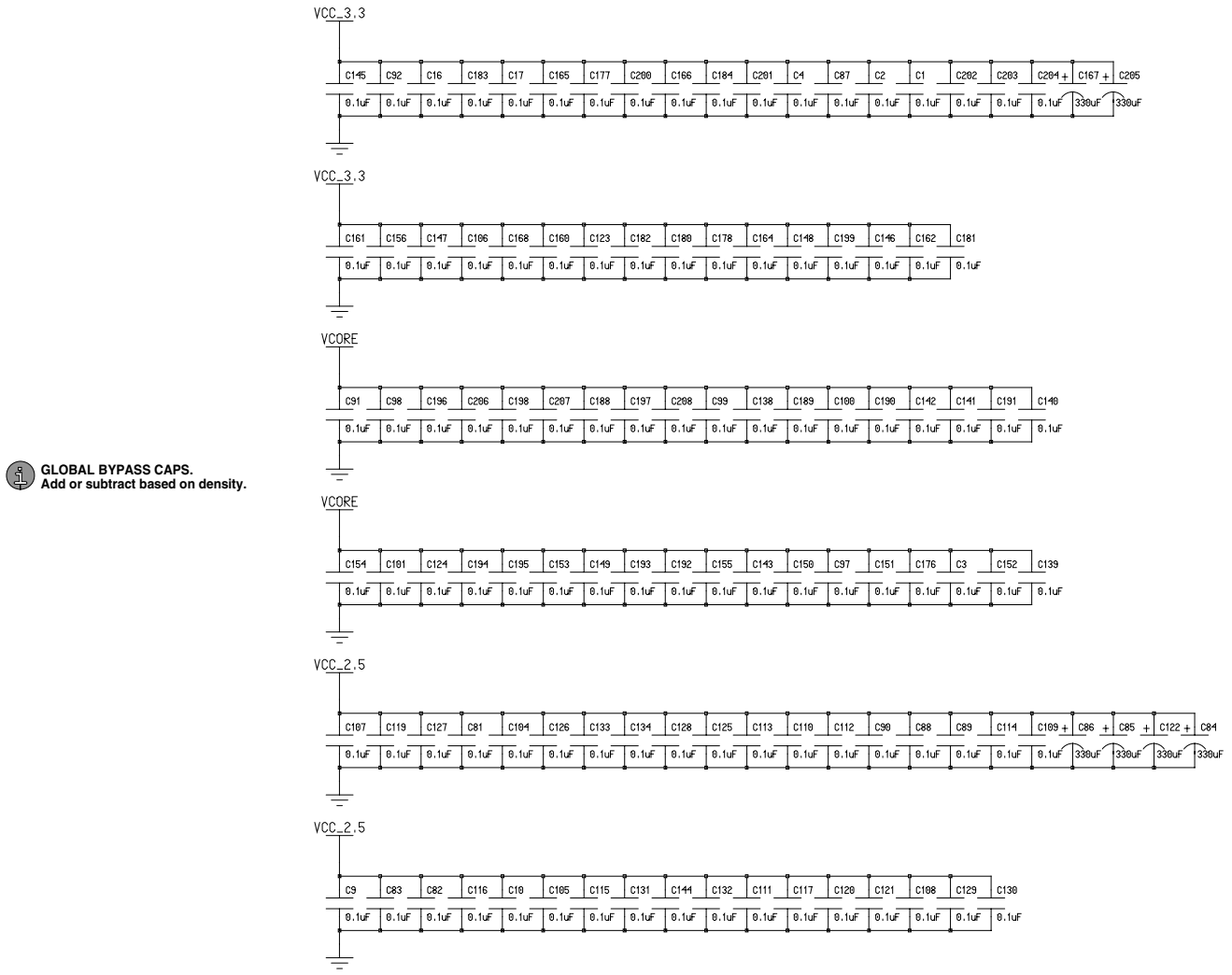




freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:27:25 pm	Title: High-Speed Differential Connector	Page: 26



freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:33:23 pm	Title: Miscellany	Page: 27

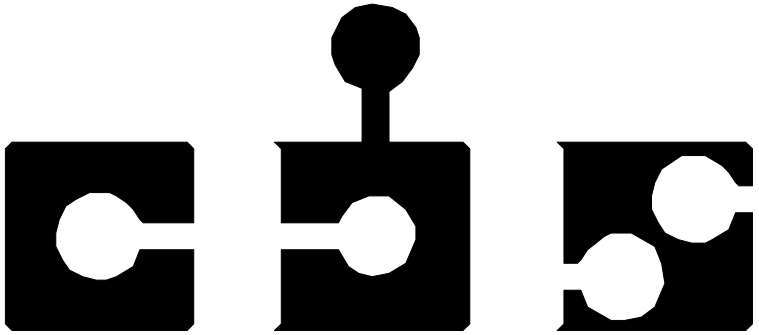


GLOBAL BYPASS CAPS.
Add or subtract based on density.

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDC_MPC85xx_783 Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 2:34:52 pm	Title: Bypass Capacitors	Page: 28

Appendix I
CDS I/O Board Schematics

This appendix provides CDS I/O board schematics.



IOCard

freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_IOCard Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 9:30:23 am	Title: Cover Story	Page: 01

Schematic Notes

1. Unless otherwise specified:
   All resistors are SMD0402, in ohms, 0.08W, +/-5%
   All capacitors are SMD0402, in microfarads (uF), +/-20%.
   All inductances are in microhenries (uH).
   All ferrites are Z=50 ohms at 100 MHz.
   All fuses are self-resetting polyswitch (PTC) devices.
   Board impedance is 55 +/- 5 ohms.

2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:

VCC_3.3	VCC_2.5	GND
VCC_5	VCC_1.2	VCORE

3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.

4.

5. The sheet-to-sheet cross reference format is:
   Sheet VertZoneLetter HorizZoneNumber

6. Components with the label "No_Stuff" are not to be installed by default; they are for test or manufacturing purposes only.

7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

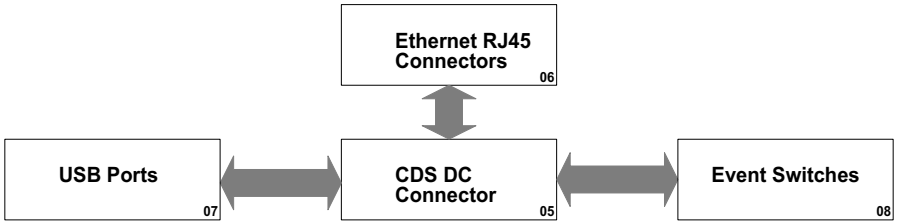
IOCard

**This schematic is provided for reference purposes only.
All information is subject to change without notice.
No warranty, expressed or applied, is made as to the accuracy of the information contained herein.**

REV	DATE	CHANGES
V1.0	03SEP25	Initial version
V1.1	04JUN11	Switch and RJ45 pinout fixes.

freescale semiconductor
Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

Project: CDS_IOCard
Revision: 1.1
Engineer: Gary Milliorn
Date Changed: 6/11/2004
Time Changed: 9:32:25 am
Title: Information, please.
Page: 02



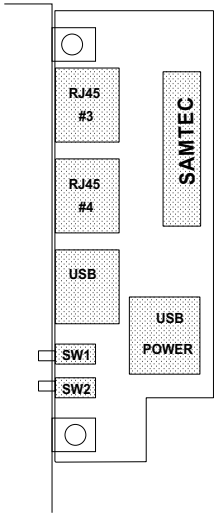
freescale semiconductor
Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

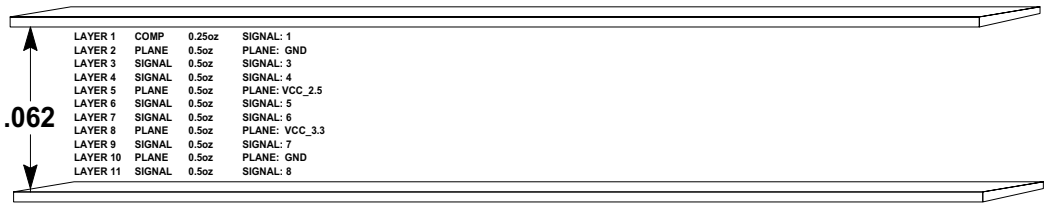
Project: CDS_IOCard
Revision: 1.1

Engineer: Gary Milliorn

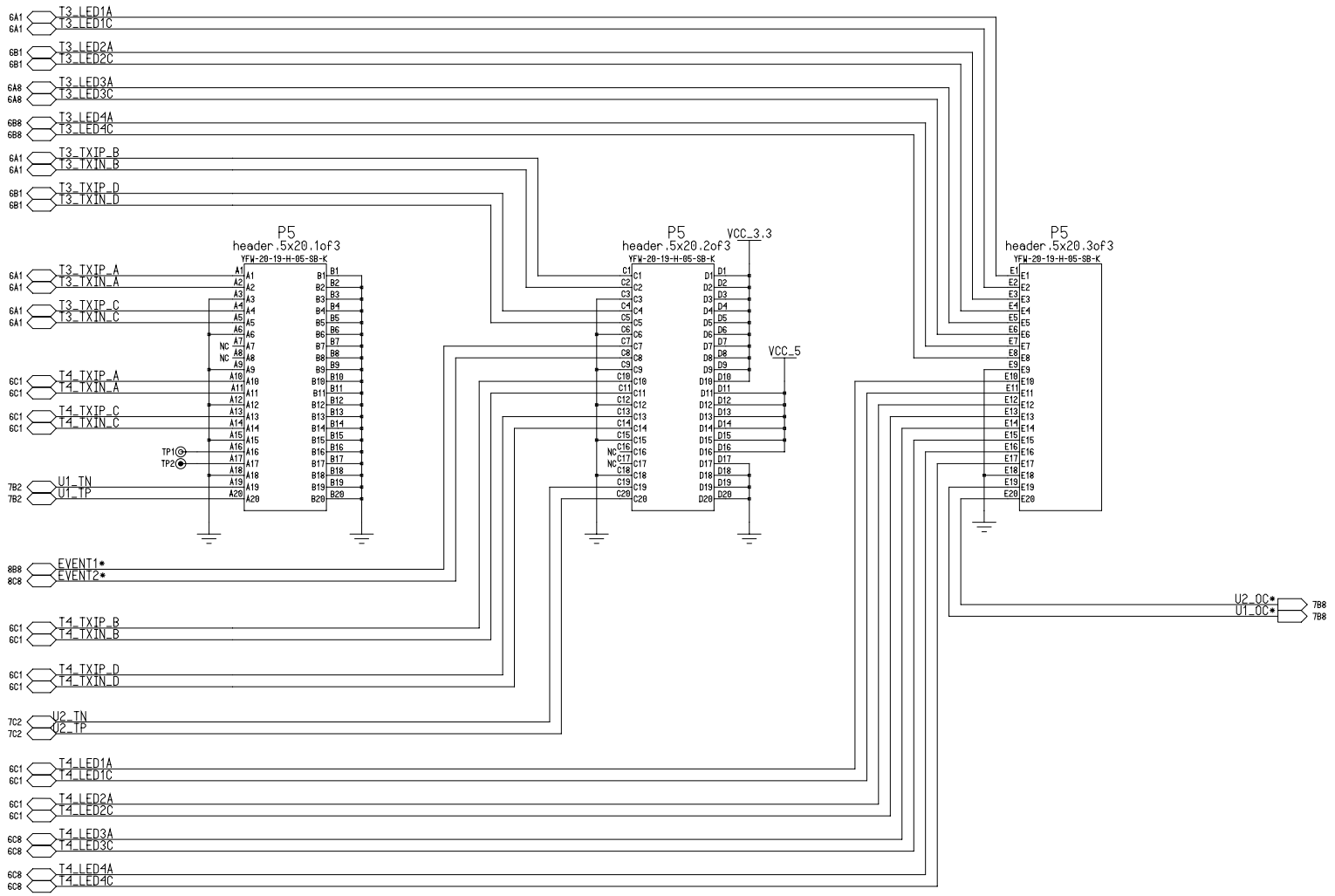
Date Changed: 6/11/2004
Time Changed: 9:13:59 am

Title: Block Diagram

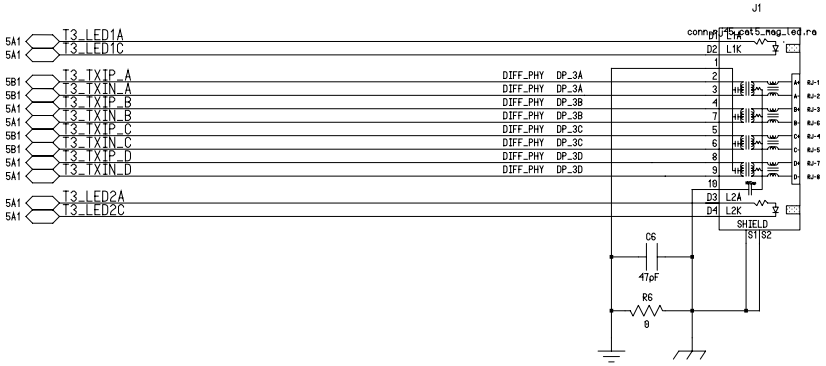




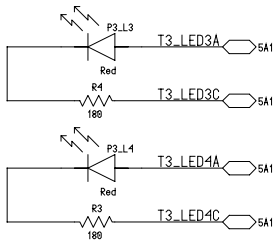
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_IOCard Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 9:12:28 am	Title: Placement and Stackup	Page: 04

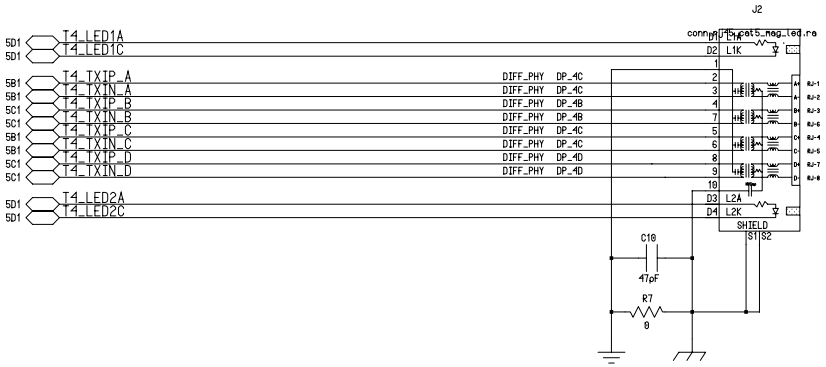


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_IOCard Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 9:09:53 am	Title: Carrier-to-IOCard Connector	Page: 05

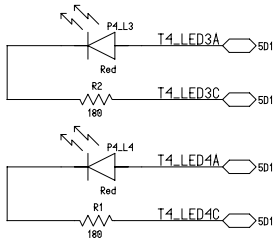


ETHERNET PORT #3

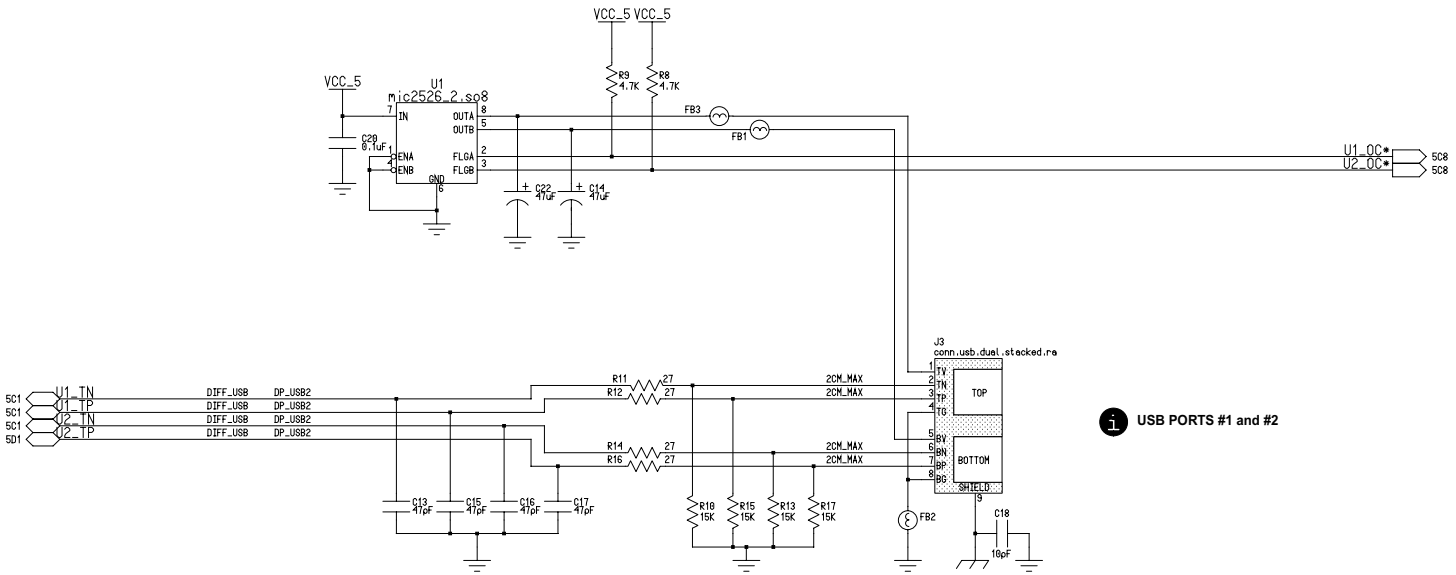




ETHERNET PORT #4

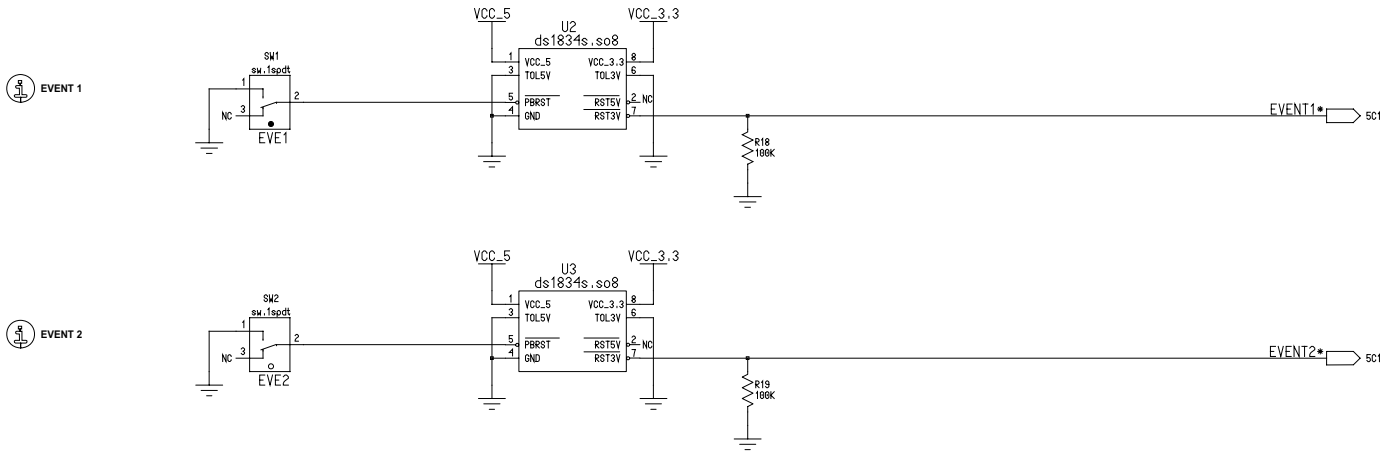


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_IOCard Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 4/9/2004 Time Changed: 1:54:15 pm	Title: Ethernet Ports #3 and #4	Page: 01

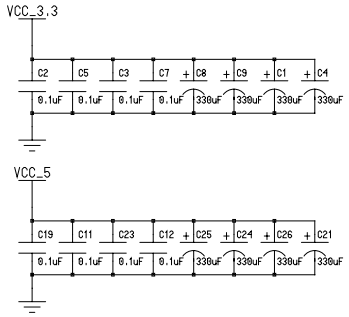


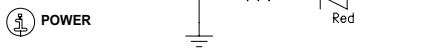
USB PORTS #1 and #2

freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_IOCard Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 4/9/2004 Time Changed: 1:54:15 pm	Title: USB Ports and Power	Page: 01



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_IOCard Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 9:53:24 am	Title: Event Switches	Page: 08

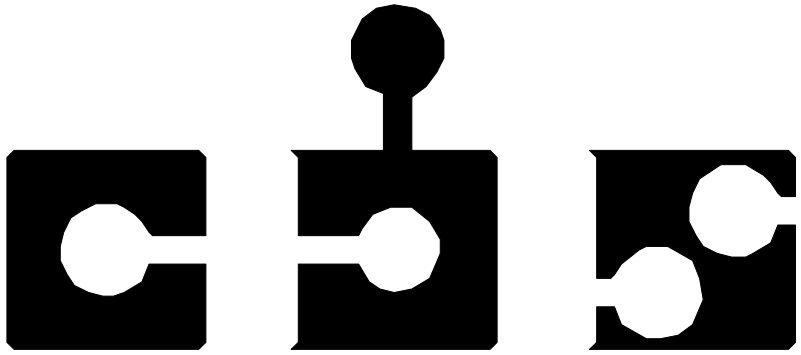




freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_IOCard Revision: 1.1	Engineer: Gary Milliorn	Date Changed: 6/11/2004 Time Changed: 10:19:09 am	Title: Miscellaneous	Page: 09

Appendix J
CDS uTCOM Schematics

This appendix provides uTCOM schematics.



uTCOM

MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 1/12/2004 Time Changed: 2:20:33 pm	Title: Title Page	Page: 01

Schematic Notes	
1.	Unless otherwise specified: All resistors are SMD0603, in ohms, +/-5% All capacitors are SMD0402, in microfarads (uF), +/-20%. All inductances are in microhenries (uH). All ferrites are Z=50 ohms at 100 MHz. All fuses are self-resetting polyswitch (PTC) devices. Board impedance is 55 +/- 5 ohms.
2.	Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are: VCC_3.3 VCC_2.5 GND VCC_5 VCC_1.2 VCORE
3.	Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.
4.	Motorola and the Motorola logo are registered trademarks of Motorola. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. All rights reserved. No warranty is made, express or implied.
5.	The sheet-to-sheet cross reference format is: Sheet VertZoneLetter HorizZoneNumber
6.	Components with the label "No_Stuff" are not to be installed by default; they are for test or manufacturing purposes only. 
7.	All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

uTCOM Adapter

This schematic is provided for reference purposes only. All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. Contact Motorola Sale/FAEs to obtain the latest information on this product.

REV	DATE	CHANGES
X1	28Jan04	Initial version

MOTOROLA

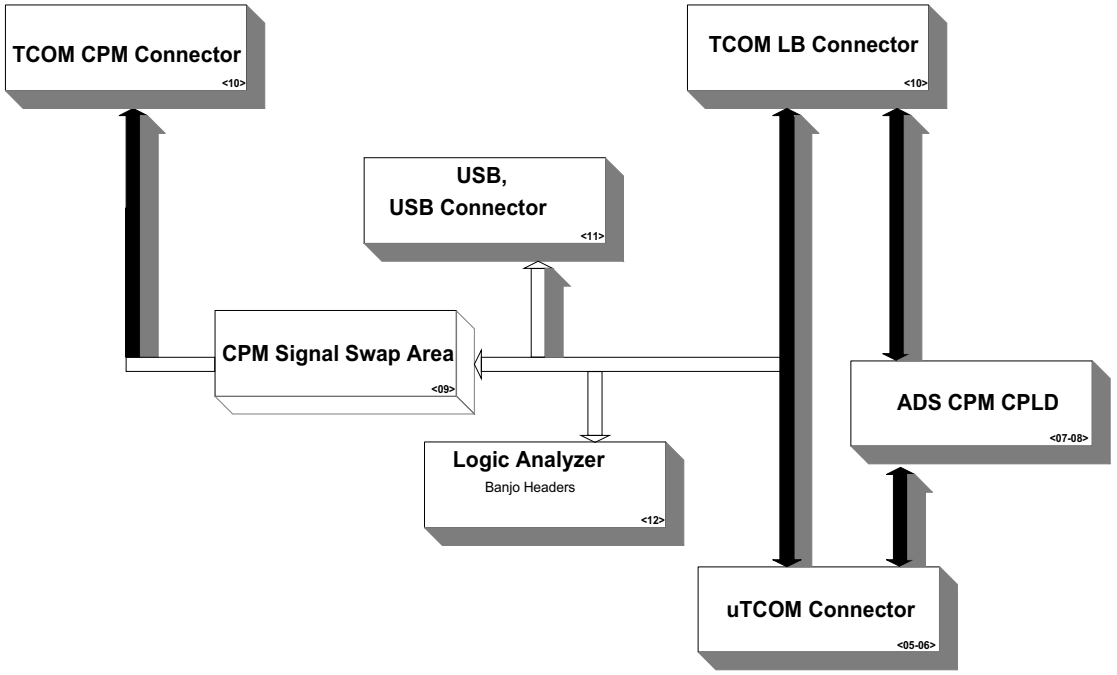
MOTOROLA INC.
7700 W. Parmer Ln
Austin, Texas 78729

Project: CDS_uTCOM
Revision: 1.0

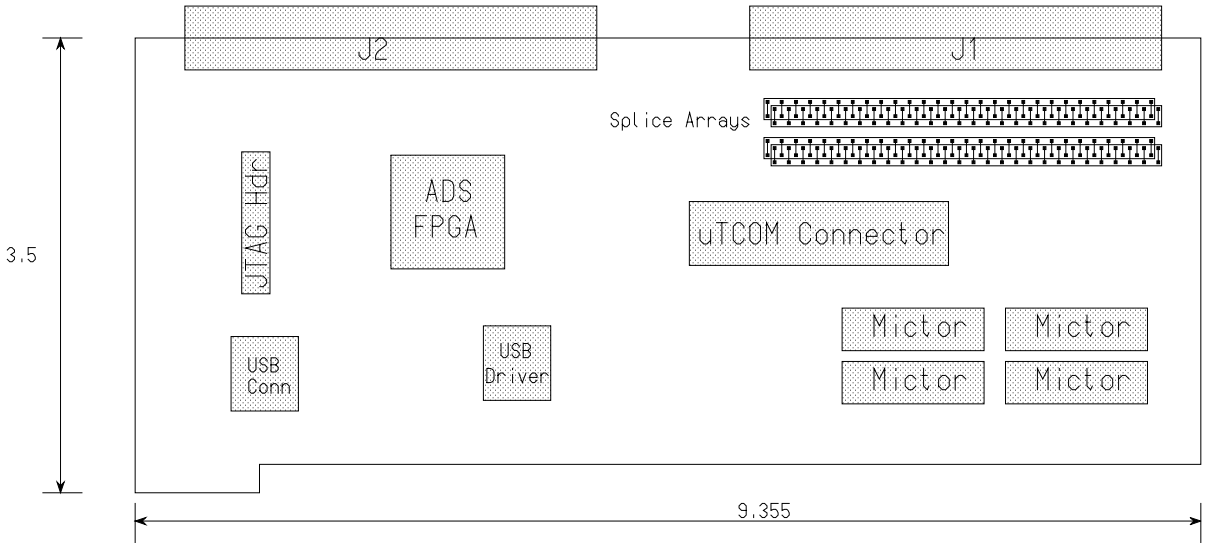
Engineer: Mark S. Harris

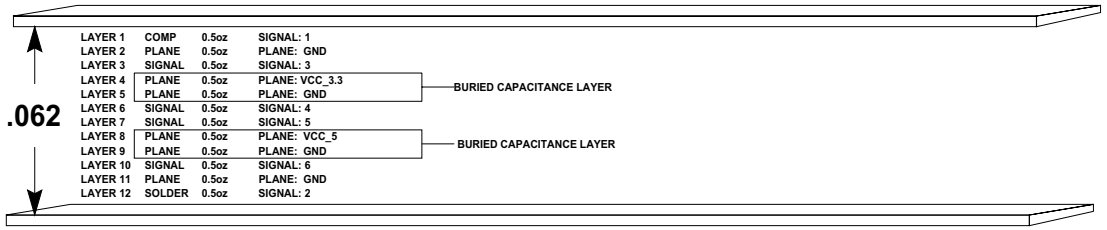
Date Changed: 1/28/2004
Time Changed: 12:20:17 pm

Title: General Information

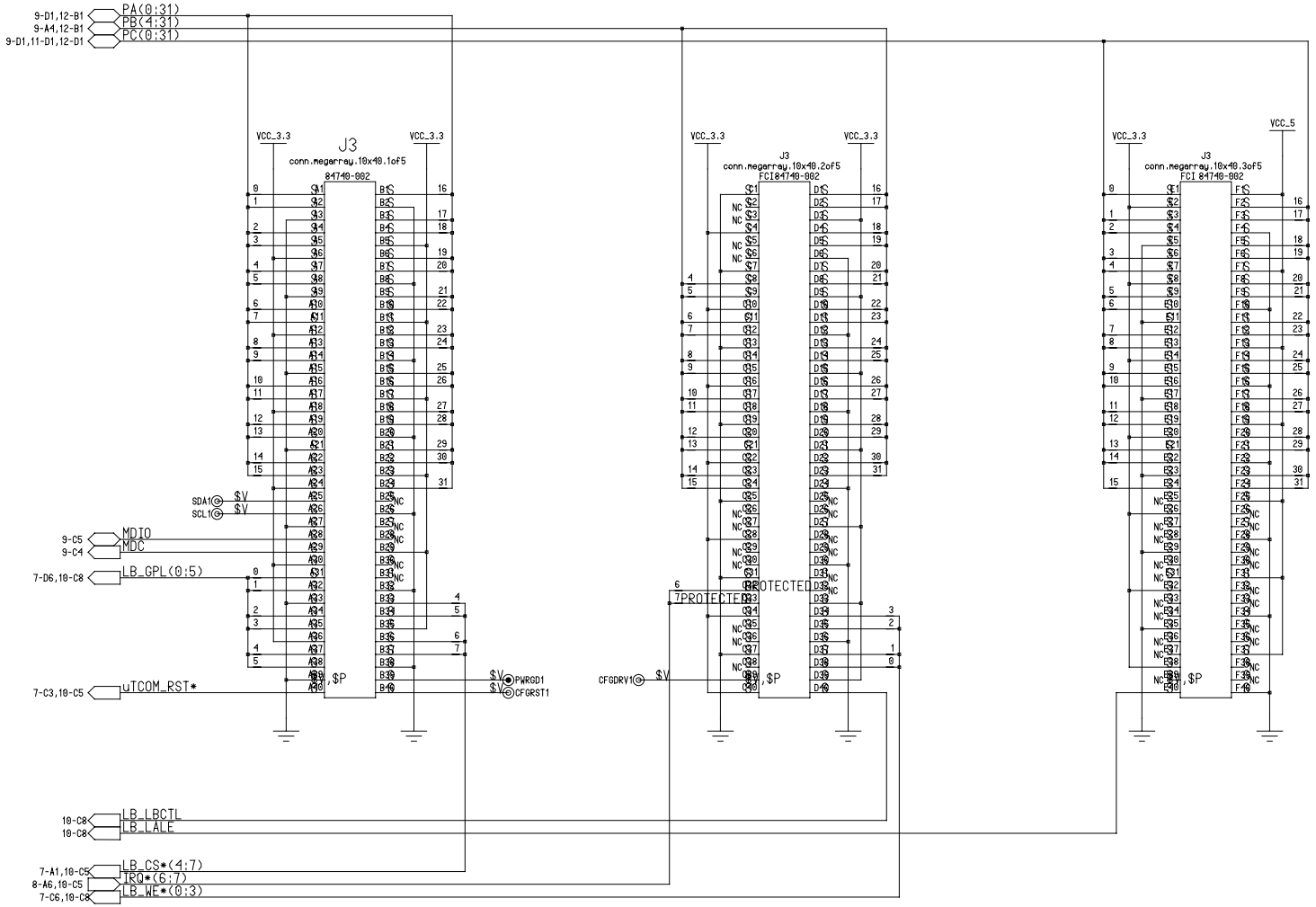


MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 1/28/2004 Time Changed: 2:15:53 pm	Title: Block Diagram	Page: 03

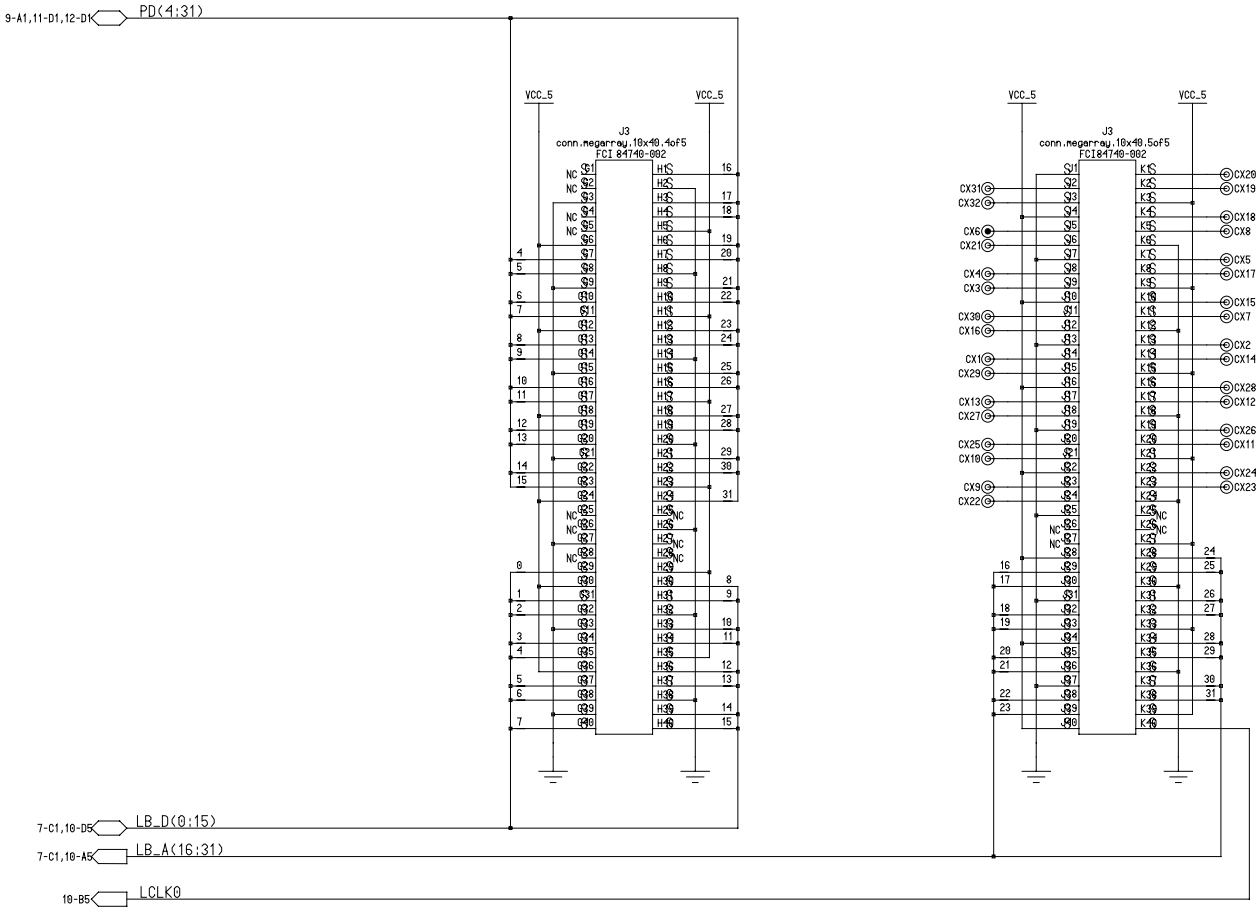




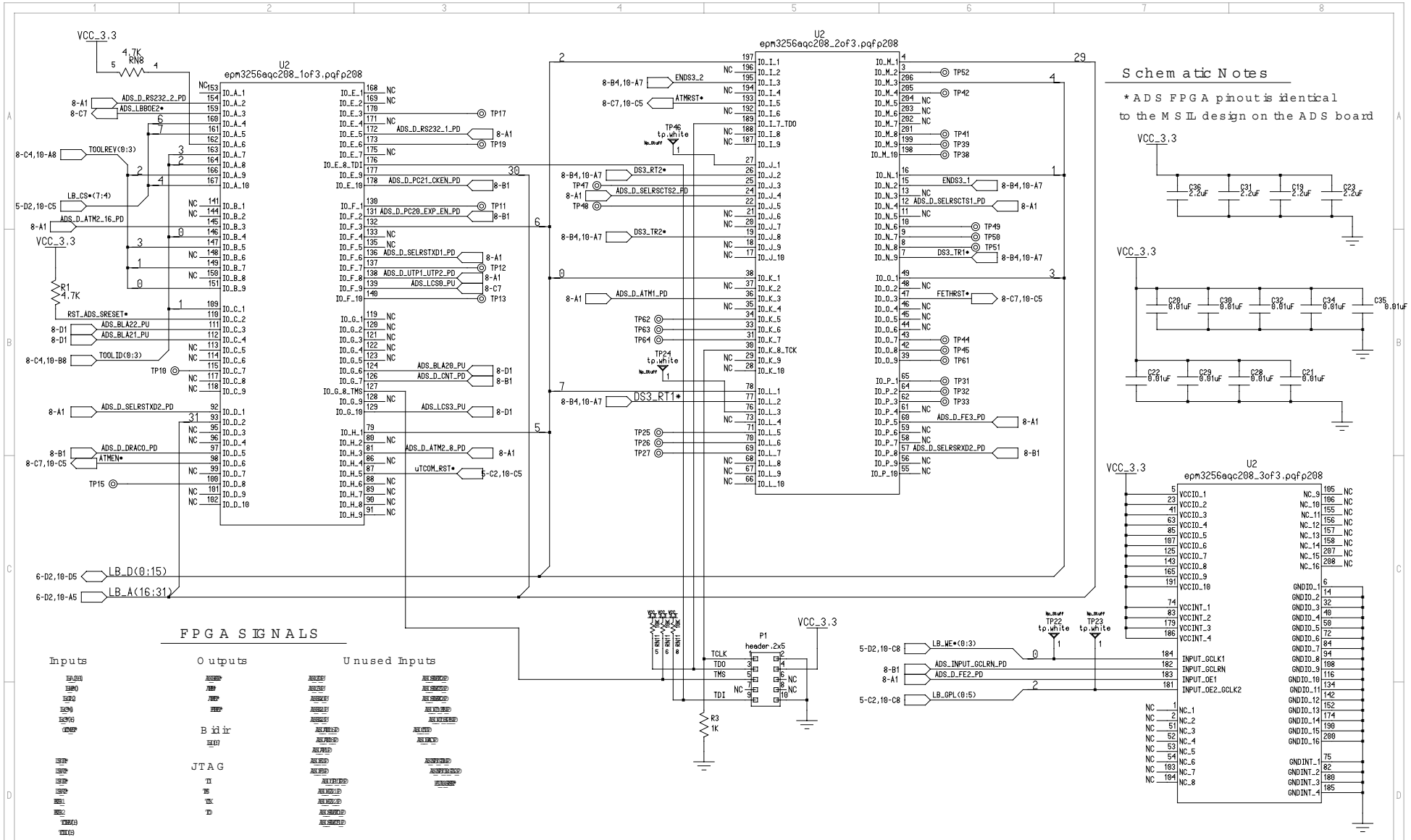
MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 6:22:57 pm	Title: Placement and PCB Stackup Page: 04



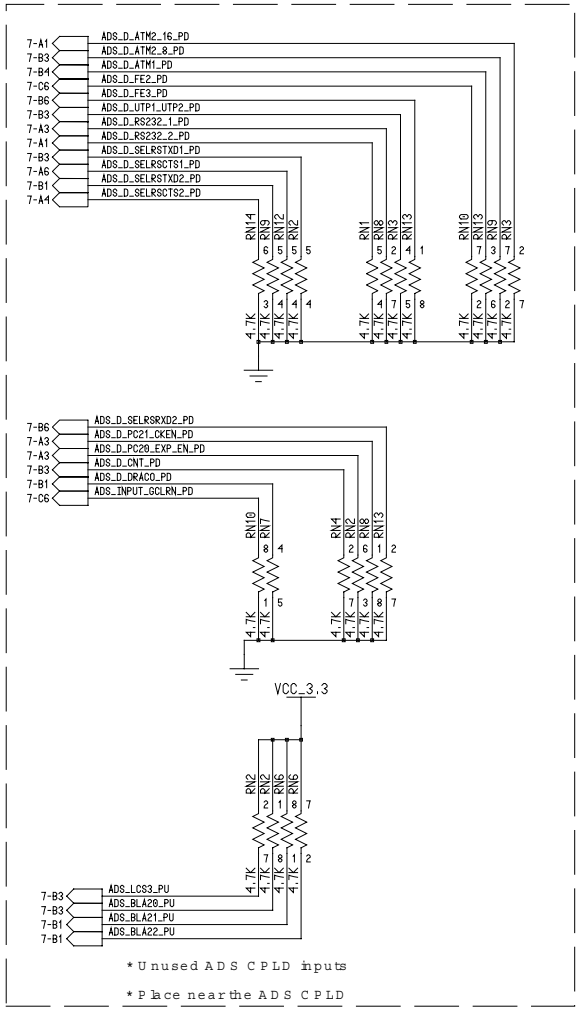
MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 2:40:22 pm	Title: Carrier-to-uTCOM Connector	Page: 05

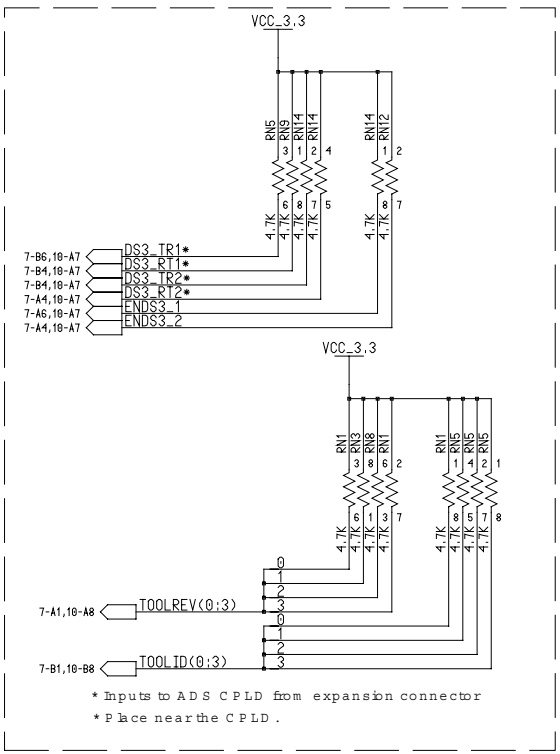


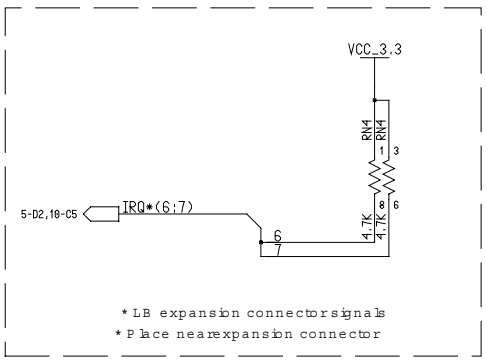
MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 2:46:19 pm	Title: Carrier-to-uTCOM Connector	Page: 06

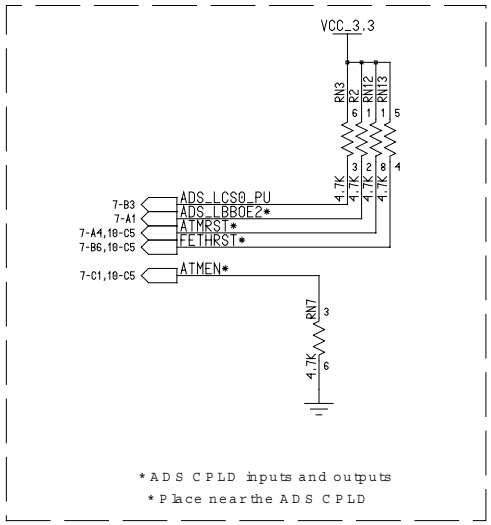


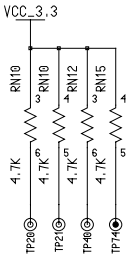
MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 5:52:37 pm	Title: ADS Local Bus FPGA	Page: 07

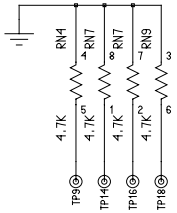




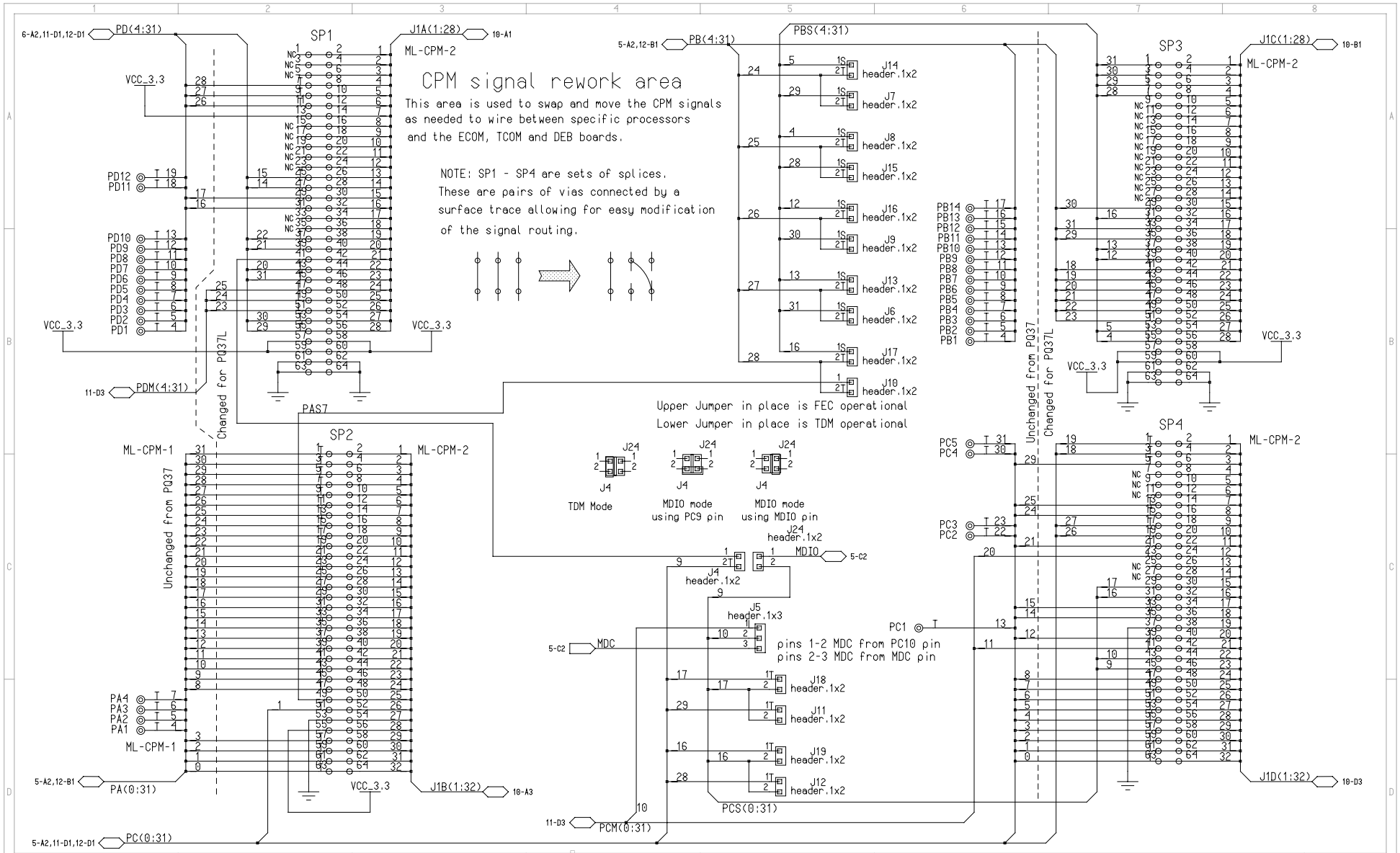




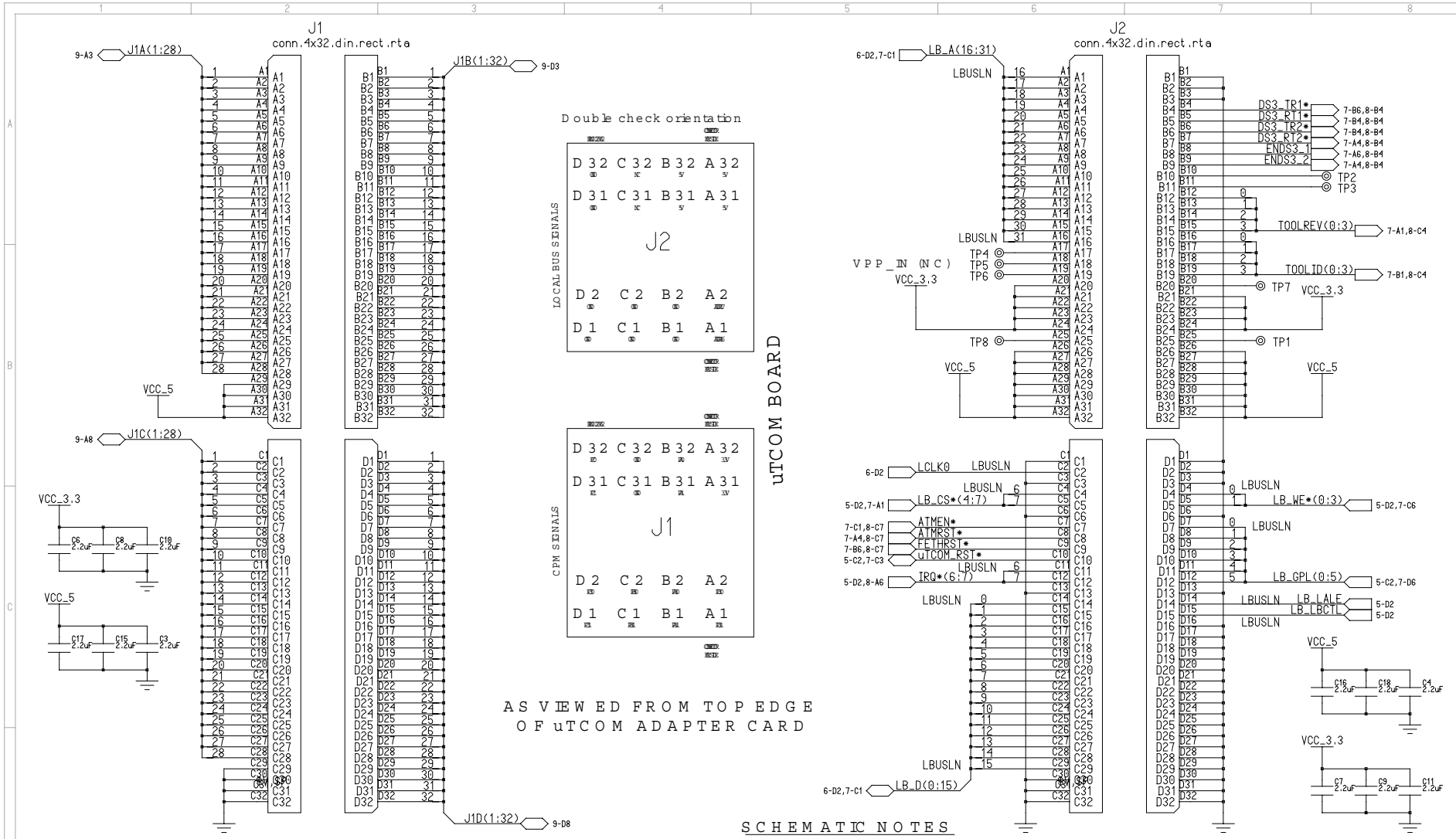




MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 2:53:45 pm	Title: Expansion Connector and CPLD Termination	Page: 08



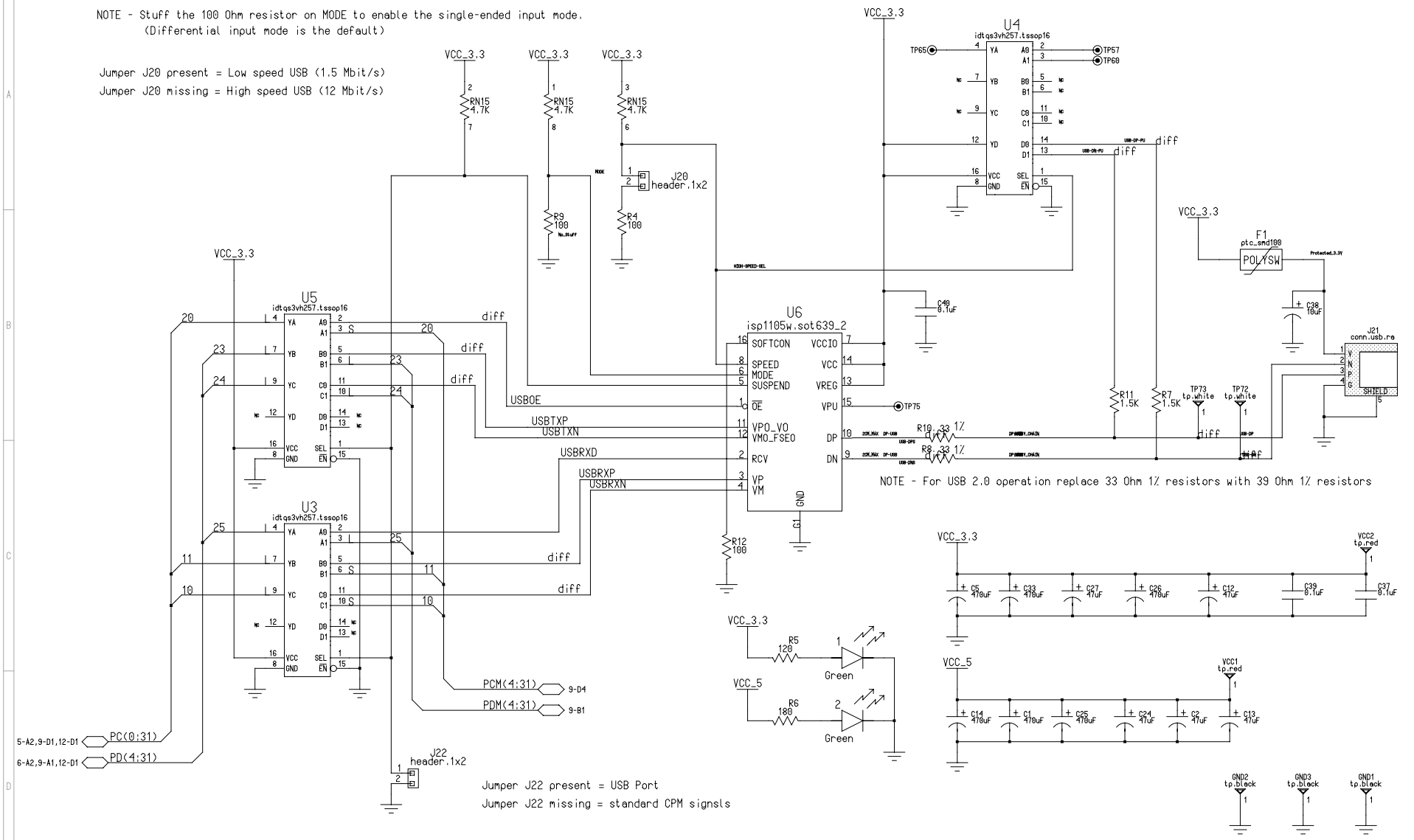
MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 2:58:37 pm	Title: CPM Signal Swap Area	Page: 09



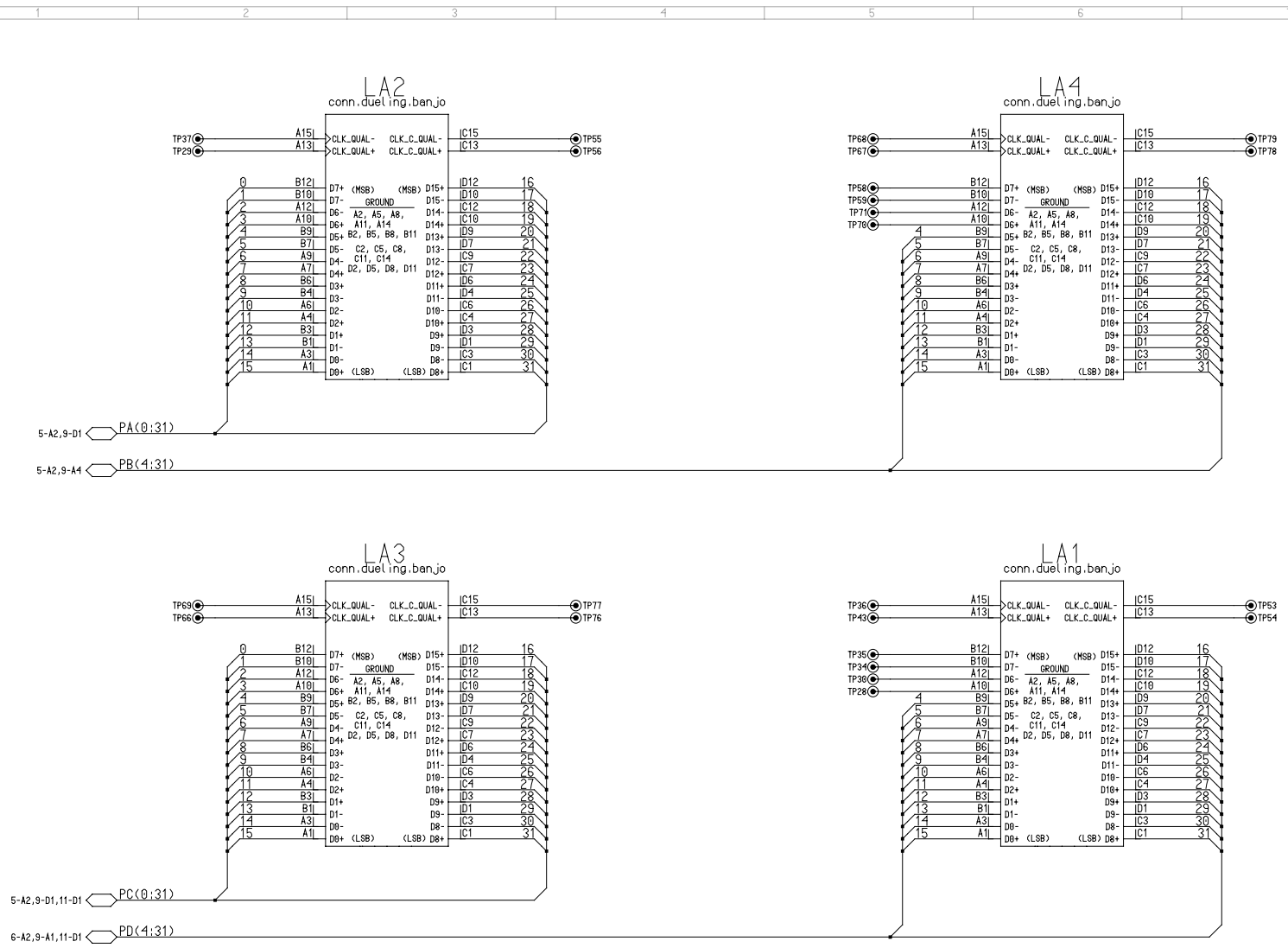
SCHEMATIC NOTES

1. IRQ6+7 must not be actively driven because of open drain outputs on the expansion card
2. VPP_IN was a 12V power input to supply the ADS board for flash programming

MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 1/29/2004 Time Changed: 11:49:00 am	Title: TCOM Connectors	Page: 10



MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 3:08:10 pm	Title: USB Interface	Page: 11



MOTOROLA	MOTOROLA INC. 7700 W. Parmer Ln Austin, Texas 78729	Project: CDS_uTCOM Revision: 1.0	Engineer: Mark S. Harris	Date Changed: 2/18/2004 Time Changed: 3:10:18 pm	Title: Visibility	Page: 12

Appendix K
CDS Arcadia BOM

This appendix provides Arcadia X3 BOM for Rev. 3.1.

Board Station BOM file
date : June 30, 2005; 15:09:37
Variant : No_Stuff

Updated on 08/19/05
Arcadia Rev X3.1

ITEM_NO	COMPANY PART NO.	GEOMETRY	COUNT	DESCRIPTION	REFERENCE
1		PCB_arcadia	1		
2	0603YC104JAT2A	cc0603	12	cap, 0.1uF, AVX, 5%	C11 C12 C14 C15 C18 C19 C20 C21 C22 C23 C30 C31
3	102972-2	header_1x2	10	header.1x2, AMP	J10 J11 J13 J14 J15 J16 J17 J18 J20 J23
4	102972-3	header_1x3	4	header.1x3, AMP	J21 J25 J27 J28
5	103309-7	header_2x17_shrouded	1	header.2x17, AMP	J19
6	103309-8	header_2x20_shrouded	2	header.vertical.shrouded.2x20, AMP	J22 J26
7	120521-1	recp2x32_amp_fh	3	conn.2x32.ieee1386, AMP	J6 J7 J8
8	120591-1	conn_battery	1	conn.battery, Keystone	J24
9	145154-4	conamp_145154_4	2	pciconn_5V_32bit_block, AMP	SLOT6 SLOT7
10	145165-1	conamp_univ_14516x	4	pcix_conn_univ_64bit_block, AMP	SLOT2 SLOT3 SLOT4 SLOT5
11	1469002-1	conn_hmzd_4x10	2	conn.amp.HM-Zd.40pr.plug.vert, Tyco	P3 P4
12	218-8LPST	sw_som16	3	sw.8spst.cts, CTS	SW1 SW2 SW3
13	223955-2	conamp_223955-2	4	conn.pwr.3pos.vert, AMP	P5 P6 P7 P8
14	223985-1	guide_pin	4	guide_pin.keyed, AMP	P1 P2 P9 P10
15	293D106X9016C2T	cct6032	5	cap_tant, 10uF, SPRAGUE, 10%	C261 C266 C275 C298 C302
16	293D226X9016C2T	cct6032	7	cap_tant, 22uF, SPRAGUE, 10%	C89 C154 C155 C216 C231 C276 C287
17	293D476X9016D2T	cct7343	2	cap_tant, 47uF, SPRAGUE, 10%	C291 C296
18	39-29-3206	atxpwr_2x10_vert	1	atxpwr_2x10vert_nopeg, Molex	J12
19	39-29-9042	conn_atx12v_2x2	1	atxpwr_12v_2x2vert, Molex	J9
20	440173-3	conn_dual_stacked_din	1	conn.din6.dual.stacked.ra, AMP	J3
21	597-5312-40X	led_0603	17	led, Dialight	D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17
22	74AHCT74DB	so14	1	74ahct74db.sso14, TI	U30
23	74LVT244APW	tssop20	1	74lvt244.tssop20, Phillips	U32
24	APA150-FG256	fbga256	1	apa150.1of2.fbga256, ACTEL	U14
25	BAS16LT1	sot23	4	bas16lt1.sot23, MOT	CR4 CR5 CR6 CR7
26	DEM9PL	conn_db9_plg_ra	2	conn.db9.plug.rta, ITT Cannon	J1 J2
27	ECE-V1CA331P	lytic_case_g	1	cap_lytic, 330uF, Panasonic, 20%	C210
28	ECPSM310T1_32_768KTR	sm_xtal_4p	1	smdxtal_32kHz, Ecliptek	Y5
29	EH2645TS-133.000M	osc_smd_5x7mm	1	osc.3_3v.smd, 133.33MHz, Ecliptek	U11

30	EMK107F224ZA	cc0603	8	cap, .22uF, TAIYO_YUDEN, +80-20%	C2 C3 C4 C5 C107 C111 C218 C224
31	EXCCL4532U1	induct_4532	19	exccl4532.smd, PANASONIC	F1 F2 F4 FB1 FB2 FB3 FB4 FB5 FB6 FB7 FB8 FB9 FB10 FB11 FB12 FB13 FB14 FB15 FB16
32	FPX250F-20	crystal_4pin_smd	1	crystal_4pin.smd, 25MHZ, FOX	Y1
33	FTSH-113-01-L-DV-K	conn_2x13_050_sma	1	conn.2x13, Samtec	J5
34	GRM39X7R104K050AD	cc0603	1	cap, 0.1uF, muRATA, 10%	C300
35	GSP-B-S2-GG-9100	rj45led_usbdual_over_ra	1	conn.rj45led_over_dualusb.ra, KYCON	J4
36	HC49SD33.333	crystal_2pin_smd	1	crystal.2pin.smd, Fox	Y3
37	HF30ACB453215-T	induct_4532	2	ferrite, TDK	F5 F6
38	IS24C02-3G	so8	2	is24c02-3g.so8, ISSI	U26 U27
39	LM393M	so8	1	lm393m.so8, NATIONAL	U13
40	LMK107F105ZA	cc0603	1	cap, 1.0uF, TAIYO_YUDEN, +80-20%	C272
41	LT1117CST-3.3	sot223	1	lt1117cst_3.3.sot223, Linear Tech.	U31
42	LT1331CG	ssop28	2	lt1331cg.ssop28, Linear	U1 U2
43	MBRS360T3	smc_403	3	mbrs360t3.smb, ONSEMI	CR1 CR2 CR3
44	MCCA104K0NRT	cc0402	216	cap, 0.1uF, SMEC, 10%	C8 C26 C29 C32 C33 C35 C36 C40 C42 C43 C44 C45 C46 C49 C50 C51 C52 C53 C54 C55 C56 C57 C60 C61 C62 C63 C64 C65 C66 C69 C70 C71 C72 C75 C76 C78 C79 C80 C81 C82 C83 C84 C85 C86 C87 C88 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 C101 C102 C103 C104 C105 C108 C109 C110 C114 C116 C117 C118 C119 C120 C121 C122 C123 C124 C125 C126 C127 C128 C129 C130 C131 C132 C133 C134 C135 C136 C139 C142 C143 C144 C145 C146 C147 C148 C149

					C150 C151 C152 C153 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C170 C171 C172 C173 C174 C175 C176 C177 C178 C179 C180 C181 C183 C185 C187 C189 C190 C192 C193 C194 C195 C196 C197 C198 C199 C200 C201 C202 C203 C204 C205 C206 C207 C208 C209 C211 C212 C213 C214 C215 C217 C219 C220 C221 C222 C223 C225 C226 C227 C228 C229 C230 C232 C233 C234 C235 C236 C237 C238 C239 C240 C241 C242 C243 C244 C245 C246 C247 C248 C251 C252 C253 C254 C255 C256 C257 C258 C259 C260 C262 C263 C264 C267 C268 C269 C270 C273 C274 C277 C279 C280 C281 C282 C284 C285 C286 C290 C293 C294 C295 C301 C303
45	MCCA180K0NRT	cc0402	2	cap, 18pF, SMEC, 10%	C24 C25
46	MCCA270K0NRT	cc0402	7	cap, 27pF, SMEC, 10%	C1 C13 C16 C17 C27 C28 C34
47	MCCA470K0NRT	cc0402	5	cap, 47pF, SMEC, 10%	C6 C7 C9 C10 C278
48	MCCE100JONRT	cc0402	2	cap, 10pF, muRATA, 5%	C265 C271
49	MCR03-EZH-F-49R9	rc0603	4	res, 49.9, Rohm, 1%	R10 R11 R12 R13

50	MIC2526-2	so8	1	mic2526_2.so8, MICREL	U3
51	MIC29152BU	to263_5p	1	mic29152bu.to263_5, MICREL	U20
52	MMBT3904	sot23	1	mmbt3904_npn.sot23, Motorola	Q1
53	MNR14-EOAB-J-102	rnet1632	1	rnet, 1K, Rohm, 5%	RN17
54	MNR14-EOAB-J-330	rnet1632	12	rnet, 33, Rohm, 5%	RN25 RN26 RN27 RN28 RN29 RN30 RN31 RN32 RN33 RN34 RN35 RN36
55	MPC9109FA	lqfp32	1	mpc9109fa.lqfp32, Freescale	U24
56	MPC9855VF	bga_10x10	1	mpc9855.bga_10x10, Freescale	U25
57	NOT_A_COMPONENT	tp_pth	9	test.pth, None	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9
58	RC73A2Z1000FT	rc0402	1	res, 100, SMEC, 1%	R275
59	RC73A2Z1002FT	rc0402	2	res, 10.0K, SMEC, 1%	R41 R45
60	RC73L2Z000JT	rc0402	7	res, 0, SMEC, 5%	R34 R40 R198 R201 R244 R245 R147
61	RC73L2Z050JT	rc0402	1	res, 5, SMEC, 5%	R33
62	RC73L2Z100JT	rc0402	1	res, 10, SMEC, 5%	R58
63	RC73L2Z101JT	rc0402	4	res, 100, SMEC, 5%	R18 R19 R291 R294
64	RC73L2Z102JT	rc0402	22	res, 1K, SMEC, 5%	R15 R16 R17 R27 R35 R56 R88 R110 R125 R126 R145 R204 R220 R229 R238 R243 R254 R261 R265 R273 R281 R285
65	RC73L2Z103JT	rc0402	13	res, 10K, SMEC, 5%	R28 R29 R30 R197 R202 R203 R221 R224 R228 R235 R264 R282 R283
66	RC73L2Z471JT	rc0402	1	res, 470, SMEC, 5%	R66
67	RC73L2Z153JT	rc0402	4	res, 15K, SMEC, 5%	R2 R4 R6 R9
68	RC73L2Z220JT	rc0402	4	res, 22, SMEC, 5%	R32 R189 R196 R280
69	RC73L2Z221JT	rc0402	18	res, 220, SMEC, 5%	R5 R54 R185 R186 R246 R249 R250 R251 R255 R256 R257 R258 R259 R260 R262 R270 R271 R272
70	RC73L2Z222JT	rc0402	2	res, 2.2K, SMEC, 5%	R31 R55
71	RC73L2Z270JT	rc0402	4	res, 27, SMEC, 5%	R1 R3 R7 R8
72	RC73L2Z272JT	rc0402	2	res, 2.7K, SMEC, 5%	R22 R24
73	RC73L2Z330JT	rc0402	33	res, 33, SMEC, 5%	R20 R26 R36 R37 R38 R39 R43 R148 R149 R150

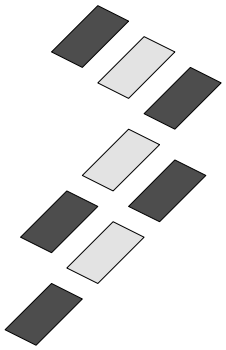
					R151 R152 R153 R156 R175 R176 R177 R179 R180 R182 R183 R190 R191 R192 R193 R194 R266 R267 R274 R286 R288 R292
74	RC73L2Z331JT	rc0402	5	res, 330, SMEC, 5%	R14 R205 R241 R242 R253
75	RC73L2Z332JT	rc0402	2	res, 3.3K, SMEC, 5%	R237 R278
76	RC73L2Z470JT	rc0402	1	res, 47, SMEC, 5%	R231
77	RC73L2Z471JT	rc0402	6	res, 470, SMEC, 5%	R69 R222 R269 R276 R287 R295
78	RC73L2Z472JT	rc0402	39	res, 4.7K, SMEC, 5%	R25 R100 R178 R181 R184 R195 R199 R200 R206 R207 R208 R209 R210 R211 R212 R213 R214 R215 R216 R217 R218 R219 R223 R225 R226 R227 R230 R232 R233 R234 R239 R240 R247 R252 R268 R279 R289 R290 R293
79	RC73L2Z562JT	rc0402	1	res, 5.6K, SMEC, 5%	R23
80	RC73L2Z563JT	rc0402	1	res, 56K, SMEC, 5%	R146
81	RC73L2Z682JT	rc0402	1	res, 6.8K, SMEC, 5%	R277
82	RC73L2Z750JT	rc0402	2	res, 75, SMEC, 5%	R263 R284
83	RC73L2Z822JT	rc0402	103	res, 8.2K, SMEC, 5%	R44 R48 R49 R50 R51 R52 R53 R57 R60 R61 R63 R64 R65 R67 R68 R70 R71 R72 R73 R74 R75 R76 R77 R78 R79 R80 R81 R82 R83 R84 R85 R86 R87 R89 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99 R101 R102 R103 R104 R105 R106 R107 R108 R109 R111 R112 R113

					R114 R115 R116 R117 R118 R119 R120 R121 R122 R123 R124 R127 R128 R129 R130 R131 R132 R133 R134 R135 R136 R137 R138 R139 R140 R141 R142 R143 R144 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 R167 R168 R169 R170 R171 R172 R173 R174
84	RK73H2AT1602F	rc0805	1	res, 16K, KOA, 1%	R236
85	RM73B1JT050JF	rc0603	4	res, 5, KOA, 5%	R21 R154 R187 R188
86	RM73B1JT100J	rc0603	2	res, 10, KOA, 5%	R46 R47
87	RM73B1JT150J	rc0603	1	res, 15, KOA, 5%	R155
88	RM73B2ETE-100J	rc1210	1	res, 10, KOA, 5%	R62
89	RNA4A8E102JT	rna4a	3	rnet8.bussed.rna4a, 1K, AVX, 5%	RN5 RN7 RN9
90	RNA4A8E103JT	rna4a	2	rnpullup_3.3v.rna4a, 10K, AVX, 5%	RN3 RN10
91	RNA4A8E472JT	rna4a	14	rnpullup_3.3v.rna4a, 4.7K, AVX, 5%	RN2 RN11 RN12 RN13 RN14 RN15 RN16 RN18 RN19 RN20 RN21 RN22 RN23 RN24
92	RNA4A8E472JT	rna4a	3	rnet8.bussed.rna4a, 4.7K, AVX, 5%	RN4 RN6 RN8
93	RNA4A8E472JT	rna4a	1	rnpullup_vcc5.rna4a, 4.7K, AVX, 5%	RN1
94	RTL8139D	pqfp100	1	rtl8139d.pqfp100, REALTEK	U7
95	SG615P-14.318	osc_smd-sg8002ja	1	osc.smd-sg8002ja, 14.318MHz, EPSON	Y4
96	SG615P-48.000	osc_smd-sg8002ja	1	osc.smd-sg8002ja, 48.000MHz, EPSON	Y2
97	SMD100	sm_case_c	1	ptc_smd100, RAYCHEM	F3
98	SN74CBTD16211CDGGR	tssop56	3	74cbt16211dggr.ssop56, TI	U16 U17 U18
99	SN74CBTLV1G125DBVR	sop5	6	74cbtlv1g125dbv.so5, TI	U5 U8 U9 U10 U19 U23
100	SN74LVC1G125DCKR	sc70	5	74lvc1g125.sc70, TI	U12 U15 U21 U33 U34
101	T510X337M010AS	cct_casee	6	cap_tant, 330uF, Kemet, 20%	C283 C288 C289 C292 C297 C299
102	TP-105-01-00	tp025	3	tp.black, Components Corporation	G1 G2 G3
103	TP12SH9ABE	sw_th_spdt	2	sw.1spdt, C&K	SW4 SW5
104	TSI310A-133CE	pbga304	1	tsi310.1of4.pci_p.pbga304, Tundra	U22
105	UWX1C470MCR	lytic_case250_smd	26	cap_lytic, 47uF, Nichicon, 20%	C37 C38 C39 C41 C47 C48 C58 C59

106	VT82C686B	pbga352	1	vt82c686b.1of3.pbga352, VIA	C67 C68 C73 C74 C77 C106 C112 C113 C115 C137 C138 C140 C141 C182 C184 C186 C188 C191 U29

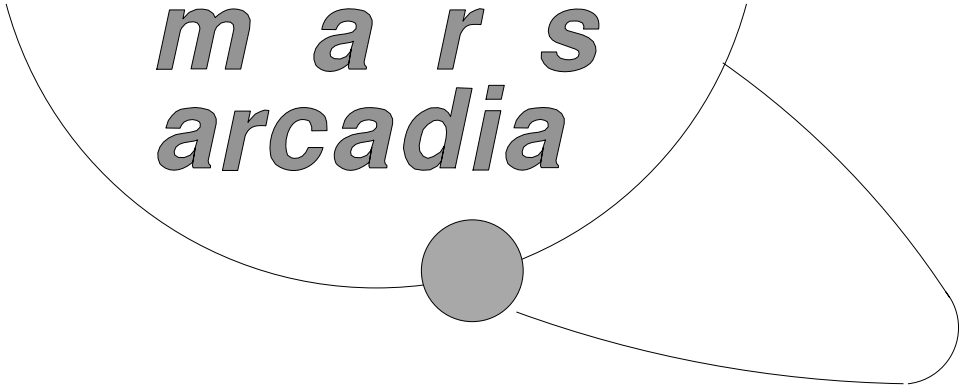
Appendix L
CDS Arcadia X3 Schematics

This appendix provides Arcadia X3 schematics for Rev. 3.1.



freescale™

semiconductor



freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Thursday, October 20, 2005 Time Changed: 2:49:23 pm	Title: Cover Story	Page: 01

Schematic Notes

1. Unless otherwise specified:
   All resistors are SMD0603, in ohms, 0.08W, +/-5%
   All capacitors are SMD0603, in microfarads (uF), +/-20%.
   All inductances are in microhenries (uH).
   All ferrites are Z=50 ohms at 100 MHz.
   All fuses are self-resetting polyswitch (PTC) devices.
   Board impedance is 55 +/- 5 ohms.

2. Integrated circuits have default connections to power and ground unless explicitly shown otherwise. Global power connections are:

   VCC_3.3 VCC_2.5
   VCC_5 GND

3. Part numbers used are for reference only; compatible parts may be used; refer to the bill of materials.

4. Motorola and the Motorola logo are registered trademarks of Motorola. PowerPC is a trademark of IBM. Other trademarks are the respective property of their respective copyright holders. Under the sycamore trees. All rights reserved. No warranty is made, express or implied.

5. The sheet-to-sheet cross reference format is:
   Sheet "-" VertZoneLetter HorizZoneNumber

6. Components with the label "No_Stuff" are not to be installed by default; they are for test or manufacturing purposes only.

7. All buses follow big-endian bit numbering order (bit 0 is the most-significant bit), except where industry standards apply (i.e. PCI). Little-endian numbering is noted at the source component.

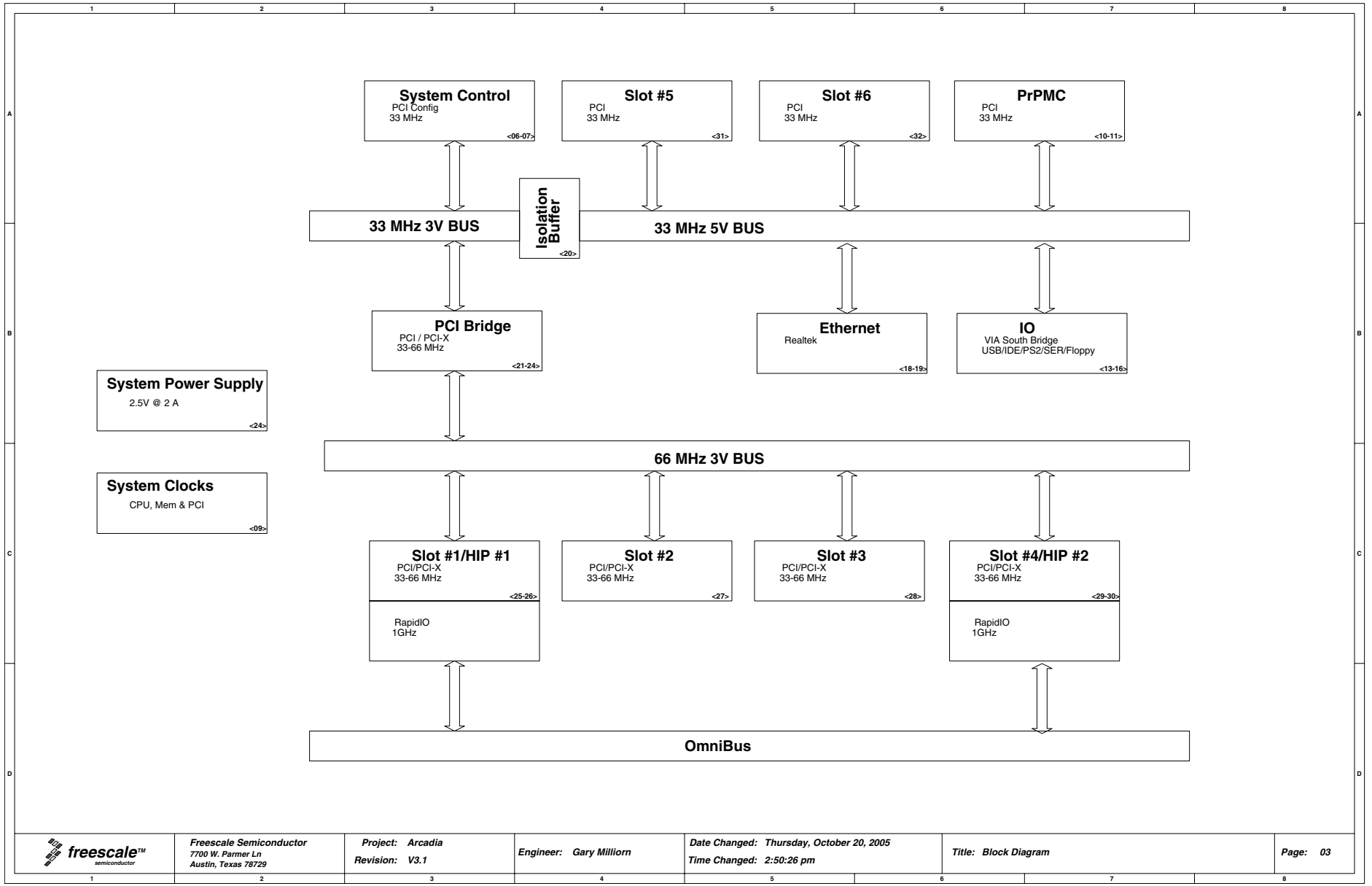
This schematic is provided for reference purposes only. All information is subject to change without notice. No warranty, expressed or applied, is made as to the accuracy of the information contained herein. Contact Freescale Sale/FAEs to obtain the latest information on this product.

arcadia

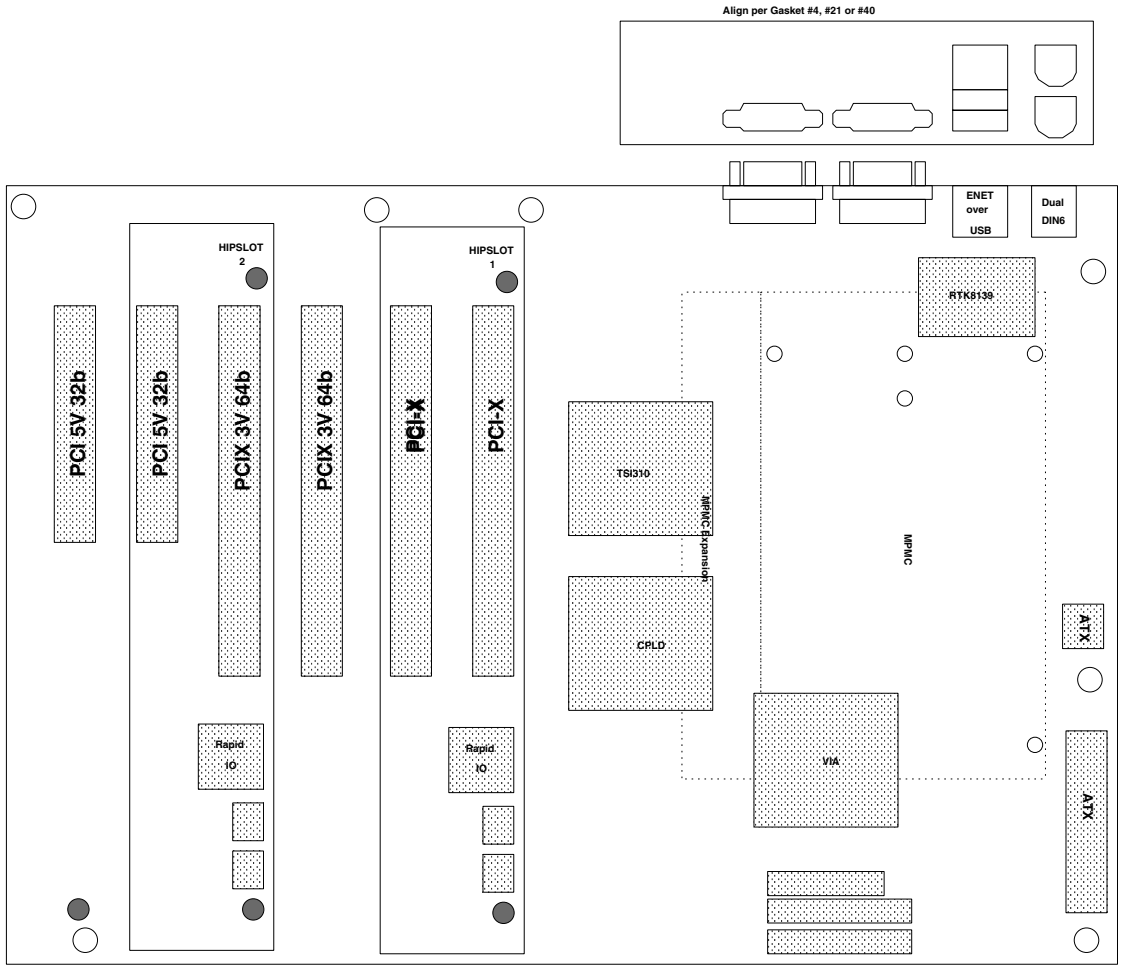
REV	DATE	CHANGES
X1	15APR02	Initial version
X2	30JUL02	Updates.
3.0	01DEC04	PCI bridge replaced.
V3.1	11OCT05	Updates

freescale semiconductor
Freescale Semiconductor
7700 W. Parmer Ln
Austin, Texas 78729

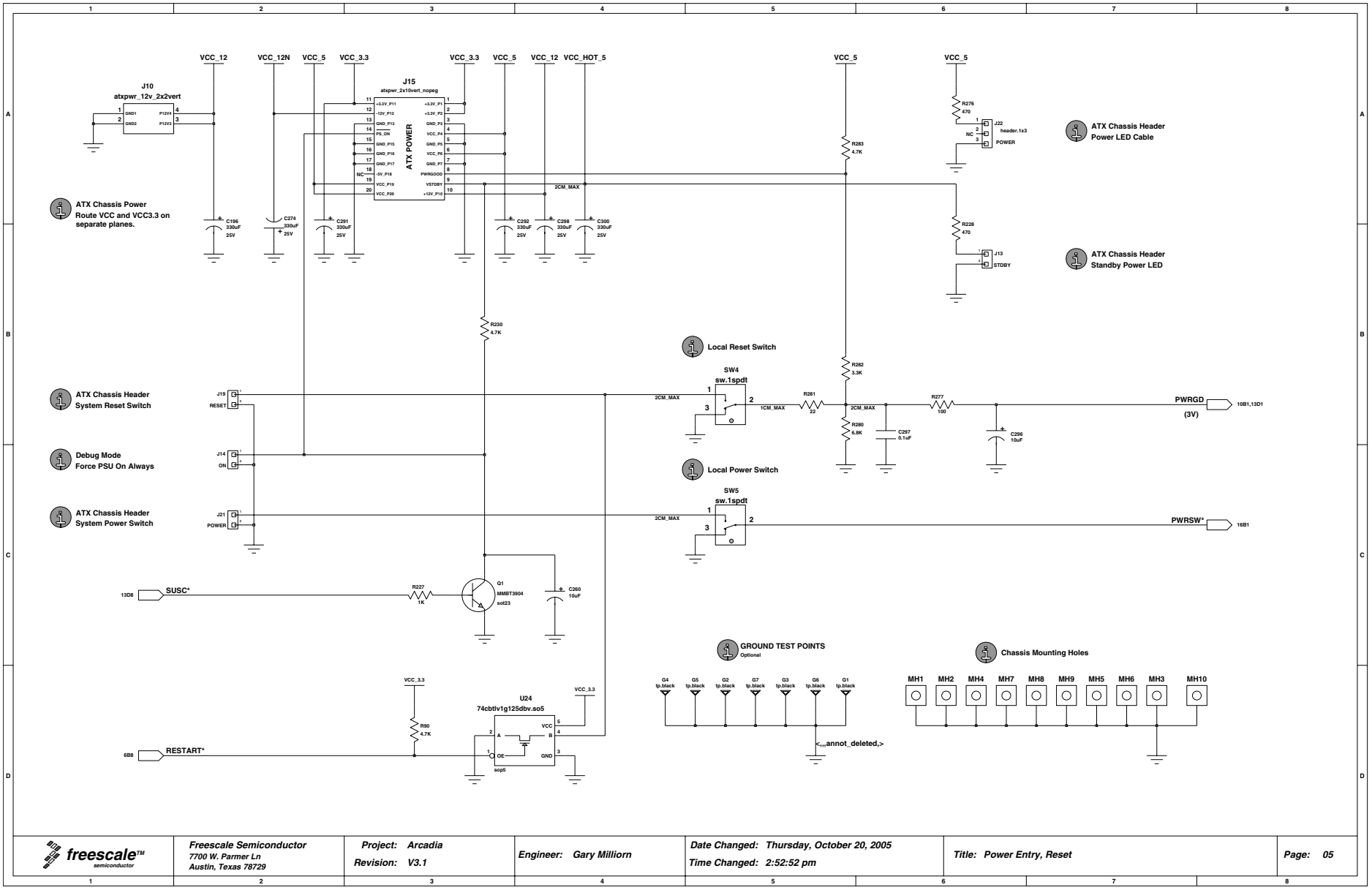
Project: Arcadia
Revision: V3.1
Engineer: Gary Milliorn
Date Changed: Thursday, October 20, 2005
Time Changed: 2:49:55 pm
Title: Information, Please
Page: 02



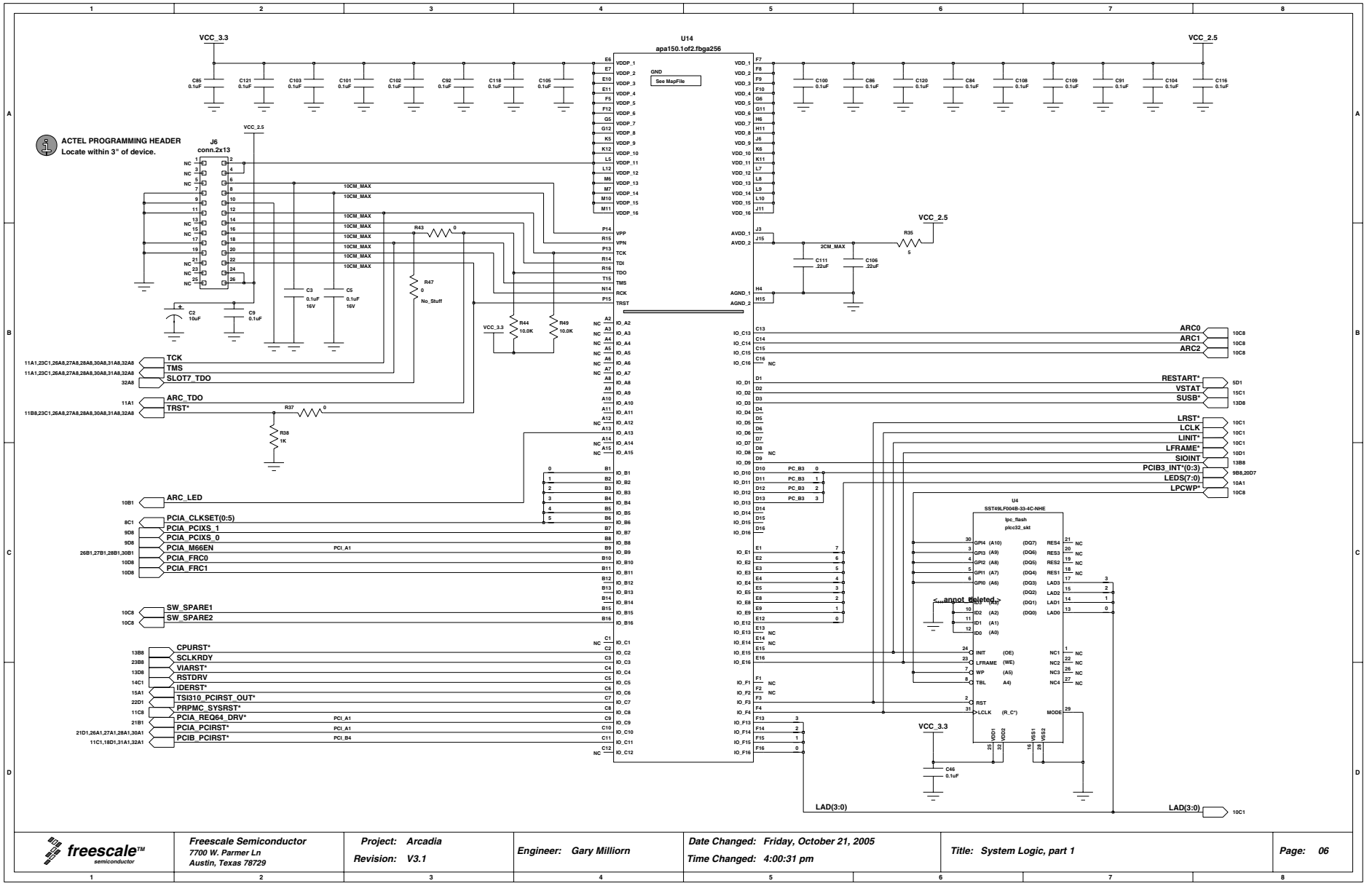
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Thursday, October 20, 2005 Time Changed: 2:50:26 pm	Title: Block Diagram	Page: 03



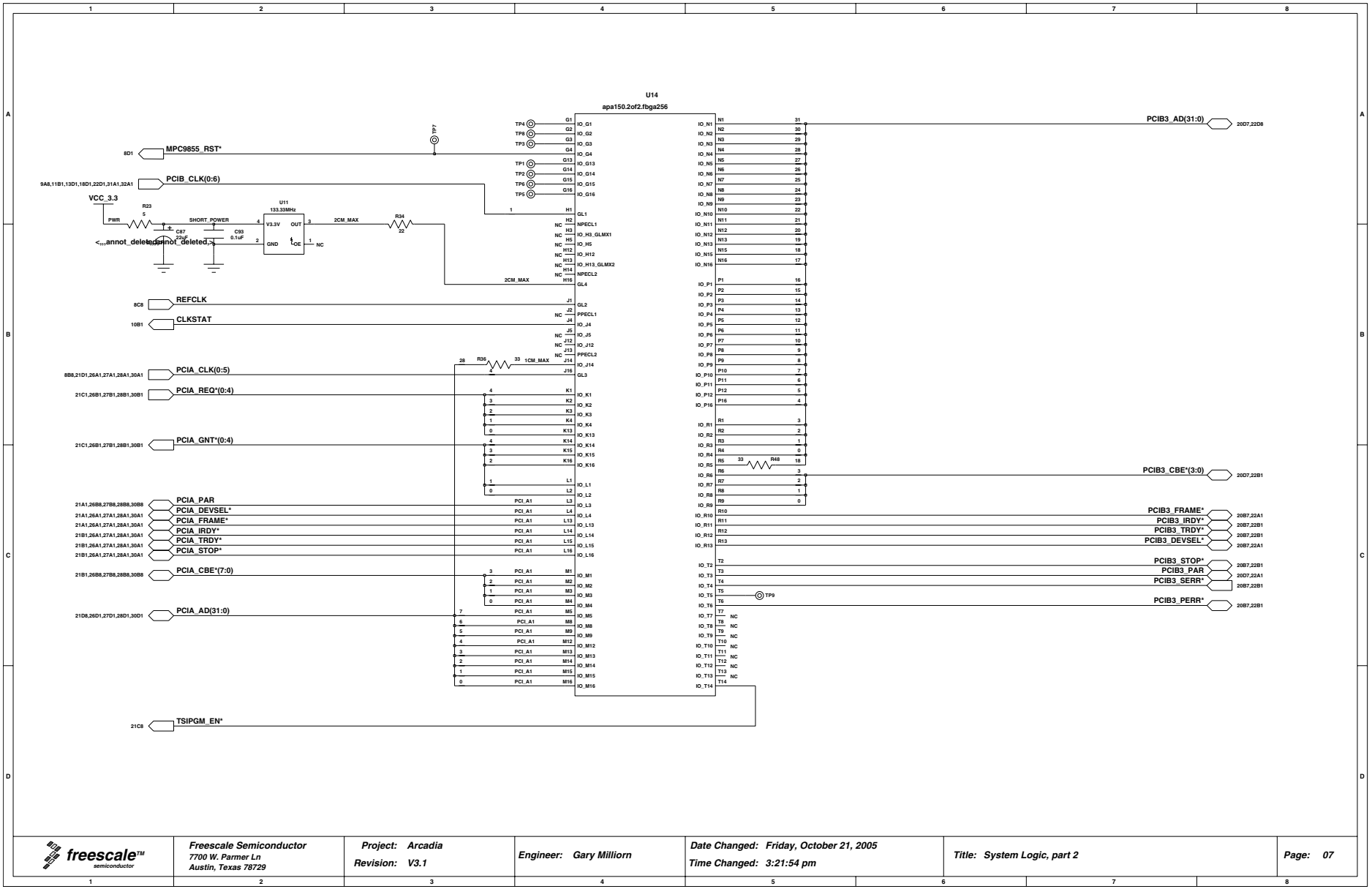
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Thursday, October 20, 2005 Time Changed: 2:52:01 pm	Title: Placement	Page: 04



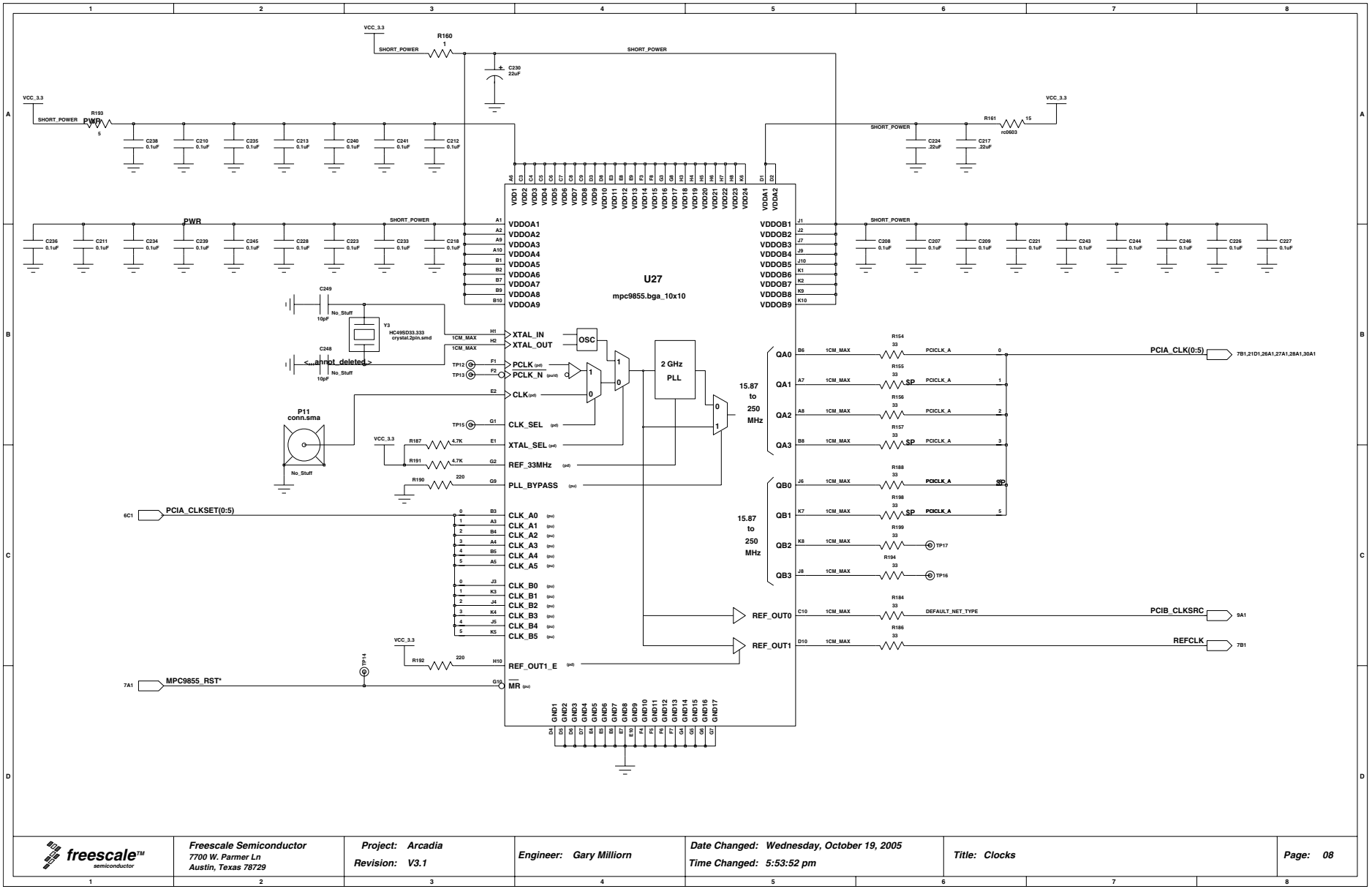
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Thursday, October 20, 2005 Time Changed: 2:52:52 pm	Title: Power Entry, Reset	Page: 05



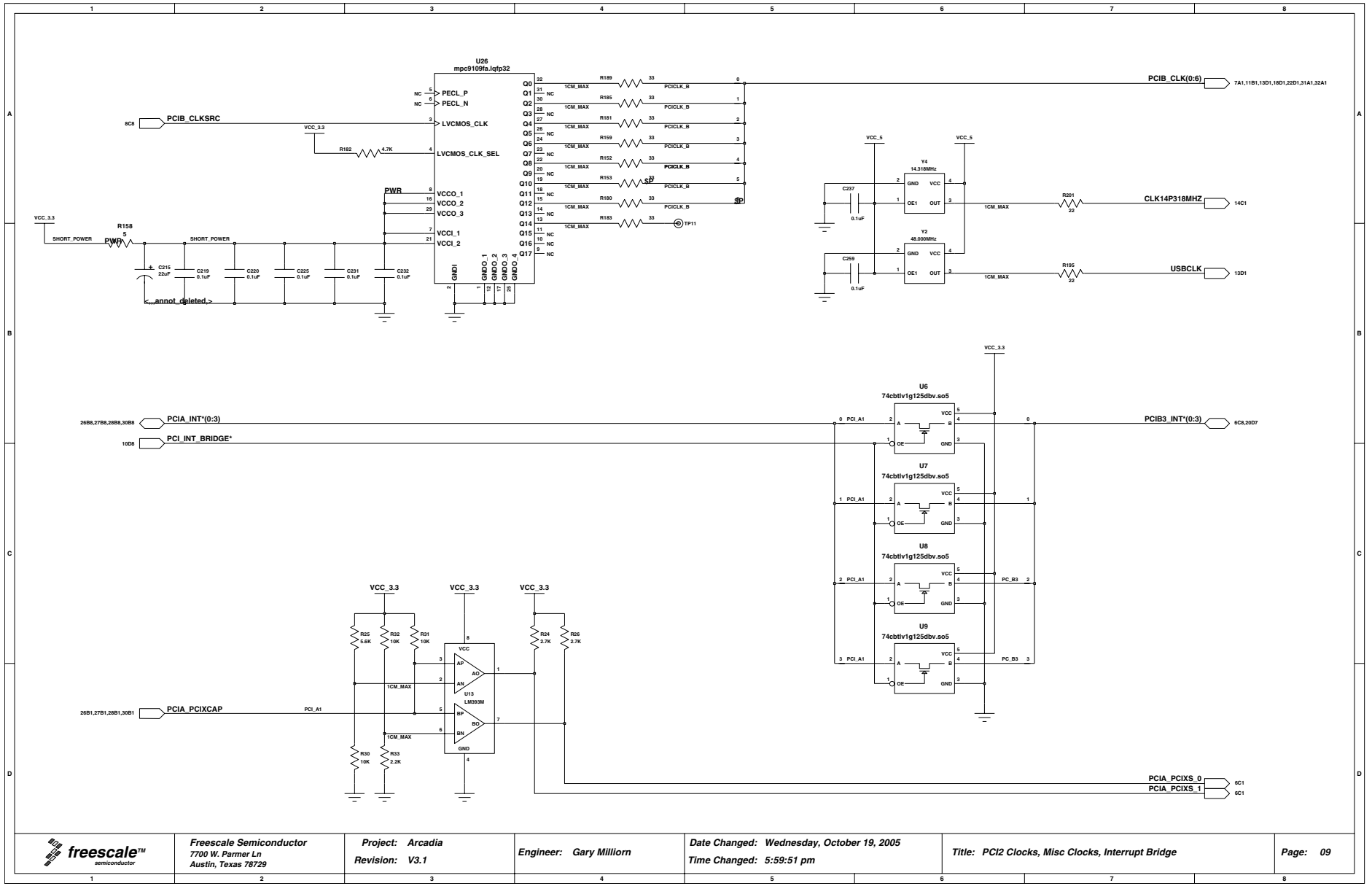
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Friday, October 21, 2005 Time Changed: 4:00:31 pm	Title: System Logic, part 1	Page: 06



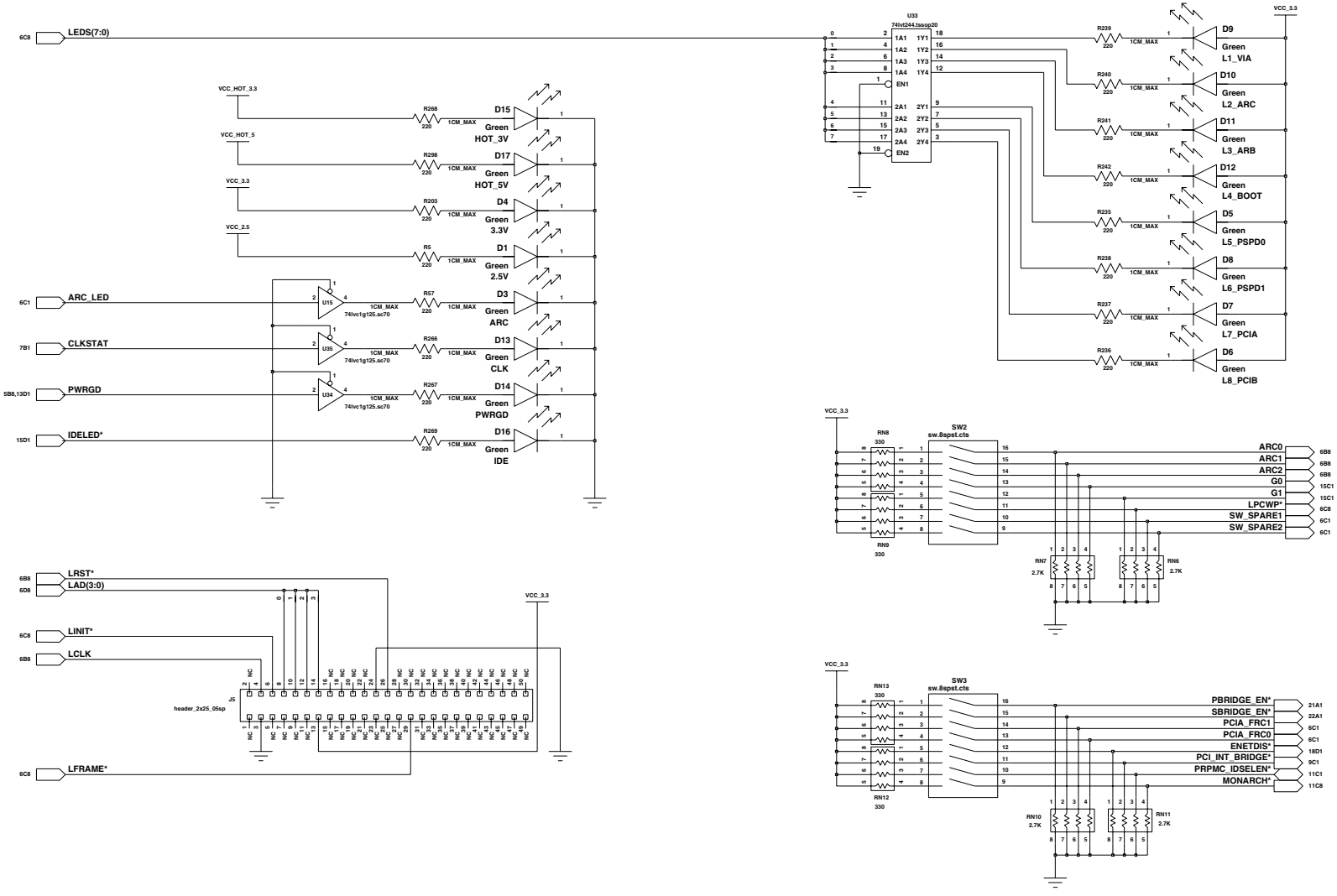
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Friday, October 21, 2005 Time Changed: 3:21:54 pm	Title: System Logic, part 2	Page: 07



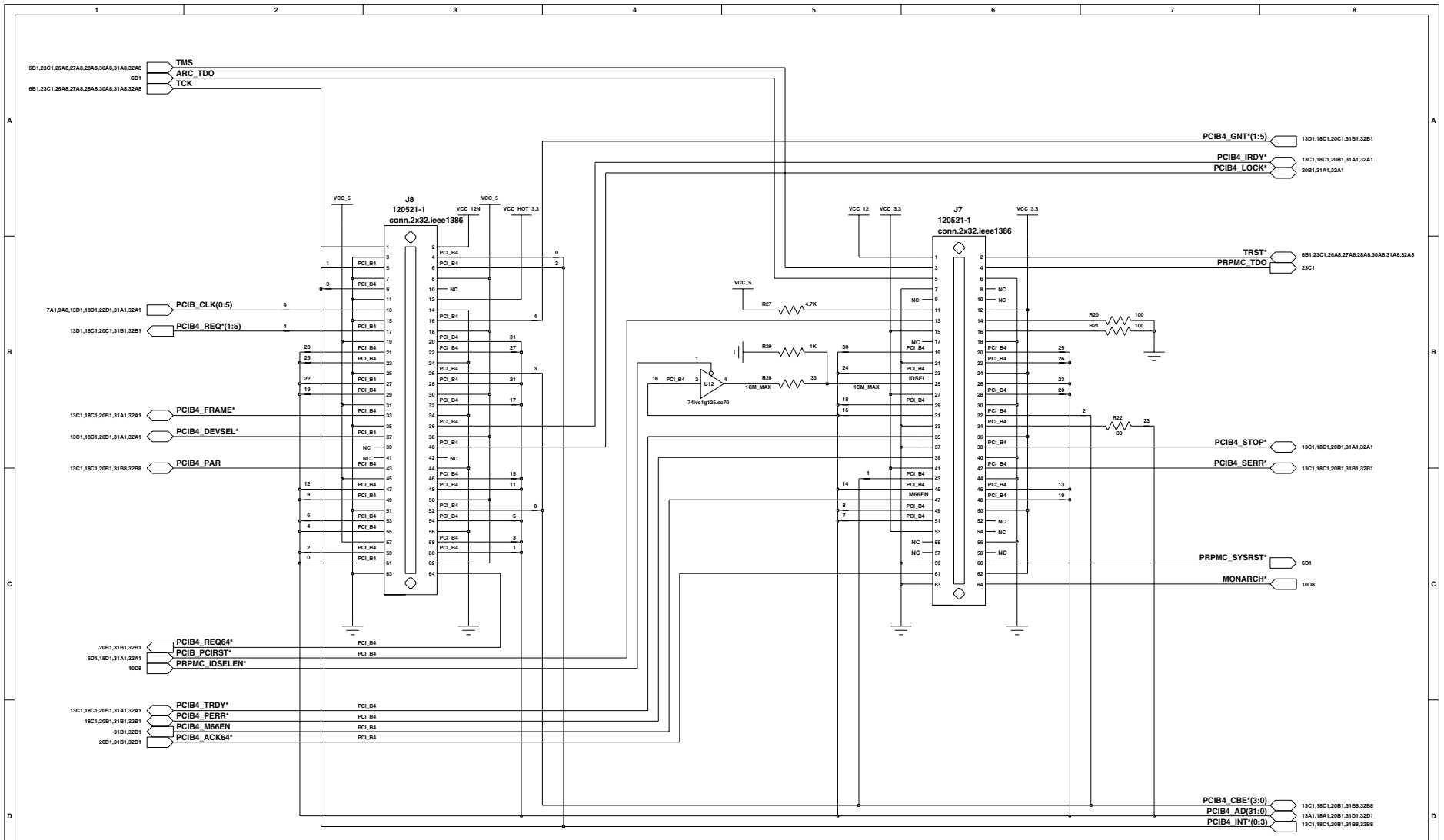
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 5:53:52 pm	Title: Clocks	Page: 08



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 5:59:51 pm	Title: PCI2 Clocks, Misc Clocks, Interrupt Bridge	Page: 09

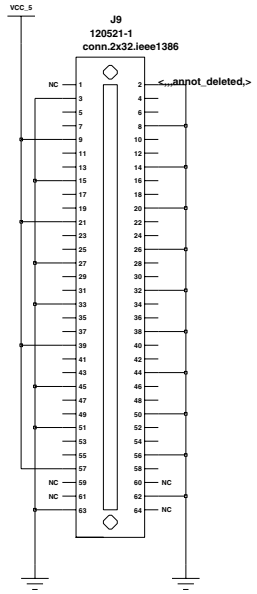


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Thursday, October 20, 2005 Time Changed: 2:39:10 pm	Title: Options, LEDs	Page: 10

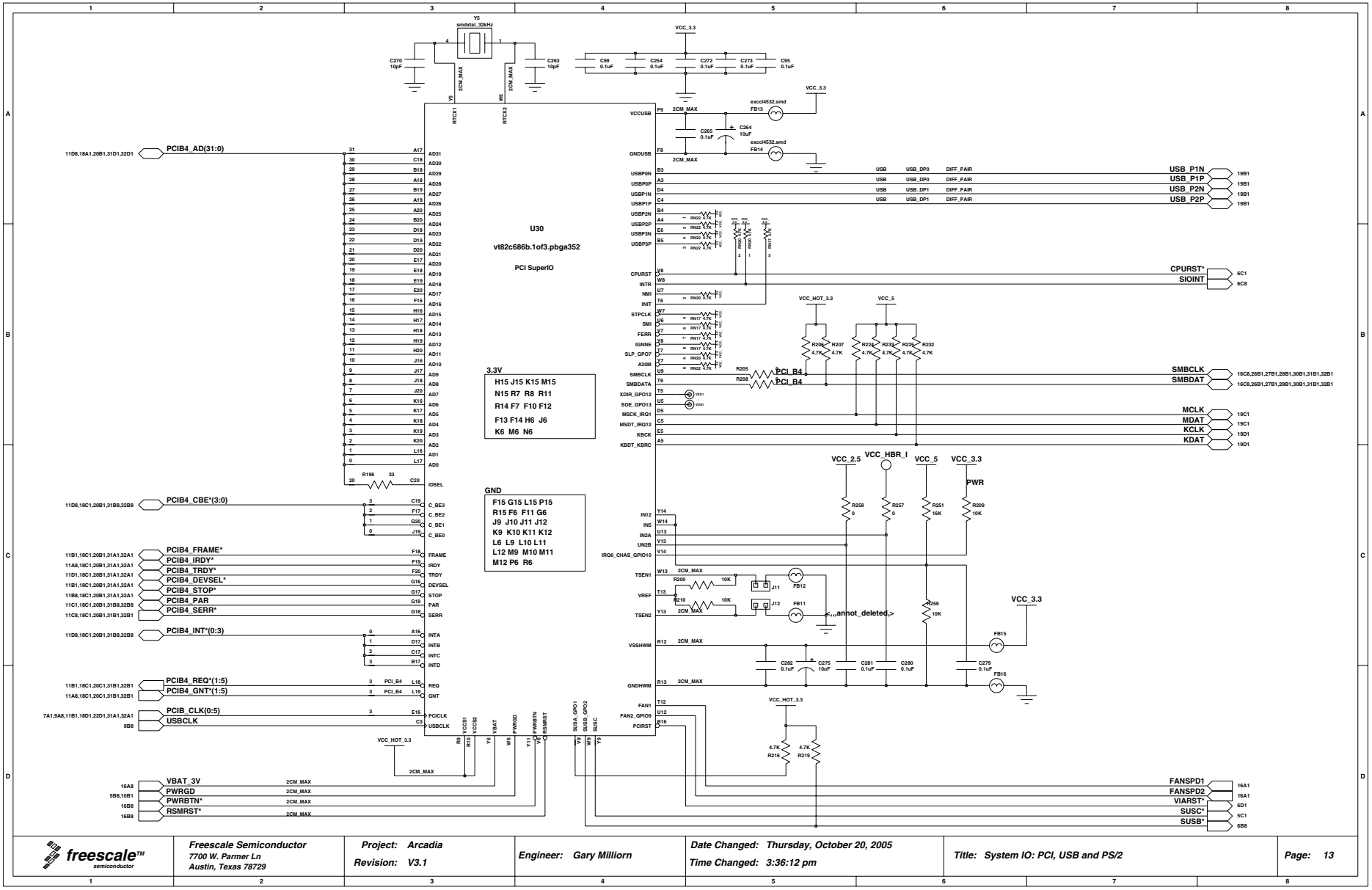


freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Thursday, October 20, 2005 Time Changed: 3:35:30 pm	Title: PrPMC Connectors	Page: 11

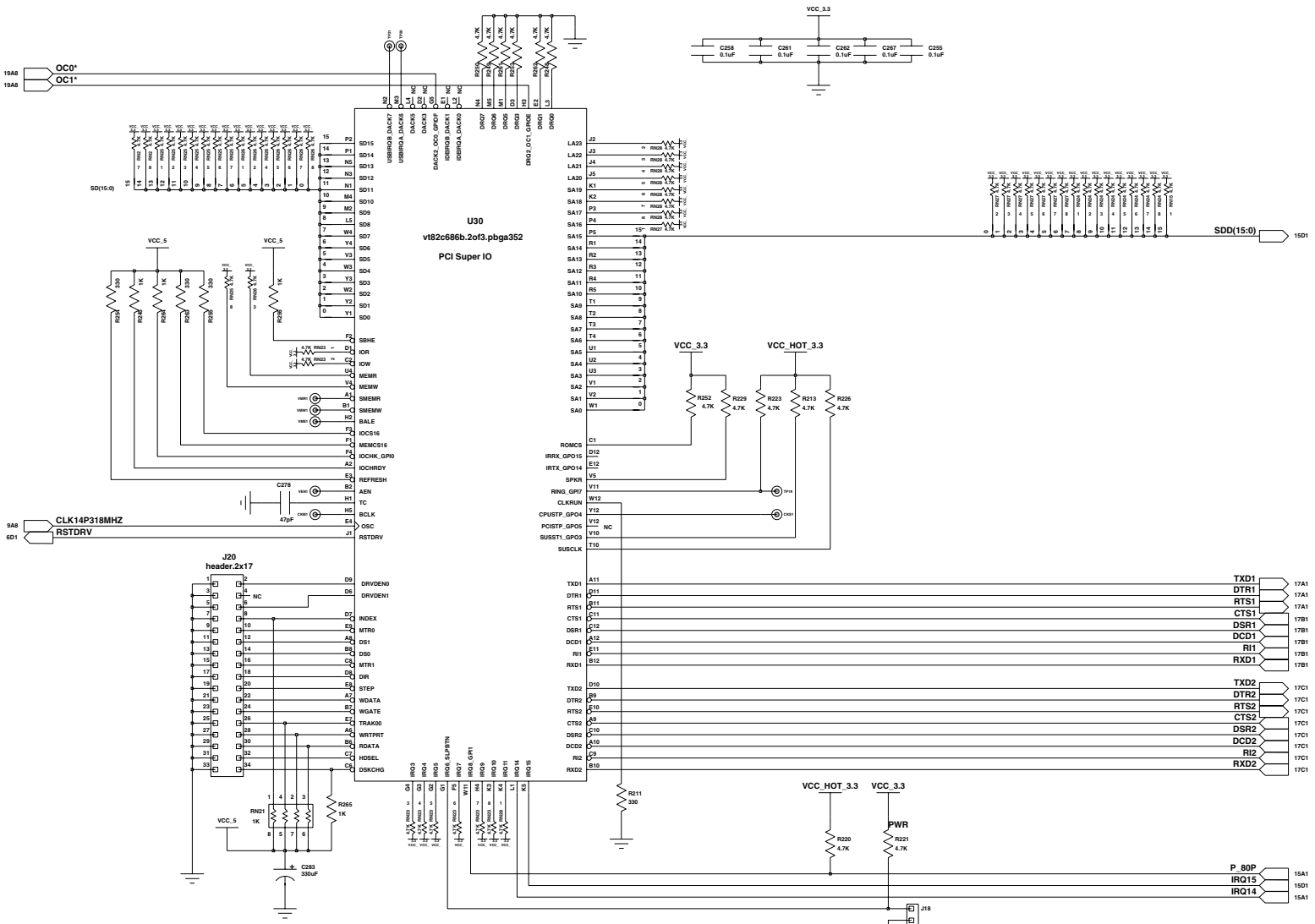
64-bit PrPMC connector used for additional 5V power only - 64bit PCI not supported.



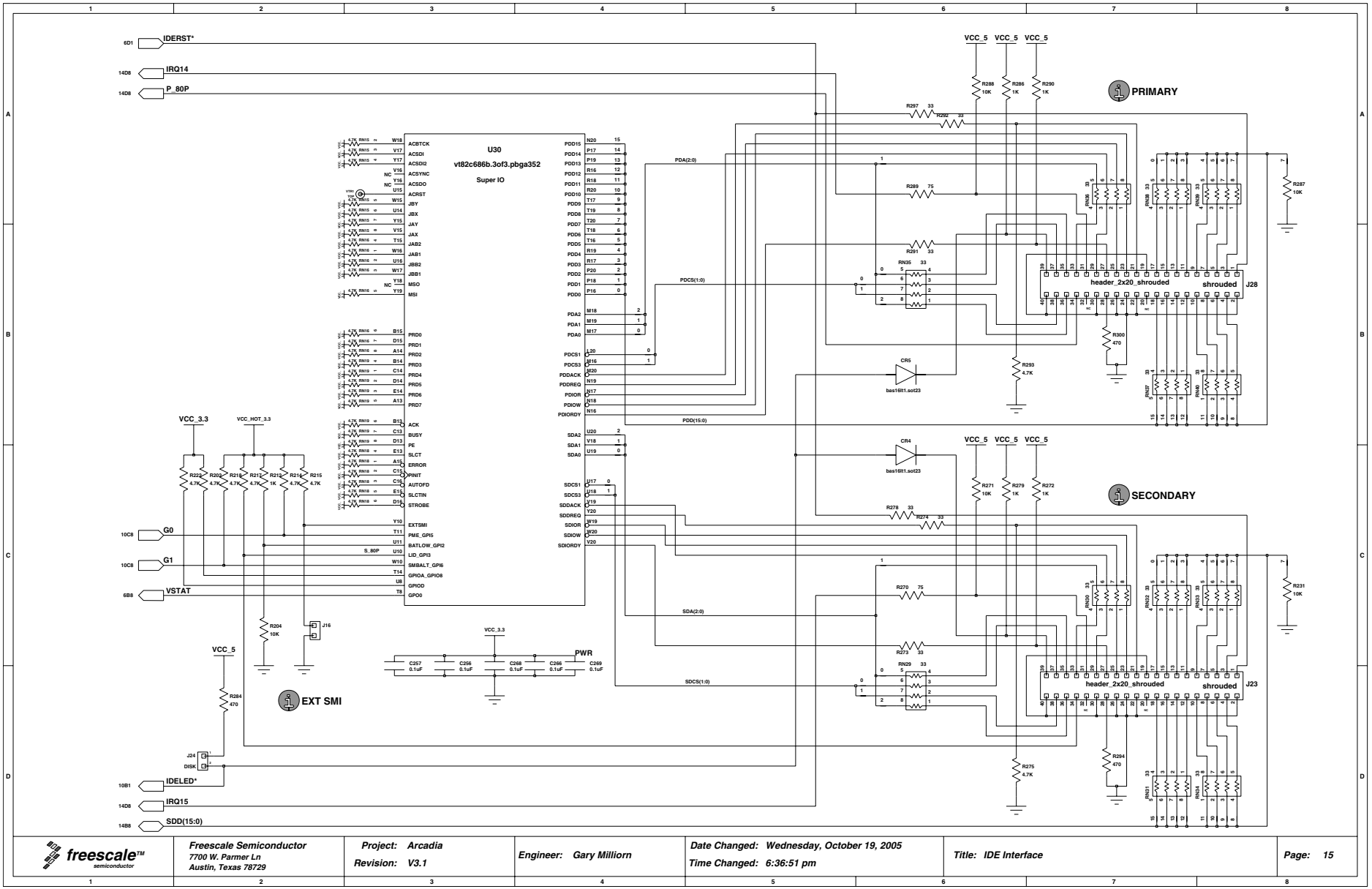
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:38:33 pm	Title: PrPMC connectors	Page: 12	



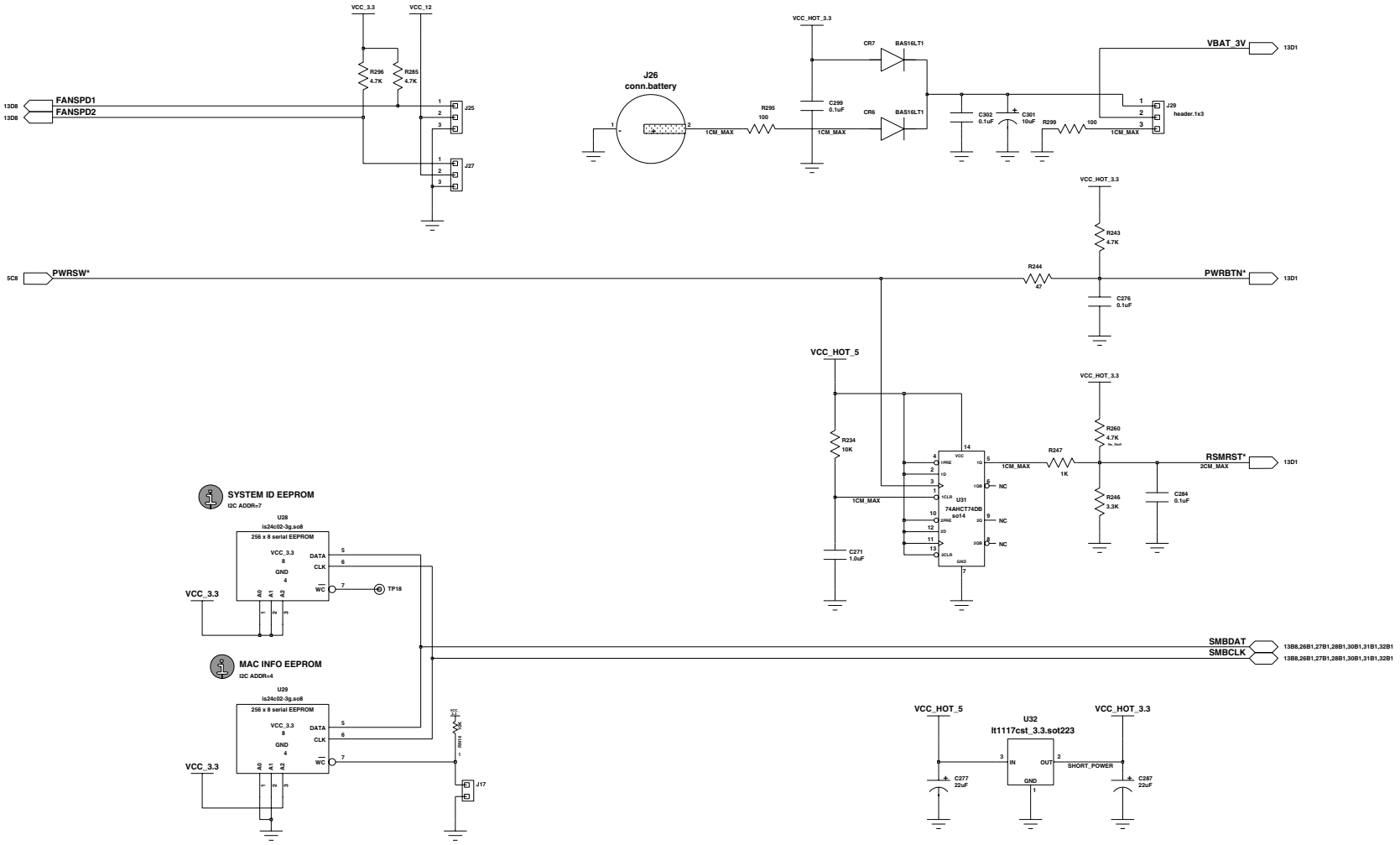
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Thursday, October 20, 2005 Time Changed: 3:36:12 pm	Title: System IO: PCI, USB and PS/2	Page: 13



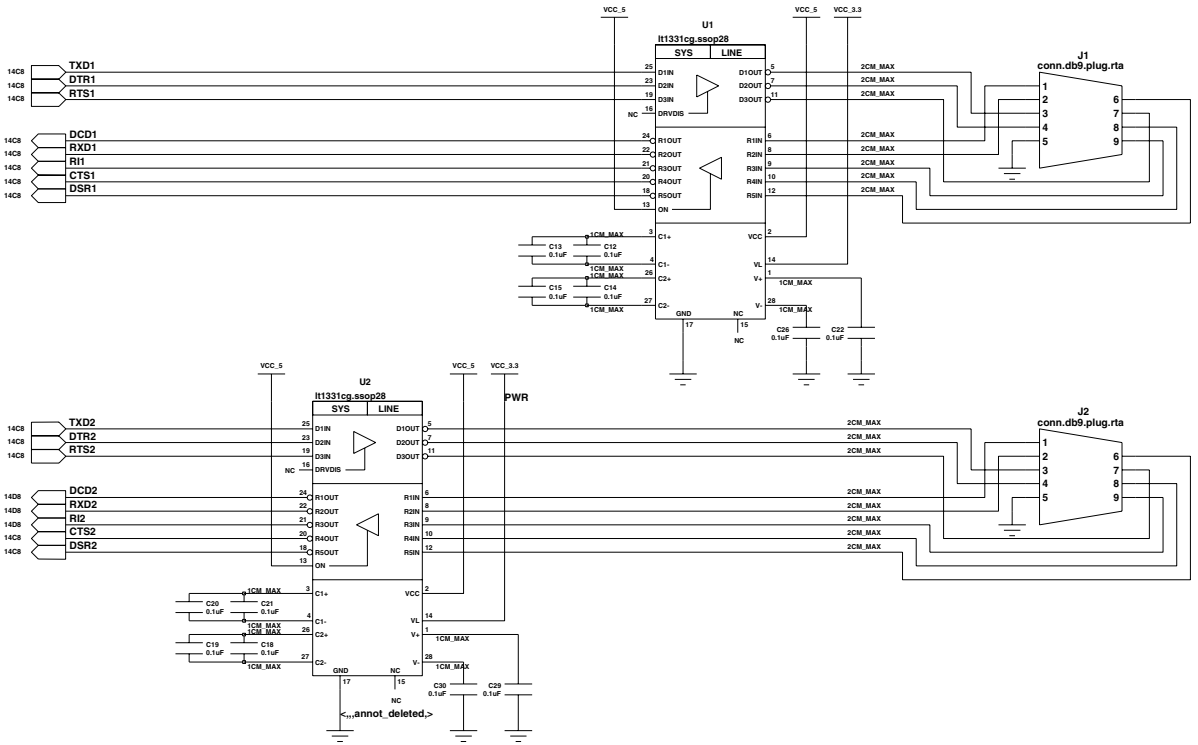
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:37:59 pm	Title: System IO: Floppy, IDE	Page: 14



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:36:51 pm	Title: IDE Interface	Page: 15



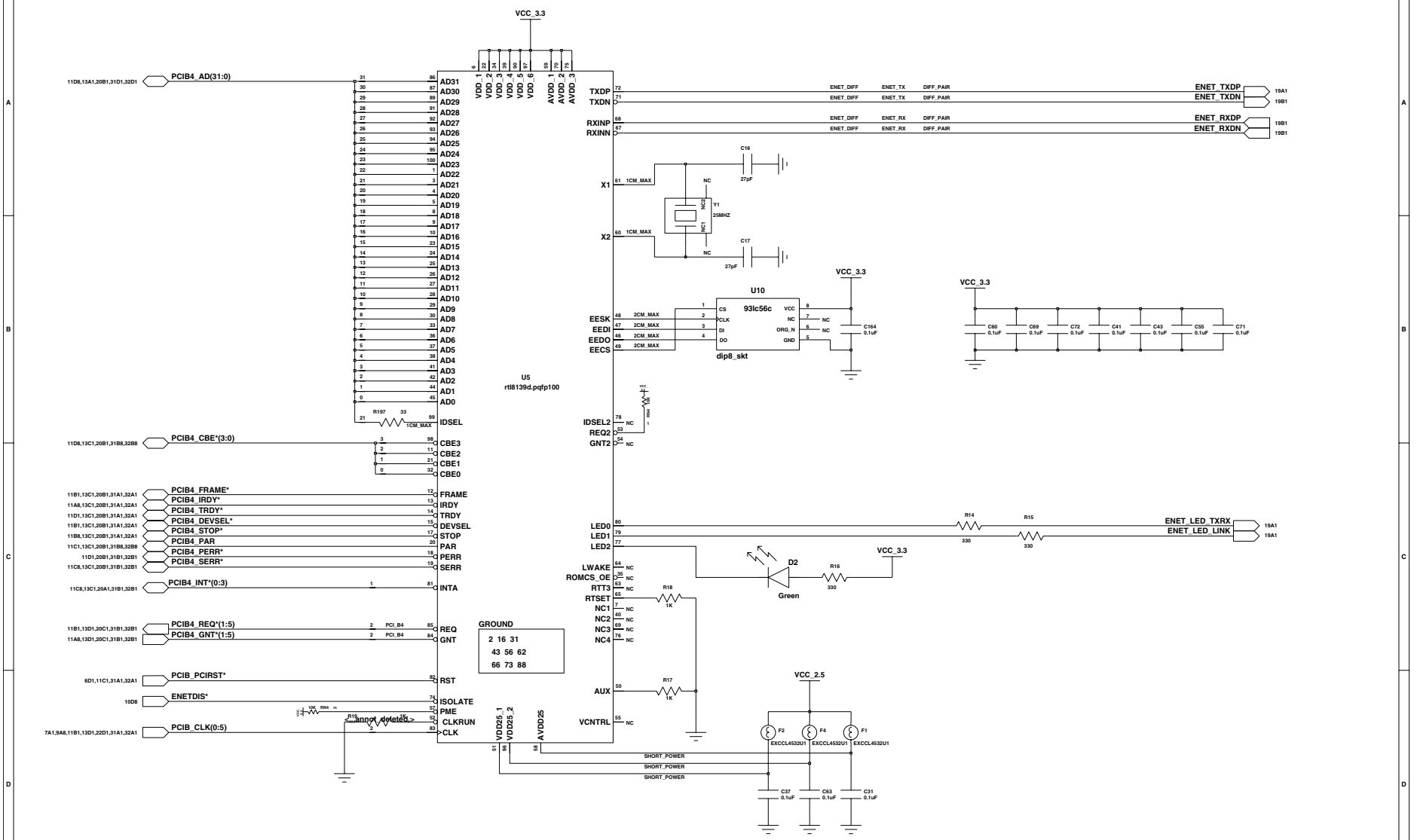
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:36:12 pm	Title: System IO: Power and Support Logic	Page: 16



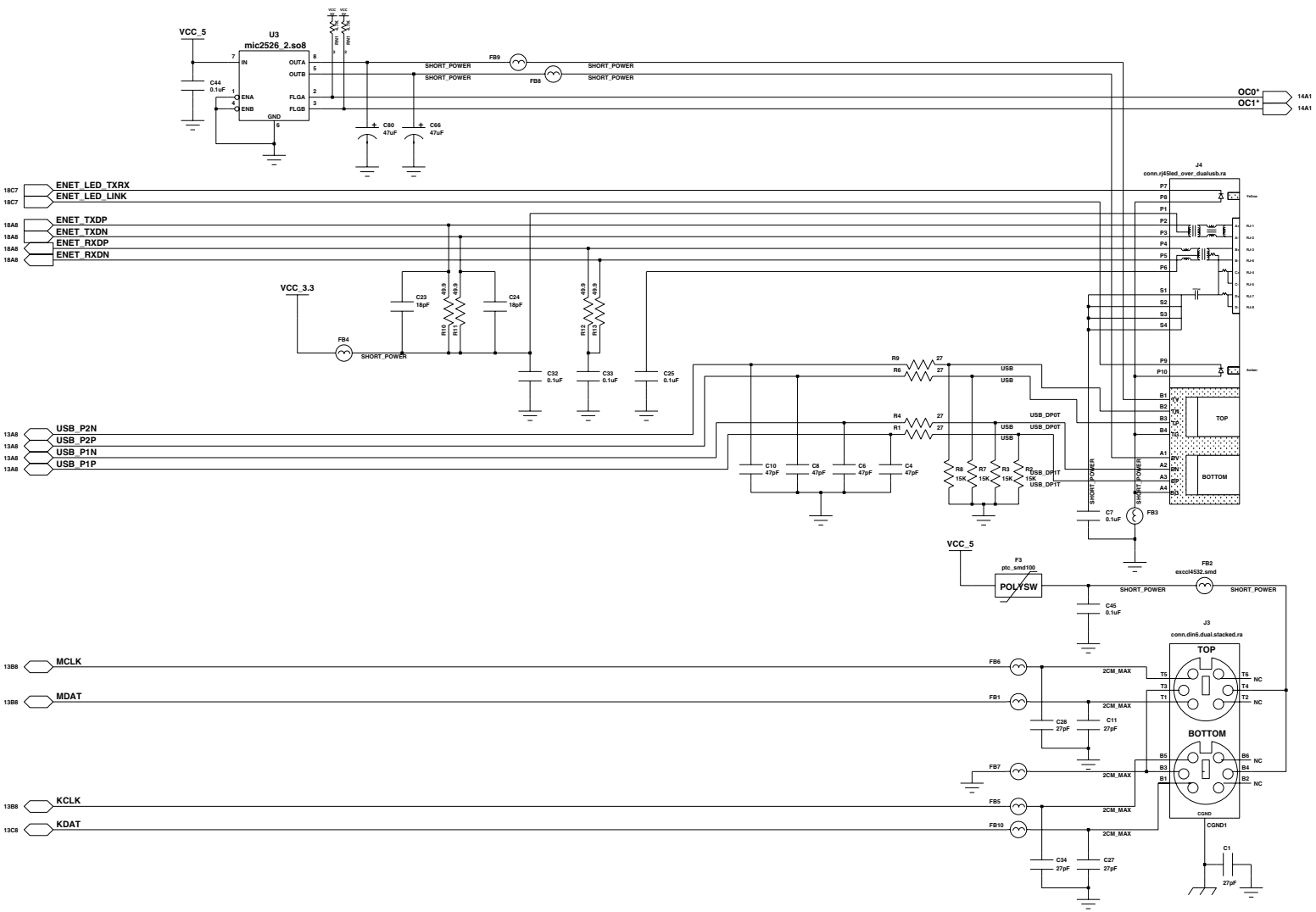
Serial Port #1
COM1: Leftmost (rear view)

Serial Port #2
COM2: Rightmost (rear view)

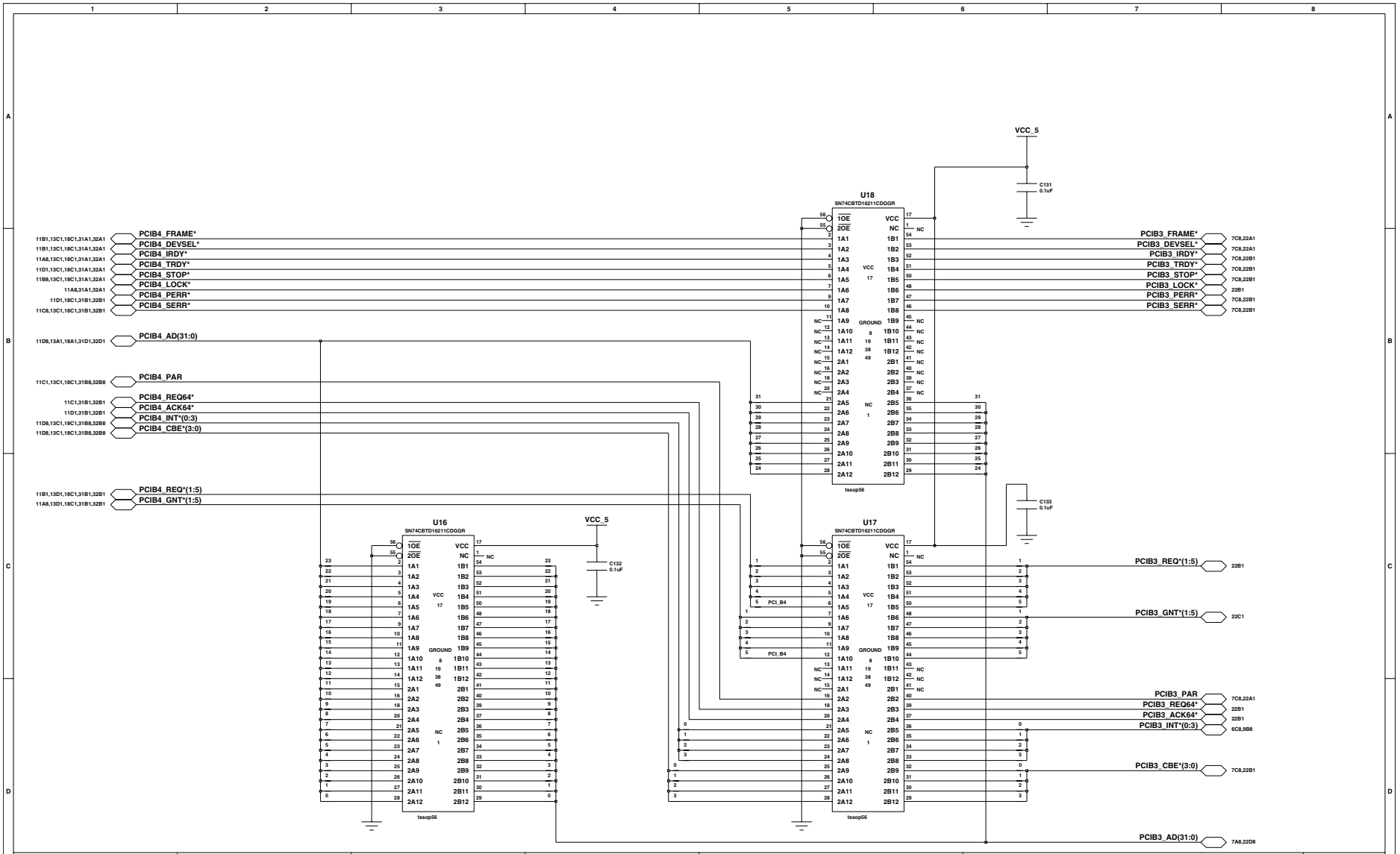
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:34:55 pm	Title: Serial Transceivers and Connectors	Page: 17



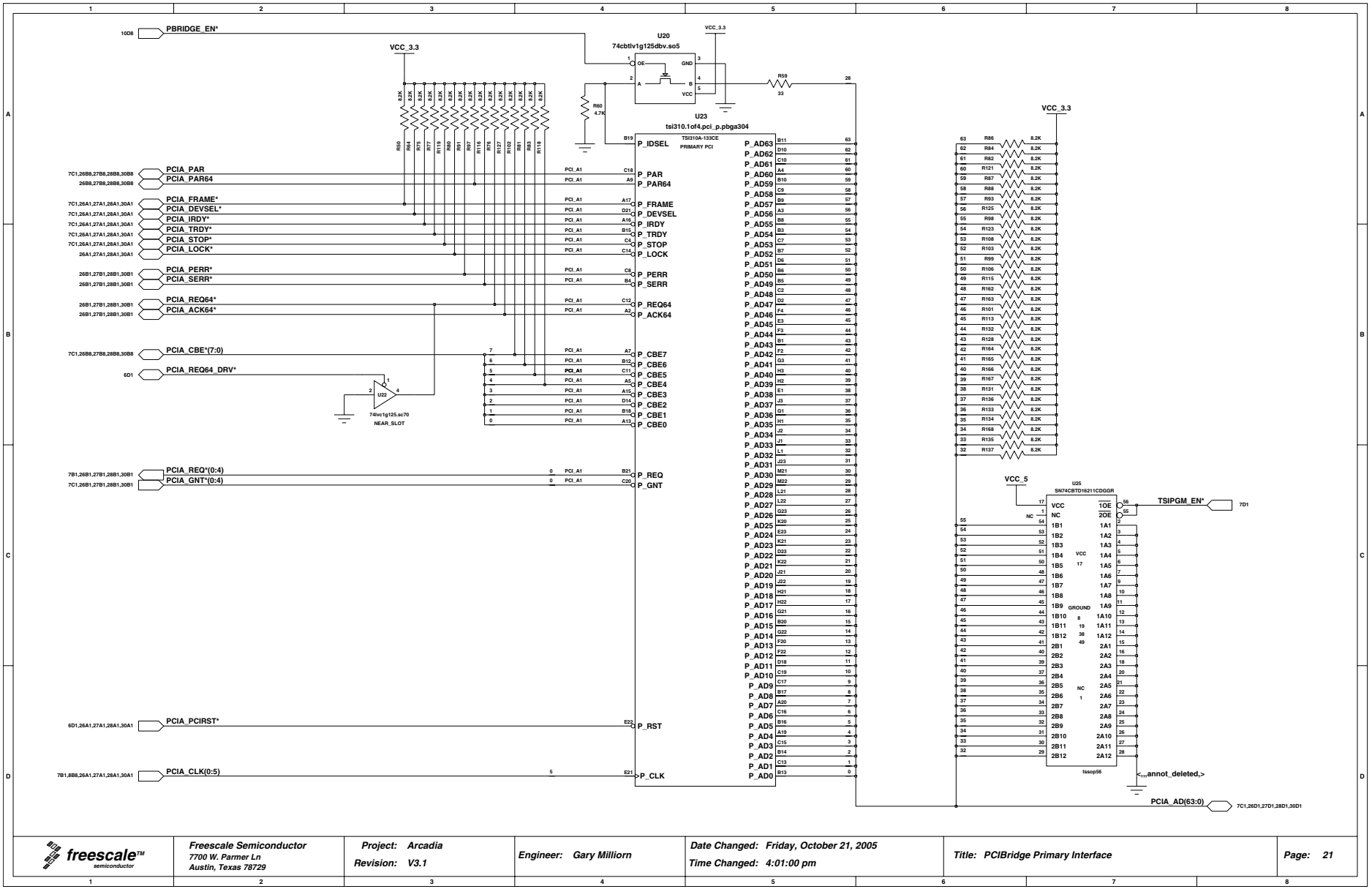
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:33:47 pm	Title: Ethernet Interface	Page: 18



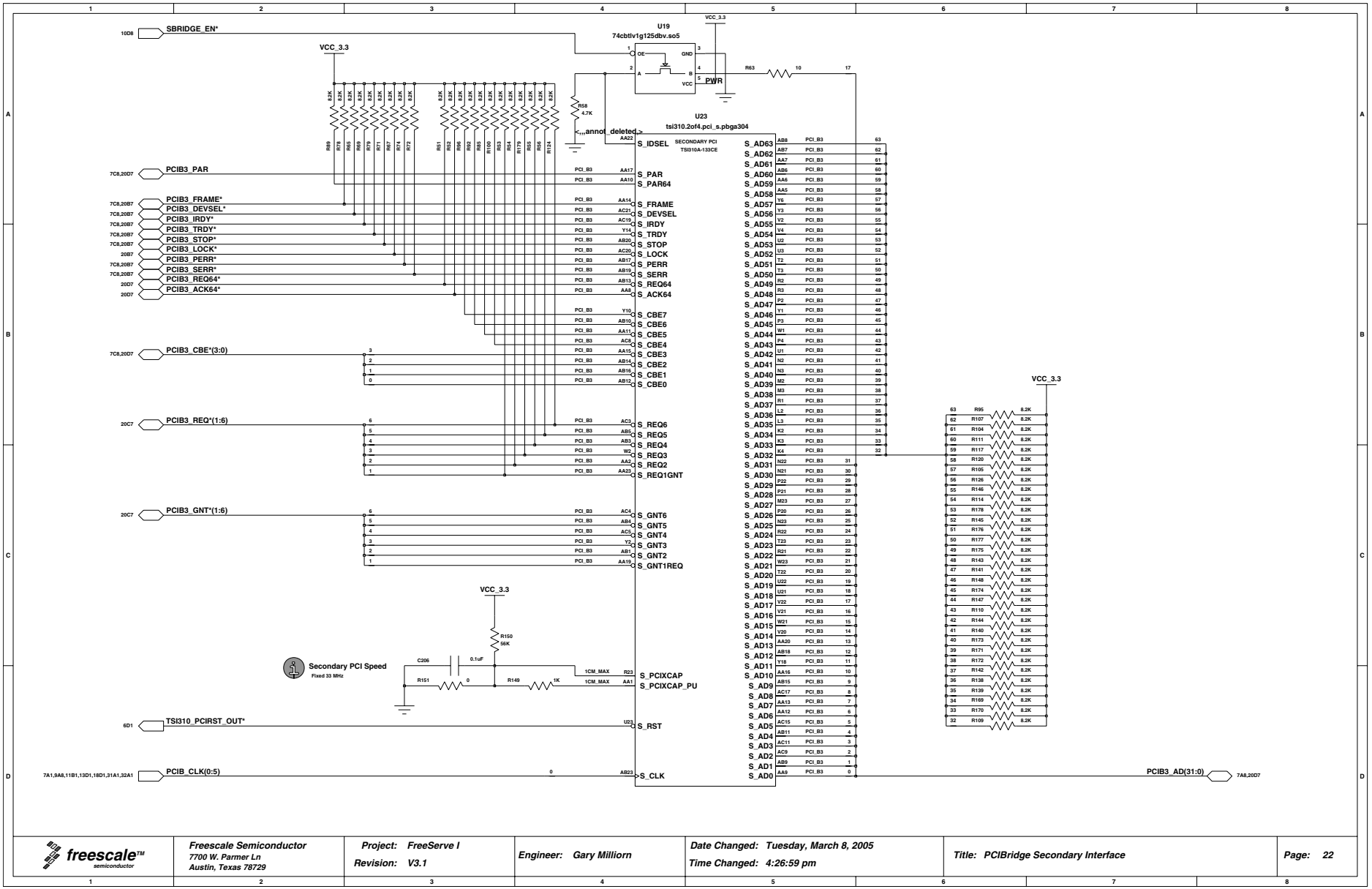
freescale™ semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:31:38 pm	Title: USB and Ethernet Connectors	Page: 19



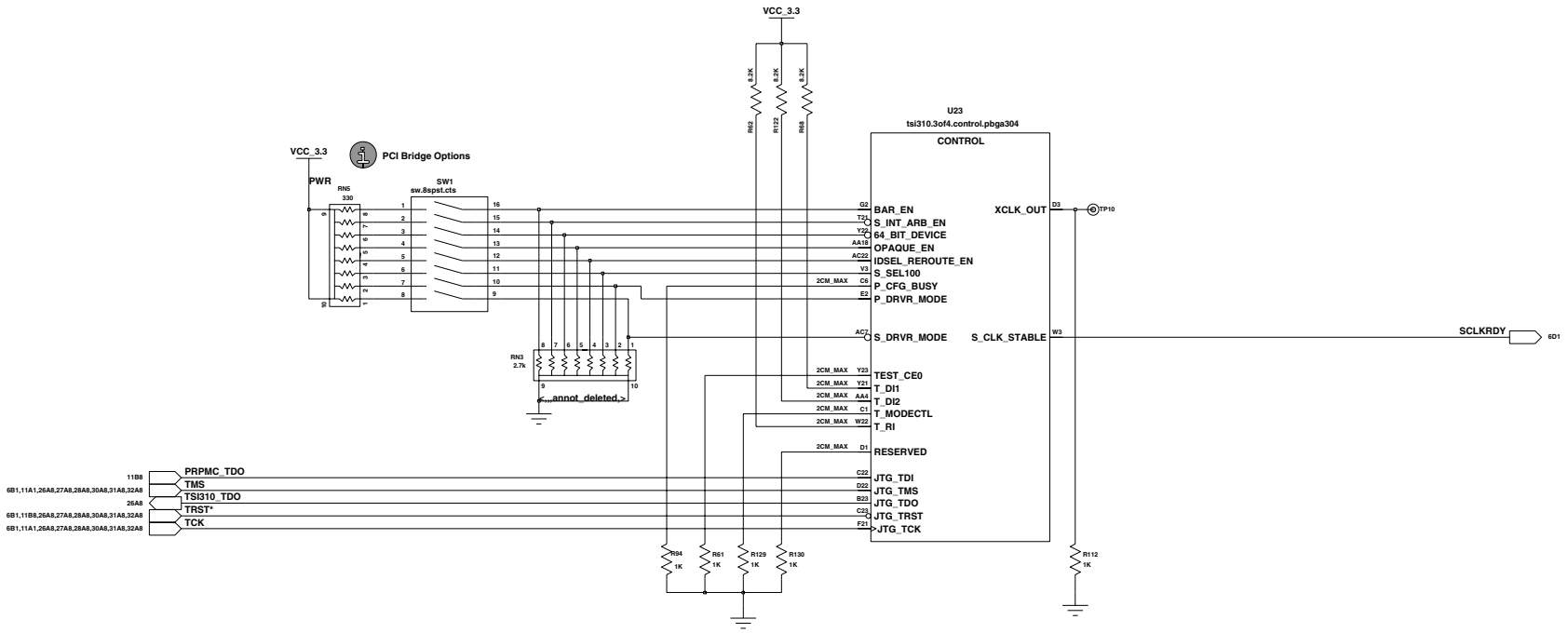
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:05:28 pm	Title: PCI1-PCI2 Bus Isolator	Page: 20



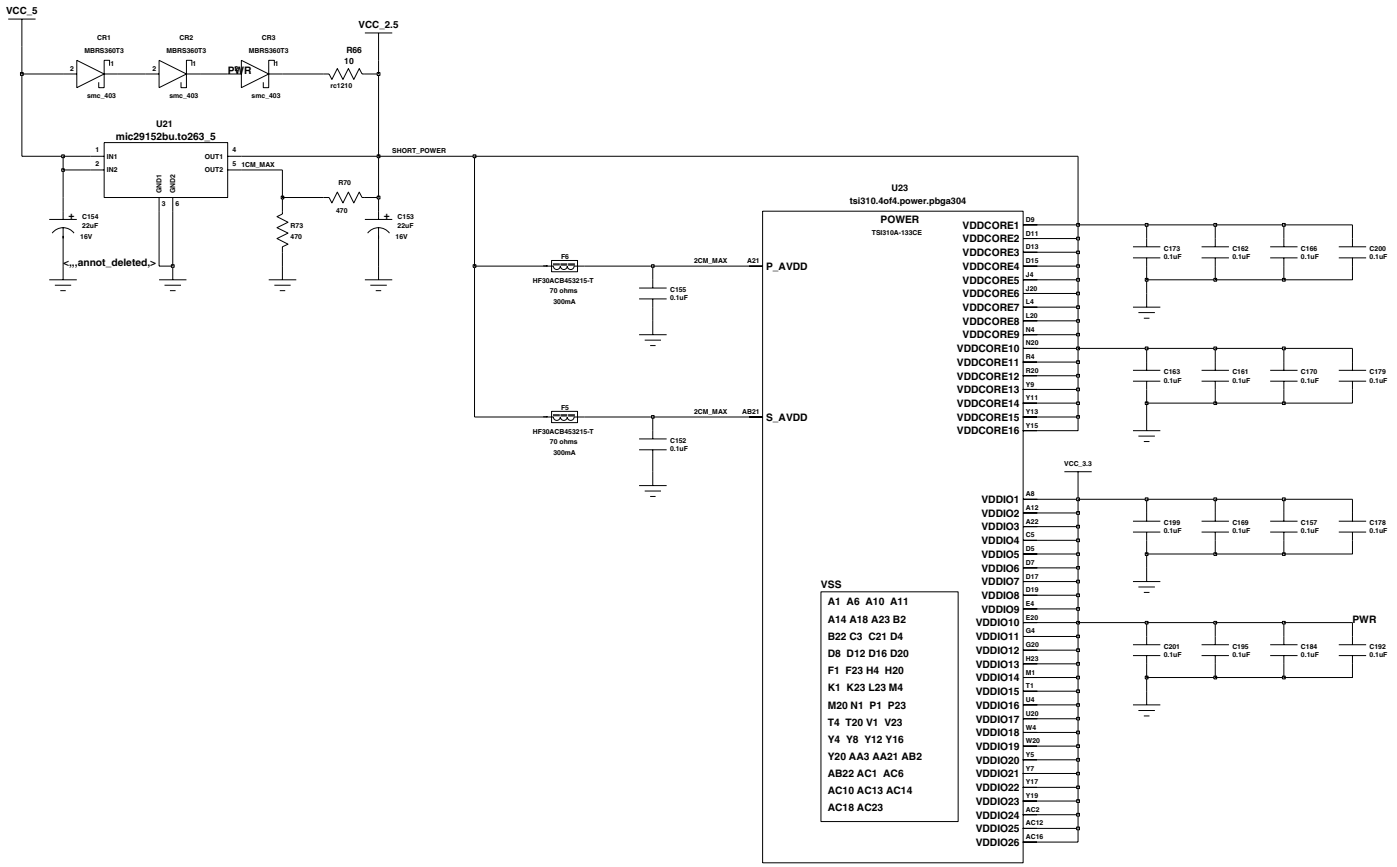
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Friday, October 21, 2005 Time Changed: 4:01:00 pm	Title: PCIBridge Primary Interface	Page: 21



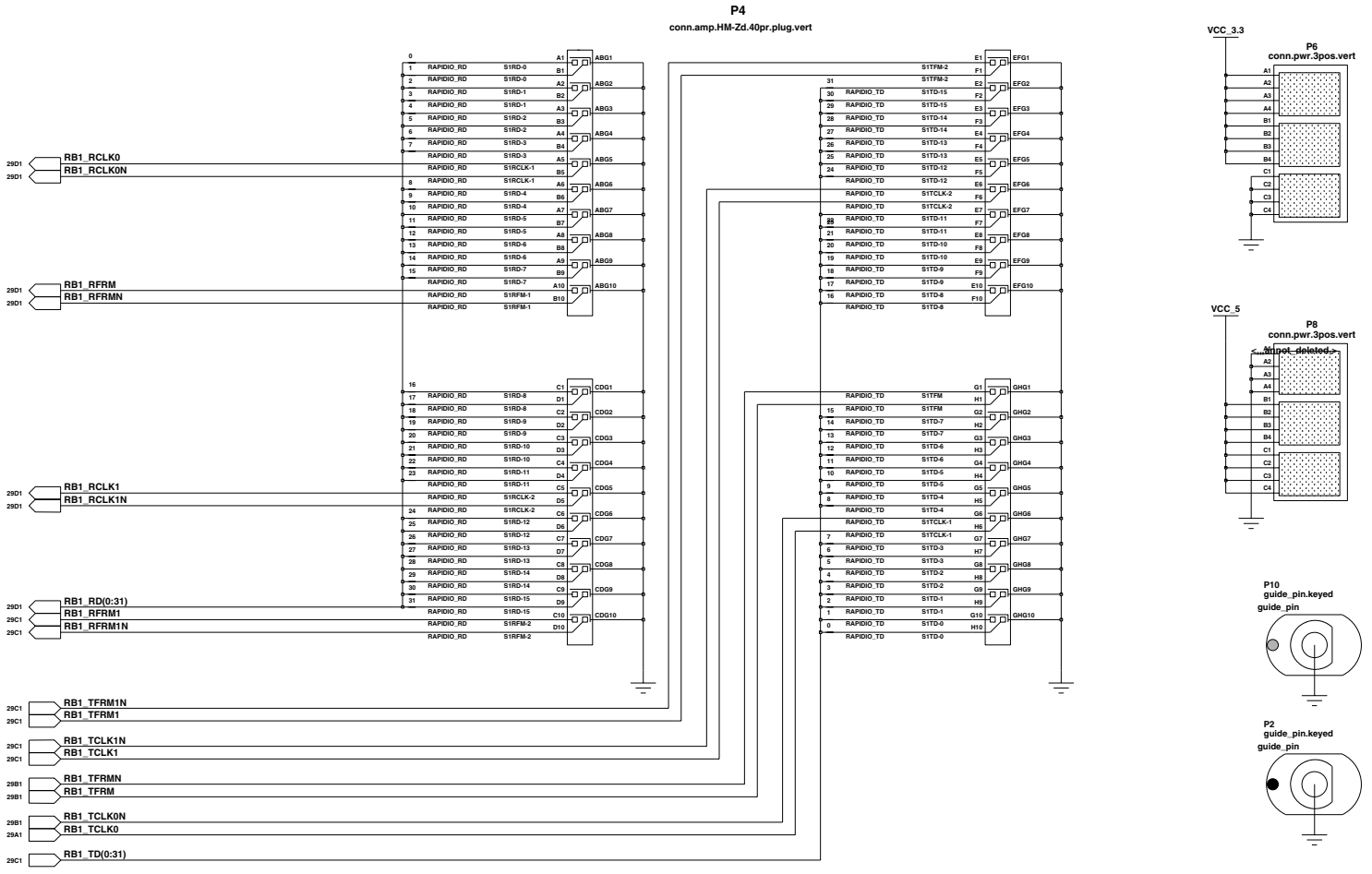
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: FreeServe I Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Tuesday, March 8, 2005 Time Changed: 4:26:59 pm	Title: PCIBridge Secondary Interface	Page: 22



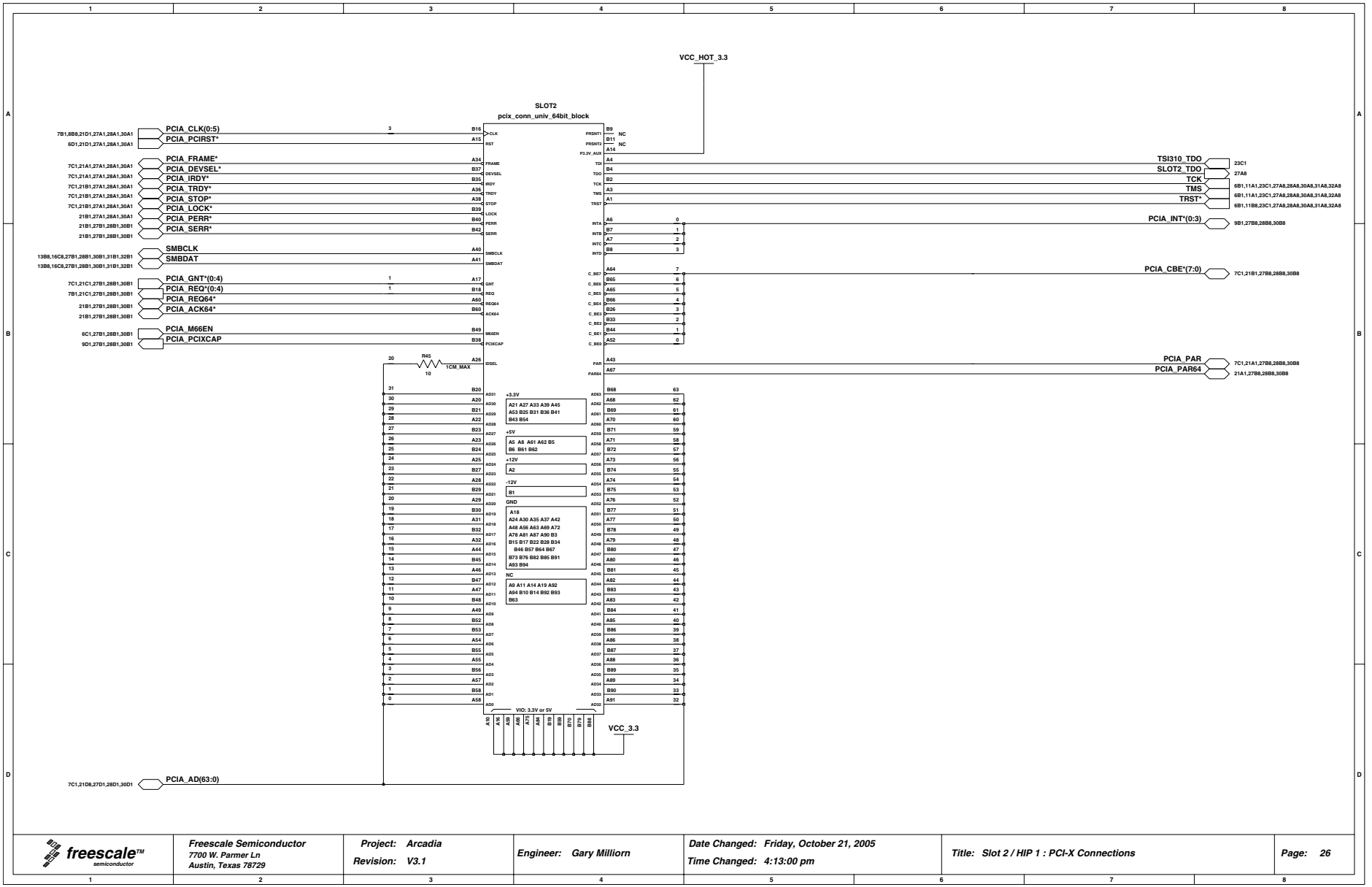
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:10:37 pm	Title: PCI Bridge Control/Options	Page: 23



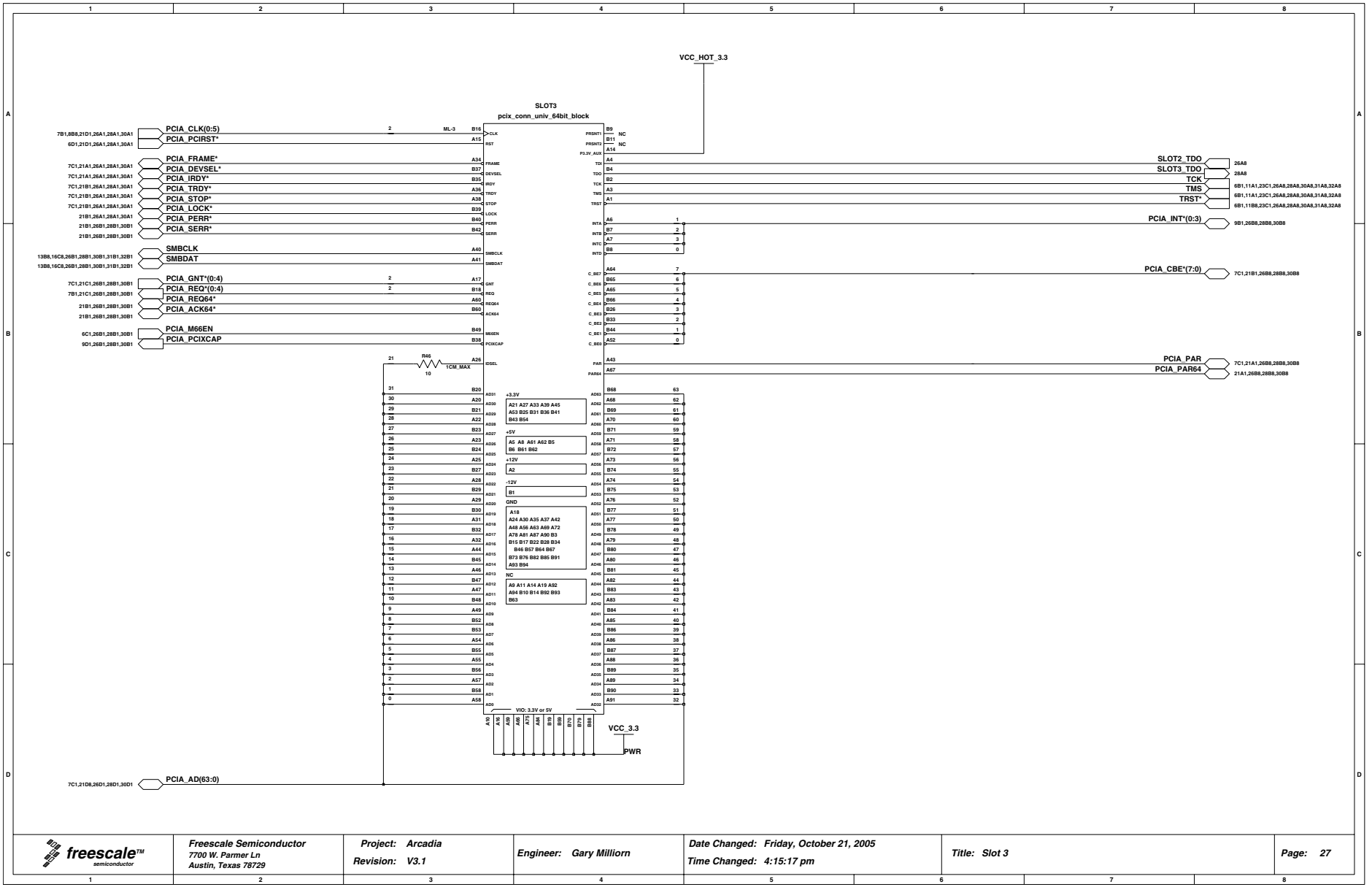
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:14:42 pm	Title: PCI Bridge: Power	Page: 24



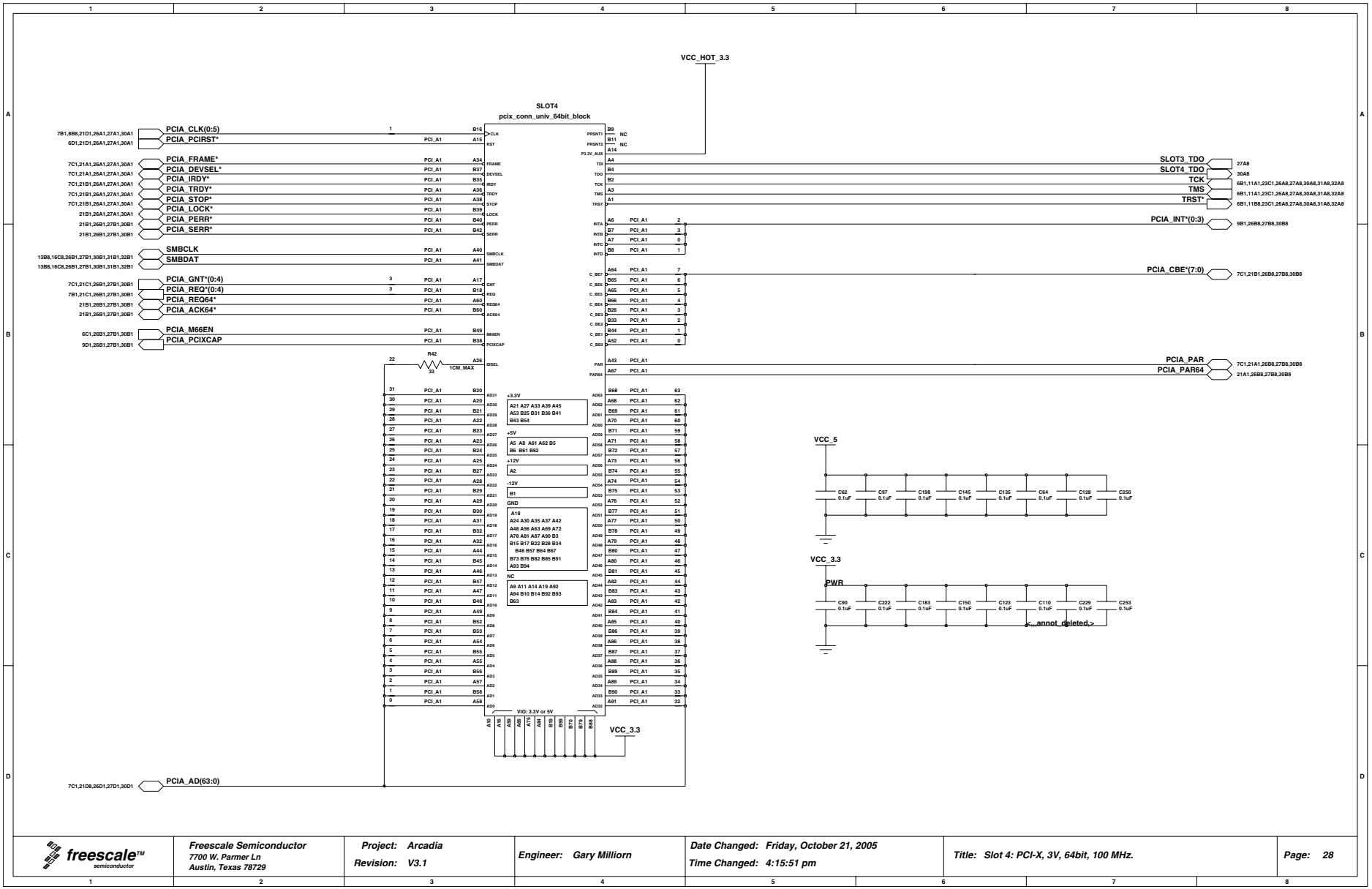
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:15:10 pm	Title: Slot 2/HIP 1 : LVDS Connection and Power	Page: 25



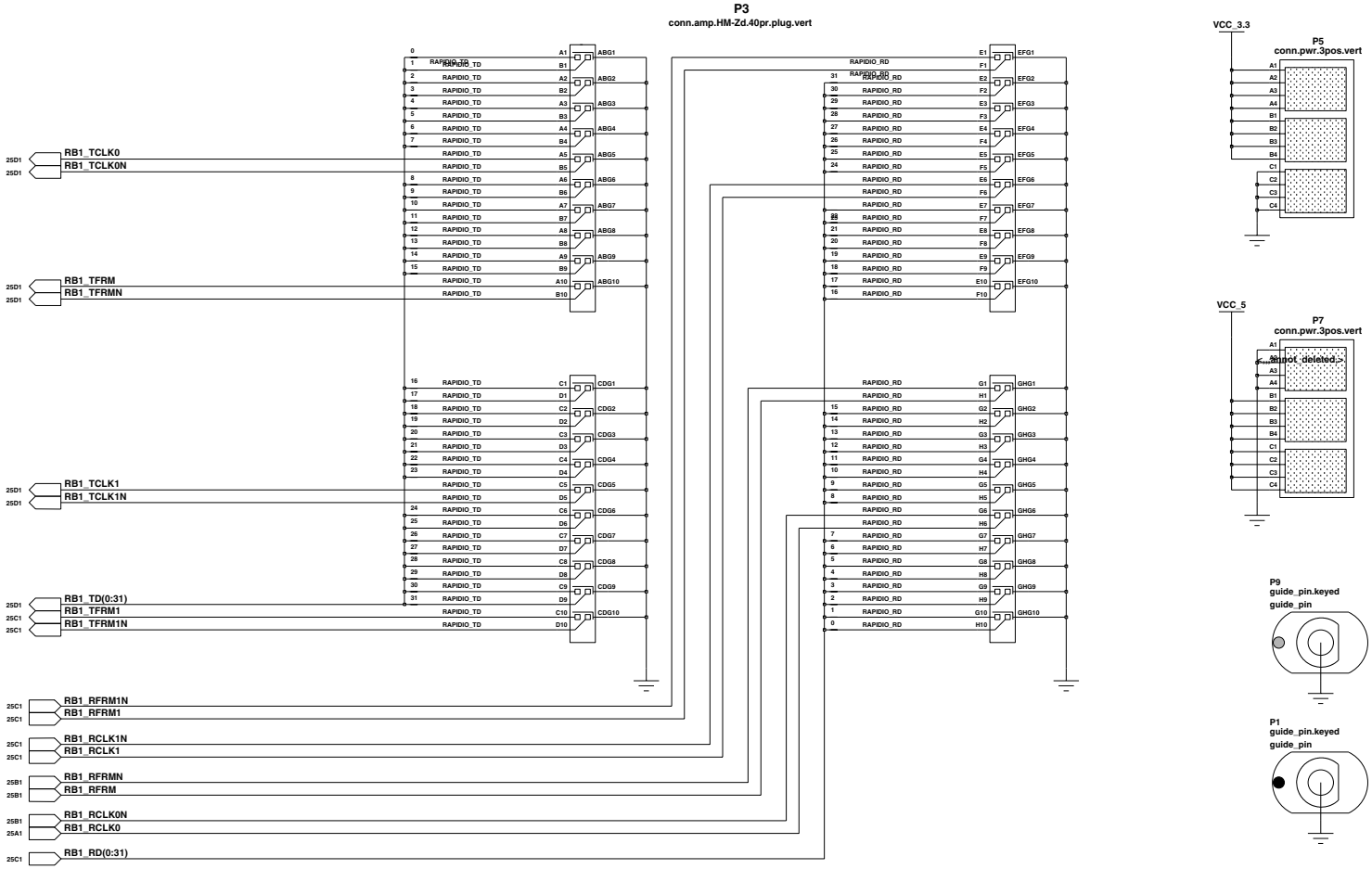
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Friday, October 21, 2005 Time Changed: 4:13:00 pm	Title: Slot 2 / HIP 1 : PCI-X Connections	Page: 26



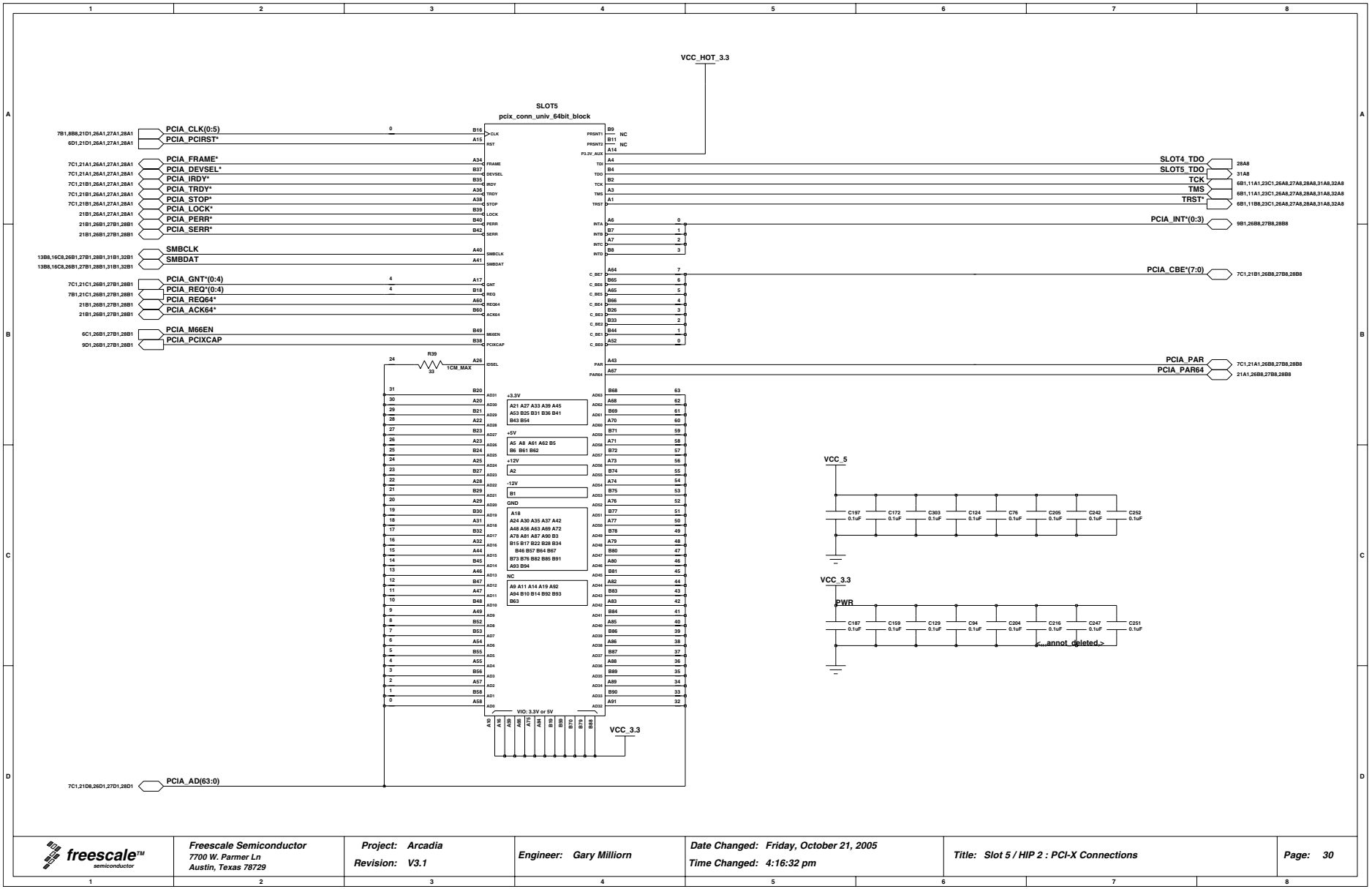
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Friday, October 21, 2005 Time Changed: 4:15:17 pm	Title: Slot 3	Page: 27



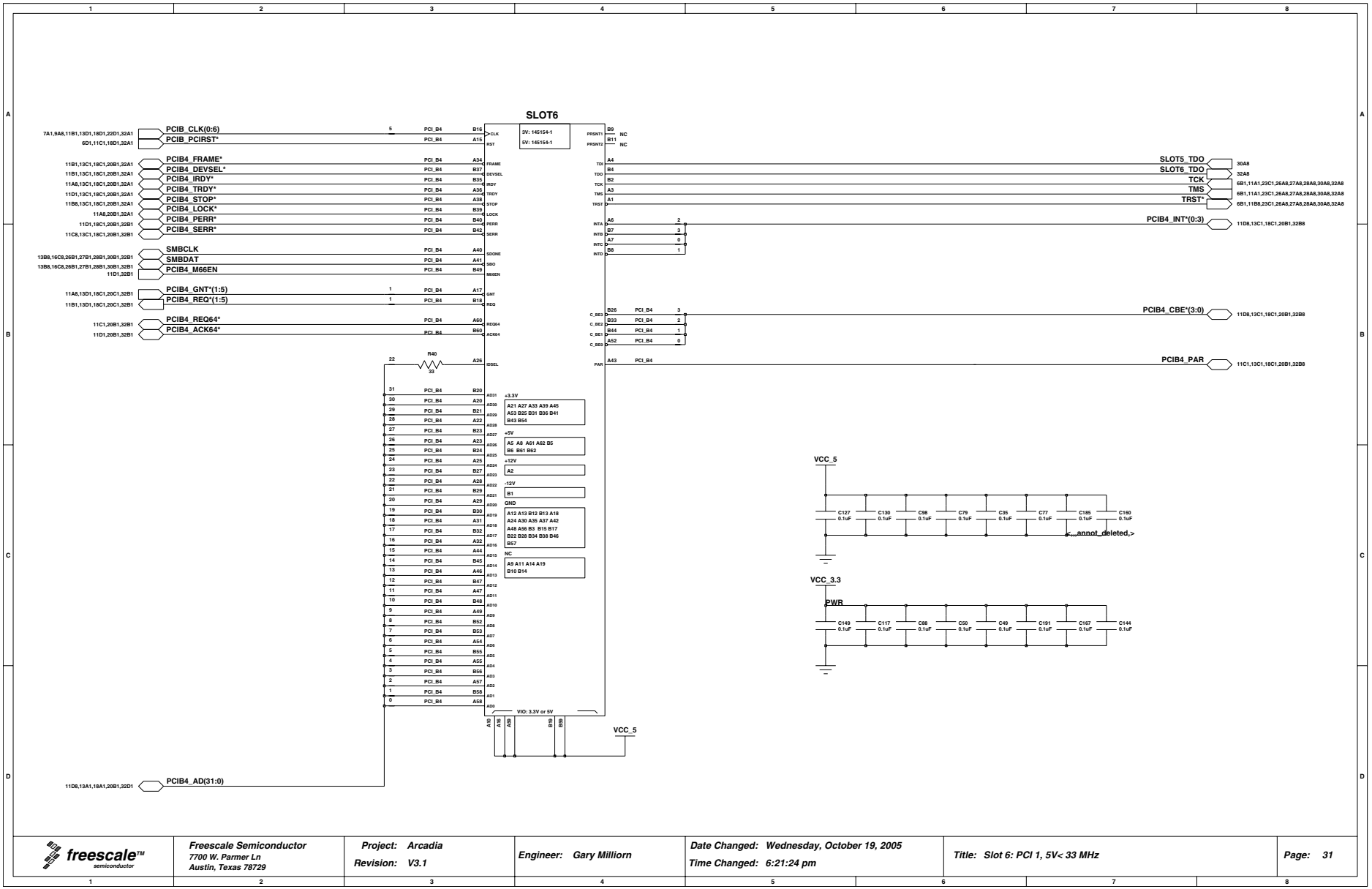
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Friday, October 21, 2005 Time Changed: 4:15:51 pm	Title: Slot 4: PCI-X, 3V, 64bit, 100 MHz.	Page: 28



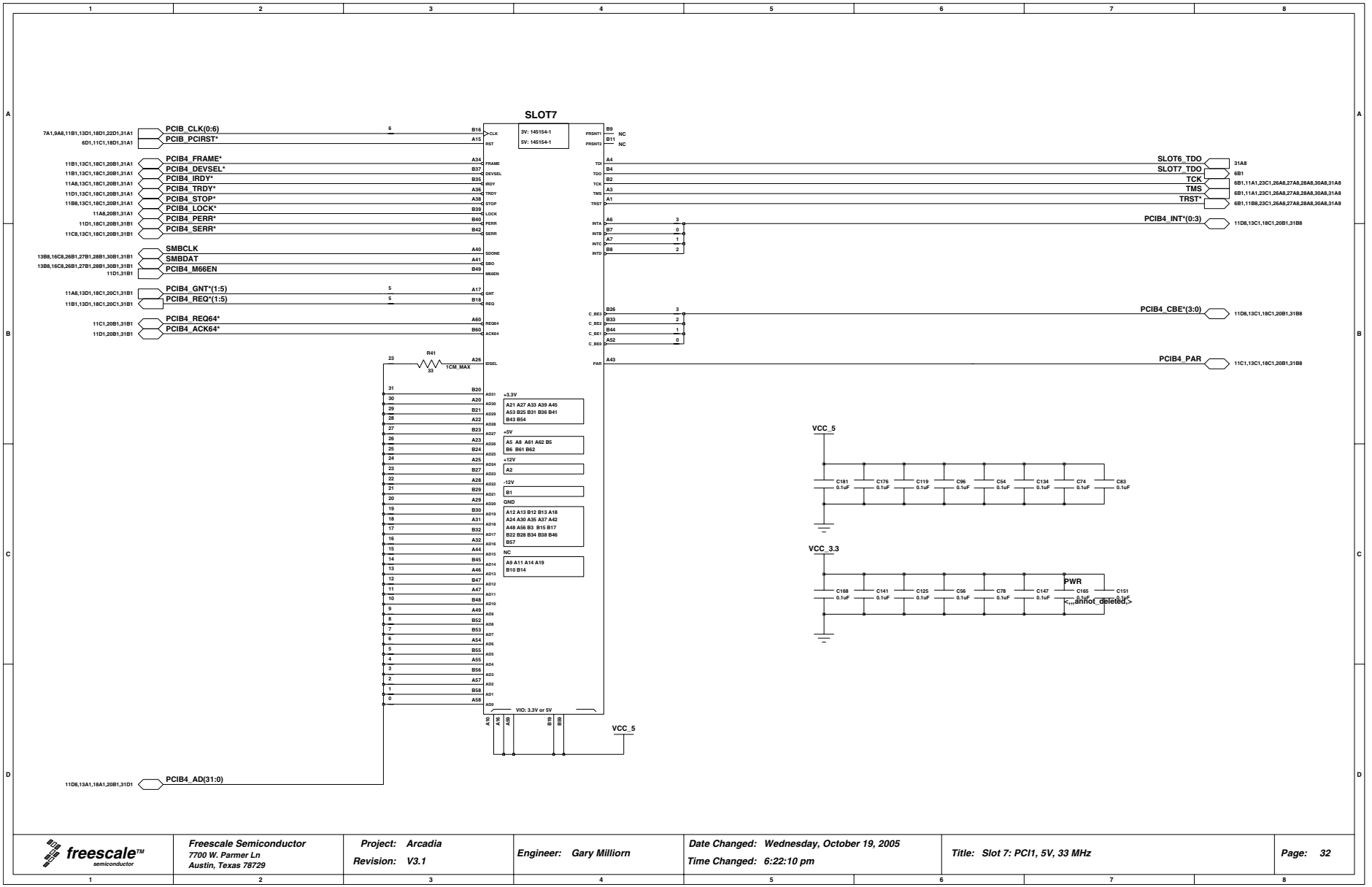
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:19:26 pm	Title: Slot 5 / HIP 2 : LVDS Connector and Power	Page: 29



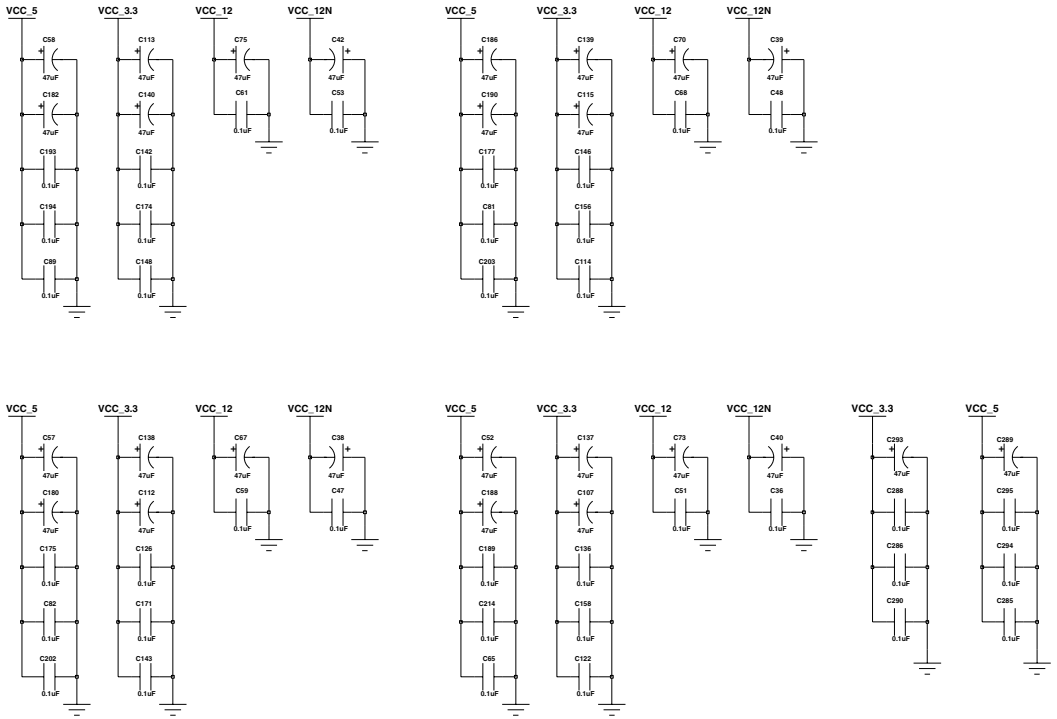
freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Friday, October 21, 2005 Time Changed: 4:16:32 pm	Title: Slot 5 / HIP 2 : PCI-X Connections	Page: 30



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:21:24 pm	Title: Slot 6: PCI 1, 5V< 33 MHz	Page: 31



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:22:10 pm	Title: Slot 7: PCI1, 5V, 33 MHz	Page: 32



freescale semiconductor	Freescale Semiconductor 7700 W. Parmer Ln Austin, Texas 78729	Project: Arcadia Revision: V3.1	Engineer: Gary Milliorn	Date Changed: Wednesday, October 19, 2005 Time Changed: 6:22:41 pm	Title: Global Bypass Capacitors	Page: 33

Glossary

The glossary contains an alphabetical list of terms, phrases, and abbreviations used in this reference manual.

A

Architecture. A detailed specification of requirements for a processor or computer system. It does not specify details of how the processor or computer system must be implemented; instead it provides a template for a family of compatible *most-significant byte*.

Atomic access. A bus access that attempts to be part of a read-write operation to the same address uninterrupted by any other access to that address (the term refers to the fact that the transactions are indivisible). The Power Architecture technology implements atomic accesses through the **lwarx**/**stwcx.** instruction pair.

Autobaud. The process of determining a serial data rate by timing the width of a single bit.

B

Beat. A single state on the MPC603e bus interface that may extend across multiple bus cycles. A MPC603e transaction can be composed of multiple address or data *beats*.

Big-endian. A byte-ordering method in memory where the address *n* of a word corresponds to the *most-significant byte*. In an addressed memory word, the bytes are ordered (left to right) 0, 1, 2, 3, with 0 being the *most-significant byte*. See *Secondary cache*.

Boundedly undefined. A characteristic of certain operation results that are not rigidly prescribed by the Power Architecture technology. Boundedly-undefined results for a given operation may vary among implementations and between execution attempts in the same implementation.

Although the architecture does not prescribe the exact behavior for when results are allowed to be boundedly undefined, the results of executing instructions in contexts where results are allowed to be boundedly undefined are constrained to ones that could have been achieved by executing an arbitrary sequence of defined instructions, in valid form, starting in the state the machine was in before attempting to execute the given instruction.

Breakpoint. A programmable event that forces the core to take a breakpoint exception.

Burst. A multiple-beat data transfer whose total size is typically equal to a cache block.

Bus clock. Clock that causes the bus state transitions.

Bus master. The owner of the address or data bus; the device that initiates or requests the transaction.

C

Cache. High-speed memory containing recently accessed data or instructions (subset of main memory).

Cache block. A small region of contiguous memory that is copied from memory into a *cache*. The size of a cache block may vary among processors; the maximum block size is one *page*. In Power Architecture processors, *cache coherency* is maintained on a cache-block basis. Note that the term ‘cache block’ is often used interchangeably with ‘cache line.’

Cache coherency. An attribute wherein an accurate and common view of memory is provided to all devices that share the same memory system. Caches are coherent if a processor performing a read from its cache is supplied with data corresponding to the most recent value written to memory or to another processor’s cache.

Cache flush. An operation that removes from a cache any data from a specified address range. This operation ensures that any modified data within the specified address range is written back to main memory. This operation is generated typically by a Data Cache Block Flush (**dcbf**) instruction.

Caching-inhibited. A memory update policy in which the *cache* is bypassed and the load or store is performed to or from main memory.

Cast out. A *cache block* that must be written to memory when a cache miss causes a cache block to be replaced.

Changed bit. One of two *page history bits* found in each *page table entry* (PTE). The processor sets the changed bit if any store is performed into the *page*. See also *page access history bits* and *referenced bit*.

Clean. An operation that causes a cache block to be written to memory, if modified, and then left in a valid, unmodified state in the cache.

Clear. To cause a bit or bit field to register a value of zero. See also *set*.

Completer. In PCI-X, a completer is the device addressed by a transaction (other than a split completion transaction). If a target terminates a transaction with a split response, the completer becomes the initiator of the subsequent split completion.

Context synchronization. An operation that ensures that all instructions in execution complete past the point where they can produce an *exception*, that all instructions in execution complete in the context in which they began execution, and that all subsequent instructions are *fetch*ed and executed in the new context. Context synchronization may result from executing specific instructions (such as **isync** or **rfi**) or when certain events occur (such as an exception).

Copy-back operation. A cache operation in which a cache line is copied back to memory to enforce cache coherency. Copy-back operations consist of snoop push-out operations and cache cast-out operations.

D

Denormalized number. A nonzero floating-point number whose exponent has a reserved value, usually the format's minimum, and whose explicit or implicit leading significand bit is zero.

Direct-mapped cache. A cache in which each main memory address can appear in only one location within the cache, operates more quickly when the memory request is a cache hit.

Double data rate. Memory that allows data transfers at the start and end of a clock cycle, thereby, doubling the data rate.

E

Effective address (EA). The 32-bit address specified for a load, store, or an instruction fetch. This address is then submitted to the MMU for translation to either a *physical memory* address or an I/O address.

Exception. A condition encountered by the processor that requires special, supervisor-level processing.

Exception handler. A software routine that executes when an exception is taken. Normally, the exception handler corrects the condition that caused the exception, or performs some other meaningful task (that may include aborting the program that caused the exception). The address for each exception handler is identified by an exception vector offset defined by the architecture and a prefix selected via the MSR.

Exclusive state. MEI state (E) in which only one caching device contains data that is also in system memory.

F

Frame-check sequence (FCS). Specifies the standard 32-bit cyclic redundancy check (CRC) obtained using the standard CCITT-CRC polynomial on all fields except the preamble, SFD, and CRC.

Fetch. Retrieving instructions from either the cache or main memory and placing them into the instruction queue.

Flush. An operation that causes a cache block to be invalidated and the data, if modified, to be written to memory.

G

General-purpose register (GPR). Any of the 32 registers in the general-purpose register file. These registers provide the source operands and destination results for all integer data manipulation instructions. Integer load instructions move data from memory to GPRs and store instructions move data from GPRs to memory.

Gigabit media-independent interface (GMII) sublayer. Sublayer that provides a standard interface between the MAC layer and the physical layer for 1000-Mbps operation. It isolates the MAC layer and the physical layer, enabling the MAC layer to be used with various implementations of the physical layer.

Guarded. The guarded attribute pertains to out-of-order execution. When a page is designated as guarded, instructions and data cannot be accessed out-of-order.

H

Harvard architecture. An architectural model featuring separate caches and other memory management resources for instructions and data.

I

IEEE 754. A standard written by the Institute of Electrical and Electronics Engineers that defines operations and representations of binary floating-point numbers.

Illegal instructions. A class of instructions that are not implemented for a particular processor. These include instructions not defined by the architecture. In addition, for 32-bit implementations, instructions that are defined only for 64-bit implementations are considered to be illegal instructions. For 64-bit implementations instructions that are defined only for 32-bit implementations are considered to be illegal instructions.

Implementation. A particular processor that conforms to the architecture, but may differ from other architecture-compliant implementations (for example, in design, feature set, and implementation of *optional* features).

Inbound ATMU windows. Mappings that perform address translation from the external address space to the local address space, attach attributes and transaction types to the transaction, and map the transaction to its target interface.

Inter-packet gap. The gap between the end of one Ethernet packet and the beginning of the next transmitted packet.

Integer unit. An execution unit in the core responsible for executing integer instructions.

In-order. An aspect of an operation that adheres to a sequential model. An operation is said to be performed in-order if, at the time that it is performed, it is known to be required by the sequential execution model. See *Out-of-order*.

Instruction latency. The total number of clock cycles necessary to execute an instruction and make ready the results of that instruction.

K

Kill. An operation that causes a *cache block* to be invalidated without writing any modified data to memory.

L

Latency. The number of clock cycles necessary to execute an instruction and make ready the results of that execution for a subsequent instruction.

L2 cache. Level-2 cache. See *Secondary cache*.

Least-significant bit (lsb). The bit of least value in an address, register, field, data element, or instruction encoding.

Least-significant byte (LSB). The byte of least value in an address, register, data element, or instruction encoding.

Little-endian. A byte-ordering method in memory where the address *n* of a word corresponds to the *least-significant byte*. In an addressed memory word, the bytes are ordered (left to right) 3, 2, 1, 0, with 3 being the *most-significant byte*. See *Big-endian*.

Local access window. Mapping used to translate a region of memory to a particular target interface, such as the DDR SDRAM controller or the PCI controller. The local memory map is defined by a set of eight local access windows. The size of each window can be configured from 4 Kbytes to 2 Gbytes.

M

Media access control (MAC) sublayer. Sublayer that provides a logical connection between the MAC and its peer station. Its primary responsibility is to initialize, control, and manage the connection with the peer station.

Medium-dependent interface (MDI) sublayer. Sublayer that defines different connector types for different physical media and PMD devices.

Media-independent interface (MII) sublayer. Sublayer that provides a standard interface between the MAC layer and the physical layer for 10/100-Mbps operations. It isolates the MAC layer and the physical layer, enabling the MAC layer to be used with various implementations of the physical layer.

Memory access ordering. The specific order in which the processor performs load and store memory accesses and the order in which those accesses complete.

Memory-mapped accesses. Accesses whose addresses use the page or block address translation mechanisms provided by the MMU and that occur externally with the bus protocol defined for memory.

Memory coherency. An aspect of caching in which it is ensured that an accurate view of memory is provided to all devices that share system memory.

Memory consistency. Refers to agreement of levels of memory with respect to a single processor and system memory (for example, on-chip cache, secondary cache, and system memory).

Memory management unit (MMU). The functional unit that is capable of translating an *effective address* (logical address) to a physical address, providing protection mechanisms, and defining caching methods.

Modified/exclusive/invalid (MEI). *Cache coherency* protocol used to manage caches on different devices that share a memory system. Note that the architecture does not specify the implementation of a MEI protocol to ensure cache coherency.

Modified state. MEI state (M) in which one, and only one, caching device has the valid data for that address. The data at this address in external memory is not valid.

Most-significant bit (msb). The highest-order bit in an address, registers, data element, or instruction encoding.

Most-significant byte (MSB). The highest-order byte in an address, registers, data element, or instruction encoding.

N

NaN. An abbreviation for not a number; a symbolic entity encoded in floating-point format. There are two types of NaNs—signaling NaNs and quiet NaNs.

No-op. No-operation. A single-cycle operation that does not affect registers or generate bus activity.

O

OCeaN. On-chip network. Non-blocking crossbar switch fabric. Enables full duplex port connections at 128 Gb/s concurrent throughput and independent per port transaction queuing and flow control. Permits high bandwidth, high performance, as well as the execution of multiple data transactions.

Out-of-order. Operation is said to be out-of-order when it is not guaranteed to be required by the sequential execution model, such as the execution of an instruction that follows another instruction that may alter the instruction flow. For example, execution of instructions in an unresolved branch is said to be out-of-order, as is the execution of an instruction behind another instruction that may yet cause an exception. The results of operations that are performed out-of-order are not committed to architected resources until it can be ensured that these results adhere to the in-order, or sequential execution model.

Outbound ATMU windows. Mappings that perform address translations from local 32-bit address space to the address spaces of RapidIO or PCI/PCI-X, which may be much larger than the local space. Outbound ATMU windows also map attributes such as transaction type or priority level.

P

Packet. A unit of binary data that can be routed through a network. Sometimes packet is used to refer to the frame plus the preamble and start frame delimiter (SFD).

Page. A region in memory. The OEA defines a page as a 4-Kbyte area of memory, aligned on a 4-Kbyte boundary.

Page access history bits. The *changed bit*s and *referenced bit*s in the PTE keep track of the access history within the page. The referenced bit is set by the MMU whenever the page is accessed for a read or write operation. The changed bit is set when the page is stored into. See *changed bit* and *referenced bit*.

Page fault. A page fault is a condition that occurs when the processor attempts to access a memory location that does not reside within a *page* not currently resident in *physical memory*. On PowerPC processors, a page fault exception condition occurs when a matching, valid *page table entry* (PTE[V] = 1) cannot be located.

Page table. A table in memory is comprised of *page table entry*s, or PTEs. It is further organized into eight PTEs per PTEG (page table entry group). The number of PTEGs in the page table depends on the size of the page table (as specified in the SDR1 register).

Page table entry (PTE). Data structures containing information used to translate *effective address* to physical address on a 4-Kbyte page basis. A PTE consists of 8 bytes of information in a 32-bit processor and 16 bytes of information in a 64-bit processor.

Physical coding sublayer (PCS). Sublayer responsible for encoding and decoding data stream to and from the MAC sublayer. Medium (1000BASEX) 8B/10B coding is used for fiber. Medium (1000BASET) 8B1Q coding is used for unshielded twisted pair (UTP).

Physical medium attachment (PMA) sublayer. Sublayer responsible for serializing code groups into a bit stream suitable for serial bit-oriented physical devices (SerDes) and vice versa. Synchronization is also performed for proper data decoding in this sublayer. The PMA sits between the PCS and the PMD sublayers. For fiber medium (1000BASEX) the interface on the PMD side of the PMA is a 1-bit 1250-MHz signal, while on the PMA PCS side the interface is a 10-bit interface (TBI) at 125 MHz. The TBI is an alternative to the GMII interface. If the TBI is used, the gigabit Ethernet controller must be capable of performing the PCS function. For UTP medium, the PMD interface side of the PMA consists of 4 pair of 62.5-MHz PAM5 encoded signals, while the PCS side provides the 1250-Mbps input to a 8B1Q4 PCS.

Physical medium dependent (PMD) sublayer. Sublayer responsible for signal transmission. The typical PMD functionality includes amplifier, modulation, and wave shaping. Different PMD devices may support different media.

Physical memory. The actual memory that can be accessed through the system's memory bus.

Pipelining. A technique that breaks operations, such as instruction processing or bus transactions, into smaller distinct stages or tenures (respectively) so that a subsequent operation can begin before the previous one has completed.

Precise exceptions. A category of exception for which the pipeline can be stopped so instructions that preceded the faulting instruction can complete and subsequent instructions can be flushed and redispatched after exception handling has completed.

Primary opcode. The most-significant 6 bits (bits 0–5) of the instruction encoding that identifies the type of instruction.

Program order. The order of instructions in an executing program. More specifically, this term is used to refer to the original order in which program instructions are fetched into the instruction queue from the cache.

Protection boundary. A boundary between *protection domains*.

Protection domain. A protection domain is a segment, a virtual page, a BAT area, or a range of unmapped effective addresses. It is defined only when the appropriate relocate bit in the MSR (IR or DR) is 1.

Q

Quad word. A group of 16 contiguous locations starting at an address divisible by 16.

Quiesce. To come to rest. The processor is said to quiesce when an exception is taken or a **sync** instruction is executed. The instruction stream is stopped at the decode stage and executing instructions are allowed to complete to create a controlled context for instructions that may be affected by out-of-order, parallel execution. See *Context synchronizations*.

R

rA. The **r**A instruction field is used to specify a GPR to be used as a source or destination.

rB. The **r**B instruction field is used to specify a GPR to be used as a source.

rD. The **r**D instruction field is used to specify a GPR to be used as a destination.

rS. The **r**S instruction field is used to specify a GPR to be used as a source.

RapidIO. High-performance, packet-switched, interconnect architecture that provides reliability, increased bandwidth, and faster bus speeds in an intra-system interconnect. Designed to be compatible with integrated communications processors, host processors, and networking digital signal processors,

Record bit. Bit 31 (or the Rc bit) in the instruction encoding. When it is set, updates the condition register (CR) to reflect the result of the operation.

Reconciliation sublayer. Sublayer that maps the terminology and commands used in the MAC layer into electrical formats appropriate for the physical layer entities.

Reduced instruction set computing (RISC). An *architecture* characterized by fixed-length instructions with nonoverlapping functionality and by a separate set of load and store instructions that perform memory accesses.

Referenced bit. One of two *page history bits* found in each *page table entry*. The processor sets the *referenced bit* whenever the page is accessed for a read or write. See also *page access history bits*.

Requester. In PCI-X, a requester is an initiator that first introduces a transaction into the PCI-X domain.If a transaction is terminated with a split response, the requester becomes the target of the subsequent split completion.

Reservation. The processor establishes a reservation on a *cache block* of memory space when it executes an **lwarx** instruction to read a memory semaphore into a GPR.

Reservation station. A buffer between the dispatch and execute stages that allows instructions to be dispatched even though the results of instructions on which the dispatched instruction may depend are not available.

S

Secondary cache. A cache memory that is typically larger and has a longer access time than the primary cache. A secondary cache may be shared by multiple devices. Also referred to as L2, or level-2, cache.

Sequence. In PCI-X, a sequence is one or more transactions associated with carrying out a single logical transfer by a requester. Each transaction in the same sequence carries the same unique sequence ID.

Set (*v*)**.** To write a nonzero value to a bit or bit field; the opposite of *clear*. The term ‘set’ may also be used to generally describe the updating of a bit or bit field.

Set (*n*)**.** A subdivision of a *cache*. Cacheable data can be stored in a given location in one of the sets, typically corresponding to its lower-order address bits. Because several memory locations can map to the same location, cached data is typically placed in the set whose *cache block* corresponding to that address was used least recently. See *Set-associative*.

Set-associative. Aspect of cache organization in which the cache space is divided into sections, called *sets*. The cache controller associates a particular main memory address with the contents of a particular set, or region, within the cache.

Slave. The device addressed by a master device. The slave is identified in the address tenure and is responsible for supplying or latching the requested data for the master during the data tenure.

Snooping. Monitoring addresses driven by a bus master to detect the need for coherency actions.

Snoop push. Response to a snooped transaction that hits a modified cache block. The cache block is written to memory and made available to the snooping device.

Stall. An occurrence when an instruction cannot proceed to the next stage.

Sticky bit. A bit that when *set* must be cleared explicitly.

Superscalar machine. A machine that can issue multiple instructions concurrently from a conventional linear instruction stream.

Supervisor mode. The privileged operation state of a processor. In supervisor mode, software, typically the operating system, can access all control registers and can access the supervisor memory space, among other privileged operations.

Synchronization. A process to ensure that operations occur strictly *in order*. See *Context synchronizations*.

Synchronous exception. An *exception* that is generated by the execution of a particular instruction or instruction sequence. There are two types of synchronous exceptions, *precise exceptions* and *imprecise*.

System memory. The physical memory available to a processor.

T

Time-division multiplex (TDM). A single serial channel used by several channels taking turns.

Tenure. The period of bus mastership. For the 603e, there can be separate address bus tenures and data bus tenures. A tenure consists of three phases: arbitration, transfer, and termination.

Throughput. The measure of the number of instructions that are processed per clock cycle.

Transaction. A complete exchange between two bus devices. A transaction is typically comprised of an address tenure and one or more data tenures, which may overlap or occur separately from the address tenure. A transaction may be minimally comprised of an address tenure only.

Transfer termination. Signal that refers to both signals that acknowledge the transfer of individual beats (of both single-beat transfer and individual beats of a burst transfer) and to signals that mark the end of the tenure.

Translation lookaside buffer (TLB). A cache that holds recently-used *page table entry*.

U

User mode. The operating state of a processor used typically by application software. In user mode, software can access only certain control registers and can access only user memory space. No privileged operations can be performed. Also referred to as problem state.

V

Virtual address. An intermediate address used in the translation of an *effective address* to a physical address.

Virtual memory. The address space created using the memory management facilities of the processor. Program access to *virtual memory* is possible only when it coincides with *physical memory*.

W

Way. A location in the cache that holds a cache block, its tags, and status bits.

Word. A 32-bit data element.

Write-back. A cache memory update policy in which processor write cycles are directly written only to the cache. External memory is updated only indirectly, for example, when a modified cache block is *cast out* to make room for newer data.

Write-through. A cache memory update policy in which all processor write cycles are written to both the cache and memory.

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
+1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

PN 924-75516, Rev. B
Document Number: MPC8555CDSx3RM
Rev. 1, 11/2006