# Errata to MPC8245 Integrated Processor Reference Manual, Rev. 3

This errata describes corrections to the *MPC8245 Integrated Processor Reference Manual*, Revision 3. Unless noted otherwise, listed changes to the reference manual that refer to the MPC8245 also apply to the MPC8241. For convenience, the section number and page number of the errata item in the reference manual are provided. Items in bold are new since the last revision of this document.

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Section, Page No.	Changes
4.1.3.1, 4-3	In Table 4-1, "Configuration Registers Accessible from the Processor Core," for PCI status register, add additional reset value of 0x0020 (post-R1.4).
4.1.3.1, 4-6	In Figure 4-1, "Processor Accessible Configuration Space," for offset address hexadecimal E0, replace the reserved register at offset 0xE3 with DLL tap count register.
4.3.2, 4-18	In Table 4-18, "Power Management Configuration Register 2—0x72," modify the first sentence of the field description of DLL_EXTEND (bit 7) to say, "This bit can be used to shift the lock-range of the DLL by half of an SDRAM clock cycle."
5.4.2.3, 5-22	Replace information regarding AN1767 with AN2129, as follows: "*Instruction and Data Cache Locking on the e300 Processor Core* application note (order number: AN2129)."
6.2.3, 6-14	In Table 6-9, "SDRAM System Configurations," change entry for "in-line RMW parity enabled" to "INLINE_WR_EN = 0 due to Chip Errata #17."
6.3.4.2, 6-57	Replace Figure 6-41, "8-Bit ROM/Flash Interface—Single-Byte Read Timing," with the following figure:
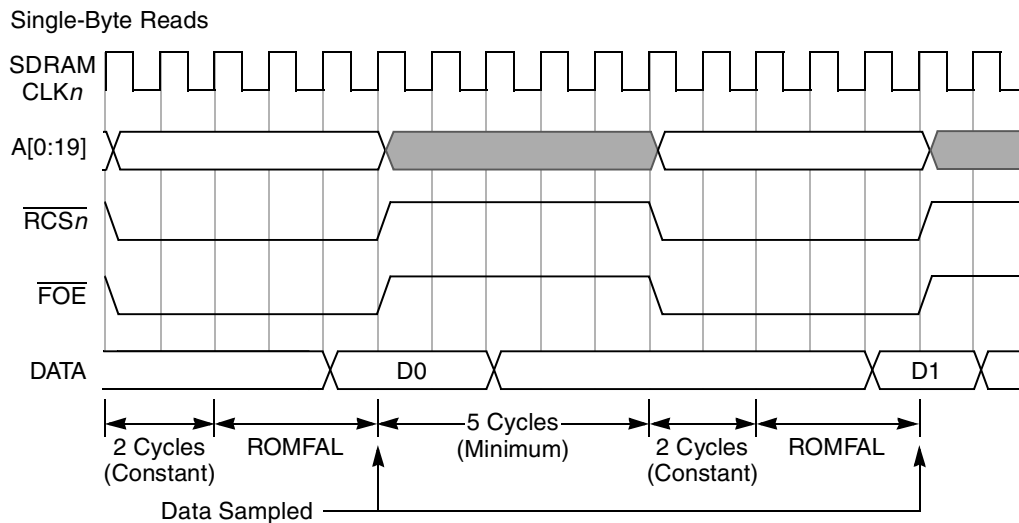
Figure 6-41. 8-Bit ROM/Flash Interface—Single-Byte Read Timing
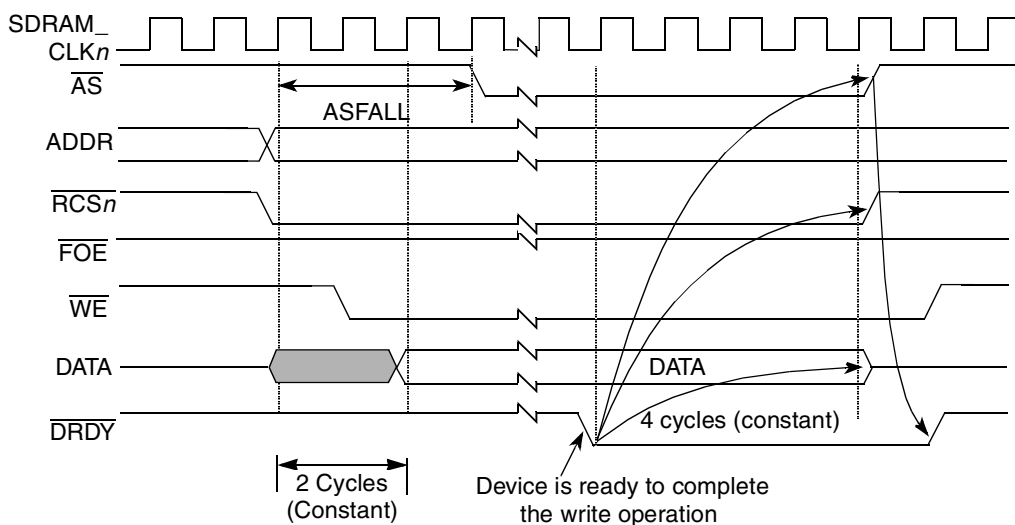
6.3.5.4, 6-64   Replace Figure 6-49, "Port X Handshake Mode Read Timing," with the following figure:
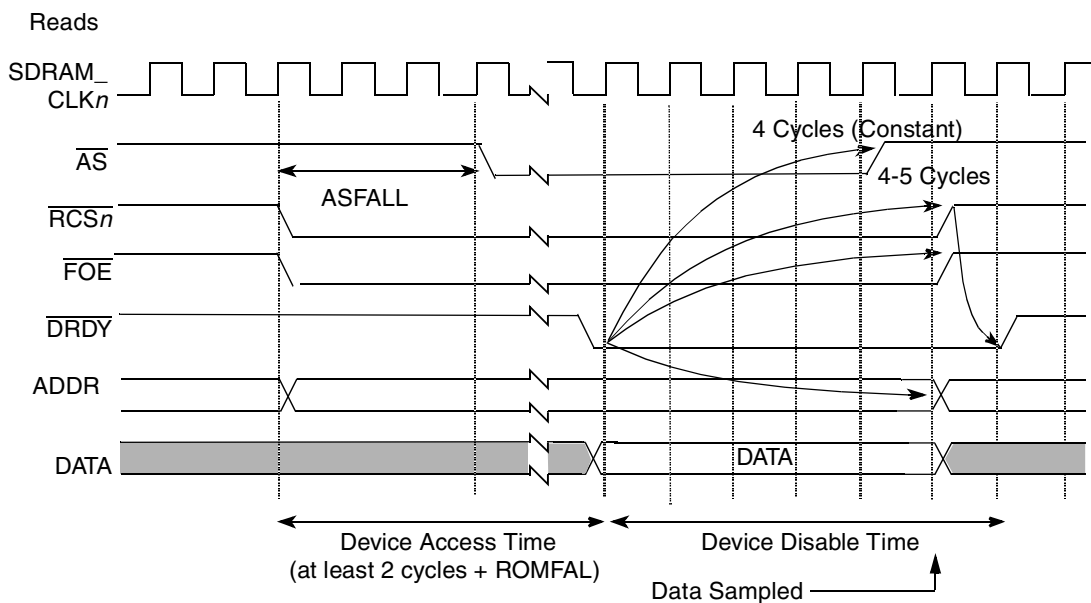
Figure 6-49. Port X Handshake Mode Read Timing

6.3.5.4, 6-65   Replace Figure 6-50, "Port X Handshake Mode Write Timing," with the following figure:

Figure 6-50. Port X Handshake Mode Write Timing

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