Preliminary Information

MPC180 HWRM/D

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MPC180
Hardware Reference Manual

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This document describes how to design a system with the MPC180 and PowerQUICC™ and PowerQUICC II™ family of communication processors. It covers the following topics:

1 Overview

The MPC180 is designed to work with Motorola's PowerQUICC family of processors. The MPC180 interfaces gluelessly to both the PowerQUICC and PowerQUICC II, accelerating the performance of computationally-intensive security functions, such as key generation and exchange, authentication, and bulk encryption. Support for 66MHz bus frequencies enables maximum utilization of the MPC8260 local bus as well as enhanced versions of the MPC8xx system bus.

The MPC180 is optimized to quickly process all the algorithms associated with IPSec, WTLS/WAP, SSL/TLS, and IKE, including the following:

- RSA
- RSA signature
- Diffie-Hellman
- Elliptic Curve Cryptography
- DES
- 3DES
- SHA-1
- MD4
- MD5
- Arc Four (compatible with RSA's RC4 algorithm)

The MPC180 works in load/store, memory-mapped systems. An external processor may execute application code from its ROM and RAM, using RAM and optional nonvolatile memory (such as EEPROM) for storing data. The MPC180 resides in the processor's memory map; therefore, an application requiring cryptographic functions simply writes to and reads from the appropriate memory mapped location of the MPC180.

As shown in Figure 1 and Figure 2, the MPC180 interfaces to the MPC8xx system bus or to the local bus of the MPC8260.

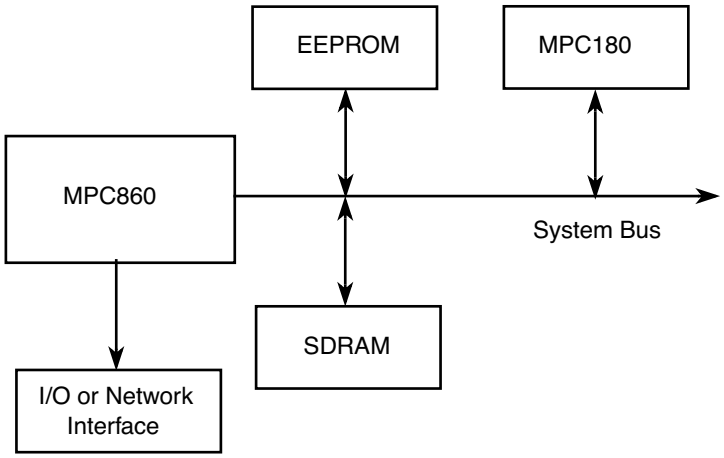


Figure 1. MPC850/MPC860 System Example

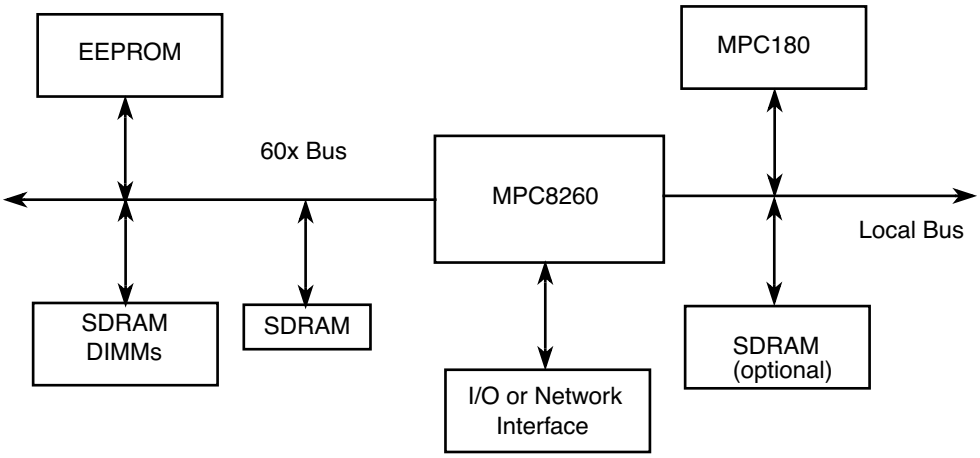


Figure 2. MPC8260 System Example

2 Features

The major features of the MPC180 are as follows:

- Public key/ asymmetric key
  - RSA
    - Programmable field size of up to 2048 bits
- Elliptic curve cryptography
  - F_2m and F(p) modes
  - Programmable field size of up to 511 bits
- DES
  - ECB (Electronic Code Book)
  - CBC (Cipher Block Chaining)
- 3DES
  - Two-key (K1 = K3) or three-key (K1, K2, K3) Triple-DES.
- Arc Four Stream Cipher
  - key lengths of 40–128 bits
- Authentication
  - MD4—hashed message of 128 bits
  - MD5—hashed message of 128 bits
  - SHA-1—hashed message of 160 bits
- Random Number Generator
- Glueless MPC8xx/82xx interface—up to 66 MHz
- DMA hardware handshaking signals
- 4-Kbit input and output FIFOs
- 1.8-V Vdd, 3.3 V I/O
- 100-pin LQFP package

3 Pin Assignments

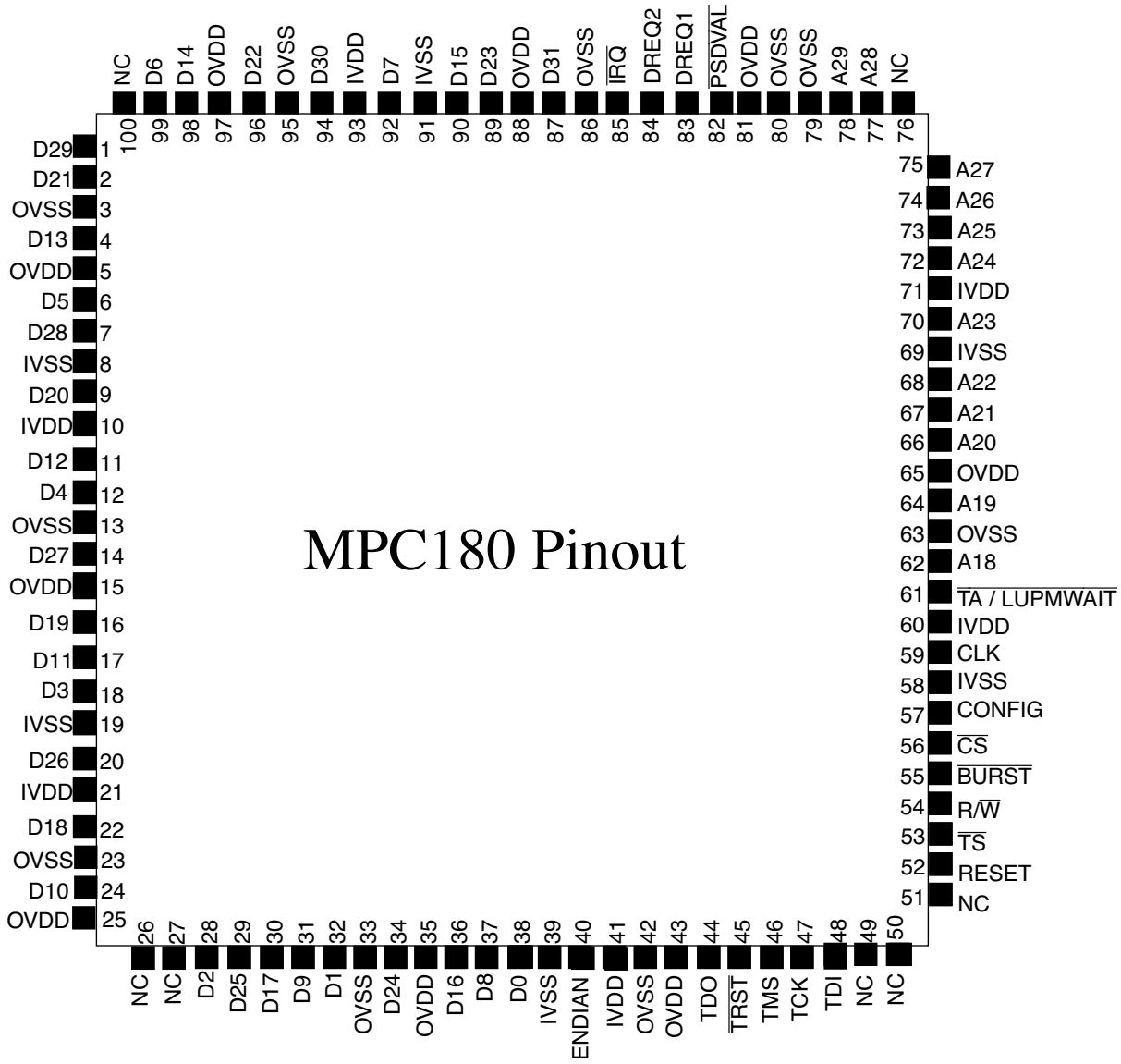


Figure 3. MPC180 Pin Diagram

4 Signal Descriptions

Table 1. Pin Descriptions

Signal name	Pin locations	Signal type	Description
Signal pins			
A[18:29]	62, 64, 66, 67, 68, 70, 72–75, 77, 78	I	Address—address bus from the processor core. These bits are decoded in the MPC180 to produce the individual module select lines to the execution units. Note that the processor address bus might be 32 bits wide, while the MPC180 address bus is only 12 bits wide. msb = bit 0 lsb = bit 31
D[0:31]	38, 32, 28, 18, 12, 6, 99, 92, 37, 31, 24, 17, 11, 4, 98, 90, 36, 30, 22, 16, 9, 2, 96, 89, 34, 29, 20, 14, 7, 1, 94, 87	I/O	Data—bidirectional data bus. This bus is connected directly to the processor core. msb = bit 0 lsb = bit 31
$\overline{CS}$	56	I	Chip Select. Active low signal that indicates when a data transfer is intended for the MPC180.
R/$\overline{W}$	54	I	Read/Write. Read/write line 1 read cycle 0 write cycle
$\overline{BURST}$	55	I	Burst Transaction. Active low signal used in the 8260 interface that indicates when the current read/write is a burst transfer.
$\overline{TS}$	53	I	Transfer Start. Transfer start pin for control port. This signal is asserted by the 850/860 to indicate the start of a bus cycle that transfers data to or from the MPC180. This is used by the MPC180 along with $\overline{CS}$, R/$\overline{W}$, and A to begin a transfer.
$\overline{PSDVAL}$	82	I	Data valid. This active low signal is ignored when CONFIG=0 (MPC860 Mode), but is active in MPC8260 Mode. The assertion of $\overline{PSDVAL}$ indicates that a data beat is valid on the data bus.
$\overline{TA}$ / LUPMWAIT	61	O	Transfer Acknowledge. This active low signal is used in 860 mode and is asserted by the MPC180 when a successful read or write has occurred. Local UPM wait. This active high signal is used in 8260 mode and is asserted to indicate the number of wait states for a transaction.
Miscellaneous pins			
$\overline{RESET}$	52	I	Reset. Asynchronous reset signal for initializing the chip to a known state. It is highly recommended that this signal be connected to a dual hardware/software reset function. Thus, the system designer can reset the MPC180 chip with optimal flexibility.
CONFIG	57	I	Configuration. Input that indicates whether the interface is to an MPC860 or MPC8260 1 8260 interface 0 860 interface

Table 1. Pin Descriptions (continued)

Signal name	Pin locations	Signal type	Description
ENDIAN	40	I	Endian. Active high for big endian mode. Low for little endian mode 1 big endian 0 little endian
$\overline{\text{IRQ}}$	85	O	Interrupt Request. Interrupt line that signifies that one or more execution units modules has asserted its $\overline{\text{IRQ}}$ hardware interrupt.
NC	26, 27, 49, 50, 51, 76, 100	—	No connection to the pin
DMA Hardware Handshake pins			
$\overline{\text{DREQ1}}$	83	O	DMA Request 1. Active high signal which indicates that either the input or output buffer is requesting data transfer by the host or DMA controller. $\overline{\text{DREQ1}}$ and $\overline{\text{DREQ2}}$ are each programmable to refer to the MPC180 chip input buffer or output buffer. This signal is designed to interoperate with a PowerQUICC IDMA channel.
$\overline{\text{DREQ2}}$	84	O	DMA request 2. Active high signal which indicates that either the input or output buffer is requesting data transfer by the host or DMA controller. $\overline{\text{DREQ1}}$ and $\overline{\text{DREQ2}}$ are each programmable to refer to the MPC180 Chip input buffer or output buffer. This signal is designed to interoperate with a PowerQUICC IDMA channel.
Clock			
CLK	59	I	Master clock input
Test			
TCK	47	I	JTAG test clock If JTAG is NOT used, this pin should be tied to OVSS
TDI	48	I	JTAG test data input If JTAG is NOT used, this pin should be tied to OVDD
TDO	44	I	JTAG test data output If JTAG is NOT used, this pin should be NC
TMS	46	I	JTAG test mode select If JTAG is NOT used, this pin should be tied to OVDD
$\overline{\text{TRST}}$	45	I	JTAG test reset If JTAG is NOT used, this pin should be tied to OVSS
Power and Ground			
IVDD	10, 21, 41, 60, 71, 93	I	+1.8 Volts (power pins for core logic)
OVDD	5, 15, 25, 35, 43, 65, 81, 88, 97	I	+3.3 Volts (Power pins for I/O pads)
OVSS	3, 13, 23, 33, 42, 63, 79, 80, 86, 95	I	0 Volts (Ground)
IVSS	8, 19, 39, 58, 69, 91	I	0 Volts (Ground)

5 Pin Connections

Table 2. Pin Connections

Signal name	Pin locations	Signal type	MPC860 / MPC850 connection	MPC860 / MPC850 design note	MPC8260 connection	MPC8260 design note
Signal pins						
A[18:29]	62, 64, 66, 67, 68, 70, 72–75, 77, 78	I	A[18:29]	1	L_A[18:29]	1
D[0:31]	1, 2, 4, 6, 7, 9, 11, 12, 14, 16-18, 20, 22, 24, 28–32, 34, 36, 37, 38, 87, 89, 90, 92, 94, 96, 98, 99	I/O	D[0:31]	1	LCL_D[0:31]	1
$\overline{CS}$	56	I	$\overline{CSx}$	2, 3	$\overline{CSx}$	1, 3
R/$\overline{W}$	54	I	R/$\overline{W}$	2	LWR	1
$\overline{BURST}$	55	I	OVDD (+3.3V)	—	LGPLx	1, 3
$\overline{TS}$	53	I	$\overline{TS}$	1	OVDD (+3.3V)	—
$\overline{PSDVAL}$	82	I	OVDD (+3.3V)	—	LGPLx	1, 3
$\overline{TA}$ / LUPMWAIT	61	O	$\overline{TA}$	2	LUPWAIT	4
Miscellaneous pins						
$\overline{RESET}$	52	I	Application Specific	1, 5	Application Specific	1, 5
CONFIG	57	I	VSS (0V)	—	OVDD (+3.3V)	—
ENDIAN	40	I	GPL_xx	1, 3, 6	LGPLx	1, 3, 6
$\overline{IRQ}$	85	O	$\overline{IRQx}$	1, 3	$\overline{IRQx}$	1, 3
NC	26, 27, 49, 50, 51,76, 100	—	NC	—	NC	—
DMA Hardware Handshake pins						
$\overline{DREQ1}$	83	O	NC	—	PA0 / PC0	3
$\overline{DREQ2}$	84	O	NC	—	PA5 / PC1	3
Clock						
CLK	59	I	Application Specific	5	Application Specific	5
Test						
TCK	47	I	Application Specific	5	Application Specific	5
TDI	48	I	Application Specific	5	Application Specific	5
TDO	44	I	Application Specific	5	Application Specific	5
TMS	46	I	Application Specific	5	Application Specific	5
$\overline{TRST}$	45	I	Application Specific	5	Application Specific	5
Power and Ground						

Table 2. Pin Connections (continued)

Signal name	Pin locations	Signal type	MPC860 / MPC850 connection	MPC860 / MPC850 design note	MPC8260 connection	MPC8260 design note
IVDD	10, 21, 41, 60, 71, 93	I	+1.8 Volts	—	+1.8 Volts	—
OVDD	5, 15, 25, 35, 43, 65, 81, 88, 97	I	+3.3 Volts	—	+3.3 Volts	—
OVSS	3, 13, 23, 33, 42, 63, 79, 80, 86, 95	I	0 Volts (Ground)	—	0 Volts (Ground)	—
IVSS	8, 19, 39, 58, 69, 91	I	0 Volts (Ground)	—	0 Volts (Ground)	—

1 It is recommended that this pin be tied to OVDD using a 10kΩ resistor.
2 It is recommended that this pin be tied to OVDD using a 1kΩ resistor.
3 Multiple system resources are available for certain signals ($\overline{CS}$, GPLs, $\overline{IRQ}$, and so on). Exact configuration depends on system configuration.
4 It is recommended that this pin be tied to VSS (ground) using a 10kΩ resistor.
5 Application-specific implementation determines exact pin-to-pin configuration of certain signals ($\overline{Reset}$, JTAG, Clk).
6 The endian pin should ideally be connected to a general purpose line to dynamically switch between big and little endian under program control. If a general purpose line is unavailable, another option is to tie the pin to OVDD and perform byte swapping in software which will result in some performance degredation.

6 Electrical and Thermal Characteristics

6.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings [1, 2]

Characteristic	Name	Absolute Min	Absolute Max	Unit
Power supply voltage—Core	V_{DD}	-0.3	+1.95	Volts
Power supply voltage—I/O	V_{DD}	-0.3	+3.6	Volts
Storage temperature	—	-55	+150	°C
Lead temperature (for 10 seconds)	—	—	+300	°C
Static input pin voltage	—	-0.3	+3.6	Volts
Input current to guarantee latch-up can not occur	—	—	+-50	mA
Operating Temperature	T_A	0	+70	°C

1 Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2 This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

6.2 Package Thermal Characteristics

Table 4. Package Thermal Characteristics

Rating		Symbol	Max	Unit
Junction to ambient [1, 2](@200lfm)	Single–layer board Four–layer board	R	40 25	°C/W
Junction to board [3] (bottom)		R	17	°C/W
Junction to case [4] (top)		R	9	°C/W

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, board population, and board thermal resistance.
2 Per SEMI G38-87.
3 Indicates the average thermal resistance between the die and the printed circuit board.
4 Indicates the average thermal resistance between the die and the case top surface via the cold plate method (MIL SPEC-883 Method 1012.1).

6.3 Operating Conditions and DC Electrical Characteristics

Table 5. Electrical Operating Conditions

Characteristic	Name	Min	Typ	Max	Units	Notes
Power supply voltage—Core	V_{DD}	1.65	—	1.95	V_{DC}	
Power supply voltage—I/O	V_{DDQ}	3.0	—	3.6	V_{DC}	
Input low voltage (Vdd = Min)	V_{il}	-0.5	—	$V_{DDQ}/2$	V_{DC}	1
Input high voltage (Vdd = Max)	V_{ih}	2.0	—	—	V_{DC}	2
AC supply current	I_{DD}	—	—	290	mA	
Standby supply current	I_{SS}	—	—	130	mA	
Input leakage current @ $V_{DD} \geq V_{in} \geq V_{SS}$	I_{leak}	—	—	+- 5	μA	
Three-state input current @ $V_{DD} \geq V_{in} \geq V_{SS}$	I_z	—	—	10	μA	
Output high voltage (I_{oh} = -400 μA)	V_{oh}	2.4	—	—	V_{DC}	
Output low voltage I_{ol} = 3.2 mA, C_L = 35 pF ($\overline{IRQ}$) I_{ol} = 3.2 mA, C_L = 50 pF (D[0:31])	V_{ol}	—	—	0.4	V_{DC}	
Output HIgh Current	I_{oh}	10mA		—	mA	3
Output Low Current	I_{ol}	—		-10mA	mA	
Input buffer/pad capacitance	C_{in}	—	5	—	pF	
Input/output buffer/pad capacitance	C_{io}	—	5	—	pF	

1 Undershoot: Vil <= 1.5v for t < 20% t_{KHKH}
2 Overshoot: Vih <=V_{DD} +1.0v (Not to exceed 4.6v) for t < 20% t_{KHKH}.
3 The $\overline{TA}$ signal has a +- 15mA output drive strength.

6.4 AC Electrical Characteristics

Table 6. AC Electrical Characteristics [1]

Condition	Name	Min	Max	Units
Input Signals				
Clock Frequency	F_{clock}	—	66	Mhz
Clock Cycle Time	t_{KHKH}	—	15.15	nS
Address Setup	t_{AVKH}	1.0	—	nS
Address Hold	t_{KHAX}	0.6	—	nS
Data Setup	t_{DVKH}	1.0	—	nS
Data Hold	t_{KHDX}	0.5	—	nS
$\overline{TS}$ Setup	t_{TSVKH}	1.0	—	nS
$\overline{TS}$ Hold	t_{KHTSX}	0.5	—	nS
R/$\overline{W}$ Setup	t_{WVKH}	1.0	—	nS
R/$\overline{W}$ Hold	t_{KHWX}	0.5	—	nS
$\overline{BURST}$ Setup	t_{BVKH}	1.0	—	nS
$\overline{BURST}$ Hold	t_{KHBX}	0.3	—	nS
$\overline{CS}$ Setup	t_{CVKH}	1.1	—	nS
$\overline{CS}$ Hold	t_{KHCX}	0.4	—	nS
$\overline{PSDVAL}$ Setup	t_{PVKH}	1.0	—	nS
$\overline{PSDVAL}$ Hold	t_{KHPX}	0.3	—	nS
ENDIAN Setup	t_{EVKH}	1.0	—	nS
ENDIAN Hold	t_{KHEX}	0.3	—	nS
Output Signals				
Clock High to Data Valid	t_{KHQV}	—	8.9	nS
Clock High to Data Hold	t_{KHQX}	3.7	—	nS
Clock High to DREQx Valid	t_{KHDV}	—	8.3	nS
Clock High to DREQx Hold	t_{KHDX}	3.4	—	nS
Clock High to $\overline{IRQ}$ Valid	t_{KHIV}	—	8.5	nS
Clock High to $\overline{IRQ}$ Hold	t_{KHIX}	3.4	—	nS
Clock High to $\overline{TA}$ Valid	t_{KHTAV}	—	8.5	nS
Clock High to $\overline{TA}$ Hold	t_{KHTAX}	3.5	—	nS

[1] All timings are valid for 50 MHz as well.

6.5 IEEE 1149.1 AC Timing Specification

Table 7. JTAG AC Timing Specifications

Condition	Name	Min	Max	Units
TCK Cycle Time	t_{THTH}	60	—	nS
TCK Clock High Time	t_{TH}	25	—	nS
TCK Clock Low Time	t_{TL}	25	—	nS
TDO Access Time	t_{TLQV}	1	10	nS
$\overline{TRST}$ pulse width	t_{TSRT}	40	—	nS
Setup TImes Capture TDI TMS	t_{CS} t_{DVTH} t_{MVTH}	5 5 5	—	nS
Hold TImes Capture TDI TMS	t_{CH} t_{THDX} t_{THMX}	13 14 14	—	nS

6.6 MPC180 and MPC8xx Timing Diagrams

A write cycle is defined as a transfer of data to the MPC180 from the host processor and a read cycle is defined as a transfer of data from the MPC180 to the host processor. The processor initiates all data transfers, acting as the bus master, and the MPC180 always acts as the bus slave. Data transfer is synchronous to the main clock input and begins on the rising edge that $\overline{TS}$ and $\overline{CS}$ are asserted. At this time, the R/$\overline{W}$ signal indicates whether the transaction is a read or a write and the address bus is decoded to select the destination within the MPC180. The MPC180 holds the $\overline{TA}$ line high to signal the appropriate number of wait states and then drives the signal low to indicate that valid data is on the bus. If $\overline{TA}$ is driven low during a read cycle, the MPC180 is driving valid data; if $\overline{TA}$ is driven low during a write cycle, the MPC180 has captured valid data.

Figure 4 shows a typical read cycle when the MPC180 interfaces to an MPC850 or MPC860 and Figure 5 shows a typical write cycle for the same interface.

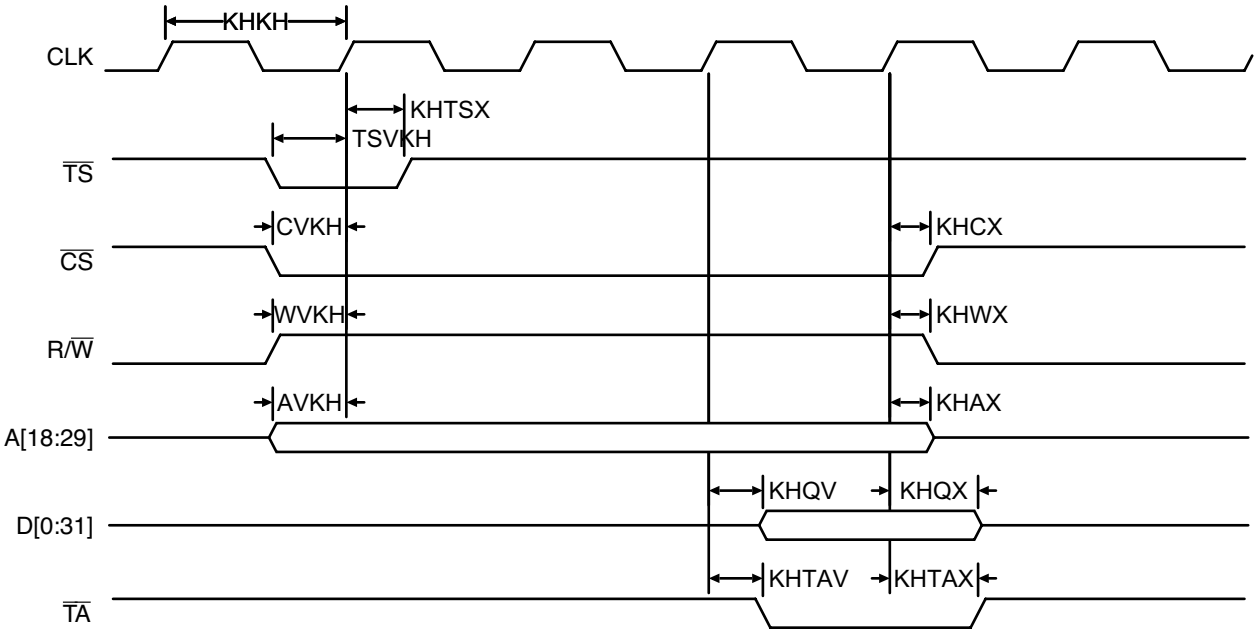


Figure 4. MPC8xx Interface: Read Cycle

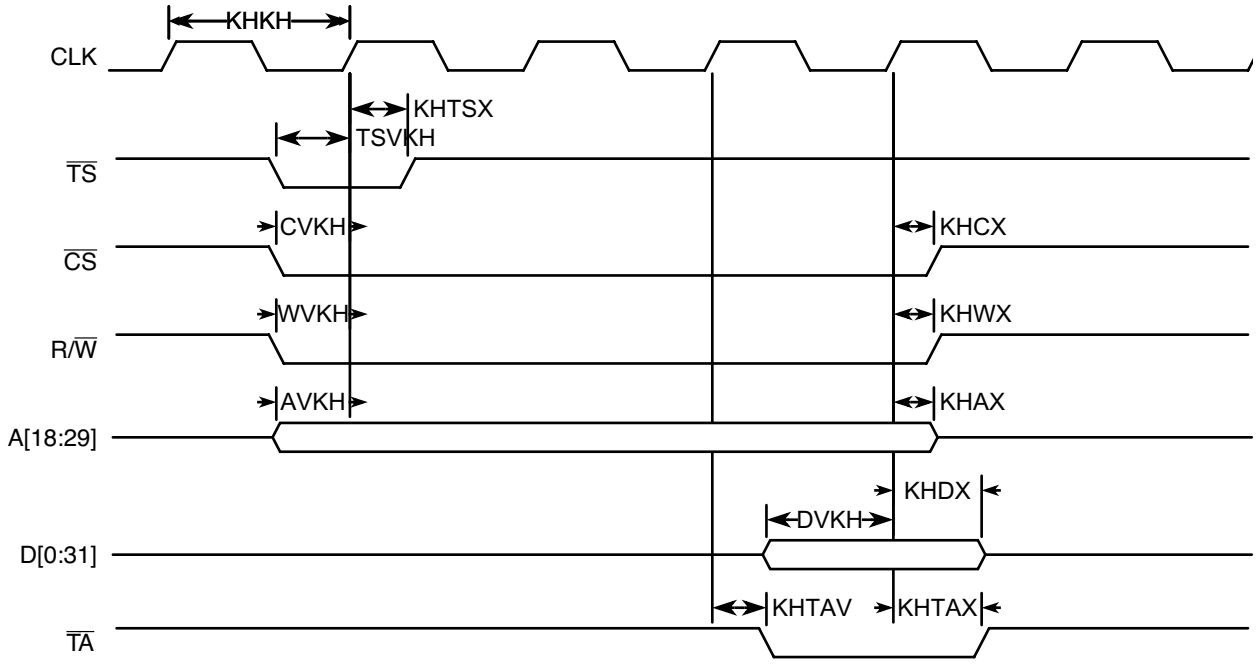


Figure 5. MPC8xx Interface: Write Cycle

6.7 MPC180 and MPC8260 Timing Diagrams

A write cycle is defined as a transfer of data to the MPC180 from the host processor and a read cycle is defined as a transfer of data from the MPC180 to the host processor. The processor initiates all data transfers, acting as the bus master, and the MPC180 always acts as the bus slave. Data transfer is synchronous to the main clock input and begins on the rising edge on which $\overline{CS}$ is asserted. At this time, the R/$\overline{W}$ signal

indicates whether the transaction is a read or a write and the address bus is decoded to select the destination within the MPC180. The $\overline{\text{LUMPWAIT}}$ signal drives high after the MPC180 is selected to signal to the MPC8260 the number of wait states that the device needs to perform a given read or write. When the $\overline{\text{LUMPWAIT}}$ signal is deasserted, the processor completes the transaction. The MPC8260 then drives the $\overline{\text{PSDVAL}}$ signal low to indicate that valid data is on the bus. If $\overline{\text{PSDVAL}}$ is driven low during a read cycle, the MPC180 is driving valid data; if $\overline{\text{PSDVAL}}$ is driven low during a write cycle, the MPC180 has captured valid data

Figure 6 shows a typical read cycle when the MPC180 is interfacing to an MPC8260 and Figure 7 shows a typical write cycle.

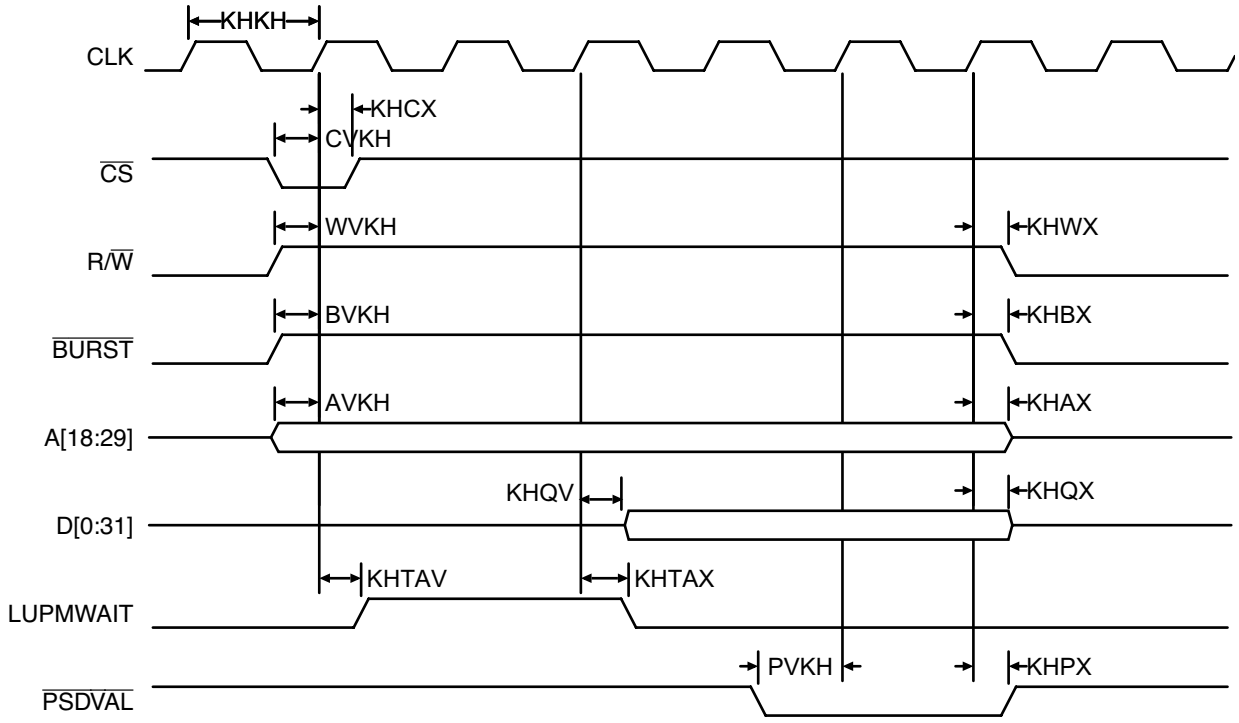


Figure 6. MPC8260 Interface: Read Cycle

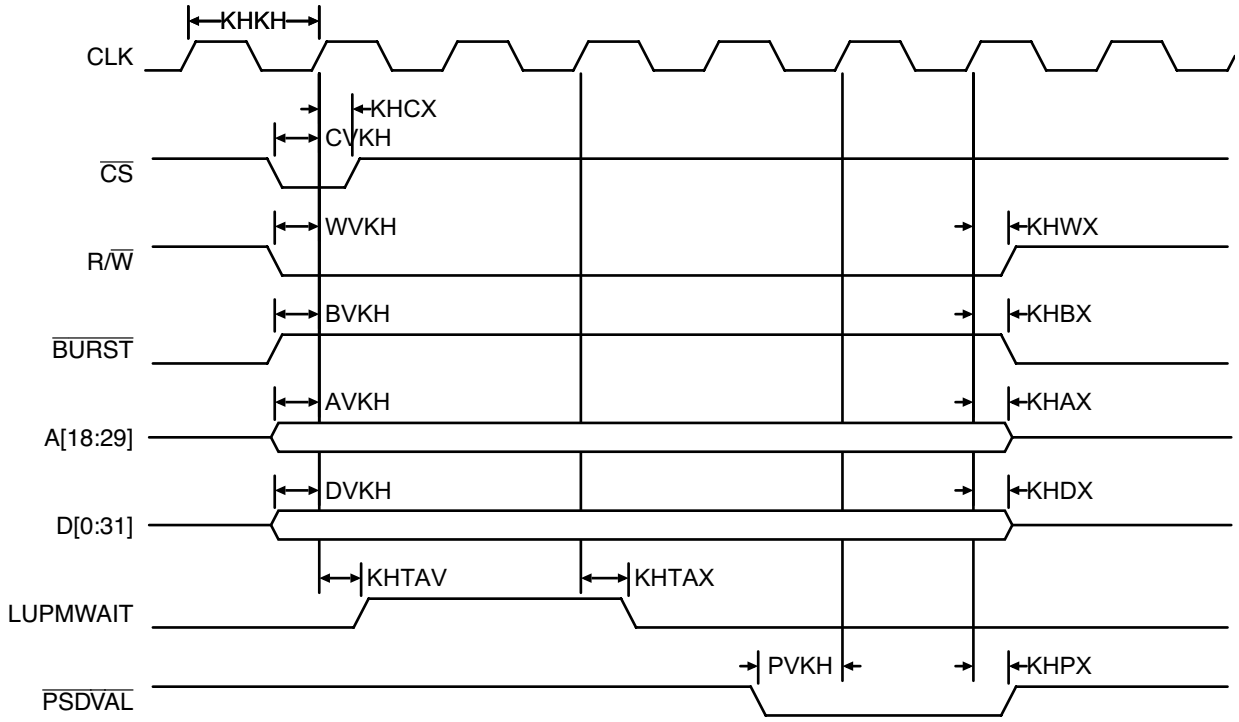


Figure 7. MPC8260 Interface: Write Cycle

When the destination or source of a transaction is the input or output FIFO or a register that resides in the external bus interface (ID, IMASK, IBCTL, IBCNT, OBCTL, OBCNT—see the *MPC180 User's Manual* for further details), the transaction occurs in a deterministic number of cycles. Therefore, the $\overline{\text{PSDVAL}}$ signal need not be asserted to indicate during which cycle valid data is on the bus.

Figure 8 shows a typical read cycle when the MPC180 is interfacing to an MPC8260 and Figure 9 shows a typical write cycle to the external bus interface.

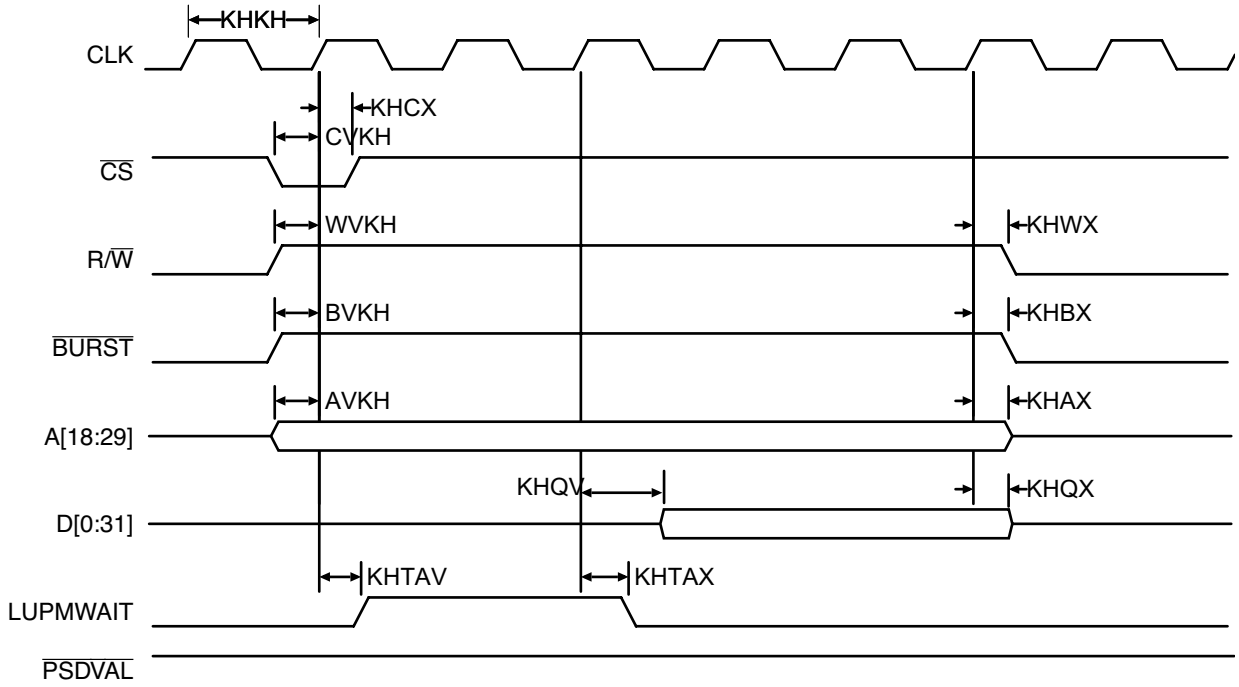


Figure 8. MPC8260 Interface: Read Cycle when Transaction Involves External Bus Interface or Output FIFO

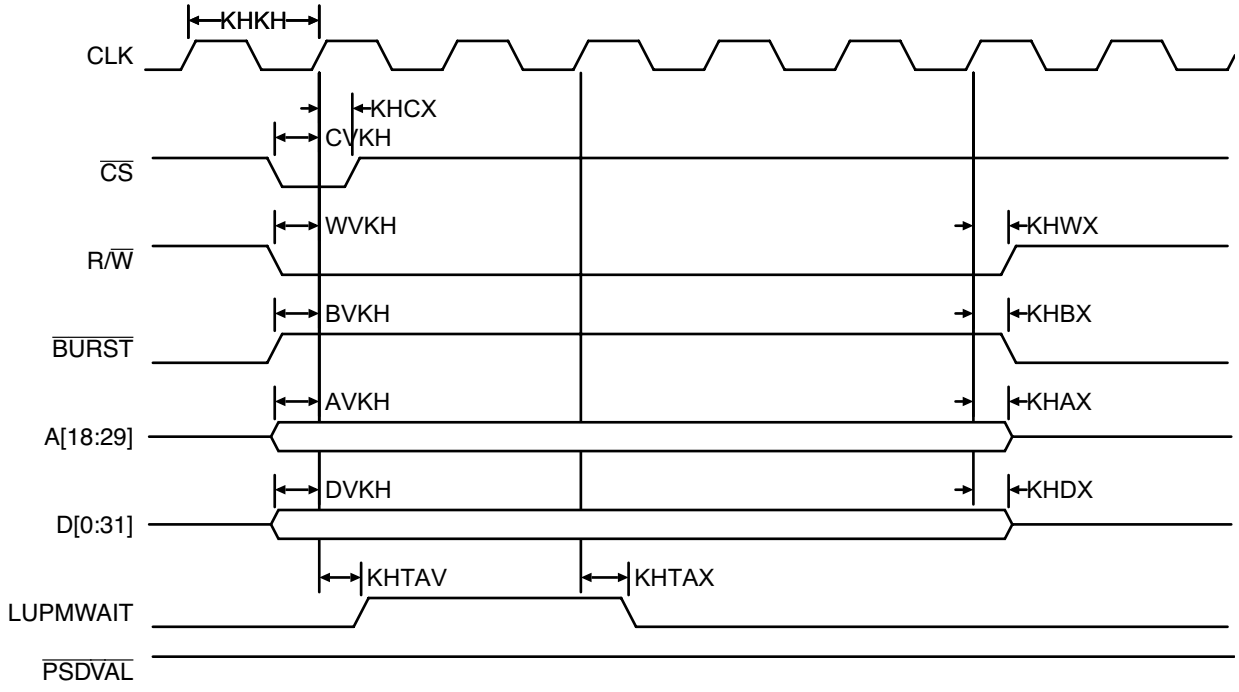


Figure 9. MPC8260 Interface: Write Cycle when Transaction Involves External Bus Interface or Input FIFO

The only supported burst transfers are to the input buffer or from the output buffer when in 8260 mode. The first data transaction in 8260 mode requires two wait states and each subsequent data transaction requires zero wait states.

Figure 10 shows a typical read cycle from the output FIFO and Figure 11 shows a typical write cycle to the input FIFO.

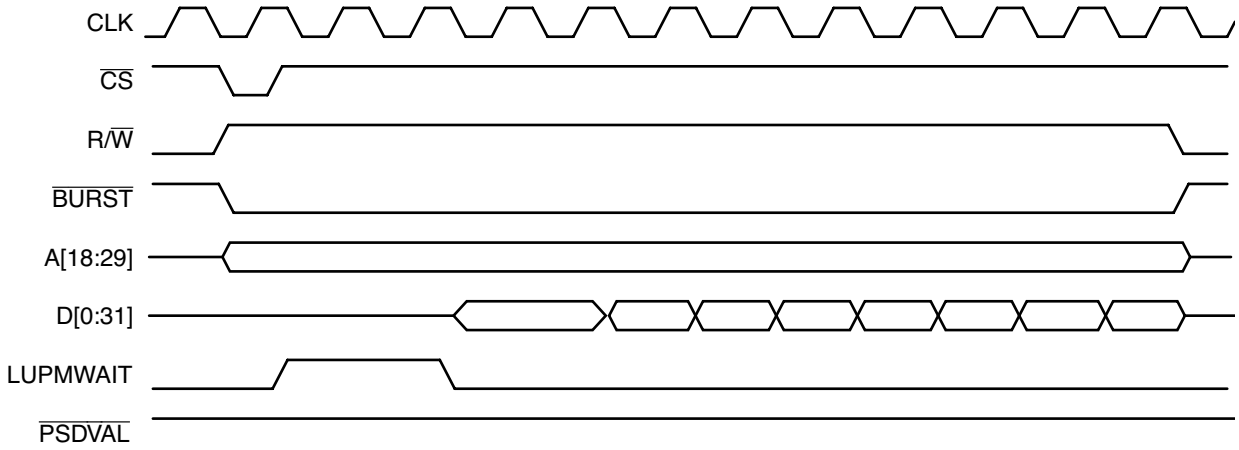


Figure 10. MPC8260 Interface: Burst Read Cycle from Output FIFO

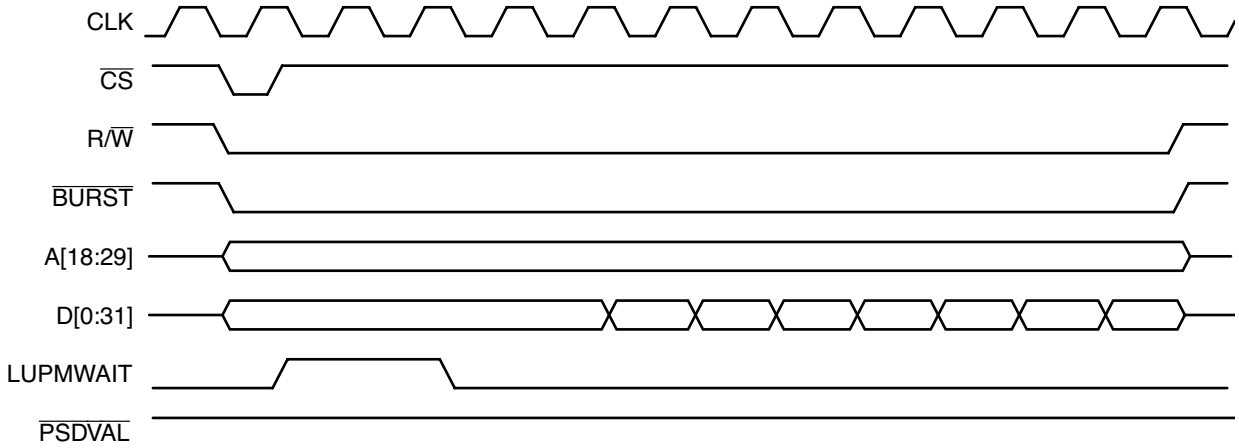


Figure 11. MPC8260 Interface: Burst Write Cycle to Input FIFO

7 System Timing Analysis

This section will perform a detailed timing analysis of the MPC180 interface to the MPC850, MPC860 and MPC8260 communication processors. It will describe the methodology to calculate the setup and hold margin, the relative timings of both the MPC180 and the host processor, how to intentionally add clock offset between the processor and MPC180 to maximize timing margin, and finally, how to translate the timing margin into the minimum and maximum length restrictions for use by the PCB layout engineer.

Table 8 defines the terms used in the timing analysis.

Table 8. Timing Analysis Terms

Term	Definition
t_{period}	Clock period.
$t_{is\_receiver}$	Input setup to the receiver. Time that an input must be valid before the rising edge of the clock; specified by the receiver of the signal.
$t_{ih\_receiver}$	Input hold to the receiver. Time that an input must remain valid after the rising edge of the clock; specified by the receiver of the signal.
t_{oh_source}	Output hold from the source. Time from the rising edge of the clock until the output becomes invalid; specified by the source of the output signal.
t_{oa_source}	Maximum output access time from the source. Time from the rising edge of the clock until the last output becomes valid; specified by the source of the output signal.
t_{clock_skew}	Clock skew (part to part and cycle to cycle)
t_{clock_offset}	An intentional offset between the MPC180 clock and the host processor clock. As a convention, the offset will be positive (+) if the MPC180 clock arrives in time before the host processor clock and negative (-) if the MPC180 clock arrives in time after the host processor clock.

7.1 Setup Time Margin and Maximum Propagation delays

The setup margin is defined as the difference between the clock period and the total setup time as shown below:

$$t_{setup\_margin} = t_{period} - t_{setup\_total} \quad \text{(EQ 1)}$$

The total setup time is the accumulation of the driver's clock to output valid, the receiver's input setup, the clock skew and clock jitter and the offset between the processor and MPC180 clock:

$$t_{setup\_total} = t_{oa\_source} + t_{is\_receiver} + t_{clock\_skew} + t_{clock\_offset}^{1} \quad \text{(EQ 2)}$$

By substituting EQ2 into EQ1, the formula for calculating the setup margin becomes:

$$t_{setup\_margin} = t_{period} - t_{oa\_source} - t_{is\_receiver} - t_{clock\_skew} - t_{clock\_offset}^{1} \quad \text{(EQ 3)}$$

NOTE

The value of the clock offset will be positive when the MPC180 is the receiver and the offset will have a net subtractive effect. The value of the clock offset will be negative when the host processor is the receiver and the offset will have a net additive effect.

7.2 Hold Time Margin and Minimum Propagation Delays

The hold time margin can be defined as the driver's output hold time, minus the receiver's input hold, minus the clock skew and clock jitter, plus the offset between the processor and MPC180 clock:

$$t_{hold\_margin} = t_{oh\_source} - t_{ih\_receiver} - t_{clock\_skew} + t_{clock\_offset}^{1} \quad \text{(EQ 4)}$$

An important note is that the hold time margin is not directly frequency dependent. It will only vary with frequency if the hold time specifications for either the driver or receiver vary with frequency.

NOTE

The value of the clock offset will be positive when the MPC180 is the receiver and the offset will have a net additive effect. The value of the clock offset will be negative when the host processor is the receiver and the offset will have a net subtractive effect.

7.3 Timing Analysis with the MPC850, MPC860 and MPC8260 without Clock Offset

We will now use the equations that were previously developed to compute the setup and hold time margin for both read and write cycles without clock offsets. The analysis will first look at the MPC180 input setup margin, then the MPC180 input hold margin. Next, the host processor input setup margin will be calculated and finally the hold time to the host processor will be computed. The following assumptions will be used throughout this portion of the analysis:

t_{period} = 20 nS for the MPC850 and MPC860

t_{period} = 15 nS for the MPC8260

t_{clock_skew} = 0.9 nS

t_{clock_offset} = 0.0 nS for this portion of the analysis

The input setup time margin is calculated for when the host processor is the source of the signal and the MPC180 is the receiver. The results are shown in Table 9.

Table 9. MPC180 Input Setup Margin without Clock Offset

Signal	MPC180 Input Setup Time	MCP850 Access Time	MPC860 Access Time	MPC8260 Access Time	Input Setup Margin with MPC850	Input Setup Margin with MPC860	Input Setup Margin with MPC8260
A[18:29]	1.0 nS	12.0 nS	11.75 nS	8.0 nS	6.1 nS	6.35 nS	5.1 nS
ENDIAN	1.0 nS	12.0 nS	11.75 nS	8.0 nS	6.1 nS	6.35 nS	5.1 nS
D[0:31]	1.0 nS	12.0 nS	11.75 nS	8.0 nS	6.1 nS	6.35 nS	5.1 nS
CS	1.1 nS	13.0 nS	11.75 nS	6.0 nS	5.0 nS	6.25 nS	7.0 nS
R/$\overline{W}$	1.0 nS	12.0 nS	11.75 nS	6.0 nS	6.1 nS	6.35 nS	7.1 nS
BURST	1.0 nS	—	—	6.0 nS	—	—	7.1 nS
TS	1.0 nS	12.25 nS	11.0 nS	—	5.85 nS	7.1 nS	—
PSDVAL	1.0 nS	—	—	10.0 nS	—	—	3.1 nS

The input hold time margin will now be calculated for when the host processor is the source of the signal and the MPC180 is the receiver. The results are shown in Table 10.

Table 10. MPC180 Input Hold Margin without Clock Offset

Signal	MPC180 Input Hold Time	MCP850 Hold Time	MPC860 Hold Time	MPC8260 Hold Time	Input Hold Margin with MPC850	Input Hold Margin with MPC860	Input Hold Margin with MPC8260
A[18:29]	0.6 nS	5.0 nS	5.0 nS	1.0 nS	3.5 nS	3.5 nS	-0.5 nS
ENDIAN	0.3 nS	5.0 nS	5.0 nS	1.0 nS	3.8 nS	3.8 nS	-0.2 nS
D[0:31]	0.5 nS	5.0 nS	5.0 nS	1.0 nS	3.6 nS	3.6 nS	-0.4 nS
CS	0.4 nS	2.0 nS	2.0 nS	1.0 nS	0.7 nS	0.7 nS	-0.3 nS
R/$\overline{W}$	0.5 nS	5.0 nS	5.0 nS	1.0 nS	3.6 nS	3.6 nS	-0.4 nS
BURST	0.3 nS	—	—	1.0 nS	—	—	-0.2 nS
TS	0.5 nS	5.0 nS	5.0 nS	—	3.6 nS	3.6 nS	—
PSDVAL	0.3 nS	—	—	1.0 nS	—	—	-0.2 nS

The input setup time margin will now be calculated for when the MPC180 is the source of the signal and the host processor is the receiver. The results are shown in Table 11.

Table 11. Processor Input Setup Margin without Clock Offset

Signal	MPC180 Access Time	MCP850 Input Setup Time	MPC860 Input Setup Time	MPC8260 Input Setup Time	Input Setup Margin to MPC850	Input Setup Margin to MPC860	Input Setup Margin to MPC8260
D[0:31]	8.9 nS	6.0 nS	6.0 nS	5.0 nS	4.2 nS	4.2 nS	0.2 nS
$\overline{TA}$ / LUPMWAIT	8.5 nS	9.75 nS	9.75 nS	6.0 nS	0.85 nS	0.85 nS	-0.4 nS
DREQx	8.3 nS	—	—	5.0 nS	—	—	0.8 nS

The input hold time margin will now be calculated for when the host processor is the source of the signal and the MPC180 is the receiver. The results are shown in Table 12.

Table 12. Processor Input Hold Margin without Clock Offset

Signal	MPC180 Input Hold Time	MCP850 Hold Time	MPC860 Hold Time	MPC8260 Hold Time	Input Hold Margin to MPC850	Input Hold Margin to MPC860	Input Hold Margin to MPC8260
D[0:31]	3.7 nS	1.0 nS	1.0 nS	1.0 nS	1.8 nS	1.8 nS	1.8 nS
$\overline{TA}$ / LUPMWAIT	3.5 nS	1.0 nS	1.0 nS	1.0 nS	1.6 nS	1.6 nS	1.6 nS
DREQx	3.4 nS	—	—	1.0 nS	—	—	1.5 nS

7.4 Timing Analysis with the MPC850, MPC860 and MPC8260 with Clock Offsets

As we can see from the timing margin analysis without clock offsets, the results show that some clock offset is recommended for improved margin, particularly in the interface to the MPC8260. There are two areas where additional margin is needed:

1. Input hold margin to the MPC180. This can be optimized by having the MPC180 clock arrive before the host processor clock.
2. Input setup margin to the host processor. This can be optimized by having the MPC180 clock arrive before the host processor clock.

Since the two areas that need optimization require the clock offset to be adjusted in the same direction, the PCB designer can intentionally offset the clock that drives the host processor in reference to the clock that drives the MPC180 to maximize the timing margins. By adjusting the offset such that the clock to the MPC180 arrives in time before the clock to the host processor, the input setup margin to the MPC180 can be exchanged for input hold margin to the MPC180 and input hold margin to the host processor can be exchanged for input setup margin to the host processor.

In choosing the appropriate clock offset, the PCB designers should make appropriate trade-offs in order to balance the margin. In this analysis, 0.55 nS was chosen for the MPC850 and MPC860 in order to balance the Data hold to the host processor with the $\overline{CS}$ hold to the MPC180. An offset of 1.0 nS was chosen for the MPC8260 interface to balance the Data input hold to the MPC180 with the $\overline{TA}$ output hold to the MPC8260.

The following clock offsets will now be taken into consideration and the timing analysis will be repeated:

t_{clock_offset} = 055 nS for the MPC850 and MPC860 (The clock that drives the MPC180 should arrive 0.55 nS in absolute time before the clock that drives the MPC850 and MPC860)

t_{clock_offset} = 1.0 nS for the MPC8260 (The clock that drives the MPC180 should arrive 1.0 nS in absolute time before the clock that drives the MPC8260)

The input setup time margin is calculated for when the host processor is the source of the signal and the MPC180 is the receiver. The results are shown in Table 13.

Table 13. MPC180 Input Setup Margin with Clock Offset

Signal	MPC180 Input Setup Time	MCP850 Access Time	MPC860 Access Time	MPC8260 Access Time	Input Setup Margin with MPC850	Input Setup Margin with MPC860	Input Setup Margin with MPC8260
A[18:29]	1.0 nS	12.0 nS	11.75 nS	8.0 nS	5.55 nS	5.8 nS	4.1 nS
ENDIAN	1.0 nS	12.0 nS	11.75 nS	8.0 nS	5.55 nS	5.8 nS	4.1 nS
D[0:31]	1.0 nS	12.0 nS	11.75 nS	8.0 nS	5.55 nS	5.8 nS	4.1 nS
CS	1.1 nS	13.0 nS	11.75 nS	6.0 nS	4.45 nS	5.7 nS	6.0 nS
R/$\overline{W}$	1.0 nS	12.0 nS	11.75 nS	6.0 nS	5.55 nS	5.8 nS	6.1 nS
BURST	1.0 nS	—	—	6.0 nS	—	—	6.1 nS
TS	1.0 nS	12.25 nS	11.0 nS	—	5.3 nS	6.55 nS	—
PSDVAL	1.0 nS	—	—	10.0 nS	—	—	2.1 nS

The input hold time margin will now be calculated for when the host processor is the source of the signal and the MPC180 is the receiver. The results are shown in Table 14.

Table 14. MPC180 Input Hold Margin with Clock Offset

Signal	MPC180 Input Hold Time	MCP850 Hold Time	MPC860 Hold Time	MPC8260 Hold Time	Input Hold Margin with MPC850	Input Hold Margin with MPC860	Input Hold Margin with MPC8260
A[18:29]	0.6 nS	5.0 nS	5.0 nS	1.0 nS	4.05 nS	4.05 nS	0.5 nS
ENDIAN	0.3 nS	5.0 nS	5.0 nS	1.0 nS	4.35 nS	4.35 nS	0.8 nS
D[0:31]	0.5 nS	5.0 nS	5.0 nS	1.0 nS	4.15 nS	4.15 nS	0.6 nS
CS	0.4 nS	2.0 nS	2.0 nS	1.0 nS	1.25 nS	1.25 nS	0.7 nS
R/$\overline{W}$	0.5 nS	5.0 nS	5.0 nS	1.0 nS	4.15 nS	4.15 nS	0.6 nS
BURST	0.3 nS	—	—	1.0 nS	—	—	0.8 nS
TS	0.5 nS	5.0 nS	5.0 nS	—	4.15 nS	4.15 nS	—
PSDVAL	0.3 nS	—	—	1.0 nS	—	—	0.8 nS

The input setup time margin will now be calculated for when the MPC180 is the source of the signal and the host processor is the receiver. The results are shown in Table 15.

Table 15. Processor Input Setup Margin with Clock Offset

Signal	MPC180 Access Time	MCP850 Input Setup Time	MPC860 Input Setup Time	MPC8260 Input Setup Time	Input Setup Margin to MPC850	Input Setup Margin to MPC860	Input Setup Margin to MPC8260
D[0:31]	8.9 nS	6.0 nS	6.0 nS	5.0 nS	4.75 nS	4.75 nS	1.2 nS
$\overline{TA}$ / LUPMWAIT	8.5 nS	9.75 nS	9.75 nS	6.0 nS	1.4 nS	1.4 nS	0.6 nS
DREQx	8.3 nS	—	—	5.0 nS	—	—	1.8 nS

The input hold time margin will now be calculated for when the host processor is the source of the signal and the MPC180 is the receiver. The results are shown in Table 16.

Table 16. Processor Input Hold Margin with Clock Offset

Signal	MPC180 Input Hold Time	MCP850 Hold Time	MPC860 Hold Time	MPC8260 Hold Time	Input Hold Margin to MPC850	Input Hold Margin to MPC860	Input Hold Margin to MPC8260
D[0:31]	3.7 nS	1.0 nS	1.0 nS	1.0 nS	1.25 nS	1.25 nS	0.8 nS
$\overline{TA}$ / LUPMWAIT	3.5 nS	1.0 nS	1.0 nS	1.0 nS	1.05 nS	1.05 nS	0.6 nS
DREQx	3.4 nS	—	—	1.0 nS	—	—	0.5 nS

7.5 Calculating PCB Trace Lengths

For all previous analysis, units have been measured in nS. Once the final allowable timing margins are known, these times must be converted to length rules for PCB routing. Due to the various factors affecting the actual propagation delays on a PCB it is highly recommended that a SPICE simulator is used to convert the time delays to length restrictions. However, for those without access to such simulators or for rough

estimates, equations using 'rules of thumb' can be used. For this example, we will use the following equation to estimate the length conversions:

$$\text{Length} = (\text{Calculated Delay} +/- \text{Load Delay}) / \text{PCB Propagation Speed} \quad \text{(EQ 5)}$$

$$\text{Load delay} = (\#\text{ of loads}) \times (\text{capacitance per load (pF)}) \times (\text{capacitive delay (ps/pF)}) \quad \text{(EQ 6)}$$

All of the timings used in this analysis are based upon the source driving a 50pF load. If the load that the source drives is greater than 50pF, the additional delay associated with the extra capacitive load should be subtracted from the calculated delay. If the load that the source drives is less than 50pF, the additional margin can be added to the calculated delay. The analysis below assumes that the PCB propagation speed is 180 psec/inch. An approximate capacitive delay value to use is 35ps/pF.

The input setup margin is now translated into a maximum length restriction. The value is calculated for when the host processor is the source of the signal and the MPC180 is the receiver. The value physically represents the maximum distance in inches that should exist between the output pin of the host processor to the input pin of the MPC180. The results are shown in Table 17.

Table 17. Maximum PCB Length Restriction

Signal	Input Setup Length with MPC850	Input Setup Length with MPC860	Input Setup Length with MPC8260
A[18:29]	30.8 in	32.2 in	22.7 in
ENDIAN	30.8 in	32.2 in	22.7 in
D[0:31]	30.8 in	32.2 in	22.7 in
CS	24.7 in	31.6 in	33.3 in
R/$\overline{W}$	30.8 in	32.2 in	22.7 in
BURST	—	—	33.8 in
TS	29.4 in	36.3 in	—
PSDVAL	—	—	11.6 in

From the previous section where the timing analysis with clock offset was performed, the results show that all of the input hold margins are positive. The input hold margin defines the minimum propagation length. Positive hold margin translates into negative minimum propagation delay. Since no trace can have negative propagation delay time, the actual hold margin will be the previously calculated hold margin plus the trace delay of the shortest signal in a given signal group. In this analysis, the minimum PCB length restrictions are all zero and are shown in Table 18 for completeness.

Table 18. Minimum PCB Length Restriction

Signal	Input Hold Margin with MPC850	Input Hold Margin with MPC860	Input Hold Margin with MPC8260
A[18:29]	0.0 in	0.0 in	0.0 in
ENDIAN	0.0 in	0.0 in	0.0 in
D[0:31]	0.0 in	0.0 in	0.0 in
CS	0.0 in	0.0 in	0.0 in

Table 18. Minimum PCB Length Restriction (continued)

Signal	Input Hold Margin with MPC850	Input Hold Margin with MPC860	Input Hold Margin with MPC8260
R/$\overline{W}$	0.0 in	0.0 in	0.0 in
BURST	—	—	0.0 in
$\overline{TA}$ / LUPMWAIT	0.0 in	0.0 in	—
PSDVAL	—	—	0.0 in

The input setup margin is now translated into a maximum length restriction. The value is calculated for when the MPC180 is the source of the signal and the host processor is the receiver. The value physically represents the maximum distance in inches that should exist between the output pin of the MPC180 to the input pin of the host processor. The results are shown in Table 19.

Table 19. Maximum PCB Length Restriction (50pF load)

Signal	Input Setup Margin to MPC850	Input Setup Margin to MPC860	Input Setup Margin to MPC8260
D[0:31]	26.3 in	26.3 in	6.6 in
$\overline{TA}$ / LUPMWAIT	7.7 in	7.7 in	3.3 in
DREQx	—	—	10.0 in

This analysis shows that the trace that should be most optimized is the $\overline{TA}$ path. One note is that this analysis assumes that all sources are driving a 50pF load. Load delay can have a significant impact on timing margin and length restrictions. If this analysis was to assume that the source was to drive a lighter load, the PCB designer would reclaim approximately 1.9 inches per 10pF of loading. The maximum PCB length restrictions are shown in Table 20for a 30pF environment for comparison.

Table 20. Maximum PCB Length Restriction (30pF load)

Signal	Input Setup Margin to MPC850	Input Setup Margin to MPC860	Input Setup Margin to MPC8260
D[0:31]	30.1 in	30.1 in	10.4 in
$\overline{TA}$ / LUPMWAIT	11.5 in	11.5 in	7.1 in
DREQx	—	—	13.8 in

From the previous section where the timing analysis with clock offset was performed, the results show that all of the input hold margins are positive. The input hold margin defines the minimum propagation length. Positive hold margin translates into negative minimum propagation delay. Since no trace can have negative propagation delay time, the actual hold margin will be the previously calculated hold margin plus the trace delay of the shortest signal in a given signal group. In this analysis, the minimum PCB length restrictions are all zero and are shown in Table 21 for completeness.

Table 21. Minimum PCB Length Restriction

Signal	Input Hold Margin to MPC850	Input Hold Margin to MPC860	Input Hold Margin to MPC8260
D[0:31]	0.0 in	0.0 in	0.0 in
$\overline{TA}$ / LUPMWAIT	0.0 in	0.0 in	0.0 in
DREQx	—	—	0.0 in

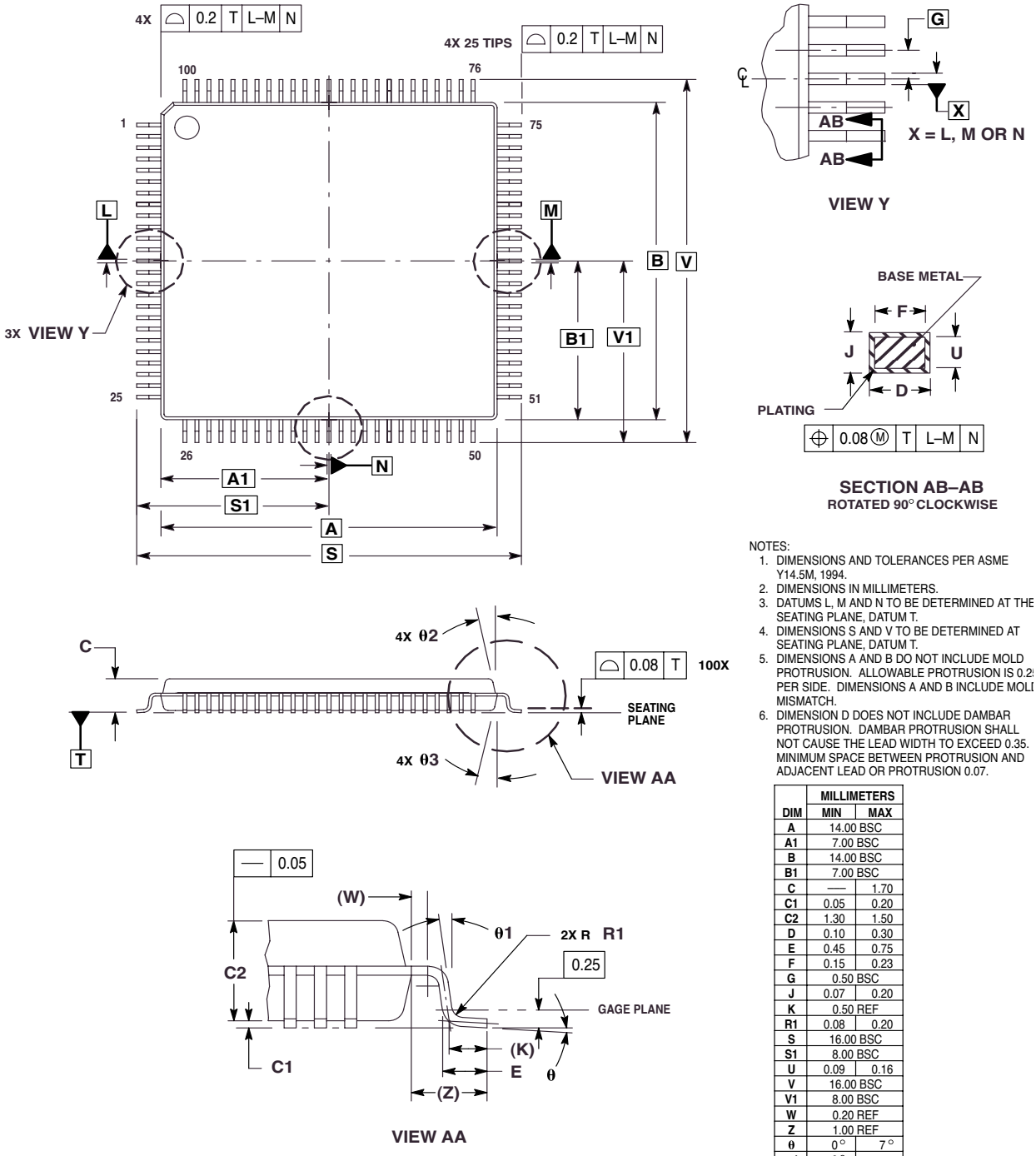
Once the PCB has been routed, the maximum lengths can be compared to the table to determine how much margin was realized. Remember that many factors will affect the conversion from time delay to length restrictions, especially loading and routing topology. Routing topology can also have a serious impact. Once again, due to the various factors affecting the actual propagation delays on a PCB it is highly recommended that a SPICE simulator is used to convert the time delays to length restrictions. This example assumes signals are routed in a manner that effectively achieves incident wave switching.

8 Decoupling Recommendations

It is recommended that decoupling capacitors should have a value of 0.01 μF or 0.1 μF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over using multiple values of capacitance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD and OVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100-330 μF (AVX TPS tantalum or Sanyo OSCON).

9 Package Description



NOTES:
1. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.2 PER SIDE. DIMENSIONS A AND B INCLUDE MOLI MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

	MILLIMETERS	
DIM	MIN	MAX
A	14.00 BSC	
A1	7.00 BSC	
B	14.00 BSC	
B1	7.00 BSC	
C	—	1.70
C1	0.05	0.20
C2	1.30	1.50
D	0.10	0.30
E	0.45	0.75
F	0.15	0.23
G	0.50 BSC	
J	0.07	0.20
K	0.50 REF	
R1	0.08	0.20
S	16.00 BSC	
S1	8.00 BSC	
U	0.09	0.16
V	16.00 BSC	
V1	8.00 BSC	
W	0.20 REF	
Z	1.00 REF	
θ	0°	7°
θ1	0°	—
θ2	12° REF	
θ3	12° REF	

Figure 12. MPC180 Case Outline Package Dimensions

10 Ordering Information

Figure 13 provides the Motorola part numbering nomenclature for the MPC180. Each part number contains a revision level. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

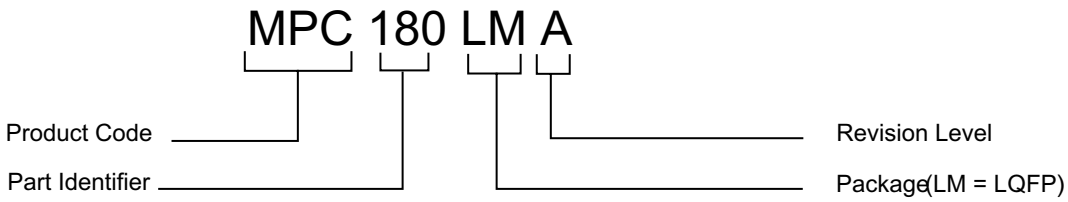


Figure 13. Motorola Part Number Key

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