MC68EN302

Errata and Added Information to

MC68EN302 Integrated Multiprotocol Processor with Ethernet Controller Reference Manual Rev 1

September 1, 1997

This document describes the latest information and changes to the first revision of the MC68EN302 Reference Manual.

Motorola MC68EN302 Design Advisory

The Seeq 80C26 Ethernet transceiver is not compatible with the 68EN302 microprocessor. Motorola does not recommend using the Seeq transceiver in designs with the 68EN302. All other known industry Ethernet transceivers are compatible with the 68EN302.

Section 2– Module Bus Controller

1. CSER Register

In Section 2.6, the CSER register FCE,DT[2:0] bits are only meaningful if EN8 is asserted and if the corresponding OR is programmed for an external DTACK. This "external" DTACK can then come either from the CSERx register logic (if EN8 bit is set) or from outside the chip (if EN8 is not set or if EN8 is set and DT[2:0] is programmed to 111). If EN8 is not asserted and the corresponding OR register is set for external DTACK, then the DTACK must be generated externally. If EN8 is set and the OR register is set for external DTACK then the FCE and DT[2:0] bits in the CSER register will control DTACK generation.

The CSPE (parity control) bit in the CSERx register operates independently of the EN8 bit. CS0 is a special case since it is used to select the boot ROM. Whether 8-bit mode is selected or not is determined during reset by the hardware by monitoring the BUSW pin.

2. PCSR Register Reset Value

In Section 2.7, the second sentence in the first paragraph states that the PSCR register is set to 0x0000 upon a hardware reset. This is correct for revision 0.1 (mask 1G97C); however, this register is reset to 0x000f upon hardware reset for revision A (mask H56B).

Section 3 – DRAM Control Module

1. External Bus Master Operation

In Section 3.6.3, the following paragraph should be added: The DRAM controller supports DRAM access by an external bus master. In this mode, the ADDR(23:0) bus is an input. Muxing of the address bus to the DRAM must take place externally under control of the AMUX pin. The AS, UDL, LDS and R/W pins are also inputs which are used by the DRAM controller logic to generate the AMUX, RAS, CAS and DRAMRW outputs.

Section 4 - Ethernet Controller

1. EMRBLR Register Description

In Section 4.1.3, add the following paragraph: To allow any frame to fit in a single buffer, the EMRBLR register should be programmed for 1520 bytes or larger, rather than 1518 bytes. In the case of excessive frame lengths (>1518 bytes) the receiver will truncate the frame at 1520 bytes.

2. Interrupt Vector Register (IVEC).

In Section 4.1.4 , for Rev 0.1 (mask 1G97C), the reset value should be $0000. The reset value shown, $000F, is correct for Rev. A (mask 1H56B).

Also in Section 4.1.4, the IVEC register diagram should have "VG" in bit 8 instead of "0". The Reserved field (immediately under the diagram) should be bits 15-9, not 15-8.

3. Ether Test Register (ETHER_TEST).

In Section 4.1.8, the ETHER_TEST register bits 15-12 are now used for a field called EN302_REV. For rev 0 (G97C) and rev A (h56b) EN302_REV = 0000. For rev B (h74p) EN302_REV = 0001.

Bits 11-8 are reserved (will return 0 if read). The function of bits 7-0 are unchanged.

Section 8 - Electrical Specifications

1. Add Section 8.1a, DC Electrical Characteristics

Characteristic		Symbol	Min	Max	Unit
Output High Voltage (I_{OH} = -1.0 mA)	TENA, TX, PARITY0/DISCPU, PARITY1/BUSW, PARITYE/THREES, TDO	V_{OH}	V_{DD}–1.0	—	V
Output Low Voltage (I_{OL} = 5.3 mA)	TENA, TX, PARITY0/DISCPU, PARITY1/BUSW, PARITYE/THREES, TDO	V_{OL}	—	0.5	V

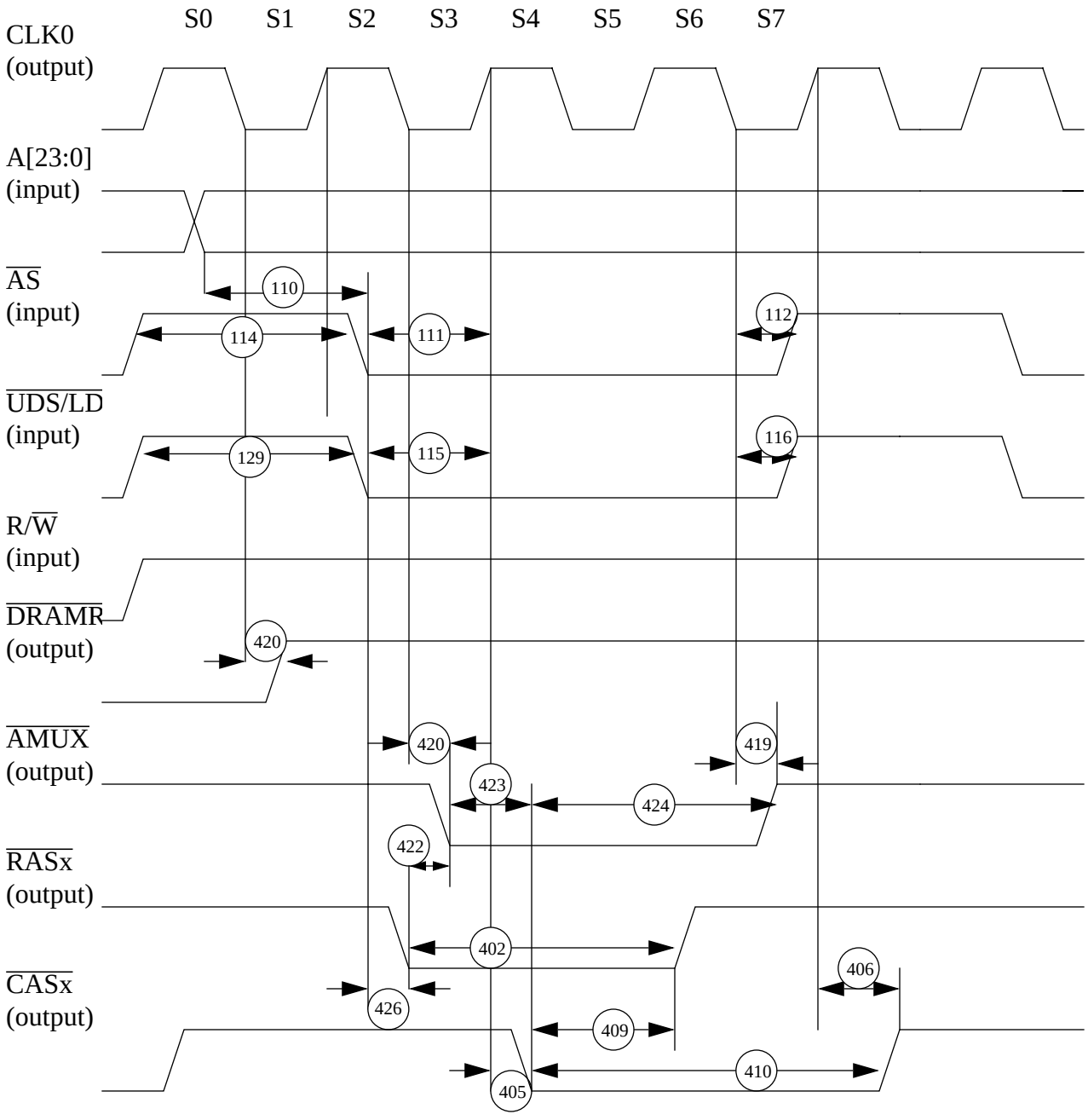

FIGURE 8-1B External Master DRAM READ CYCLE

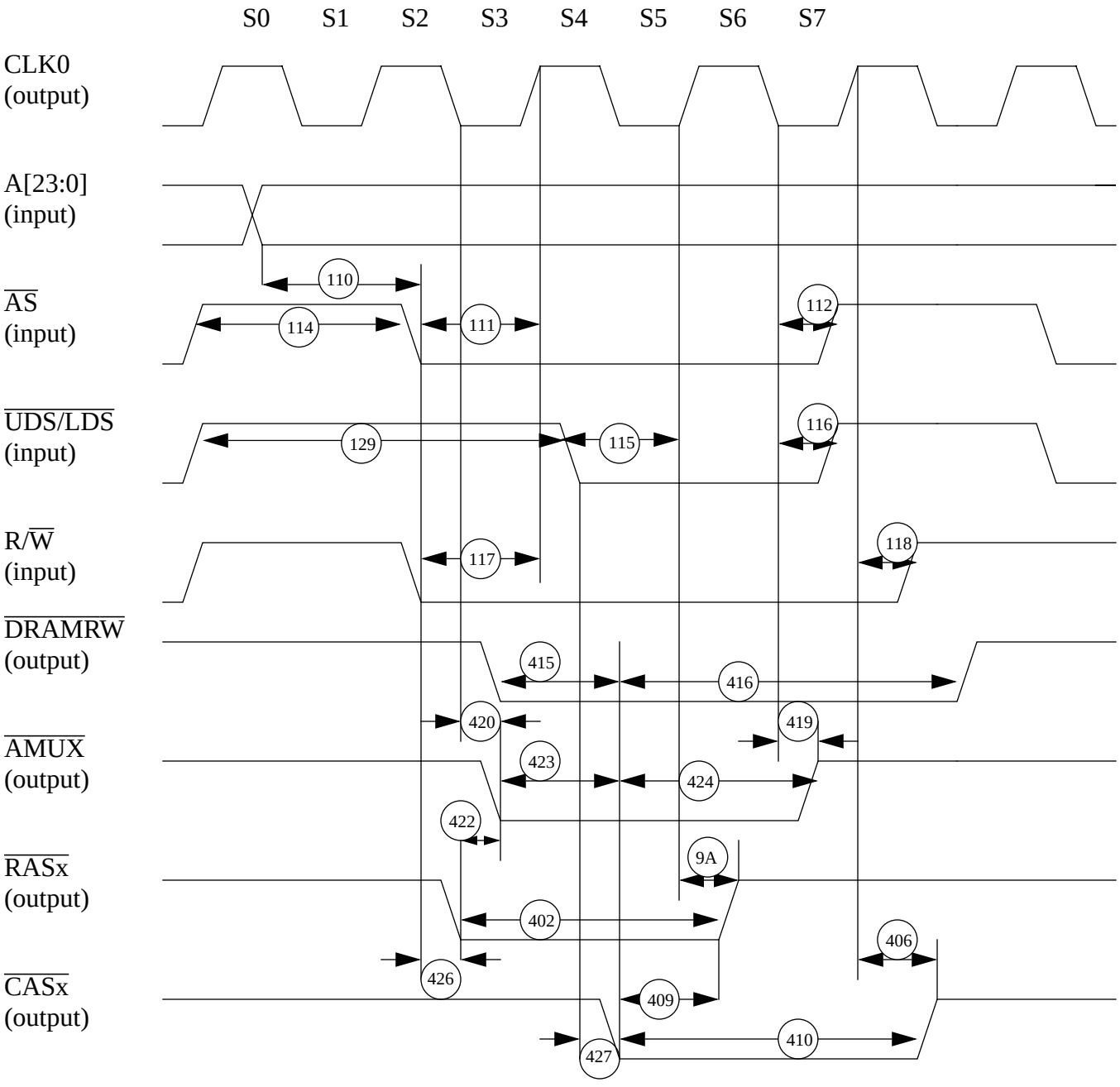

FIGURE 8-2B External Master DRAM Write Cycle

2. Changes to Existing 68302 Timing Specs

In Section 8.2 there should be three specs listed as changing on the EN302 from the 68302, specs 5a, 27, and 47. The changes are different for revision 0.1 and A, as shown below:

Rev. 0.1 (Mask 1G97C)

NUM	Characteristic		20MHz		25MHz		UNIT
		Symbol	Min	Max	Min	Max	
5a	EXTAL to CLKO Delay	tcd	2	12	2	12	ns
27	Data-in Valid to Clock Low(Setup Time on Read)	tdicl	10	-	10	-	ns
47	Asynchronous Input Setup Time	tasi	14	-	14	-	ns

Rev. A (Mask H56B)

NUM	Characteristic		20MHz		25MHz		UNIT
		Symbol	Min	Max	Min	Max	
5a	EXTAL to CLKO Delay	tcd	2	9	2	9	ns
27	Data-in Valid to Clock Low(Setup Time on Read)	tdicl	10	-	10	-	ns
47	Asynchronous Input Setup Time	tasi	12	-	12	-	ns

3. Additions to Table 8-1.

In Section 8.3, the following entries should be added (refer to Figures 8-1b and 8-2b):

NUM	Characteristic	20MHz		25MHz		UNIT
		Min	Max	Min	Max	
426	AS low to RASx low	-	25	-	20	ns
427	UDS (LDS) low to CASx low	-	22	-	18	ns

4. Ethernet Timing Specs (531, 532)

In Section 8.4, Table 8-2, the Ethernet Timing specs 531 and 532 should be changed to:

NUM	Characteristic	Min	Max	UNIT
531	TCLK low to TXD, TENA High Delay	0	15	ns
532	TCLK low to TXD, TENA Low Delay	0	15	ns

Note 1 from Table 8-2 is no longer needed.

As a result of the changes in specs 531 and 532, Figure 8-6 changes to the following:

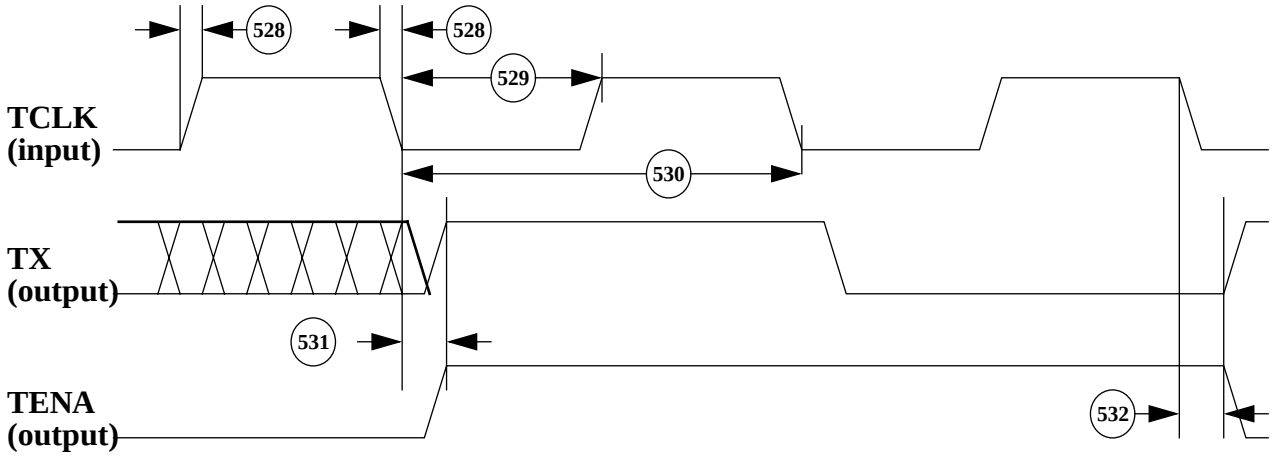

FIGURE 8-6 Ethernet Transmit Timing

4. Test Access Port Timing Diagram

In Section 8.5, Figure 8-10 should be replaced with the following figure:

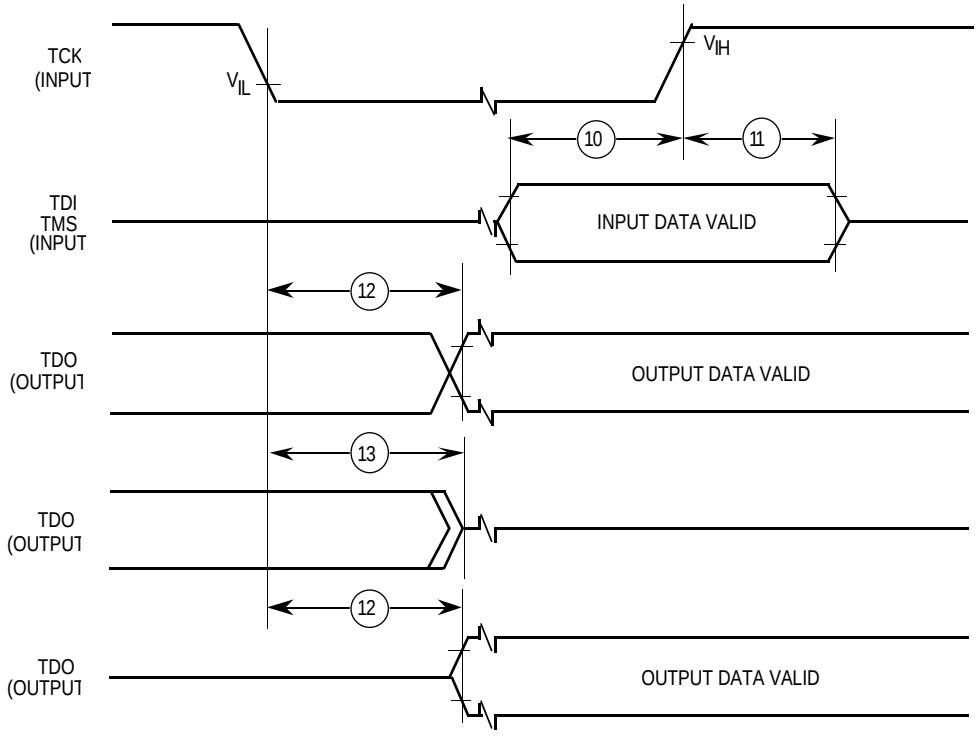

Figure 8-10. Test Access Port Timing Diagram.

Section 9 – Ordering and Mechanical Information

1. Typo

In Section 9.2.2, p. 9-5, dimension G inches version is incorrect; it should read “0.02 BSC” instead of “0.2 BSC.”

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