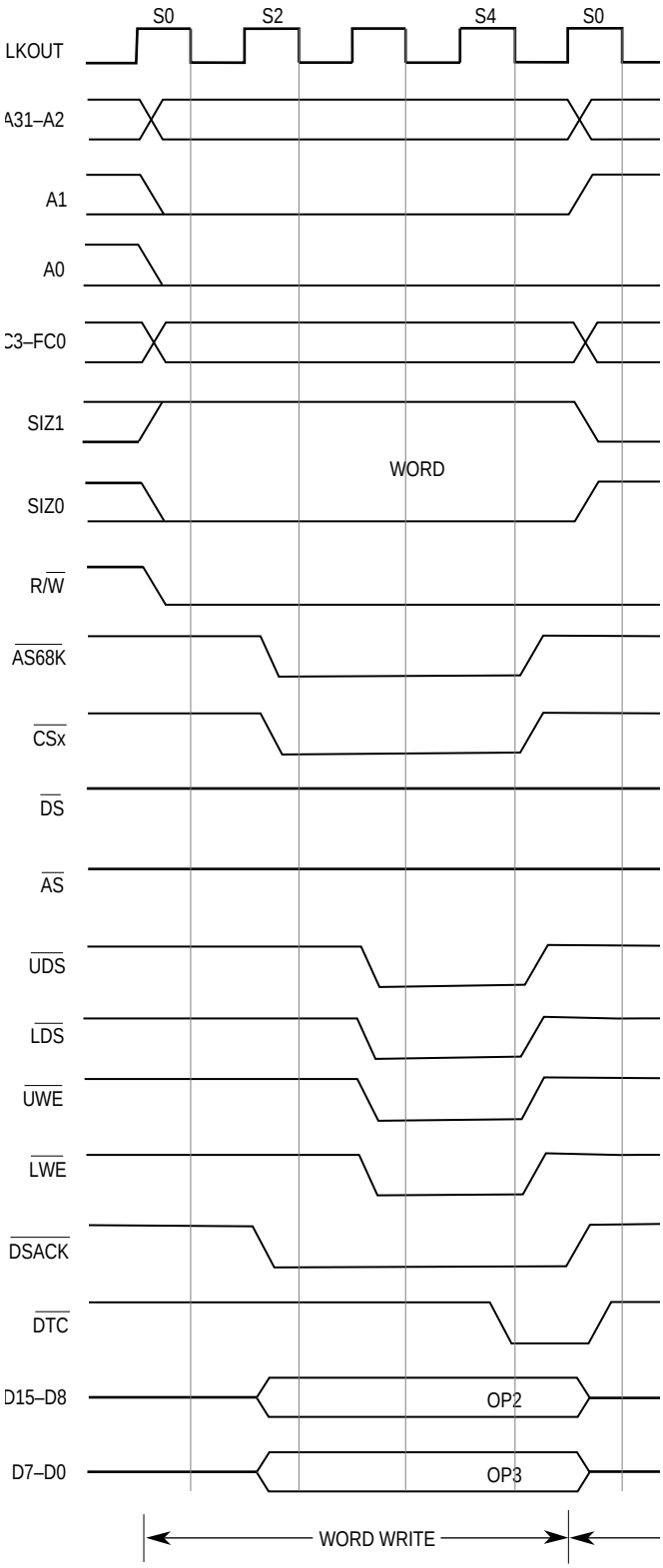

Figure 3-14. M68000 '

MOTOROLA

Microprocessor and Memory Technologies Group

ADDENDUM TO
MC68341 Integrated Pro

April 19, 1995

This addendum to the initial release of the MC68341 text, plus additional information not included in the or is maintained on the AESOP BBS, which can be r (512)891-3650. Configure modem for up to 14.4Kb should support VT100 emulation. Internet acce [129.38.233.1] or through the World Wide Web at ht

1. Signal Index

On page 2-4, Table 2-4, the QSPI serial clock QSCL 2-5, FC3/$\overline{\text{DTC}}$ is an output-only signal.

2. Operand Alignment

On page 3-9, last paragraph, change the first two li instructions) to be word-aligned. That is, word and lo Long-word operands do not have to be long-word al

3. $\overline{\text{WE}}$ on Fast Termination

On page 3-17, Figure 3-6, $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ do not as

4. Write Cycle Timing Waveforms

On page 3-25, the M68300 write cycle timing diagra $\overline{\text{LWE}}$. On page 3-28, the M68000 write cycle timing $\overline{\text{CSx}}$, $\overline{\text{UDS}}$/$\overline{\text{LDS}}$, and $\overline{\text{UWE}}$/$\overline{\text{LWE}}$. Replace these figu

5. Additional Note on MBAR Decod

Add to the CPU Space Cycles description on page 3 block from $3FF00-3FFFF to the SIM module. An in for any access to this range, but selection of specific

Accesses to the MBAR register at long word $3FF0 cycles. Users should directly access only the MBAR LPSTOP broadcast access to $3FFFE. The remainir should not be accessed.

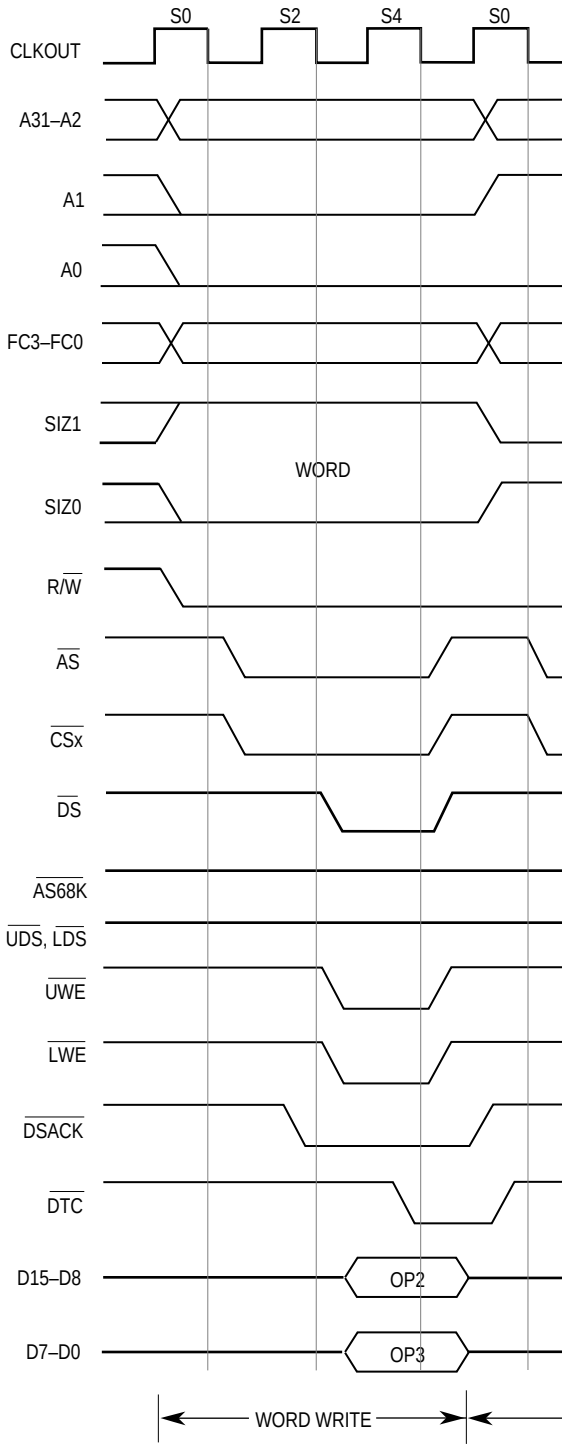

Figure 3-12. M68300

This document contains information on a product under development. Motor

Table 4-2. System Frequencies

Y	CLKOUT (kHz)				VCO (kHz)
	W = 0				W = 0
	Z = 0		Z = 1		Z = x
	X = 0	X = 1	X = 0	X = 1	X = x
0	16	33	131	262	524
1	33	66	262	524	1049
2	49	98	393	786	1573
3	66	131	524	1049	2097
4	82	164	655	1311	2621
5	98	197	786	1573	3146
6	115	229	918	1835	3670
7	131	262	1049	2097	4194
8	147	295	1180	2359	4719
9	164	328	1311	2621	5243
10	180	360	1442	2884	5767
11	197	393	1573	3146	6291
12	213	426	1704	3408	6816
13	229	459	1835	3670	7340
14	246	492	1966	3932	7864
15	262	524	2097	4194	8389
16	279	557	2228	4456	8913
17	295	590	2359	4719	9437
18	311	623	2490	4981	9961
19	328	655	2621	5243	10486
20	344	688	2753	5505	11010
21	360	721	2884	5767	11534
22	377	754	3015	6029	12059
23	393	786	3146	6291	12583
24	410	819	3277	6554	13107
25	426	852	3408	6816	13631
26	442	885	3539	7078	14156
27	459	918	3670	7340	14680
28	475	950	3801	7602	15204
29	492	983	3932	7864	15729
30	508	1016	4063	8126	16253
31	524	1049	4194	8389	16777

6. Additional Notes on CPU Space Ad

On page 3-31, Figure 3-16, the BKPT field for the Breal and the T bit is on bit 1. The Interrupt Acknowledge LEV

7. Breakpoints

On page 3-31, the last paragraph implies that either a breakpoint can be used to insert an instruction. As r breakpoint can be used to insert an instruction on the br

8. Interrupt Latency

Add to the Interrupt Acknowledge Bus Cycles section prefetch of the first instruction in the interrupt handler i clocks (using 2-clock memory and autovector termination (DIVS.L with worst-case <fea>) = 108 clocks worst ca shorter interrupt response time the latency can be reduce use of longer instructions (specifically DIVS.L, DIVU.L, M

9. Interrupt Hold Time and Spurious I

Add to the Interrupt Acknowledge Bus Cycles section c asserted until the corresponding IACK cycle; otherwise, rupt may be ignored entirely. This is also true for level se ing either the $\overline{\text{AVEC}}$ signal or the AVEC register, since th on the IMB if the external interrupt at that level has been sitive only have to be held a minimum of 1.5 clocks - s REGISTER (PIR).

Note that the level 7 interrupt is also level sensitive, and interrupt is unique in that it cannot be masked - anothe IACK cycle by negating IRQ7 and reasserting, even tho level 7.

10. Typos in IACK Cycle Timing Wave

On page 3-38, Figure 3-21, the text “VECTOR FROM FROM 8-BIT PORT” should be on D15-D8. The respond nificant byte of the data port.

11. Additional Note on Internal Autov

Add to the Autovector Interrupt Acknowledge Cycle se autovectored either by the AVEC register programming started and terminated internally. The interrupting devic resulting operation is undefined.

12. Additional Notes on Retry Termin

On page 3-42, Table 3-4: When $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are ass bus cycle, relative timing of $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ must be c

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mination case #3. This can be done by asserting $\overline{\text{HALT}}$ a control which edge each is recognized on, or asynchro 47B] ns before $\overline{\text{BERR}}$ to guarantee recognition on or be

13. Active Negate on Bus Arbitration

The 68341 actively pulls up all tri-stateable bus pins oth arbitration. This pullup function is not guaranteed to res reduce rise time on these signals when using weak exte

14. Additional Note on Bus Arbitratio

For the bus arbitration description beginning on page 3- ters for this device is external request via $\overline{\text{BR}}$ (highest p channels 1 and 2 relative to each other is selected by th

15. Additional Note on Bus Arbitratio

For the bus arbitration description beginning on page 3 when a higher priority request is recognized. For examp results in a sequence of four bus cycles to complete the until the completion of the fourth bus cycle. A single addi a dual address DMA transfer, the read and write portions tion between the read and write bus cycles. Also, if diffe for the source and destination, arbitration can occur be must be made to the smaller port for each operand acce for a TAS instruction is also indivisible to guarantee data erand transfer of a multi-operand operation such as a M

16. Additional Notes on RESET Intera

Add to the Reset Operation description beginning page

Hardware resets are held off until completion of the curr herency. The processor resets at the end of the bus cycle or after the bus monitor has timed out. The bus monitor c not, for the period of time that the BMT bits are set to.

The following reset sources reset all internal registers to double bus fault, loss of clock. Execution of a RESET in the exception of the MCR registers. The MCR register in are not affected by execution of a RESET instruction.

17. External Reset

On page 3-56, Figure 3-33, the $\overline{\text{RESET}}$ signal negates fo not one. Note that $\overline{\text{RESET}}$ is not actively negated, and it

18. Power-On Reset

On page 3-57, Figure 3-34. Power-Up Reset Timing Dia ternal control signals, and can begin toggling as soon a operating. For crystal mode and external clock with VCO

stable value, the 328*TCLKIN delay is counted down, a delay. For external clock mode without VCO, the 328*TC are recognized. See note for page11-3 for more POR in

19. Internal IMB Arbitration

On page 4-6, first paragraph, change the first sentence to bus masters on the MC68341 to access the inter-modul

20. Additional Note for External Clock

On page 4-9, Table 4-1, External Clock Mode with PLL: falling edge of the EXTCLK input clock. Maximum skew signals is specified in the Section 12 Electrical Characte

21. External Clock Mode Operation

The next-to-last paragraph on page 4-11 incorrectly state the system frequency in external clock mode. In externa cy, by selecting either EXTCLK or EXTCLK/2 as referenc divided by 2 is used both for CLKOUT as well as the fee V=0, resulting in an initial processor operating frequency

For applications using external clock mode, the 32KHz c if the realtime clock function is needed - ground EXTAL CLK should be very clean when the 32KHz oscillator is fast edge rates may result in coupling to the adjacent XT

22. Recommended XFC Capacitor Va

On page 4-12, third paragraph, and page 11-2, last para to 0.1µF applies specifically to crystal mode operation. V detector refernce frequencies > 1MHz start with a cap 16.0MHz the recommended XFC capacitance is approxi standard value available.

23. CLKOUT and VCO Frequency Pro

On pages 4-13 and 4-14, the column for W=1:Z=0:X=1 column is 2x the frequency in the X=0 column immediate ing pages. Note that although a complete table is shown frequency limits must be observed when programming th cy (CLKOUT) of 25.16MHz can be selected with W:X:Y:Z However, programming W:X:Y:Z=1:0:47:1 to achieve th quency of greater than 100MHz, which is outside the sp

24. Additional Note for Global Chip S

On page 4-16, section 4.2.4.2: When operating as a glo either the MBAR or to internal peripheral module registe

38. Additional Notes on DMA Feature

In the feature set listed on page 6-1, bullet six is “Opera
fers”. This packing is for transfers between different por
e.g. Byte <> Word transfers. The DMA controller does n
problem of residual bytes left in the controller when a ch

39. Additional Note on Internal Reque

Add to the Internal Request Generation section on page
$\overline{Ex}$ are not active as outputs during transfers. $\overline{DONEx}$ is
operation if asserted - pull up if not used.

40. Additional Note on DMA Transfer

Add to the External Request Generation section beginni
synchronization and IMB bus arbitration activity before
sertion will preempt the next CPU bus cycle if it is recogr
bus cycle, unless the current cycle is not the last cycle o
Operand transfers and RMC read/write sequences are i
not be arbitrated from the CPU until the complete opera
sizing results in multiple bus cycles.

For a $\overline{DREQx}$ assertion during an idle bus period, bus sta
clock falling edge which $\overline{DREQx}$ is recognized on. Th
$\overline{DREQx}$ is recognized on to the falling edge that $\overline{AS}$ for
table for various memory speeds.

DREQ Latency (Clocks) vs. Bus

Access Type	Maximum D		
	16-Bit Bus Clocks/Bus Cyc		
	2	3	4
Longword	7	9	11
RMC (TAS)	10	12	14

41. Additional Note on Burst Transfer

On page 6-5, replace the 2nd paragraph of 6.3.2.1 Exte
negated one clock before the end of the last DMA bus c
being generated. Also, $\overline{DREQx}$ must be negated two cloc
an idle clock between that transfer and the following CP

42. Additional Note on Cycle steal DM

Add to the External Cycle Steal Mode description on pa
ently. However, for some 2-clock accesses using cycle s
incomplete overlap of the DMA transfer with internal IM
single address 2-clock transfers and 2) dual address tra
completely overlapped for all other cases.

Table 4-2. System Frequencies from 3

Y	CLKOUT (kHz)				VCO (kHz)
	W = 0				W = 0
	Z = 0		Z = 1		Z = x
	X = 0	X = 1	X = 0	X = 1	X = x
32	541	1081	4325	8651	17302
33	557	1114	4456	8913	17826
34	573	1147	4588	9175	18350
35	590	1180	4719	9437	18874
36	606	1212	4850	9699	19399
37	623	1245	4981	9961	19923
38	639	1278	5112	10224	20447
39	655	1311	5243	10486	20972
40	672	1343	5374	10748	21496
41	688	1376	5505	11010	22020
42	705	1409	5636	11272	22544
43	721	1442	5767	11534	23069
44	737	1475	5898	11796	23593
45	754	1507	6029	12059	24117
46	770	1540	6160	12321	24642
47	786	1573	6291	12583	25166
48	803	1606	6423	12845	25690
49	819	1638	6554	13107	26214
50	836	1671	6685	13369	26739
51	852	1704	6816	13631	27263
52	868	1737	6947	13894	27787
53	885	1769	7078	14156	28312
54	901	1802	7209	14418	28836
55	918	1835	7340	14680	29360
56	934	1868	7471	14942	29884
57	950	1901	7602	15204	30409
58	967	1933	7733	15466	30933
59	983	1966	7864	15729	31457
60	999	1999	7995	15991	31982
61	1016	2032	8126	16253	32506
62	1032	2064	8258	16515	33030
63	1049	2097	8389	16777	33554

NOTES:
1. Some W/X/Y/Z bit combinations shown may select a CLK
   tion 11 Electrical Characteristics for CLKOUT and VC
2. Any change to W or Y results in a change in the VCO frequ

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25. Additional Note on PORTA/B Outp

Add to the External Bus Interface Operation description
sition after the S4 falling edge for the internal write to th
tions at roughly the same time DS negates for the data
specified in the Electrical Specifications.

26. RTC Memory Map

The RTC register offsets shown on page 4-21 are incor
dresses within the RTC can be accessed as either byte
offset $0CE. Note that RTC registers marked S/U are re
user mode.

ADDR	FC	15 8
0C0	S	RTC INTER
0C2	S/U	MINUTES (MIN)
0C4	S/U	DATE
0C6	S/U	MONTH
0C8	S	RTC CONTROL/STATUS (RCR)
0CA	S/U	MINUTES ALARM (MINA)
0CC	S/U	DATE ALARM (DATEA)
0CE	-	RESERVED

27. MBAR Register Reset Values

On page 4-22, the reset values for MBAR bits 31-12 are

28. MBAR AS7 Bit and IACK Cycles

On page 4-23, the second code sequence initializes th
dress decode for the internal 4K register block from res
vents the register block decode of $FFFFFxxx from inte
possibly corrupting the vector number returned. Normal
ules is not affected by this change.

Early versions of the MC68330 User's Manual (original
Rev. 1 releases) did not show AS7 set. Code which was
be checked for this problem when porting to the MC68
MC68330 and/or MC68340.

29. Additional Note on VCO Overshoo

On page 4-30 place the following note under the Y-bits

A VCO overshoot can occur when increasing the opera
register. The effects of this overshoot can be controlled

1. Write the X bit to zero. This will reduce the previous
2. Write the Y bits to the desired frequency divided by
3. After the VCO lock has occurred, write the X bit to c
   clock frequency to the desired frequency.

Steps 1 and 2 may be combined.

30. RCCR Initialization

Add to the RCCR description on page 4-41: the RCCR re
an arbitrary value on initial powerup of the RTC. Calibra
beginning the calibration process, since RTC operation
reserved - on current silicon it always reads 0, and shou

31. RCCR Typos

On page 4-42, delete the first description for RCD4-RCD

32. MONTH Register Range

The valid range for the MONTH register on page 4-43 is
responding to December.

33. SIM41 Example Code

On page 4-49, about mid-page, change "MOVEQ #8-1
lects.

34. Bus Error Stack Frame

On page 5-61, in the next-to-last paragraph, delete "(the
and the SSW is located at SP+12)". The stack space allo
internal count register and SSW remains the same. The
counter location SP+10 and SP+12 will contain invalid
frames, look at the first nibble of the faulted exception fo
the four-word frame, and $2 for the six-word frame.

35. DSO Timing

On page 5-71, Figure 5-23, DSO transitions one clock la

36. Typo on BDM RSREG Command

On page 5-77, Section 5.6.2.8.6, RSREG register bit #8

37. $\overline{\text{IPIPE}}$ Timing

On page 5-88, Figure 5-29 shows the third $\overline{\text{IPIPE}}$ assert
additional 0.5 CLKs. $\overline{\text{IPIPE}}$ transitions occur after the fal

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```
* Timer register offsets from timer1 ba
IR      EQU       $4   interrupt regist
CR      EQU       $6   control register
SR      EQU       $8   status register
CNTR    EQU       $A   counter register
PRLD1   EQU       $C   preload register
COM     EQU       $10  compare register
```

On page 8-27, change the last code line from "CLR.W S
TC interrupt status bits are cleared by writing a "1" to
cleared without affecting the other bits.

On page 8-28, second code line down, the "MOVE.W #$
initialized vector - change the $0F to a user-definable v
just past mid-page.

61. MC68341 BSDL File

An electronic copy of the BSDL file for the MC68341 is m
of this document for information on accessing AESOP.

62. Additional Note on Oscillator Lay

Add to the Processor Clock Circuitry (page 11-1) and S
short connections and place external oscillator compone
through or near the oscillator circuit, especially high fre
note above on $\overline{\text{DREQ1}}$ and serial oscillator for page7-5).
a separate trace for ground to the oscillator so that it do

63. Recommended 32KHz Oscillator (

On page 11-2, Figure 11-2, a 10M resistor can be subst

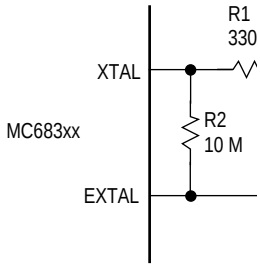

Figure 11-2. Sampl

64. SRAM Interface

The SRAM interface shown in Figure 11-5 on page 11-4
$\overline{\text{LWE}}$ do not assert for 2-clock writes.

43. Additional Note on Cycle Steal

For the external cycle steal mode description on page
held off until after the channel is started. If $\overline{\text{DREQx}}$ is alr
the channel start bit, an internal $\overline{\text{DREQx}}$ assertion is gen
to start.

44. $\overline{\text{DREQx}}$ Negation on Burst

On page 6-8, Figure 6-5, and on page 6-10, Figure 6-7,
(one clock earlier than shown) to prevent another DMA
6-5 on Burst Transfer $\overline{\text{DREQx}}$ Negation.

45. $\overline{\text{DREQ}}$ Assert Time

On page 6-21, Figure 6-13: The second $\overline{\text{DREQx}}$ assertion
antee recognition on 2 consecutive clock falling edges.
1 should be deleted.

46. Fast Termination and Burst Requ

On the last paragraph of page 6-21, delete the referenc
incorrectly - it actually shows operation with fast termina
second $\overline{\text{DREQx}}$ signal should be held for 2 consecutive
1 clock edge. Note 1 of Figure 6-14 should be deleted.

47. Typo in DAPI

On page 6-26, for DAPI = 1, the DAR is incremented ac

48. Additional note on DMA limited ra

On page 6-27, in the BB-Bus Bandwidth Field: The DMA
is the bus master (each channel has its own counter).
relinquish the bus before completion of the active count
Higher priority requests could come from 1) the other
CPU32 core (if either the interrupt mask level in the SR
channel's ISM level), or 3) an external bus request. Wh
releases the bus, and the “idle” count increments regard

49. Configuration Error

The Configuration Error description paragraph at the top
error results when 1) either the SAR or DAR contains a
in the CCR, or 2) the BTC register does not match the la

50. Additional Note on DMA Interrupt

Add to the Interrupt Register description on page 6-31: W
interrupt level, channel 1 is higher priority than channel

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51. Single Address Enable

6-33 SE-Single Address Enable: The note “used for in
68341 does not support intermodule single address tran
“0”.

52. Code Examples - Immediate Addr

On pages 6-40 through 6-44 make the following change
and NUMBYTE (change to immediate addressing mode

MOVE.L SARADD,DMASAR1(A0) should be MOVE.

MOVE.L DARADD,DMADAR1(A0) should be MOVE.

MOVE.L NUMBYTE,DMABTC1(A0) should be MOVE

53. Serial Oscillator Problems with DI

Add to the Crystal Input or External Clock (X1) section o
1MHz) with excessive undershoot on $\overline{\text{DREQ1}}$ can result
lator X1 pin, damping out oscillation. Avoid routing $\overline{\text{DREQ}}$
use termination techniques such as series termination o
of the signal and accompanying undershoot.

54. Additional Note on $\overline{\text{RTSx}}$ operatio

Add to the $\overline{\text{RTSA}}$ and $\overline{\text{RTSB}}$ descriptions on page 7-6: T
logic “0” when set, and a logic “1” when cleared.

$\overline{\text{RTSx}}$ can be set (output logic level 0) by any of the follo

- Writing a “1” to the corresponding bit in the OPSET
- Issuing an “Assert RTS” command using command
- If RxRTS=1, set by receiver FIFO transition from FU

$\overline{\text{RTSx}}$ can be cleared (output logic level 1) by any of the

- Hardware reset of the serial module
- Writing a “1” to the corresponding bit in the OPRESI
- Issuing a “Negate RTS” command using command
- If RxRTS=1, cleared by receiver FIFO transition fror
- If TxRTS=1, cleared by completion of last character

55. Serial Frequency Restriction

On page 7-8, place the following notes at the end of **Sec**

The current implementation of the serial module restricts
rate generators can be used to approximately 8.3MHz.
nized internal clock which is at a lower frequency than th
One method to extend the minimum CLKOUT frequen
shown in the table below. The corresponding baud rates

scaled by the same factor. This method preserves most

Serial XTAL Frequency	CLKOUT F_n
3.6864MHz	8.29MHz
1.8432	4.15
0.9216	2.07

CLKOUT min = 2.25*XTAL frequency

Alternatively, the baud rate clock can be supplied directly
input, both serial channels must use the same baud rate
and the other in the 16x mode. When using this method
quired.

56. 68341 Serial Module RTS Differen

Add to the description for receiver-controlled RTS operat
the 68681, the RTSx signal does not have to be manually
flow capability on the receiver.

57. Additional Note on Serial multidro

Add to the Multidrop Mode section beginning on page 7-
the transmitter to manipulate the A/D bit, as generally i
the previous character completes transmission (i.e. TxE
pends it to the data character when the character is tra
shift register. Once this transfer occurs (as indicated b
changed without affecting the character in progress. Th
bit for the next character would be:

1.) poll TxRDY until asserted (or interrupt on TxRDY
2.) set/clear A/D bit in MR1 for new character
3.) write character to transmit buffer (TB)
4.) A/D bit can be changed only after TxRDY assert

No other bits in MR1 should be modified when changing

58. Typo in CPE Description

The CPE bit header on page 8-20 should be "Counter/P

59. Typo in Status Register Configura

On page 8-26, Section 8.5.1, the Status Register (SR)
bits to reset the interrupts."

60. Typos in Timer Initialization Exam

On pages 8-27 and 8-29, the Timer register offsets shou
base address. The correct equates for the Timer registe

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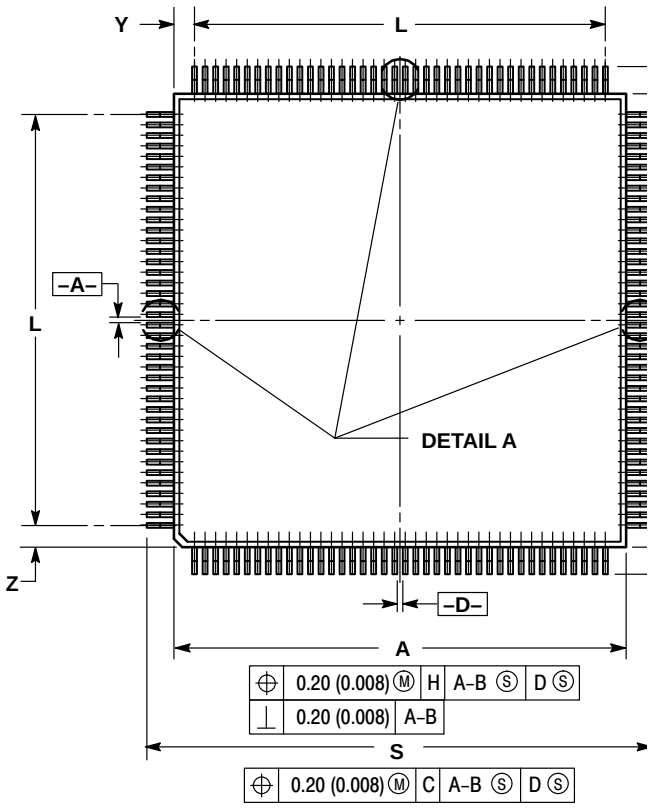

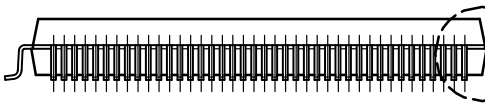

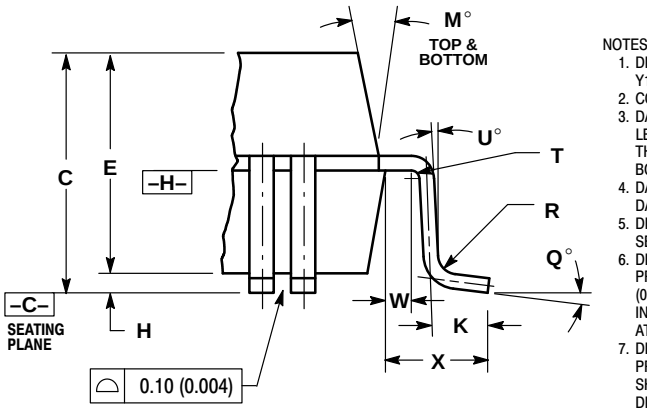

DETAIL C

Case 86

65. Corrections to 8/16-Bit DMA Cont

On page 11-10, the logic driving $\overline{OE}$ on the 74F245 in Fi
though not detailed, the byte enables for the memory blo
tention between the upper and lower bytes of the data b

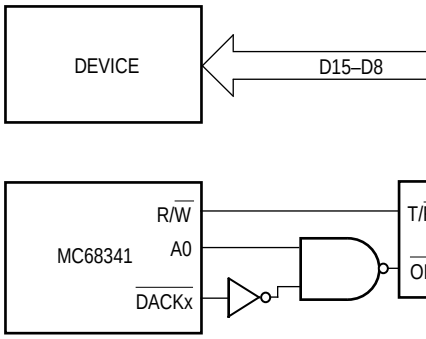

**Figure 11-14. Circuit For Interfacin
in Single-Addre**

66. X1 and $\overline{BSW}$ Input Levels

On page 12-5, the Clock Input High Voltage spec also a

67. Operating IDD Limits

On page 12-5, the spec operating (RUN) currents are sh

Product	Frequency	Max Idd
68341FT16V	16.78MHz	95mA@3.6V
68341FT16	16.78MHz	150mA@5.25V
68341FT25	25.16MHz	210mA@5.25V

68. Input Clock Duty Cycle in Externa

On page 12-7, External Clock With PLL Mode: The inpu
mode can be used when the VCO is not turned off during
the input clock is used for clocking the SIM, and must
External Clock Mode Without PLL.

69. Clock Skew Notes

12-7, External Clock With PLL Mode, Clock Input to CLK

edges of the clock signals - the PLL phase locks the fall

70. Data Setup Time for 3.3V

On page 12-9, electrical specification #27 (Data Setup changed from 5ns to 8ns.

71. $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ Signals

In Figure 12-3 on page 12-12, $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ will asser
In the fast termination write cycle in Figure 12-5 on pag
like $\overline{\text{DS}}$.

72. Serial Module Specs

Note 1 on page 12-25 should reference synchronous op

73. Ordering Information

Replace the the ordering information table in Section 11

Supply Voltage	Package Type	Frequen (MHz)
5.0 V	Plastic Quad Flat Pack FT Suffix	0 – 25
5.0 V	Plastic Quad Flat Pack FT Suffix	0 – 16.7
3.3 V	Plastic Quad Flat Pack FT Suffix	0 – 16.7

74. Upper and Lower Data Strobes

In paragraph 3.2.8 page 3-6, change (D15–D0) to (D15-

75. Figure 3-2

Change Note 1 to reference MC68341 instead of MC68

76. Figure 4-8

The Periodic Interrupt Control Register (PICR) and Perio
instead of 2 bytes. Disregard the Scale Select Register.

77. Page 4-24

Refer to 4-17 for more information on the AVEC-Automa

78. Page 4-48

The lake at the start of the code should be INIT341 inste

79. Page 6-5, Paragraph 6.3.1.2

The table reference in the last sentence should be 6-4 n

80. Page 9-19,

The timing diagrams reference as Figures 9-24 — 9-27

81. Page 9-29, DT–Delay

A value of 1 enable this bit and 0 disables it.

82. Package Dimensions

The package dimension drawing on page 13-3 should b

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