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MOTOROLA

MC68341

Integrated Processor User's Manual

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PREFACE

The complete documentation package for the MC68341 consists of the MC68341UM/AD, *MC68341 Integrated Processor User's Manual*, M68000PM/AD, *MC68000 Family Programmer's Reference Manual,* and the MC68341P/D, *MC68341 Integrated Processor Product Brief*.

The *MC68341 Integrated Processor User's Manual* describes the programming, capabilities, registers, and operation of the MC68341; the *MC68000 Family Programmer's Reference Manual* provides instruction details for the MC68341; and the *MC68341 Integrated Processor Product Brief* provides a brief description of the MC68341 capabilities.

This user's manual is organized as follows:

Section 1	Device Overview
Section 2	Signal Descriptions
Section 3	Bus Operation
Section 4	System Integration Module
Section 5	CPU32
Section 6	DMA Controller Module
Section 7	Serial Module
Section 8	Timer Modules
Section 9	Queued Serial Peripheral Module
Section 10	IEEE 1149.1 Test Access Port
Section 11	Applications
Section 12	Electrical Characteristics
Section 13	Ordering Information and Mechanical Data

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SECTION 1
DEVICE OVERVIEW

The MC68341 is a member of the M68300 family of integrated processors designed specifically for the compact disc-interactive (CD-I) market. It improves on the feature set of the MC68340 for a more complete and cost effective integrated system solution to CD-I's specific needs.

The MC68341 contains a 68020-based CPU32, a two channel DMA controller, two serial channels, a timer, and a queued serial peripheral interface. The 68341's system integration module (SIM41) contains clock circuitry, system protection, external bus interface, timers, and additional chip selects. New to the SIM is the real time clock and an MC68000 bus interface. The MC68000 bus interface is dynamically selectable to give a glueless interface to peripherals and memory designed for the MC68000 while allowing higher performance transfers using the standard 68300 bus interface. Complete code compatibility with the MC68000 affords the designer access to a broad base of established real-time kernels, operating systems, languages, applications, and development tools—many oriented towards embedded control.

As a low voltage part, the MC68341V can operate with a 3.3-V power supply and is particularly useful for battery applications. MC68341 is used throughout this document to refer to both the low voltage and standard 5-V parts since both are functionally equivalent. Figure 1-1 illustrates a block diagram of the MC68341.

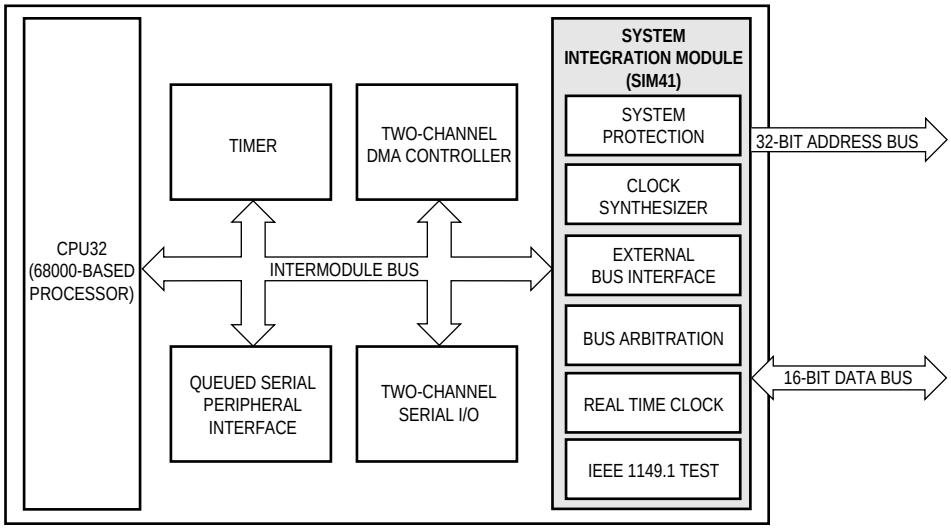

Figure 1-1. MC68341 Simplified Block Diagram

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MC68341 FEATURES

The primary features of the MC68341 are as follows:

- High Performance CPU32 Core Processor
  — Upward Object-Code Compatible with MC68000 and MC68010
  — Additional 32-Bit MC68020 Instructions and Addressing Modes
  — Fast Two-Clock Register Instructions
- High-Speed Dual DMA Controllers for Low-Latency Transfers
  — 50-Mbyte/Sec Sustained Transfer Rate
  — Dual or Single Address Transfers
  — 8-, 16-, or 32-Bit Transfers
- Counter/Timer
  — 16-Bit Timer with 8-Bit Prescaler
  — Multi-mode Operation
  — 80 nS Resolution
- Dual Serial Communication Ports
  — Synchronous or Asynchronous Operation
  — 3-Mbit/Sec Sustained Transfer Rate
  — Modem Control
  — Baud Rate Generation
  — 68681/261 Compatible
- Queued Serial Peripheral Interface (QSPI)
  — Communications with Slow Peripherals without Tying Up the CPU
  — Queued Transmit and Receive Buffers
  — Programmable for Master or Slave SPI Operation
- System Integration Module for Flexible and Cost-Effective System Interface
  — 32-Bit Address Bus; 16-Bit Data Bus with Dynamic Bus Sizing
  — System Protection, Reset, and Configuration Control
  — Periodic Interrupt/System Timer
  — Chip-Select, Wait State Generation, Bus Watchdog
  — Interrupt Controller
  — IEEE 1149.1 Boundary Scan (JTAG)
  — Dual 8-Bit Parallel Ports
  — Real Time Clock
  — Time and Date with Leap Year Correction
  — Programmable Alarm for Interrupt or External Output
  — Calibration Register Eliminates Need for Trim Capacitor
  — Battery Backup Capability
- Power Management
  — 5 V or 3.3 V Operation
  — Fully Static HCMOS Technology
  — Programmable Clock Synthesizer for Full Frequency Control
  — Power-Down/Low Power Stop Capabilities
  — Idle Modules Can Be Individually Powered Down
- 0–16 or 25 MHz Operation
- 160-Pin Plastic Quad Flat Pack (QFP)

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CENTRAL PROCESSING UNIT

The CPU32 is a powerful central processor that supervises system function, makes decisions, manipulates data, and directs I/O. A special debugging mode simplifies processor emulation during system debug.

CPU32

The CPU32 is a 68000-based microprocessor that can execute most 32-bit operations in two clock periods. Additional instructions enhance lookup table interpolation and power consumption control. In addition to performing basic instruction execution, the CPU32 provides a sophisticated background debug port for non-invasive instrumentation in the software development and debug environments.

On-Chip Peripherals

To improve total system throughput and reduce part count, board size, and cost of system implementation, the M68300 family integrates on-chip, intelligent peripheral modules, and typical glue logic. These functions on the MC68341 include the SIM41, a DMA controller, a serial module, a queued serial peripheral interface, and a timer.

The IMB is the backbone of the MC68341, and is similar to traditional external buses with address, data, clock, interrupt, arbitration, and handshake signals. Because bus masters (like the CPU32 and DMA), peripherals, and the SIM41 are on the same processor, the IMB ensures that communication between these modules is fully synchronized and that arbitration and interrupts can be handled in parallel with data transfers, greatly improving system performance. Internal accesses across the IMB can be monitored from outside of the processor.

System Integration Module

The MC68341 system integration module (SIM41) handles a wide array of functions, eliminating the need for much of the glue logic which typically supports the microprocessor and its interface with peripherals and external memory. The SIM41 includes:

- External Bus Interface—Transfers information between the CPU32 or DMA controller and external memory or peripherals by providing up to 32 address lines and 16 data lines. Both the 68300 bus interface and the original MC68000 bus interface are provided.
- System Configuration and Protection—Achieves maximum system protection by providing various monitors and timers to prevent system lockup, recover from catastrophic failure, exit infinite loops, provide refresh, etc.
- Clock Synthesizer—Generates the clock signals used by all internal operations as well as a clock output used by external devices.
- Chip Select and Wait State Generation—Offers eight programmable chip selects which provide signals to enable external memory and peripheral circuits and create all external handshaking and timing signals. Up to six wait states can be automatically inserted.

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- Interrupt Control—Provides up to seven discrete interrupt inputs for external devices.
- IEEE 1149.1 Test Access Port (JTAG)—Aids in system diagnostics by providing dedicated, user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability.
- Real Time Clock—The real time clock can be sustained on a separate power supply for battery backup. This simple counter is driven by 32.768 KHz clock for low power consumption. The real time clock counts seconds, minutes, hours, days, day of the week, date of the month, and year with leap year compensation. The real time clock has internal interrupt generation capability and includes a programmable output pin, which can provide an interrupt or other output signal based upon an alarm or time matching function. Software calibration eliminates the need for an external trim capacitor.

Queued Serial Peripheral Interface (QSPI) Module

The QSPI eases peripheral expansion or interprocessor communications. This function allows interface to and control of other integrated controllers (such as, MC6805 or MC68HC11 family devices) and peripherals (such as, LCD drivers, A/D–D/A converters, digital signal processors, EEPROM). The QSPI can handle up to 16 serial transfers of 8 to 16 bits each or transmit a stream of data up to 256 bits long without CPU intervention, because of a small RAM in the QSPI. A special wrap-around mode allows the QSPI to continuously sample a serial peripheral, automatically updating the QSPI RAM for efficient interfacing to serial analog-to-digital converters.

Timer Module

The timer consists of a 16-bit countdown counter with an 8-bit countdown prescaler for a composite 24-bit resolution. The finest resolution of the timer is 80 ns with a 25-MHz system clock (125 ns @ 16.78 MHz). The programmable timer operating modes are input capture, output compare, square-wave generation, variable duty-cycle square-wave generation, variable-width single-shot pulse generation, event counting, period measurement, and pulse-width measurement.

POWER CONSUMPTION MANAGEMENT

The MC68341 is very power efficient due to its advanced 0.8-µ HCMOS process technology and its static logic design. The resulting power consumption is typically 500 mW in full operation—far less than the comparable discrete component implementation the MC68341 can replace. For applications employing reduced voltage operation, selection of the MC68341V, which requires only a 3.3-V power supply, reduces current consumption by 40–60% in all modes of operation (as well as reducing noise emissions).

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COMPACT DISC-INTERACTIVE

The MC68341 was designed to meet the needs of many markets, including compact disc-interactive (CD-I). CD-I is an standard for a publishing medium that will bring multimedia to a broad general audience—the consumer. CD-I players combine television and stereo systems as output devices, with interactive control using a TV remote-control-like device to provide a multimedia experience selected from software titles contained in compressed form on standard compact discs.

The on-chip real-time clock eliminates the need for a separate chip to keep time-of-day. The 68000 bus interface simplifies the use of existing CD-DA and CD-I peripherals and ASICs that were designed for use with the 68000.

The highly integrated MC68341 is ideal as the central processor for CD-I players. It provides the M68000 microprocessor code compatibility and DMA functions required by the *CD-I Green Book* specification as well as many other useful on-chip functions for a very cost-effective solution. The extra demands of full-motion video CD-I systems make the best use of the MC68341 high performance. The MC68341 is CD-I compliant and has been CD-I qualified. With its low voltage operation, the MC68341V is the only practical choice for portable CD-I.

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SECTION 2
SIGNAL DESCRIPTIONS

This section contains brief descriptions of the MC68341 input and output signals in their functional groups as shown in Figure 2-1.

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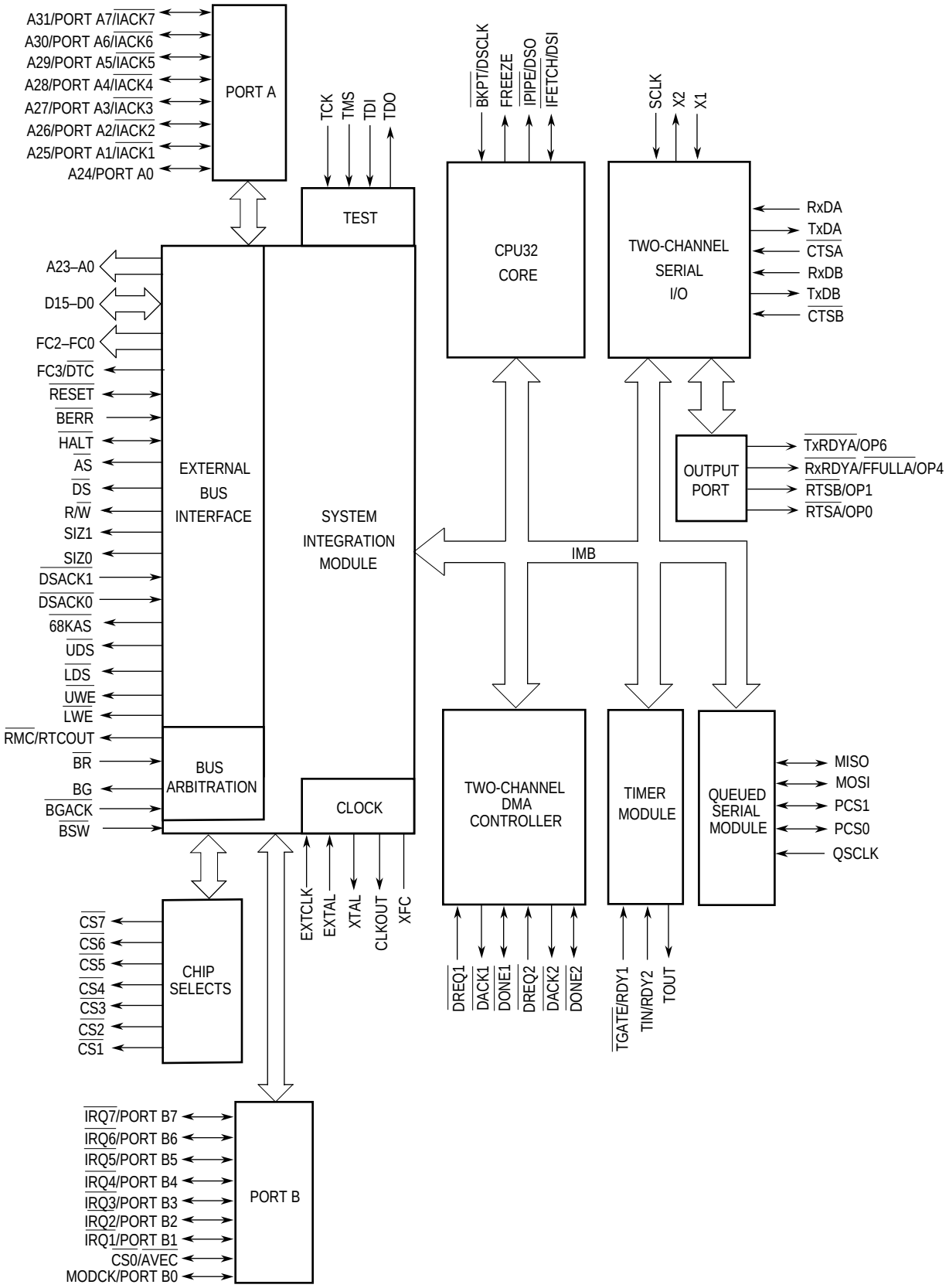

Figure 2-1. Functional Signal Groups

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2.1 SIGNAL INDEX

The input and output signals for the MC68341 are listed in Table 2-1 through 2-8. The name, mnemonic, and brief functional description are presented. For more detail on each signal, refer to the signal paragraph. Guaranteed timing specifications for the signals listed in the following tables can be found in **Section 12 Electrical Characteristics**.

Table 2-1. Bus Signal Summary

Signal Name	Mnemonic	Input/ Output	Three-State During Bus Arbitration
Address Bus	A23–A0	Out	Yes
Address Bus/Port A7–A0/ Interrupt Acknowledge7–1	A31–A24/ IACK7–1	Out/I/O/ Out	Yes
Data Bus	D15–D0	I/O	Yes
Function Code 3/$\overline{\text{DTC}}$,	FC3/$\overline{\text{DTC}}$	Out	Yes
Function Code 2–0	FC2–FC0	Out	Yes
Chip Select 7–1	$\overline{\text{CS7}}$–$\overline{\text{CS1}}$	Out	Yes
Interrupt Request Level/ Port B7–B1	$\overline{\text{IRQ7}}$–$\overline{\text{1}}$/ B7–B1	In, I/O	–
Chip Select 0/Autovector	$\overline{\text{CS0}}$/$\overline{\text{AVEC}}$	Out/In	–
Bus Request	$\overline{\text{BR}}$	In	–
Bus Grant	$\overline{\text{BG}}$	Out	No
Bus Grant Acknowledge	$\overline{\text{BGACK}}$	In	–
Data and Size Acknowledge	$\overline{\text{DSACK1}}$, $\overline{\text{DSACK0}}$	In	–
Read-Modify-Write Cycle/ Real-Time Clock Out	$\overline{\text{RMC}}$/RTCOUT	Out	Yes/No
Address Strobe	$\overline{\text{AS}}$	Out	Yes
Data Strobe	$\overline{\text{DS}}$	Out	Yes
M68000 Address Strobe	$\overline{\text{68KAS}}$	Out	Yes
Upper Data Strobe	$\overline{\text{UDS}}$	Out	Yes
Lower Data Strobe	$\overline{\text{LDS}}$	Out	Yes
Upper Write Enable	$\overline{\text{UWE}}$	Out	Yes
Lower Write Enable	$\overline{\text{LWE}}$	Out	Yes
Size	SIZ1, SIZ0	Out	Yes
Read/Write	R/$\overline{\text{W}}$	Out	Yes
Reset	$\overline{\text{RESET}}$	I/O	No
Halt	$\overline{\text{HALT}}$	I/O	No
Bus Error	$\overline{\text{BERR}}$	In	–

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Table 2-2. CPU32 Serial Port

Signal Name	Mnemonic	Input/ Output
Instruction Fetch/ Development Serial In	$\overline{\text{IFETCH}}$ /DSI	Out/In
Instruction Pipe/ Development Serial Out	$\overline{\text{IPIPE}}$/DSO	Out/Out
Breakpoint/Development Serial Clock	$\overline{\text{BKPT}}$/DSCLK	In/—
Freeze	FREEZE	Out

Table 2-3. Serial Module

Signal Name	Mnemonic	Input/ Output
Receive Data	RxDB, RxDA	In
Transmit Data	TxDB, TxDA	Out
Clear-to-Send	$\overline{\text{CTSB}}$, $\overline{\text{CTSA}}$	In
Request-to-Send/OP1, OP0	$\overline{\text{RTSB}}$, $\overline{\text{RTSA}}$	Out/Out
Serial Crystal Oscillator	X1, X2	In
Serial Clock	SCLK	In
Transmitter Ready/OP6	$\overline{\text{TxRDYA}}$	Out/Out
Receiver Ready/FIFO Full/OP4	$\overline{\text{RxRDYA}}$	Out/Out/ Out

Table 2-4. Queued Serial Module

Signal Name	Mnemonic	Input/ Output
QSPI Peripheral Chip Slect	PCS1, PCS0	I/O
QSPI Serial Clock	QSCLK	In
Master-In Slave-Out	MISO	I/O
Master-Out Slave-In	MOSI	I/O

Table 2-5. DMA Module

Signal Name	Mnemonic	Input/ Output
DMA Request	$\overline{\text{DREQ2}}$, $\overline{\text{DREQ1}}$	In
DMA Acknowledge	$\overline{\text{DACK2}}$ $\overline{\text{DACK1}}$	Out
DMA Done	$\overline{\text{DONE2}}$, $\overline{\text{DONE1}}$	I/O
DMA RDY1/Timer Gate	$\overline{\text{TGATE}}$, $\overline{\text{RDY1}}$	In
DMA RDY2/Timer Input	TIN, $\overline{\text{RDY2}}$	In
DTC/FC3	TIN, $\overline{\text{RDY2}}$	In

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Table 2-6. Timer Module

Signal Name	Mnemonic	Input/ Output
Timer Gate/DMA RDY1	$\overline{\text{TGATE}}$, $\overline{\text{RDY1}}$	In
Timer Input/DMA RDY2	TIN, $\overline{\text{RDY2}}$	In
Timer Output	TOUT	Out

Table 2-7. IEEE 1149.1

Signal Name	Mnemonic	Input/ Output
Test Clock	TCK	In
Test Mode Select	TMS	In
Test Data In	TDI	In
Test Data Out	TDO	Out

Table 2-8. Power, Clock, and Control

Signal Name	Mnemonic	Input/ Output
Clock Mode Select/ Port B0	MODCK/Port B0	In/I/O
Battery Switch	$\overline{\text{BSW}}$	
Battery Power In	V_{BATT}	In
System Power Supply and Ground	V_{CC}, GND	—
System Clock	CLKOUT	Out
Crystal Oscillator	EXTAL, XTAL	In, Out
External Clock	EXTCLK	In
External Filter Capacitor	XFC	In

NOTE

The terms *assert* and *negate* are used throughout this section to avoid confusion when dealing with a mixture of active-low and active-high signals. The term *assert* or *assertion* indicates that a signal is active or true, independent of the level represented by a high or low voltage. The term *negate* or *negation* indicates that a signal is inactive or false.

2.2 BUS SIGNALS

The MC68341 can interface using either a 68000 family bus or an MC68341 Family bus. Many of the signals are common to both bus types. Refer to **Section 3 Bus Operation** for more information on the two types of buses.

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2.2.1 Address Bus

The address bus signals are outputs that define the address of the byte (or the most significant byte) to be transferred during a bus cycle. The MC68341 places the address on the bus at the beginning of a bus cycle. The address is valid while $\overline{AS}$ is asserted.

The address bus consists of the following two groups. Refer to **Section 3 Bus Operation** for information on the address bus and its relationship to bus operation.

2.2.1.1 Address Bus (A23–A0). These three-state outputs (along with A31–A24) provide the address for the current bus cycle, except in the CPU address space.

2.2.1.2 Address Bus (A31–A24). These pins can be programmed as the most significant eight address bits, port A parallel I/O, or interrupt acknowledge signals. These pins can be used for more than one of their multiplexed functions as long as the external demultiplexing circuit properly resolves interaction between the different functions.

A31–A24

These pins can function as the most significant eight address bits.

Port A7–A0

These eight pins can serve as a dedicated parallel I/O port. See **Section 4 System Integration Module** for more information on programming these pins.

$\overline{IACK7}$–$\overline{IACK1}$

The MC68341 asserts one of these pins to indicate the level of an external interrupt during an interrupt acknowledge cycle. Peripherals can use the $\overline{IACKx}$ signals instead of monitoring the address bus and function codes to determine that an interrupt acknowledge cycle is in progress and to obtain the current interrupt level.

2.2.2 Address Strobe ($\overline{AS}$)

$\overline{AS}$ is an output timing signal for MC68300 cycles that indicates the validity of both an address on the address bus and many control signals. $\overline{AS}$ is asserted approximately one-half clock cycle after the beginning of a bus cycle.

2.2.3 M68000 Address Strobe ($\overline{AS68K}$)

$\overline{AS68K}$ is an output timing signal for MC68000 cycles that indicates that the information on the address bus is a valid address.

2.2.4 Data Bus (D15–D0)

This bidirectional, nonmultiplexed, parallel bus contains the data being transferred to or from the MC68341. A read or write operation may transfer 8 or 16 bits of data (one or two bytes) in one bus cycle. During a read cycle, the data is latched by the MC68341 on the last falling edge of the clock for that bus cycle. For a write cycle, all 16 bits of the data bus are driven, regardless of the port width or operand size. The MC68341 places the data on the data bus approximately one-half clock cycle after $\overline{AS}$ is asserted in a write cycle.

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2.2.5 Data Strobe ($\overline{DS}$)

$\overline{DS}$ is an output timing signal for M68300 transfers that applies to the data bus. For a read cycle, the MC68341 asserts $\overline{DS}$ and $\overline{AS}$ simultaneously to signal the external device to place data on the bus. For a write cycle, $\overline{DS}$ signals to the external device that the data to be written is valid. The MC68341 asserts $\overline{DS}$ approximately one clock cycle after the assertion of $\overline{AS}$ during a write cycle.

2.2.6 Upper And Lower Data Strobes ($\overline{UDS}$, $\overline{LDS}$)

These three-state signals and R/$\overline{W}$ control the flow of data on the data bus for M68000 transfers. Table 2-9 lists the combinations of these signals and the corresponding data on the bus. $\overline{UDS}$ and $\overline{LDS}$ assert with $\overline{AS68K}$ for read cycles, and one clock after $\overline{AS}$ for write cycles. The equations of the data strobes are as follows:

$$\overline{UDS} = A0$$
$$\overline{LDS} = \overline{A0} \times \overline{SIZ1} \times SIZ0$$

Table 2-9. Data Strobe Control of Data Bus

$\overline{UDS}$	$\overline{LDS}$	R/$\overline{W}$	D15–D8	D7–D0
Low	Low	High	Valid Data Bits 15–8	Valid Data Bits 7–0
High	Low	High	No Valid Data	Valid Data Bits 7–0
Low	High	High	Valid Data Bits 15–8	No Valid Data
Low	Low	Low	Valid Data Bits 15–8	Valid Data Bits 7–0

2.2.7 Byte Write Enable ($\overline{UWE}$, $\overline{LWE}$)

On a write cycle to a 16-bit port, these active-low output signals indicate when the upper or lower eight bits of the data bus contain valid data. The upper write enable ($\overline{UWE}$) indicates that the upper eight bits of the data bus contain valid data during a write cycle. The lower write enable ($\overline{LWE}$) indicates that the lower eight bits of the data bus contain valid data during a write cycle. $\overline{UWE}$ and $\overline{LWE}$ assert with $\overline{DS}$ for an MC68300 write and with $\overline{UDS}$/$\overline{LDS}$ for a 68000 write cycle. The equations of the byte write enables are as follows:

$$\overline{UWE} = R/\overline{W} + \overline{AS} + A0$$
$$\overline{LWE} = R/\overline{W} + \overline{AS} + (\overline{A0} \times SIZ0)$$

2.2.8 Read/Write (R/$\overline{W}$)

This active-high output signal is driven by the bus master to indicate the direction of a data transfer on the bus. A logic one indicates a read from a slave device; a logic zero indicates a write to a slave device.

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2.2.9 Transfer Size (SIZ1, SIZ0)

These output signals are driven by the bus master to indicate the number of operand bytes remaining to be transferred in the current bus cycle as noted in Table 2-10.

Table 2-10. SIZx Signal Encoding

SIZ1	SIZ0	Transfer Size
0	1	Byte
1	0	Word
1	1	Three Byte
0	0	Long Word

2.2.10 Function Codes (FC3–FC0)

These signals are outputs that indicate one of 16 address spaces to which the address applies. Fifteen of these spaces are designated as either user or supervisor, program or data, and normal or direct memory access (DMA) spaces. One other address space is designated as CPU space to allow the CPU32 to acquire specific control information not normally associated with read or write bus cycles. The function code signals are valid while $\overline{AS}$ is asserted. See Table 2-11 for more information.

Table 2-11. Address Space Encoding

Function Code Bits				Address Spaces
3	2	1	0	
0	0	0	0	Reserved (Motorola)
0	0	0	1	User Data Space
0	0	1	0	User Program Space
0	0	1	1	Reserved (User)
0	1	0	0	Reserved (Motorola)
0	1	0	1	Supervisor Data Space
0	1	1	0	Supervisor Program Space
0	1	1	1	CPU Space
1	x	x	x	DMA Space

2.2.11 Chip Selects ($\overline{CS7}$–$\overline{CS1}$, $\overline{CS0}$/$\overline{AVEC}$)

The chip select output signals ($\overline{CS7}$–$\overline{CS1}$) enable peripherals at programmed addresses. These signals are inactive high (not high impedance) after reset.

$\overline{CS0}$ is the chip select for a boot ROM containing the reset vector and initialization program. It functions as the boot chip select immediately after reset. $\overline{AVEC}$ requests an automatic vector during an interrupt acknowledge cycle.

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2.2.12 Interrupt Request Level ($\overline{IRQ7}$ – $\overline{IRQ1}$)

These pins can be programmed to be either prioritized interrupt request lines or port B parallel I/O.

$\overline{IRQ7}$ – $\overline{IRQ1}$

$\overline{IRQ7}$, the highest priority, is nonmaskable. $\overline{IRQ6}$–$\overline{IRQ1}$ are internally maskable interrupts. Refer to **Section 5 CPU32** for more information on interrupt request lines.

Port B7 – B1

These pins can be used as port B parallel I/O. Refer to **Section 4 System Integration Module** for more information on parallel I/O signals.

2.3 BUS CONTROL SIGNALS

These signals control the bus transfer operations of the MC68341. Refer to **Section 3 Bus Operation** for more information on these signals.

2.3.1 Data and Size Acknowledge ($\overline{DSACK1}$, $\overline{DSACK0}$)

These two active-low input signals allow asynchronous data transfers and dynamic data bus sizing between the MC68341 and external devices as listed in Table 2-12. During bus cycles, external devices assert $\overline{DSACK1}$ and/or $\overline{DSACK0}$ as part of the bus protocol. During a read cycle, this signals the MC68341 to terminate the bus cycle and to latch the data. During a write cycle, this indicates that the external device has successfully stored the data and that the cycle may terminate.

Table 2-12. $\overline{DSACKx}$ Encoding

$\overline{DSACK1}$	$\overline{DSACK0}$	Result
1	1	Insert Wait States in Current Bus Cycle
1	0	Complete Cycle—Data Bus Port Size Is 8 Bits
0	1	Complete Cycle—Data Bus Port Size Is 16 Bits
0	0	Reserved—Defaults to 16-Bit Port Size. Can Be Used for 32-Bit DMA Cycles

2.4 BUS ARBITRATION SIGNALS

The following signals are the bus arbitration control signals used to determine the bus master. Refer to **Section 3 Bus Operation** for more information on these signals.

2.4.1 Bus Request ($\overline{BR}$)

This active-low input signal indicates that an external device needs to become the bus master.

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2.4.2 Bus Grant ($\overline{BG}$)

Assertion of this active-low output signal indicates that the MC68341 has relinquished the bus.

2.4.3 Bus Grant Acknowledge ($\overline{BGACK}$)

Assertion of this active-low input indicates that an external device has become the bus master.

2.4.4 Read-Modify-Write Cycle ($\overline{RMC}$/RTCOUT)

$\overline{RMC}$ is an output signal that identifies the bus cycle as part of an indivisible read-modify-write operation. It remains asserted during all bus cycles of the read-modify-write operation to indicate that bus ownership cannot be transferred.

RTCOUT is an output signal from the real-time clock in the SIM41.

2.5 EXCEPTION CONTROL SIGNALS

These signals are used by the MC68341 to recover from an exception.

2.5.1 Reset ($\overline{RESET}$)

This active-low, open-drain, bidirectional signal is used to initiate a system reset. An external reset signal (as well as a reset from the SIM41) resets the MC68341 and all external devices. A reset signal from the CPU32 (asserted as part of the RESET instruction) resets external devices; the internal state of the CPU32 is not affected. The on-chip modules are reset, except for the SIM41. However, the module configuration register for each on-chip module is not altered. When asserted by the MC68341, this signal is guaranteed to be asserted for a minimum of 512 clock cycles. Refer to **Section 3 Bus Operation** for a description of bus reset operation and **Section 5 CPU32** for information about the reset exception.

2.5.2 Halt ($\overline{HALT}$)

This active-low, open-drain, bidirectional signal is asserted to suspend external bus activity, to request a retry when used with $\overline{BERR}$, or to perform a single-step operation. As an output, $\overline{HALT}$ indicates a double bus fault by the CPU32. Refer to **Section 3 Bus Operation** for a description of the effects of $\overline{HALT}$ on bus operation.

2.5.3 Bus Error ($\overline{BERR}$)

This active-low input signal indicates that an invalid bus operation is being attempted or, when used with $\overline{HALT}$, that the processor should retry the current cycle. Refer to **Section 3 Bus Operation** for a description of the effects of $\overline{BERR}$ on bus operation.

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2.6 CLOCK SIGNALS

These signals are used by the MC68341 for controlling or generating the system clocks. See **Section 4 System Integration Module** for more information on the various clocking methods and frequencies.

2.6.1 System Clock (CLKOUT)

This output signal is the system clock output and is used as the bus timing reference by external devices. CLKOUT can be varied in frequency or slowed in low power stop mode to conserve power.

2.6.2 Crystal Oscillator (EXTAL, XTAL)

These two pins are the connections for an external crystal to the internal oscillator circuit.

2.6.3 External Clock (EXTCLK)

This pin used to connect an external clcok source. This input is divided by two until the V-bit in the SYNCR is set.

2.6.4 External Filter Capacitor (XFC)

This pin is used to add an external capacitor to the filter circuit of the phase-locked loop. The capacitor should be connected between XFC and VCCSYN.

2.6.5 Clock Mode Select (MODCK, Port B0)

This pin selects the source of the internal system clock during reset. After reset, it can be programmed to be port B parallel I/O.

MODCK

The state of this active-high input signal during reset selects the source of the internal system clock. If MODCK is high during reset, the internal voltage-controlled oscillator (VCO) furnishes the system clock in crystal mode. If MODCK is low during reset, an external clock source at the EXTCLK pin furnishes the system clock output in external clock mode.

Port B0

This pin can be used as a port B parallel I/O.

2.7 INSTRUMENTATION AND EMULATION SIGNALS

These signals are used for test or software debugging. See **Section 5 CPU32** for more information on these signals and background debug mode.

2.7.1 Instruction Fetch ($\overline{\text{IFETCH}}$ / DSI)

This pin functions as $\overline{\text{IFETCH}}$ in normal operation and as DSI in background debug mode.

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$\overline{\text{IFETCH}}$

This active-low output signal indicates when the CPU32 is performing an instruction word prefetch and when the instruction pipeline has been flushed.

DSI

This development serial input signal helps to provide serial communications for background debug mode.

2.7.2 Instruction Pipe ($\overline{\text{IPIPE}}$/DSO)

This pin functions as $\overline{\text{IPIPE}}$ in normal operation and as DSO in background debug mode.

$\overline{\text{IPIPE}}$

This active-low output signal is used to track movement of words through the instruction pipeline.

DSO

This development serial output signal helps to provide serial communications for background debug mode.

2.7.3 Breakpoint ($\overline{\text{BKPT}}$/DSCLK)

This pin functions as $\overline{\text{BKPT}}$ in normal operation and as DSCLK in background debug mode.

$\overline{\text{BKPT}}$

This active-low input signal is used to signal a hardware breakpoint to the CPU32.

DSCLK

This development serial clock input helps to provide serial communications for background debug mode.

2.7.4 Freeze (FREEZE)

Assertion of this active-high output signal indicates that the CPU32 has acknowledged a breakpoint and has initiated background mode operation.

2.8 DMA MODULE SIGNALS

The following signals are used by the direct memory access (DMA) controller module to provide external handshake for either a source or destination. See **Section 6 DMA Module** for additional information on these signals.

2.8.1 DMA Request ($\overline{\text{DREQ2}}$, $\overline{\text{DREQ1}}$)

This active-low input is asserted by a peripheral device to request an operand transfer between that peripheral and memory. The assertion of $\overline{\text{DREQx}}$ starts the DMA process.

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The assertion level in external burst mode is level sensitive; in external cycle steal mode, it is falling-edge sensitive.

2.8.2 DMA Acknowledge ($\overline{\text{DACK2}}$, $\overline{\text{DACK1}}$)

$\overline{\text{DACKx}}$ is asserted by the DMA to signal to a peripheral that an operand is being transferred in response to a previous transfer request. A delayed version of $\overline{\text{DACKx}}$ is provided to allow operation with differing speed memories. The delayed form of $\overline{\text{DACK2}}$ and $\overline{\text{DACK1}}$ can be selected by setting bits 4 and 5 in the PPARC (See **Section 6 DMA Controller Module**).

2.8.3 DMA Done ($\overline{\text{DONE2}}$, $\overline{\text{DONE1}}$)

This active-low output signal is asserted by the DMA or a peripheral device during any DMA bus cycle to indicate that the last data transfer is being performed. $\overline{\text{DONEx}}$ is an active input in any mode. As an output, it is only active in external request mode. An external pullup resistor is required even during operation in the internal request mode.

2.8.4 Data Transfer Complete ($\overline{\text{DTC}}$)

This active-low bidirectional signal is asserted on all bus cycles (DMA and CPU initiated) as an extra signal in standard bus timing. $\overline{\text{DTC}}$ is multiplexed with FC3, and is selected by setting PPARC bit 3.

2.8.5 DMA Ready ($\overline{\text{RDY2}}$, $\overline{\text{RDY1}}$)

These active-low bidirectional signal is only asserted on DMA single-address transfers to indicate that the device has supplied data or is ready to receive data from memory. $\overline{\text{RDY2}}$ is multiplexed with TIN, and $\overline{\text{RDY1}}$ is multiplexed with TGATE. $\overline{\text{RDY2}}$ is selected by setting PPARC bit 0, and $\overline{\text{RDY1}}$ is selected by setting PPARC bit 1.

2.9 SERIAL MODULE SIGNALS

The following signals are used by the serial module for data and clock signals. See **Section 7 Serial Module** for more information on these signals.

2.9.1 Serial Crystal Oscillator (X2, X1)

These pins furnish the connection to a crystal or external clock, which must be supplied when using the baud rate generator. An external clock can be connected to the X1 pin; X2 is left floating in this case.

2.9.2 Serial External Clock Input (SCLK)

This input can be used as the external clock input for channel A or channel B, bypassing the baud rate generator.

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2.9.3 Receive Data (RxDA, RxDB)

These signals are the receiver serial data input for each channel. Data received on this signal is sampled on the rising edge of the clock source, with the least significant bit received first.

2.9.4 Transmit Data (TxDA, TxDB)

These signals are the transmitter serial data output for each channel. The output is held high ('mark' condition) when the transmitter is disabled, idle, or operating in the local loopback mode. Data is shifted out on this signal at the falling edge of the clock source, with the least significant bit transmitted first.

2.9.5 Clear to Send (CTSA, CTSB)

These active-low signals can be programmed as the clear-to-send inputs for each channel.

2.9.6 Request to Send (RTSA/OP0, RTSB / OP1)

These active-low signals can be programmed as request-to-send outputs or used as discrete outputs.

RTSB, RTSA

When used for this function, these signals function as the request-to-send outputs.

OP1, OP0

When used for this function, these outputs are controlled by the value of bit 1 and bit 0, respectively, in the output port data registers.

2.9.7 Transmitter Ready (TÅRDYA / OP6)

This active-low output can be programmed as the channel A transmitter ready status indicator or used as a discrete output.

TÅRDYA

When used for this function, this signal reflects the complement of the status of bit 2 of the channel A status register. This signal can be used to control parallel data flow by acting as an interrupt to indicate when the transmitter contains a character.

OP6

When used for this function, this output is controlled by bit 6 in the output port data registers.

2.9.8 Receiver Ready (RÅRDYA / FFULLA/ OP4)

This active-low output signal can be programmed as the channel A receiver ready, channel A FIFO full indicator, or a dedicated parallel output.

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$\overline{\text{RxRDYA}}$

When used for this function, this signal reflects the complement of the status of bit 1 of the interrupt status register. This signal can be used to control parallel data flow by acting as an interrupt to indicate when the receiver contains a character.

$\overline{\text{FFULLA}}$

When used for this function, this signal reflects the complement of the status of bit 1 of the interrupt status register. This signal can be used to control parallel data flow by acting as an interrupt to indicate when the receiver FIFO is full.

OP4

When used for this function, this output is controlled by bit 4 in the output port data registers.

2.10 QUEUED SERIAL MODULE SIGNALS

The following external signals are used by the queued serial peripheral module. See **Section 9 QSPM** for additional information on these signals.

2.10.1 Master In Slave Out (MISO)

This bidirectional signal can be the serial data input to the QSPI when the QSPI is the master device, or the the serial data output when using an external master.

2.10.2 Master Out Slave In (MOSI)

This bidirectional signal can be the serial data input to the QSPI when using an external master, or the the serial data output when the QSPI is the master device.

2.10.3 QSPI Serial Clock (QSCLK)

This input is the external clock input for the QSPI.

2.10.4 QSPI Peripheral Chip Select ($\overline{\text{PCS1}}$, $\overline{\text{PCS0}}$)

These output signals are the chip selects for the QSPI.

2.11 TIMER SIGNALS

The following external signals are used by the timer modules. See **Section 8 Timer Modules** for additional information on these signals.

2.11.1 Timer Gate ($\overline{\text{TGATE2}}$)

This active-low input can be programmed to enable and disable the counters and prescalers. $\overline{\text{TGATE}}$ can also be programmed as a simple input.

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2.11.2 Timer Input (TIN)

This input can be programmed as a clock that causes events to occur in the counters and prescalers.

2.11.3 Timer Output (TOUT)

This output drives the various output waveforms generated by the timers.

2.12 TEST SIGNALS

The following signals are used with the on-board test logic defined by the IEEE 1149.1 standard. See **Section 10 IEEE 1149.1 Test Access Port** for more information on the use of these signals.

2.12.1 Test Clock (TCK)

This input provides a clock for on-board test logic defined by the IEEE 1149.1 standard.

2.12.2 Test Mode Select (TMS)

This input controls test mode operations for on-board test logic defined by the IEEE 1149.1 standard.

2.12.3 Test Data In (TDI)

This input is used for serial test instructions and test data for on-board test logic defined by the IEEE 1149.1 standard.

2.12.4 Test Data Out (TDO)

This output is used for serial test instructions and test data for on-board test logic defined by the IEEE 1149.1 standard.

2.13 REAL TIME CLOCK SIGNALS

2.13.1 Battery Switch (BSW)

This signal determines whether the entire chip is powered from V_{CC} or only the real-time clock is powered from V_{BATT} or V_{CC}. See **Section 4 System Integration Module** for more information.

2.13.2 Battery Voltage (V_{BATT})

This pin supplies power to maintain the real-time clock when the rest of the chip is powered down. See **Section 4 System Integration Module** for more information.

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2.13.3 Real Time Clock Output (RMC/RTCOUT)

RTCOUT is an output signal that is selected by setting PPARC bit 2. The function is defined by RCR bits 3 and 4.

2.14 SYSTEM POWER AND GROUND (V_{CC} AND GND)

These pins provide system power and ground to the MC68341. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

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SECTION 3
BUS OPERATION

This section provides a functional description of the bus, the signals that control it, and the bus cycles provided for data transfer operations. It also describes the error and halt conditions, bus arbitration, and reset operation. Operation of the external bus is the same whether the MC68341 or an external device is the bus master; the names and descriptions of bus cycles are from the viewpoint of the bus master. For exact timing specifications, refer to **Section 12 Electrical Characteristics**.

The MC68341 architecture supports byte, word, and long-word operands allowing access to 8- and 16-bit data ports through the use of asynchronous cycles controlled by the SIZ1/SIZ0 outputs and $\overline{\text{DSACK1}}$/$\overline{\text{DSACK0}}$ inputs. The MC68341 requires word and long-word operands to be located in memory on word boundaries. The only type of transfer that can be performed to an odd address is a single-byte transfer, referred to as an odd-byte transfer. For an 8-bit port, multiple bus cycles may be required for an operand transfer due to either misalignment or a word or long-word operand.

The MC68341 also supports basic MC68000 bus interface timing compatibility, in addition to the normal M68300 bus interface timing used by other members of the M68300 family such as the MC68332 and MC68340. This 68000 bus support allows ASICs and other custom logic developed for MC68000-style buses to more easily migrate to the MC68341. In this section, reference to 68000 bus timing refers to bus cycle timing used by the MC68000, MC68EC000, MC68HC000, MC68HC001, MC68008, and MC68010.

3.1 68000 BUS MODE

The MC68341 bus interface is dynamically selectable between M68300 and 68000 bus timing, and is individually controlled for each chip select by programming the Bus Select Register (BSR) in the SIM41. Accesses which match a chip select configured for 68000 bus timing cause an 68000 bus access. All other accesses use normal M68300 bus cycle signals and timing.

NOTE

Bus cycle examples in this section show normal M68300 bus cycle timing unless specifically noted as an 68000 bus cycle.

The three strobe signals $\overline{\text{AS68K}}$, $\overline{\text{UDS}}$, and $\overline{\text{LDS}}$ are dedicated for 68000 bus cycles. These signals assert only for 68000 bus cycles, while $\overline{\text{AS}}$ and $\overline{\text{DS}}$ assert only for M68300 bus cycles. The timing of shared signals $\overline{\text{CSx}}$, $\overline{\text{UWE}}$, and $\overline{\text{LWE}}$ is modified depending on

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selection of the bus cycle type. All other bus interface signals retain the same timing and functionality between the two bus timing modes.

The dual nature of the MC68341 bus interface can result in 68000 bus functionality which is not supported by the original MC68000. Designs which are intended to provide reverse compatibility to the MC68000 should not utilize this superset functionality. The following list notes differences between the 68000 bus timing implemented on the MC68341 and bus timing on the MC68000.

- Address strobe $\overline{\text{AS68K}}$ negates between the read and write cycles of a read-modify-write operation.
- R/$\overline{\text{W}}$ transitions with address timing instead of with address strobe, and does not negate between writes.
- On write cycles, the data bus is driven 1/2 clock sooner (during S2 rather than S3).
- $\overline{\text{DSACKx}}$ and $\overline{\text{BERR}}$ can be recognized on the falling edge of state S2 (one clock earlier than on the MC68000), allowing a three clock 68000 bus cycle.
- Data strobes and write enables are asserted for aproximately one-half clock for a three-clock write cycle.
- 68000 chip selects can be programmed for zero wait-state (three clock bus cycles) internal termination. Programming a 68000 chip select for fast termination (two clock bus cycles) results in undefined strobe timing.
- The MC68341 recognizes late bus error and late retry on 68000 accesses.
- The MC68341 supports dynamic bus sizing on 68000 accesses, allowing both 8-bit ($\overline{\text{DSACK0}}$ termination) and 16-bit ($\overline{\text{DSACK1}}$ termination) port sizes. For an 8-bit port, $\overline{\text{UDS}}$ and $\overline{\text{LDS}}$ must be combined externally to obtain a single 68000 data strobe signal, since $\overline{\text{DS}}$ does not assert for 68000 bus accesses.
- 68000 chip selects are programmed with $\overline{\text{AS68K}}$ timing instead of $\overline{\text{UDS}}$/$\overline{\text{LDS}}$. These selects contain the byte address information of $\overline{\text{UDS}}$/$\overline{\text{LDS}}$.
- Upper and lower write enables ($\overline{\text{UWE}}$ and $\overline{\text{LWE}}$) are provided to support a glueless interface to external SRAM.
- $\overline{\text{DACKx}}$ asserts with $\overline{\text{AS}}$ timing for both M68300 and 68000 bus cycles.

3.2 BUS TRANSFER SIGNALS

The bus transfers information between the MC68341 and external memory or a peripheral device. External devices can accept or provide 8 bits or 16 bits in parallel and must follow the handshake protocol described in this section. The maximum number of bits accepted or provided during a bus transfer is defined as the port width. The MC68341 contains an address bus that specifies the address for the transfer and a data bus that transfers the data. Control signals indicate the beginning and type of the cycle as well as the address space and size of the transfer. The selected device then controls the length of the cycle with the signal(s) used to terminate the cycle. Strobe signals, one for the address bus and another for the data bus, indicate the validity of the address and provide timing information for the data. Both asynchronous and synchronous operation is possible for any port width.

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In asynchronous operation, the bus and control input signals are internally synchronized to the MC68341 clock, introducing a delay. This delay is the time required for the MC68341 to sample an input signal, synchronize the input to the internal clocks, and determine whether it is high or low. In synchronous mode, the bus and control input signals must be timed to setup and hold times. Since no synchronization is needed, bus cycles can be completed in three clock cycles in this mode. Additionally, using the fast-termination option of the chip select signals, two-clock operation is possible.

Furthermore, for all inputs, the MC68341 latches the level of the input during a sample window around the falling edge of the clock signal. This window is illustrated in Figure 3-1, where t_{su} and t_h are the input setup and hold times, respectively. To ensure that an input signal is recognized on a specific falling edge of the clock, that input must be stable during the sample window. If an input makes a transition during the window time period, the level recognized by the MC68341 is not predictable; however, the MC68341 always resolves the latched level to either a logic high or low before using it. In addition to meeting input setup and hold times for deterministic operation, all input signals must obey the protocols described in this section.

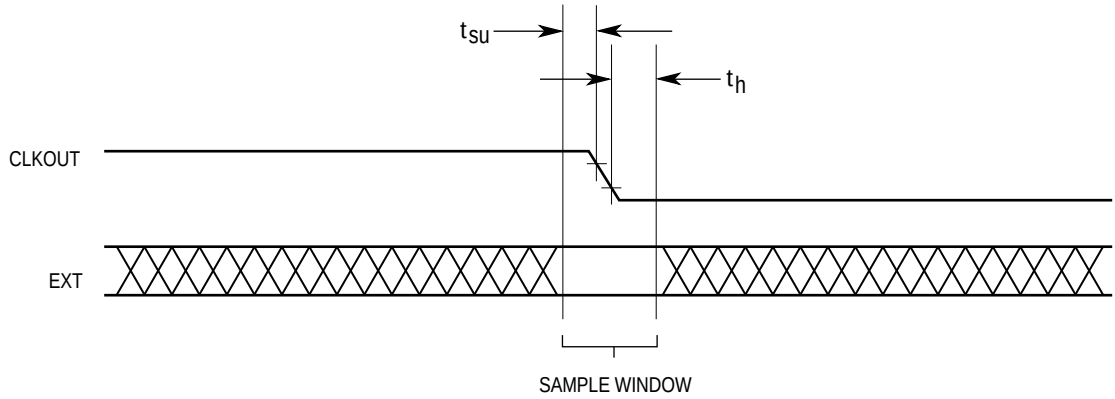

Figure 3-1. Input Sample Window

NOTE

The terms *assert* and *negate* are used throughout this section to avoid confusion when dealing with a mixture of active-low and active-high signals. The term *assert* or *assertion* indicates that a signal is active or true independent of the level represented by a high or low voltage. The term *negate* or *negation* indicates that a signal is inactive or false.

3.2.1 Bus Control Signals

The MC68341 initiates a bus cycle by driving the A31–A0, SIZx, FCx, and R/$\overline{W}$ outputs. At the beginning of a bus cycle, SIZ1 and SIZ0 are driven with FC3–FC0. SIZ1 and SIZ0 indicate the number of bytes remaining to be transferred during an operand cycle (consisting of one or more bus cycles). Table 3-1 lists the encoding of the SIZx signal. These signals are valid while $\overline{AS}$ or $\overline{AS68K}$ is asserted. The R/$\overline{W}$ signal determines the

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direction of the transfer during a bus cycle. Driven at the beginning of a bus cycle, R/$\overline{W}$ is valid while $\overline{AS}$ or $\overline{AS68K}$ is asserted. R/$\overline{W}$ only transitions when a write cycle is preceded by a read cycle or vice versa. The signal may remain low for consecutive write cycles. The $\overline{RMC}$ signal is asserted at the beginning of the first bus cycle of a read-modify-write operation and remains asserted until completion of the final bus cycle of the operation.

Table 3-1. SIZx Signal Encoding

SIZ1	SIZ0	Transfer Size
0	1	Byte
1	0	Word
1	1	Three Bytes
0	0	Long Word

3.2.2 Function Code Signals

FC3–FC0 are outputs that indicate one of 16 address spaces to which the address applies. Fifteen of these spaces are designated as either user or supervisor, program or data, and normal or direct memory access (DMA) spaces. One other address space is designated as CPU space to allow the CPU32 to acquire specific control information not normally associated with read or write bus cycles. FC3–FC0 are valid while $\overline{AS}$ or $\overline{AS68K}$ is asserted.

Function codes (see Table 3-2) can be considered as extensions of the 32-bit address that can provide up to 16 different 4-Gbyte address spaces. Function codes are automatically generated by the CPU32 to select address spaces for data and program at both user and supervisor privilege levels, a CPU address space for processor functions, and an alternate master address space. User programs access only their own program and data areas to increase protection of system integrity and can be restricted from accessing other information. The S-bit in the CPU32 status register is set for supervisor accesses and cleared for user accesses to provide differentiation. Refer to **3.5 CPU Space Cycles** for more information.

Function code FC3 is multiplexed with $\overline{DTC}$, and the ability to use FC3 is lost if $\overline{DTC}$ is selected. If DMA transfers are programmed with FC3 set, this signal can be used externally to distinguish DMA bus activity from CPU accesses.

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Table 3-2. Address Space Encoding

Function Code Bits				Address Spaces
3	2	1	0	
0	0	0	0	Reserved (Motorola)
0	0	0	1	User Data Space
0	0	1	0	User Program Space
0	0	1	1	Reserved (User)
0	1	0	0	Reserved (Motorola)
0	1	0	1	Supervisor Data Space
0	1	1	0	Supervisor Program Space
0	1	1	1	CPU Space
1	x	x	x	DMA Space

3.2.3 Address Bus (A31–A0)

These signals are outputs that define the address of the byte (or the most significant byte) to be transferred during a bus cycle. The MC68341 places the address on the bus at the beginning of a bus cycle. The address is valid while $\overline{AS}$ or $\overline{AS68K}$ is asserted.

3.2.4 Address Strobe ($\overline{AS}$)

This output timing signal indicates the validity of many control signals and the address on the address bus. $\overline{AS}$ is asserted for M68300 bus cycles approximately one-half clock cycle after the beginning of a bus cycle. $\overline{AS}$ remains negated for a 68000 bus cycle.

3.2.5 68000 Address Strobe ($\overline{AS68K}$)

$\overline{AS68K}$ is asserted for 68000 bus cycles approximately one clock cycle after the beginning of a bus cycle. $\overline{AS68K}$ remains negated for normal M68300 bus cycles.

3.2.6 Data Bus (D15–D0)

This bidirectional, nonmultiplexed, parallel bus contains the data being transferred to or from the MC68341. A read or write operation may transfer 8 or 16 bits of data (one or two bytes) in one bus cycle. During a read cycle, the data is latched by the MC68341 on the last falling edge of the clock for that bus cycle. For a write cycle, all 16 bits of the data bus are driven, regardless of the port width or operand size. The MC68341 places the data on the data bus approximately one-half clock cycle after $\overline{AS}$ is asserted in a write cycle, or at the same time as $\overline{AS68K}$ is asserted.

3.2.7 Data Strobe ($\overline{DS}$)

$\overline{DS}$ is an M68300 output timing signal that applies to the data bus. For an M68300 read cycle, the MC68341 asserts $\overline{DS}$ and $\overline{AS}$ simultaneously to signal the external device to place data on the bus. For an M68300 write cycle, $\overline{DS}$ signals to the external device that the data to be written is valid. The MC68341 asserts $\overline{DS}$ approximately one clock cycle

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after the assertion of $\overline{AS}$ during a write cycle. $\overline{DS}$ remains negated during 68000 bus cycles.

3.2.8 Upper and Lower Data Strobes ($\overline{UDS}$ and $\overline{LDS}$)

$\overline{UDS}$ and $\overline{LDS}$ are asserted for the active bytes of a 68000 bus cycle, one-half clock later than $\overline{DS}$ on the corresponding M68300 bus cycle. $\overline{UDS}$ is asserted to select the upper 8 bits of the data bus (D15-D0) and $\overline{LDS}$ is asserted for the lower 8 bits (D8-D0). $\overline{UDS}$ and $\overline{LDS}$ remain negated for normal M68300 bus cycles.

3.2.9 Upper and Lower Write Enables ($\overline{UWE}$ and $\overline{LWE}$)

On a write cycle to a 16-bit port, these active-low output signals indicate when the upper or lower eight bits of the data bus contain valid data. The upper write enable ($\overline{UWE}$) indicates that the upper eight bits of the data bus contain valid data during a write cycle. The lower write enable ($\overline{LWE}$) indicates that the lower eight bits of the data bus contain valid data during a write cycle. The equations of the byte write enables are as follows:

68300 bus cycle:

$$\overline{UWE} = R/\overline{W} + \overline{DS} + A0$$
$$\overline{LWE} = R/\overline{W} + \overline{DS} + (\overline{A0} \bullet SIZ0)$$

68000 bus cycle:

$$\overline{UWE} = R/\overline{W} + \overline{UDS}$$
$$\overline{LWE} = R/\overline{W} + \overline{LDS}$$

3.2.10 Data Transfer Complete ($\overline{DTC}$)

This active-low output signal indicates the last clock of a normally terminated bus cycle. $\overline{DTC}$ does not assert for bus cycles terminated with normal bus error or normal retry terminations, but does assert for late bus error and late retry.

3.2.11 Bus Cycle Termination Signals

The following signals can terminate a bus cycle.

3.2.11.1 DATA TRANSFER AND SIZE ACKNOWLEDGE SIGNALS ($\overline{DSACK1}$ AND $\overline{DSACK0}$). During bus cycles, external devices assert $\overline{DSACK1}$ and/or $\overline{DSACK0}$ as part of the bus protocol. During a read cycle, this signals the MC68341 to terminate the bus cycle and to latch the data. During a write cycle, this indicates that the external device has successfully stored the data and that the cycle may terminate. These signals also indicate to the MC68341 the size of the port for the bus cycle just completed (see Table 3-3). Refer to **3.4.1 Read Cycle** for timing relationships of $\overline{DSACK1}$ and $\overline{DSACK0}$.

Additionally, the system integration module (SIM41) chip select address mask register can be programmed to internally generate $\overline{DSACK1}$ and $\overline{DSACK0}$ for external accesses, eliminating logic required to generate these signals. However, if external $\overline{DSACKx}$ signals are returned earlier than indicated by the EDS and DD bits in the chip select address mask register, the cycle will terminate sooner than programmed. Refer to **Section 4 System Integration Module** for additional information. The SIM41 can alternatively be

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programmed to generate a fast termination cycle, providing a two-cycle external access. Refer to **3.3.6 Fast Termination Cycles** for additional information on these cycles.

3.1.11.2 BUS ERROR ($\overline{\text{BERR}}$). This signal is also a bus cycle termination indicator and can be used in the absence of $\overline{\text{DSACKx}}$ to indicate a bus error condition. $\overline{\text{BERR}}$ can also be asserted in conjunction with $\overline{\text{DSACKx}}$ to indicate a bus error condition, provided it meets the appropriate timing described in this section and in **Section 12 Electrical Characteristics**. Additionally, $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ can be asserted together to indicate a retry termination. Refer to **3.6 Bus Exception Control Cycles** for additional information on the use of these signals.

The internal bus monitor can be used to generate an internal bus error signal for internal and internal-to-external transfers. If the bus cycles of an external bus master are to be monitored, external $\overline{\text{BERR}}$ generation must be provided since the internal bus error monitor has no information about transfers initiated by an external bus master.

3.2.11.3 AUTOVECTOR ($\overline{\text{AVEC}}$). This signal can be used to terminate interrupt acknowledge cycles, indicating that the MC68341 should internally generate a vector (autovector) number to locate an interrupt handler routine. $\overline{\text{AVEC}}$ can be generated either externally or internally by the SIM41 (see **Section 4 System Integration Module** for additional information). $\overline{\text{AVEC}}$ is ignored during all other bus cycles.

3.3 DATA TRANSFER MECHANISM

The MC68341 supports byte, word, and long-word operands, allowing access to 8- and 16-bit data ports through the use of asynchronous cycles controlled by $\overline{\text{DSACK1}}$ and $\overline{\text{DSACK0}}$. The MC68341 also supports byte, word, and long-word operands, allowing access to 8- and 16-bit data ports through the use of synchronous cycles controlled by the fast termination capability of the SIM41.

3.3.1 Dynamic Bus Sizing

The MC68341 dynamically interprets the port size of the addressed device during each bus cycle, allowing operand transfers to or from 8- and 16-bit ports. During an operand transfer cycle, the slave device signals its port size (byte or word) and indicates completion of the bus cycle to the MC68341 through the use of the $\overline{\text{DSACKx}}$ inputs. Refer to Table 3-3 for $\overline{\text{DSACKx}}$ encoding.

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Table 3-3. $\overline{\text{DSACKx}}$ Encoding

$\overline{\text{DSACK1}}$	$\overline{\text{DSACK0}}$	Result
1 (Negated)	1 (Negated)	Insert Wait States in Current Bus Cycle
1 (Negated)	0 (Asserted)	Complete Cycle—Data Bus Port Size Is 8 Bits
0 (Asserted)	1 (Negated)	Complete Cycle—Data Bus Port Size Is 16 Bits
0 (Asserted)	0 (Asserted)	Reserved—Defaults to 16-Bit Port Size Can Be Used for 32-Bit DMA cycles

For example, if the MC68341 is executing an instruction that reads a long-word operand from a 16-bit port, the MC68341 latches the 16 bits of valid data and runs another bus cycle to obtain the other 16 bits. The operation from an 8-bit port is similar, but requires four read cycles. The addressed device uses $\overline{\text{DSACKx}}$ to indicate the port width. For instance, a 16-bit device always returns $\overline{\text{DSACKx}}$ for a 16-bit port (regardless of whether the bus cycle is a byte or word operation).

Dynamic bus sizing requires that the portion of the data bus used for a transfer to or from a particular port size be fixed. A 16-bit port must reside on data bus bits 15–0, and an 8-bit port must reside on data bus bits 15–8. This requirement minimizes the number of bus cycles needed to transfer data to 8- and 16-bit ports and ensures that the MC68341 correctly transfers valid data.

The MC68341 always attempts to transfer the maximum amount of data on all bus cycles; for a word operation, it always assumes that the port is 16 bits wide when beginning the bus cycle. The bytes of operands are designated as shown in Figure 3-2. The most significant byte of a long-word operand is OP0, and OP3 is the least significant byte. The two bytes of a word-length operand are OP0 (most significant) and OP1. The single byte of a byte-length operand is OP0. These designations are used in the figures and descriptions that follow.

Figure 3-2 shows the required organization of data ports on the MC68341 bus for both 8- and 16-bit devices. The four bytes shown in Figure 3-2 are connected through the internal data bus and data multiplexer to the external data bus. The data multiplexer establishes the necessary connections for different combinations of address and data sizes. The multiplexer takes the two bytes of the 16-bit bus and routes them to their required positions. The positioning of bytes is determined by the SIZ1/SIZ0 and A0 outputs. The SIZ1/SIZ0 outputs indicate the number of bytes to be transferred during the current bus cycle (see Table 3-1). The number of bytes transferred during a read or write bus cycle is equal to or less than the size indicated by the SIZ1/SIZ0 outputs, depending on port width. For example, during the first bus cycle of a long-word transfer to a word port, the size outputs indicate that four bytes are to be transferred although only two bytes are moved on that bus cycle.

The address line A0 also affects the operation of the data multiplexer. During an operand transfer, A31–A1 indicate the word base address of that portion of the operand to be

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accessed, and A0 indicates the byte offset from the base (i.e., either odd or even byte). Figure 3-2 lists the bytes required on the data bus for read cycles. The entries shown as OPn are portions of the requested operand that are read or written during that bus cycle and are defined by SIZ1/SIZ0 and A0 for the bus cycle.

OPERAND				
OP0	OP1	OP2	OP3	
31	OP0	OP1	OP2	
	23	OP0	OP1	
		15	OP0	
			7	0

Case	Transfer Case	SIZ1	SIZ0	A0	$\overline{\text{DSACK1}}$	$\overline{\text{DSACK0}}$	Data Bus D15 D8	Data Bus D7 D0
(a)	Byte to Byte	0	1	X	1	0	OP0	(OP0)
(b)	Byte to Word (Even)	0	1	0	0	X	OP0	(OP0)
(c)	Byte to Word (Odd)	0	1	1	0	X	(OP0)	OP0
(d)	Word to Byte (Aligned)	1	0	0	1	0	OP0	(OP1)
(e)	Word to Word (Aligned)	1	0	0	0	X	OP0	OP1
(f)	Long Word to Byte (Aligned)	0	0	0	1	0	OP0	(OP1)
(g)	Long Word to Word (Aligned)	0	0	0	0	X	OP0	OP1

NOTES:
1. Operands in parentheses are ignored by the MC68340 during read cycles.
2. A 3-byte to byte transfer does occur as the second byte transfer of a long-word to byte port transfer.

Figure 3-2. MC68341 Interface to Various Port Sizes

3.3.2 Misaligned Operands

In this architecture, the basic operand size is 16 bits. Operand misalignment refers to whether an operand is aligned on a word boundary or overlaps the word boundary, determined by address line A0. When A0 is low, the address is even and is a word and byte boundary. When A0 is high, the address is odd and is a byte boundary only. A byte operand is properly aligned at any address; a word or long-word operand is misaligned at an odd address.

At most, each bus cycle can transfer a word of data aligned on a word boundary. If the MC68341 transfers a long-word operand over a 16-bit port, the most significant operand word is transferred on the first bus cycle, and the least significant operand word is transferred on a following bus cycle.

The CPU32 restricts all operands (both data and instructions) to be aligned. That is, word and long-word operands must be located on a word or long-word boundary, respectively. The only type of transfer that can be performed to an odd address is a single-byte transfer, referred to as an odd-byte transfer. If a misaligned access is attempted, the CPU32 generates an address error exception, and enters exception processing. Refer to **Section 5 CPU32** for more information on exception processing.

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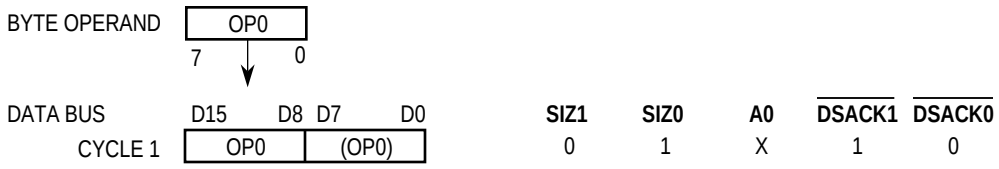
3.3.3 Operand Transfer Cases

The following cases are examples of the allowable alignments of operands to ports.

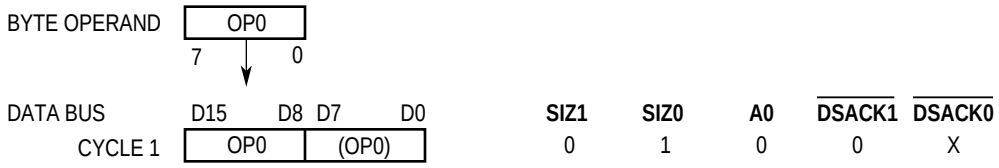
3.3.3.1 BYTE OPERAND TO 8-BIT PORT, ODD OR EVEN (A0 = X). The MC68341 drives the address bus with the desired address and the SIZx pins to indicate a single-byte operand.



For a read operation, the slave responds by placing data on bits 15–8 of the data bus, asserting $\overline{\text{DSACK0}}$ and negating $\overline{\text{DSACK1}}$ to indicate an 8-bit port. The MC68341 then reads the operand byte from bits 15–8 and ignores bits 7–0.

For a write operation, the MC68341 drives the single-byte operand on both bytes of the data bus because it does not know the port size until the $\overline{\text{DSACKx}}$ signals are read. The slave device reads the byte operand from bits 15–8 and places the operand in the specified location. The slave then asserts $\overline{\text{DSACK0}}$ to terminate the bus cycle.

3.3.3.2 BYTE OPERAND TO 16-BIT PORT, EVEN (A0 = 0). The MC68341 drives the address bus with the desired address and the SIZx pins to indicate a single-byte operand.



For a read operation, the slave responds by placing data on bits 15–8 of the data bus and asserting $\overline{\text{DSACK1}}$ to indicate a 16-bit port. The MC68341 then reads the operand byte from bits 15–8 and ignores bits 7–0.

For a write operation, the MC68341 drives the single-byte operand on both bytes of the data bus because it does not know the port size until the $\overline{\text{DSACKx}}$ signals are read. The slave device reads the operand from bits 15–8 of the data bus and uses the address to place the operand in the specified location. The slave then asserts $\overline{\text{DSACK1}}$ to terminate the bus cycle.

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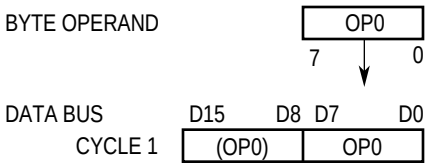
3.3.3.3 BYTE OPERAND TO 16-BIT PORT, ODD (A0 = 1). The MC68341 drives the address bus with the desired address and the SIZx pins to indicate a single-byte operand.

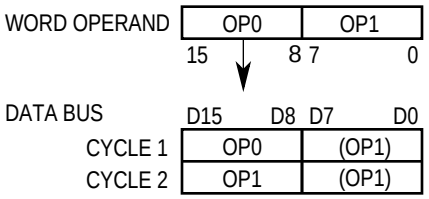


SIZ1	SIZ0	A0	$\overline{\text{DSACK1}}$	$\overline{\text{DSACK0}}$
0	1	1	0	X

For a read operation, the slave responds by placing data on bits 7–0 of the data bus and asserting $\overline{\text{DSACK1}}$ to indicate a 16-bit port. The MC68341 then reads the operand byte from bits 7–0 and ignores bits 15–8.

For a write operation, the MC68341 drives the single-byte operand on both bytes of the data bus because it does not know the port size until the $\overline{\text{DSACKx}}$ signals are read. The slave device reads the operand from bits 7–0 of the data bus and uses the address to place the operand in the specified location. The slave then asserts $\overline{\text{DSACK1}}$ to terminate the bus cycle.

3.3.3.4 WORD OPERAND TO 8-BIT PORT, ALIGNED. The MC68341 drives the address bus with the desired address and the SIZx pins to indicate a word operand.



SIZ1	SIZ0	A0	$\overline{\text{DSACK1}}$	$\overline{\text{DSACK0}}$
1	0	0	1	0
0	1	1	1	0

For a read operation, the slave responds by placing the most significant byte of the operand on bits 15–8 of the data bus and asserting $\overline{\text{DSACK0}}$ to indicate an 8-bit port. The MC68341 reads the most significant byte of the operand from bits 15–8 and ignores bits 7–0. The MC68341 then decrements the transfer size counter, increments the address, and reads the least significant byte of the operand from bits 15–8 of the data bus.

For a write operation, the MC68341 drives the word operand on bits 15–0 of the data bus. The slave device then reads the most significant byte of the operand from bits 15–8 of the data bus and asserts $\overline{\text{DSACK0}}$ to indicate that it received the data but is an 8-bit port. The MC68341 then decrements the transfer size counter, increments the address, and writes the least significant byte of the operand to bits 15–8 of the data bus.

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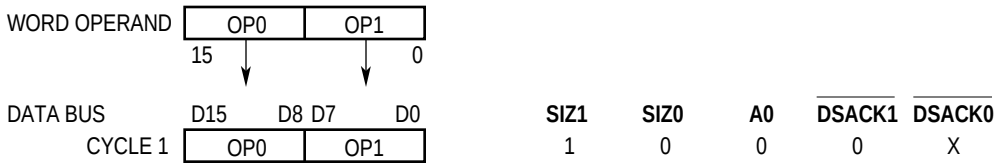
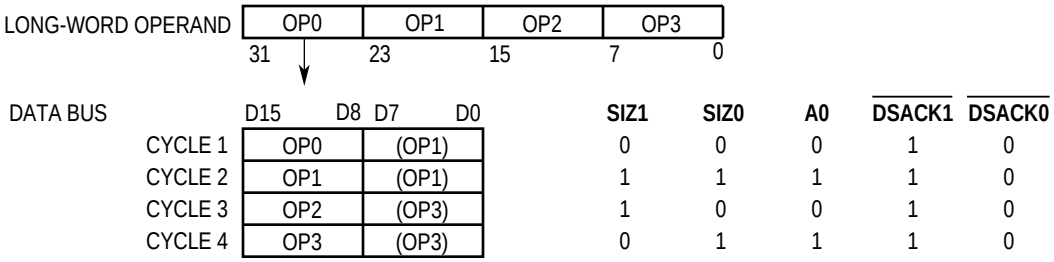
3.3.3.5 WORD OPERAND TO 16-BIT PORT, ALIGNED. The MC68341 drives the address bus with the desired address and the size pins to indicate a word operand.



For a read operation, the slave responds by placing the data on bits 15–0 of the data bus and asserting $\overline{\text{DSACK1}}$ to indicate a 16-bit port. When $\overline{\text{DSACK1}}$ is asserted, the MC68341 reads the data on the data bus and terminates the cycle.

For a write operation, the MC68341 drives the word operand on bits 15–0 of the data bus. The slave device then reads the entire operand from bits 15–0 of the data bus and asserts $\overline{\text{DSACK1}}$ to terminate the bus cycle.

3.3.3.6 LONG-WORD OPERAND TO 8-BIT PORT, ALIGNED. The MC68341 drives the address bus with the desired address and the SIZx pins to indicate a long-word operand.



For a read operation, shown in Figure 3-3, the slave responds by placing the most significant byte of the operand on bits 15–8 of the data bus and asserting $\overline{\text{DSACK0}}$ to indicate an 8-bit port. The MC68341 reads the most significant byte of the operand (byte 0) from bits 15–8 and ignores bits 7–0. The MC68341 then decrements the transfer size counter, increments the address, initiates a new cycle, and reads byte 1 of the operand from bits 15–8 of the data bus. The MC68341 repeats the process of decrementing the transfer size counter, incrementing the address, initiating a new cycle, and reading a byte to transfer the remaining two bytes.

For a write operation, shown in Figure 3-4, the MC68341 drives the two most significant bytes of the operand on bits 15–0 of the data bus. The slave device then reads only the most significant byte of the operand (byte 0) from bits 15–8 of the data bus and asserts $\overline{\text{DSACK0}}$ to indicate reception and an 8-bit port. The MC68341 then decrements the transfer size counter, increments the address, and writes byte 1 of the operand to bits 15–8 of the data bus. The MC68341 continues to decrement the transfer size counter, increment the address, and write a byte to transfer the remaining two bytes to the slave device.

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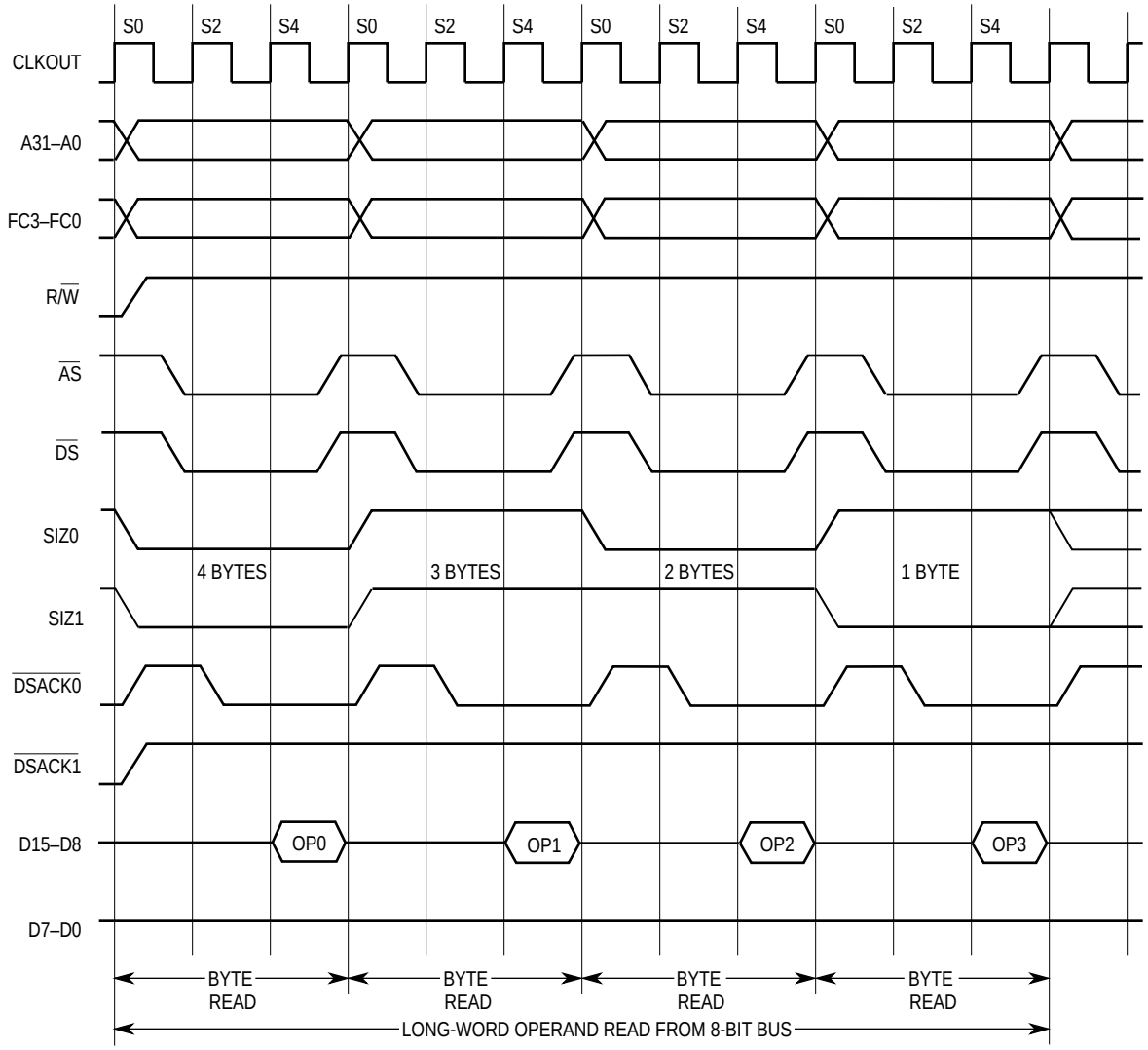

Figure 3-3. Long-Word Operand Read Timing from 8-Bit Port

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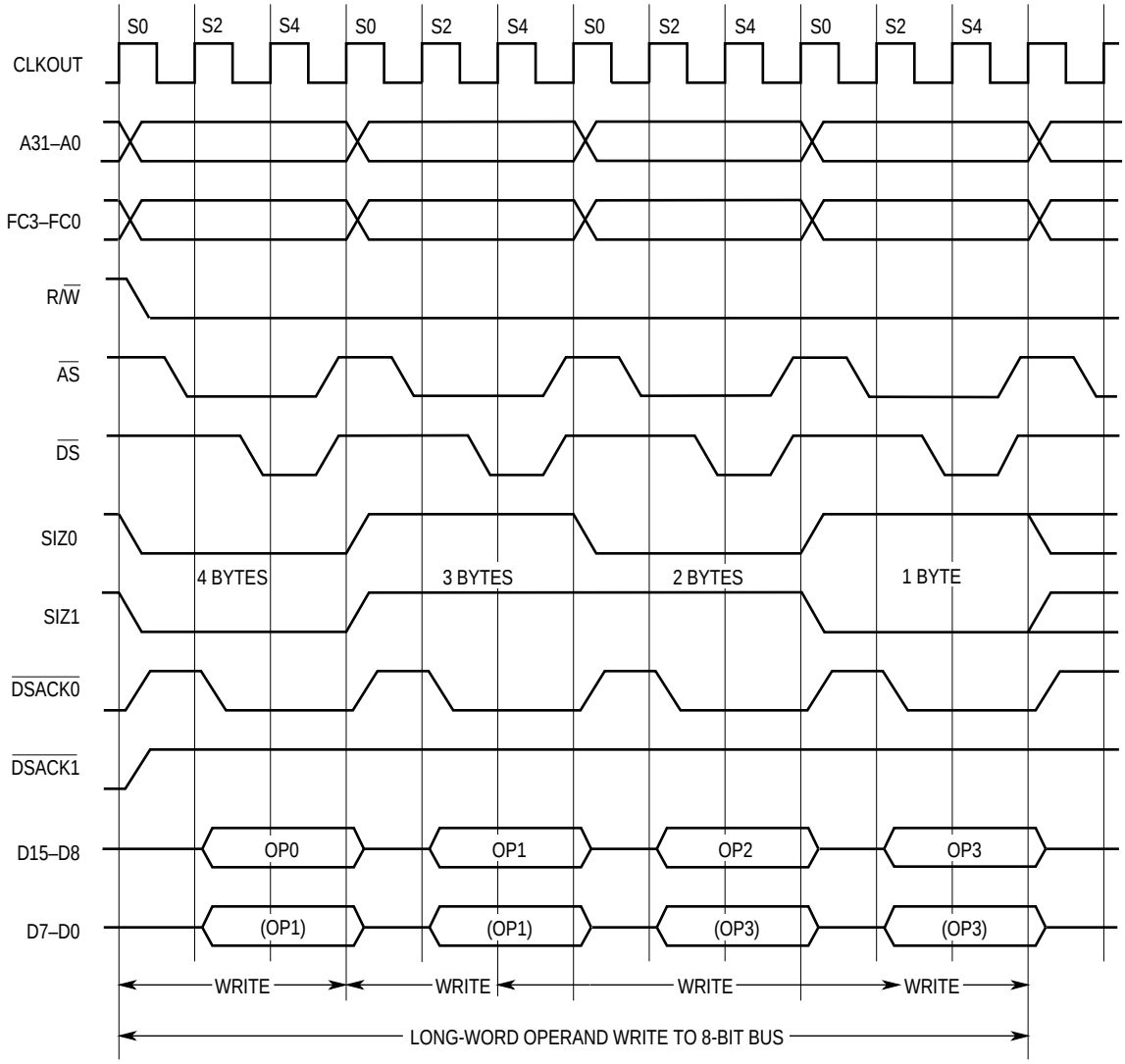
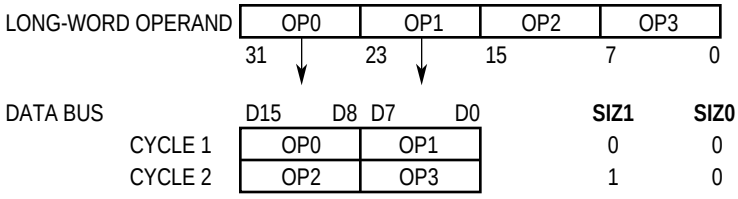


Figure 3-4. Long-Word Operand Write Timing to 8-Bit Port

3.3.3.7 LONG-WORD OPERAND TO 16-BIT PORT, ALIGNED. Figure 3-5 shows both long-word and word read and write timing to a 16-bit port.



			SIZ1	SIZ0	A0	$\overline{\text{DSACK1}}$	$\overline{\text{DSACK0}}$
CYCLE 1	OP0	OP1	0	0	0	0	X
CYCLE 2	OP2	OP3	1	0	0	0	X

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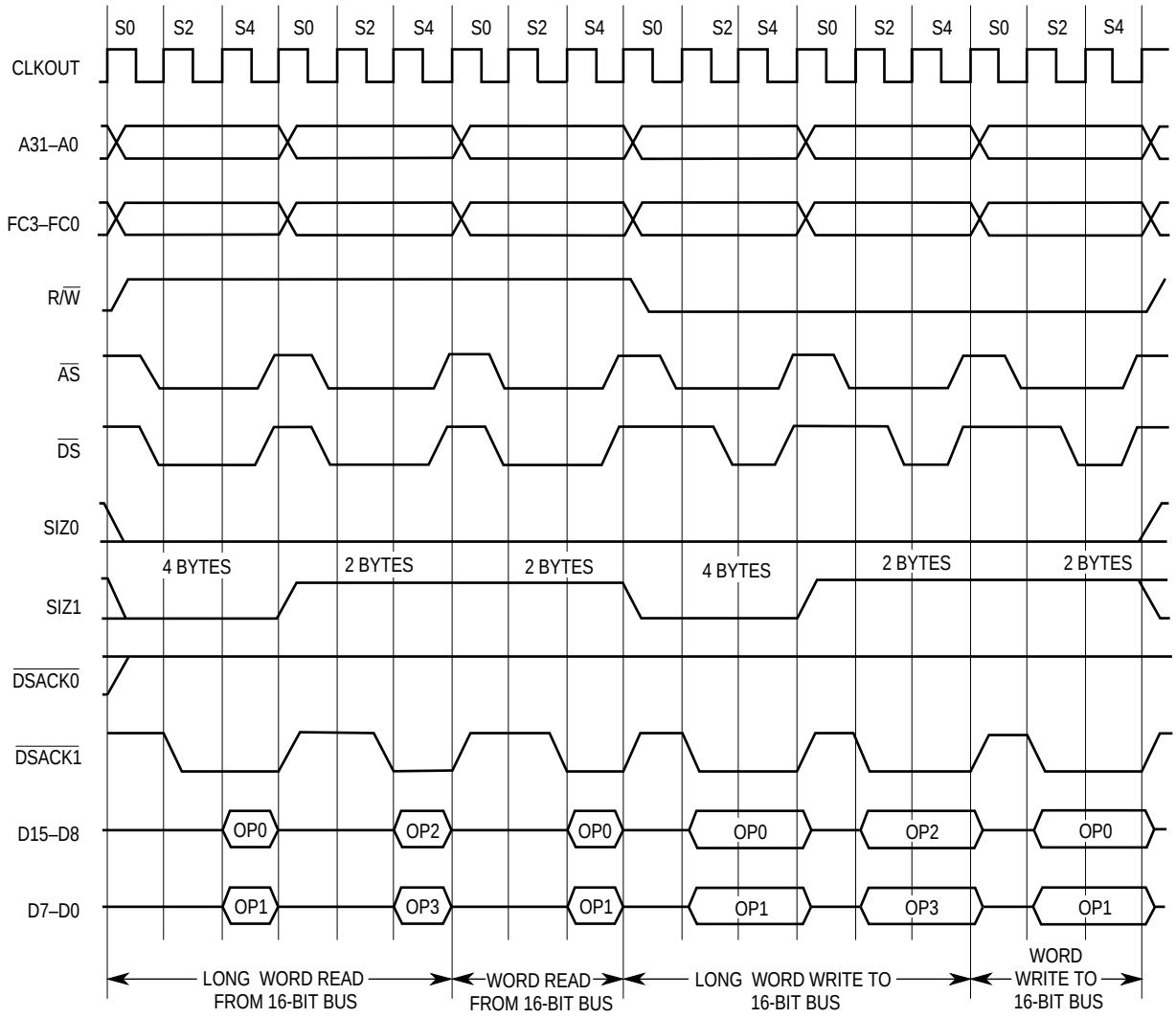

Figure 3-5. Long-Word and Word Read and Write Timing—16-Bit Port

The MC68341 drives the address bus with the desired address and drives the SIZx pins to indicate a long-word operand. For a read operation, the slave responds by placing the two most significant bytes of the operand on bits 15–0 of the data bus and asserting $\overline{\text{DSACK1}}$ to indicate a 16-bit port. The MC68341 reads the two most significant bytes of the operand (bytes 0 and 1) from bits 15–0. The MC68341 then decrements the transfer size counter by 2, increments the address by 2, initiates a new cycle, and reads bytes 2 and 3 of the operand from bits 15–0 of the data bus.

For a write operation, the MC68341 drives the two most significant bytes of the operand on bits 15–0 of the data bus. The slave device then reads the two most significant bytes of the operand (bytes 0 and 1) from bits 15–0 of the data bus and asserts $\overline{\text{DSACK1}}$ to indicate reception and a 16-bit port. The MC68341 then decrements the transfer size counter by 2, increments the address by 2, and writes bytes 2 and 3 of the operand to bits 15–0 of the data bus.

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3.3.4 Bus Operation

The MC68341 bus is asynchronous, allowing external devices connected to the bus to operate at clock frequencies different from the clock for the MC68341. Bus operation uses the handshake lines ($\overline{AS}$, $\overline{DS}$, $\overline{DSACK1}$/$\overline{DSACK0}$, $\overline{BERR}$, and $\overline{HALT}$) to control data transfers. $\overline{AS}$ signals a valid address on the address bus, and $\overline{DS}$ is used as a condition for valid data on a write cycle. Decoding the SIZx outputs and lower address line A0 provides strobes that select the active portion of the data bus. The slave device (memory or peripheral) responds by placing the requested data on the correct portion of the data bus for a read cycle or by latching the data on a write cycle; the slave asserts the $\overline{DSACK1}$/$\overline{DSACK0}$ combination that corresponds to the port size to terminate the cycle. Alternatively, the can be programmed to assert the $\overline{DSACK1}$/$\overline{DSACK0}$ combination internally and respond for the slave. If no slave responds or the access is invalid, external control logic may assert $\overline{BERR}$ to abort the bus cycle or $\overline{BERR}$ with $\overline{HALT}$ to retry the bus cycle.

$\overline{DSACKx}$ can be asserted before the data from a slave device is valid on a read cycle. The length of time that $\overline{DSACKx}$ may precede data must not exceed a specified value in any asynchronous system to ensure that valid data is latched into the MC68341. (See **Section 12 Electrical Characteristics** for timing parameters.) Note that no maximum time is specified from the assertion of $\overline{AS}$ to the assertion of $\overline{DSACKx}$. Although the MC68341 can transfer data in a minimum of three clock cycles when the cycle is terminated with $\overline{DSACKx}$, the MC68341 inserts wait cycles in clock-period increments until $\overline{DSACKx}$ is recognized. $\overline{BERR}$ and/or $\overline{HALT}$ can be asserted after $\overline{DSACKx}$ is asserted. $\overline{BERR}$ and or $\overline{HALT}$ must be asserted within the time specified after $\overline{DSACKx}$ is asserted in any asynchronous system. If this maximum delay time is violated, the MC68341 may exhibit erratic behavior.

3.3.5 Synchronous Operation with $\overline{DSACKx}$

Although cycles terminated with $\overline{DSACKx}$ are classified as asynchronous, cycles terminated with $\overline{DSACKx}$ can also operate synchronously in that signals are interpreted relative to clock edges. The devices that use these cycles must synchronize the response to the MC68341 clock (CLKOUT) to be synchronous. Since the devices terminate bus cycles with $\overline{DSACKx}$, the dynamic bus sizing capabilities of the MC68341 are available. The minimum cycle time for these cycles is also three clocks. To support systems that use the system clock to generate $\overline{DSACKx}$ and other asynchronous inputs, the asynchronous input setup time and the asynchronous input hold time are given. If the setup and hold times are met for the assertion or negation of a signal such as $\overline{DSACKx}$, the MC68341 is guaranteed to recognize that signal level on that specific falling edge of the system clock. If the assertion of $\overline{DSACKx}$ is recognized on a particular falling edge of the clock, valid data is latched into the MC68341 (for a read cycle) on the next falling clock edge if the data meets the data setup time. In this case, the parameter for asynchronous operation can be ignored. The timing parameters are described in **Section 12 Electrical Characteristics**.

If a system asserts $\overline{DSACKx}$ for the required window around the falling edge of S2 and obeys the proper bus protocol by maintaining $\overline{DSACKx}$ (and/or $\overline{BERR}$/$\overline{HALT}$) until and

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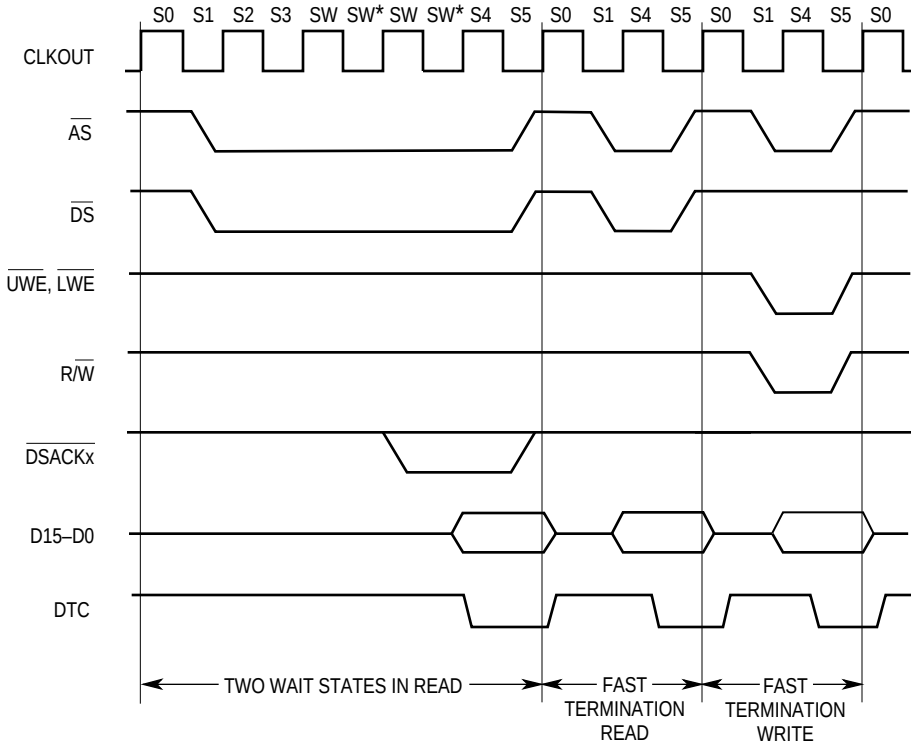
throughout the clock edge that negates $\overline{AS}$ (with the appropriate asynchronous input hold time), no wait states are inserted. The bus cycle runs at its maximum speed for bus cycles terminated with $\overline{DSACKx}$ (three clocks per cycle). When $\overline{BERR}$ (or $\overline{BERR}$ and $\overline{HALT}$) is asserted after $\overline{DSACKx}$, $\overline{BERR}$ (and $\overline{HALT}$) must meet the appropriate setup time prior to the falling clock edge one clock cycle after $\overline{DSACKx}$ is recognized. This setup time is critical, and the MC68341 may exhibit erratic behavior if it is violated. When operating synchronously, the data-in setup and hold times for synchronous cycles may be used instead of the timing requirements for data relative to $\overline{DS}$.

3.3.6 Fast Termination Cycles

With an external device that has a fast access time, the fast termination capability of the chip select circuit can provide a two-clock external bus transfer. Since the chip select circuits are driven from the system clock, the bus cycle termination is inherently synchronized with the system clock. Refer to **Section 4 System Integration Module** for more information on chip selects. Fast termination can only be used for M68300 bus cycles. To use the fast termination option, an external device should be fast enough to have data ready, within the specified setup time, by the falling edge of S4. Figure 3-6 shows the $\overline{DSACKx}$ timing for a read with two wait states, followed by a fast termination read and write. When using the fast termination option, $\overline{DS}$ is asserted only in a read cycle, not in a write cycle.



* $\overline{DSACKx}$ only internally asserted for fast termination cycles.

Figure 3-6. Fast Termination Timing

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3.4 DATA TRANSFER CYCLES

The transfer of data between the MC68341 and other devices involves the following signals:

- Address Bus A31–A0
- Data Bus D15–D0
- Control Signals

The address bus and data bus are parallel, nonmultiplexed buses. The bus master moves data on the bus by issuing control signals, and the bus uses a handshake protocol to ensure correct movement of the data. In all bus cycles, the bus master is responsible for de-skewing all signals it issues at both the start and end of the cycle. In addition, the bus master is responsible for de-skewing the acknowledge and data signals from the slave devices. The following paragraphs define read, write, and read-modify-write cycle operations. Each bus cycle is defined as a succession of states that apply to the bus operation. These states are different from the MC68341 states described for the CPU32. The clock cycles used in the descriptions and timing diagrams of data transfer cycles are independent of the clock frequency. Bus operations are described in terms of external bus states.

3.4.1 M68300 Read Cycle

During a read cycle, the MC68341 receives data from a memory or peripheral device. If the instruction specifies a long-word or word operation, the MC68341 attempts to read two bytes at once. For a byte operation, the MC68341 reads one byte. The section of the data bus from which each byte is read depends on the operand size, address signal A0, and the port size. Refer to **3.3.1 Dynamic Bus Sizing** and **3.3.2 Misaligned Operands** for more information. Figure 3-7 is a flowchart of a word read cycle. Figure 3-8 is an example of a functional timing diagram of a read bus cycle specified in terms of clock periods.

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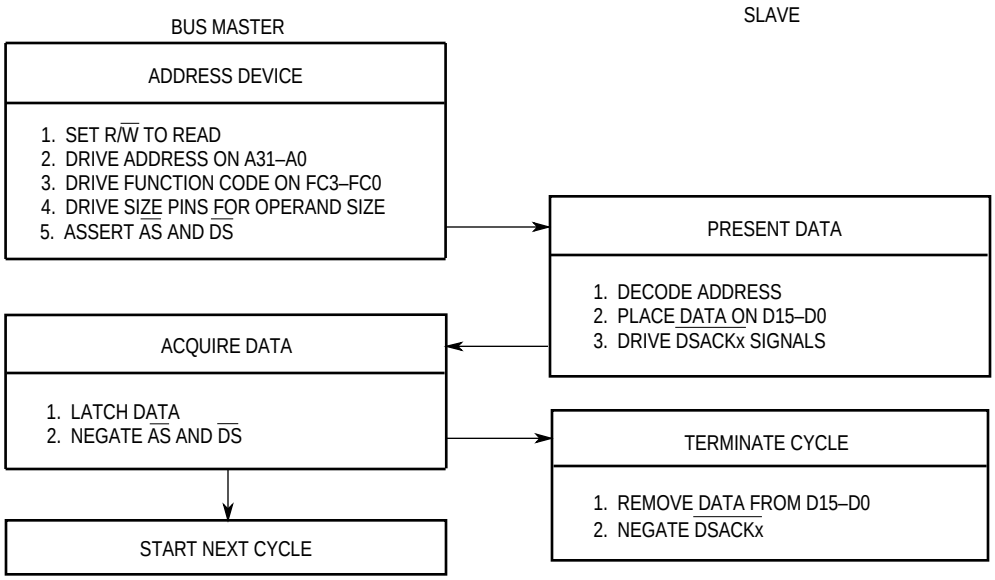

Figure 3-7. Word Read Cycle Flowchart

State 0—The read cycle starts in state 0 (S0). During S0, the MC68341 places a valid address on A31–A0 and valid function codes on FC3–FC0. The function codes select the address space for the cycle. The MC68341 drives R/$\overline{W}$ high for a read cycle. SIZ1/SIZ0 become valid, indicating the number of bytes requested for transfer.

State 1—One-half clock later, in state 1 (S1), the MC68341 asserts $\overline{AS}$ indicating a valid address on the address bus. The MC68341 also asserts $\overline{DS}$ during S1. The selected device uses R/$\overline{W}$, SIZ1 or SIZ0, A0, and $\overline{DS}$ to place its information on the data bus. One or both of the bytes (D15–D8 and D7–D0) are selected by SIZ1/SIZ0 and A0.

State 2—As long as at least one of the $\overline{DSACKx}$ signals is recognized on the falling edge of S2 (meeting the asynchronous input setup time requirement), data is latched on the falling edge of S4, and the cycle terminates.

State 3—If $\overline{DSACKx}$ is not recognized by the start of state 3 (S3), the MC68341 inserts wait states instead of proceeding to states 4 and 5. To ensure that wait states are inserted, both $\overline{DSACK1}$ and $\overline{DSACK0}$ must remain negated throughout the asynchronous input setup and hold times around the end of S2. If wait states are added, the MC68341 continues to sample $\overline{DSACKx}$ on the falling edges of the clock until one is recognized.

State 4—$\overline{DTC}$ asserts during S4 to indicate the end of the current bus cycle. At the falling edge of state 4 (S4), the MC68341 latches the incoming data and samples $\overline{DSACKx}$ to get the port size.

State 5—The MC68341 negates $\overline{AS}$ and $\overline{DS}$ during state 5 (S5), and negates $\overline{DTC}$ after the rising edge of S5. It holds the address valid during S5 to provide address hold time for memory systems. R/$\overline{W}$, SIZ1 and SIZ0, and FC3–FC0 also remain valid throughout S5. The external device keeps its data and $\overline{DSACKx}$ signals asserted until it detects the negation of $\overline{AS}$ or $\overline{DS}$ (whichever it detects first). The device must remove its data and

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negate $\overline{\text{DSACKx}}$ within approximately one clock period after sensing the negation of $\overline{\text{AS}}$ or $\overline{\text{DS}}$. $\overline{\text{DSACKx}}$ signals that remain asserted beyond this limit may be prematurely detected for the next bus cycle.

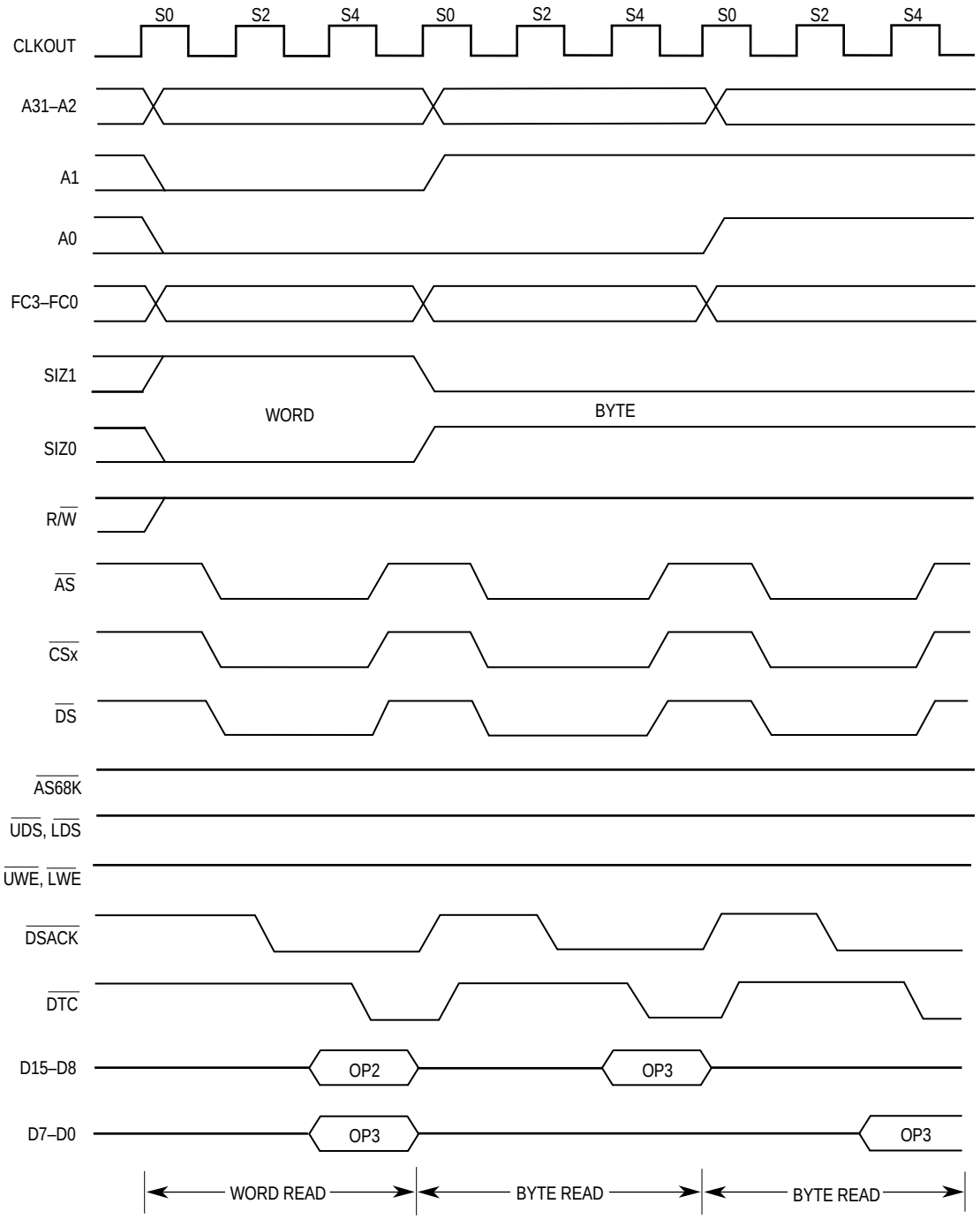

Figure 3-8. Read Cycle Timing

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3.4.2 68000 Read Cycle

During a 68000 read cycle, the 68000 strobes $\overline{AS68K}$, $\overline{UDS}$, and $\overline{LDS}$ are asserted instead of $\overline{AS}$ and $\overline{DS}$, with timing compatible with MC68000 bus cycles. Although the dynamic bus sizing capability of the MC68341 allows assertion of either $\overline{DSACK1}$ or $\overline{DSACK0}$ to terminate the bus cycle as a 16-bit or 8-bit access, $\overline{UDS}$ and $\overline{LDS}$ will always assert for a 16-bit bus. $\overline{UDS}$ and $\overline{LDS}$ must be combined into a single data strobe externally when used with an 8-bit 68000 bus. Figure 3-9 is a flowchart of a 68000 word read cycle. Figure 3-10 is an example of a functional timing diagram of a 68000 read bus cycle specified in terms of clock periods.

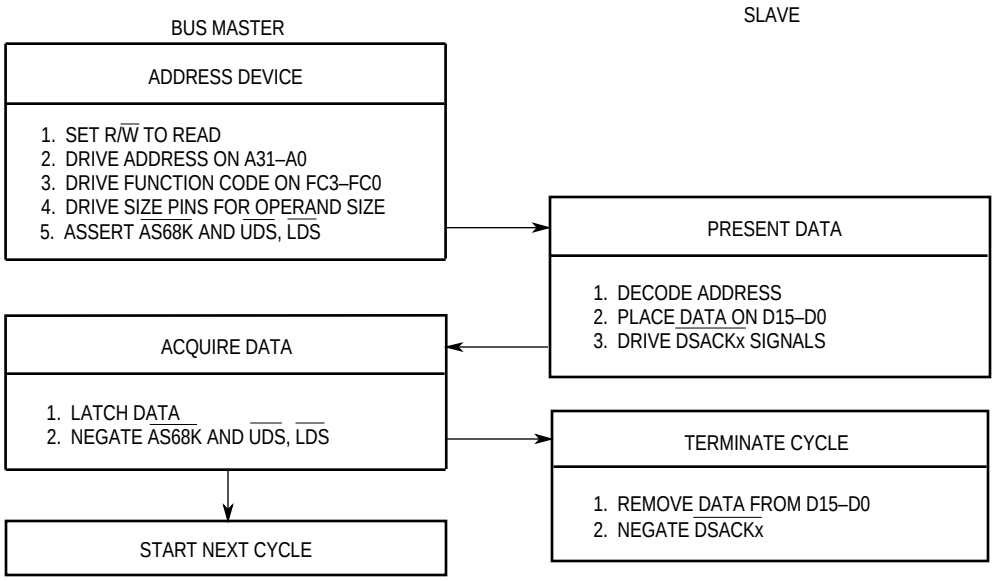

Figure 3-9. 68000 Word Read Cycle Flowchart

State 0—The read cycle starts in state 0 (S0). During S0, the MC68341 places a valid address on A31–A0 and valid function codes on FC3–FC0. The function codes select the address space for the cycle. The MC68341 drives R/$\overline{W}$ high for a read cycle. SIZ1/SIZ0 become valid, indicating the number of bytes requested for transfer.

State 1—The MC68341 issues no new control signals during S1.

State 2—In state 2 (S2), the MC68341 asserts $\overline{AS68K}$ indicating a valid address on the address bus. The MC68341 also asserts $\overline{UDS}$/$\overline{LDS}$ during S2. The selected device uses R/$\overline{W}$, $\overline{UDS}$, and $\overline{LDS}$ to place its information on the data bus. The upper byte (D15–D8) and lower byte (D7–D0) are selected by assertion of $\overline{UDS}$ and $\overline{LDS}$, respectively. If $\overline{DSACKx}$ is recognized on the falling edge of S2 (meeting the asynchronous input setup time requirement), data is latched on the falling edge of S4, and the cycle terminates as a three clock bus cycle.

State 3—If $\overline{DSACKx}$ is not recognized by the start of state 3 (S3), the MC68341 inserts wait states instead of proceeding to states 4 and 5. To ensure that wait states are inserted, both $\overline{DSACK1}$ and $\overline{DSACK0}$ must remain negated throughout the asynchronous

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input setup and hold times around the end of S2. If wait states are added, the MC68341 continues to sample $\overline{\text{DSACKx}}$ on the falling edges of the clock until one is recognized.

State 4—$\overline{\text{DTC}}$ asserts during S4 to indicate the end of the current bus cycle. At the falling edge of state 4 (S4), the MC68341 latches the incoming data and samples $\overline{\text{DSACKx}}$ to get the port size.

State 5—The MC68341 negates $\overline{\text{AS68K}}$ and $\overline{\text{UDS}}/\overline{\text{LDS}}$ during state 5 (S5), and negates $\overline{\text{DTC}}$ after the rising edge of S5. It holds the address valid during S5 to provide address hold time for memory systems. R/$\overline{\text{W}}$, SIZ1 and SIZ0, and FC3–FC0 also remain valid throughout S5. The external device keeps its data and $\overline{\text{DSACKx}}$ signals asserted until it detects the negation of $\overline{\text{AS68K}}$ or $\overline{\text{UDS}}/\overline{\text{LDS}}$ (whichever it detects first). The device must remove its data and negate $\overline{\text{DSACKx}}$ within approximately one clock period after sensing the negation of $\overline{\text{AS68K}}$ or $\overline{\text{UDS}}/\overline{\text{LDS}}$. $\overline{\text{DSACKx}}$ signals that remain asserted beyond this limit may be prematurely detected for the next bus cycle.

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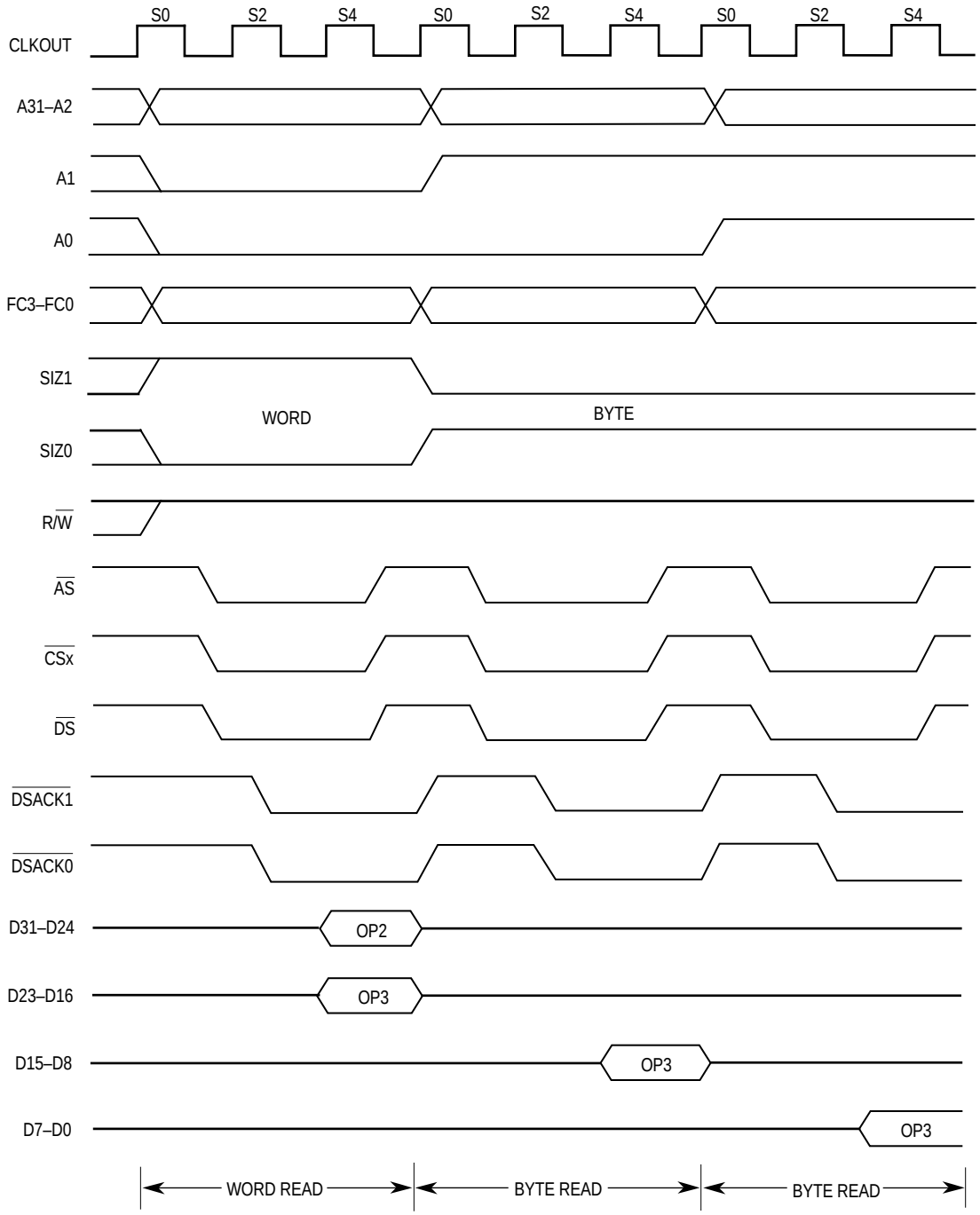

Figure 3-10. 68000 Read Cycle Timing

3.4.3 M68300 Write Cycle

During a write cycle, the MC68341 transfers data to memory or a peripheral device. Figure 3-11 is a flowchart of a word write cycle. Figure 3-12 is an example of a functional timing diagram of a write bus cycle specified in terms of clock periods.

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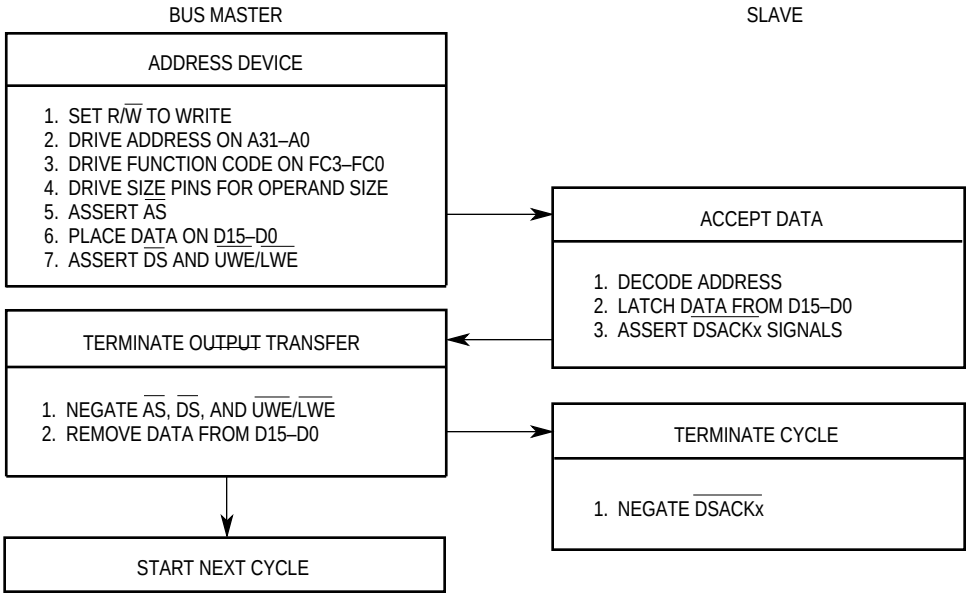

Figure 3-11 Word Write Cycle Flowchart

State 0—The write cycle starts in S0. During S0, the MC68341 places a valid address on A31–A0 and valid function codes on FC3–FC0. The function codes select the address space for the cycle. The MC68341 drives R/$\overline{W}$ low for a write cycle. SIZ1/SIZ0 become valid, indicating the number of bytes to be transferred.

State 1—One-half clock later during S1, the MC68341 asserts $\overline{AS}$, indicating a valid address on the address bus.

State 2—During S2, the MC68341 places the data to be written onto D15–D0, and samples $\overline{DSACKx}$ at the end of S2.

State 3—The MC68341 asserts $\overline{DS}$ during S3, indicating that data is stable on the data bus. Write enable strobes $\overline{UWE}$ and $\overline{LWE}$ for the active bytes of the data bus are also asserted during S3. As long as at least one of the $\overline{DSACKx}$ signals is recognized by the end of S2 (meeting the asynchronous input setup time requirement), the cycle terminates one clock later. If $\overline{DSACKx}$ is not recognized by the start of S3, the MC68341 inserts wait states instead of proceeding to S4 and S5. To ensure that wait states are inserted, both $\overline{DSACK1}$ and $\overline{DSACK0}$ must remain negated throughout the asynchronous input setup and hold times around the end of S2. If wait states are added, the MC68341 continues to sample $\overline{DSACKx}$ on the falling edges of the clock until one is recognized. The selected device uses R/$\overline{W}$, SIZ1/SIZ0, and A0 to latch data from the appropriate byte(s) of D15–D8 and D7–D0. SIZ1/SIZ0 and A0 select the bytes of the data bus. If it has not already done so, the device asserts $\overline{DSACKx}$ to signal that it has successfully stored the data.

State 4—$\overline{DTC}$ asserts during S4 to indicate the end of the current bus cycle.

State 5—The MC68341 negates $\overline{AS}$ and $\overline{DS}$ during S5, and negates $\overline{DTC}$ after the rising edge of S5. It holds the address and data valid during S5 to provide address hold time for memory systems. R/$\overline{W}$, SIZ1/SIZ0, and FC3–FC0 also remain valid throughout S5. The

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external device must keep $\overline{DSACKx}$ asserted until it detects the negation of $\overline{AS}$ or $\overline{DS}$ (whichever it detects first). The device must negate $\overline{DSACKx}$ within approximately one clock period after sensing the negation of $\overline{AS}$ or $\overline{DS}$. $\overline{DSACKx}$ signals that remain asserted beyond this limit may be prematurely detected for the next bus cycle.

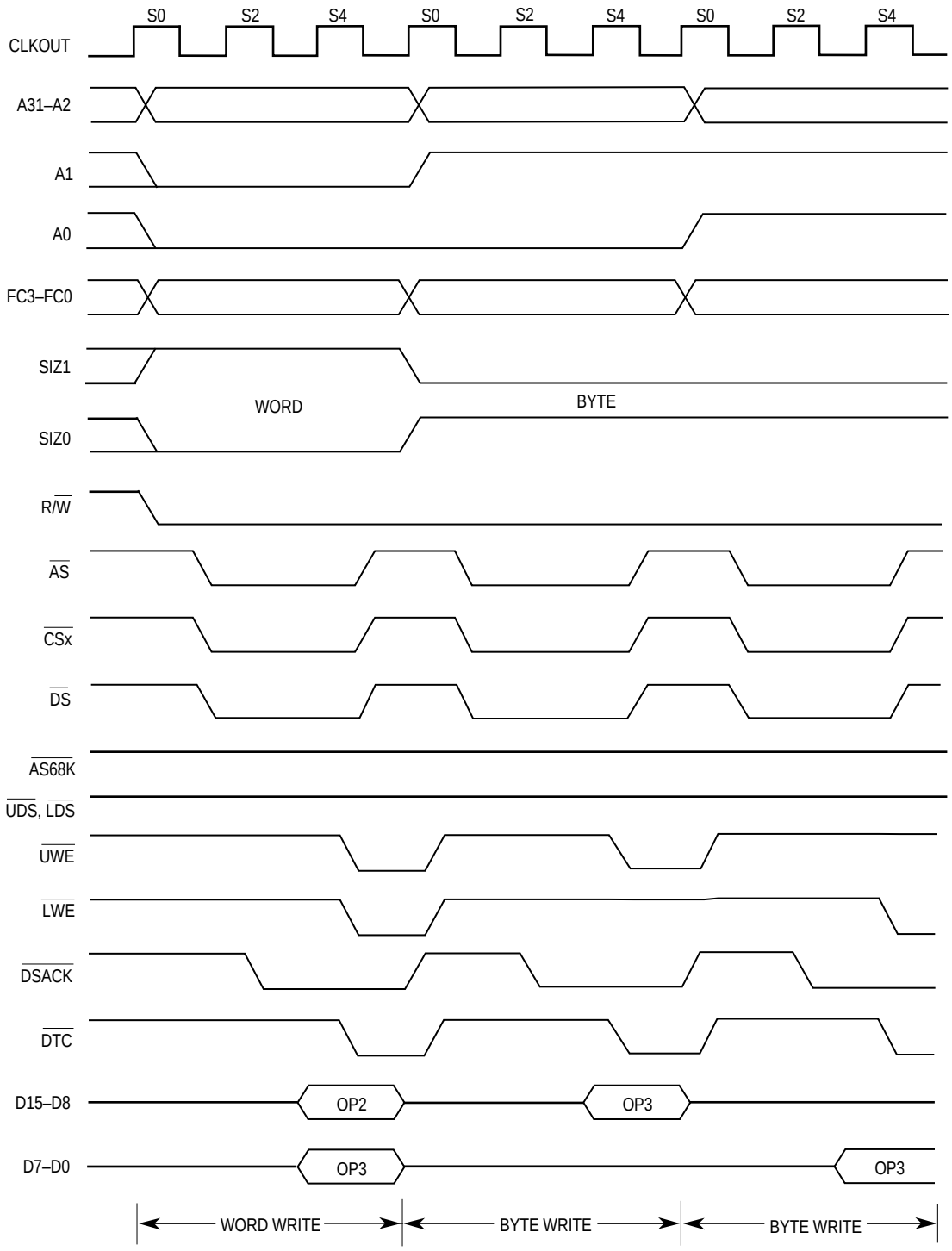

Figure 3-12. M68300 Write Cycle Timing

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3.4.4 68000 Write Cycle

During a 68000 write cycle, the 68000 strobes AS68K, UDS, and LDS are asserted instead of AS and DS, with timing compatible with MC68000 bus cycles. Although the dynamic bus sizing capability of the MC68341 allows assertion of either DSACK1 or DSACK0 to terminate the bus cycle as a 16-bit or 8-bit access, UDS and LDS will always assert for a 16-bit bus. UDS and LDS must be combined into a single data strobe externally when used with an 8-bit 68000 bus. Figure 3-13 is a flowchart of a 68000 word write cycle. Figure 3-14 is an example of a functional timing diagram of a 68000 write bus cycle specified in terms of clock periods.

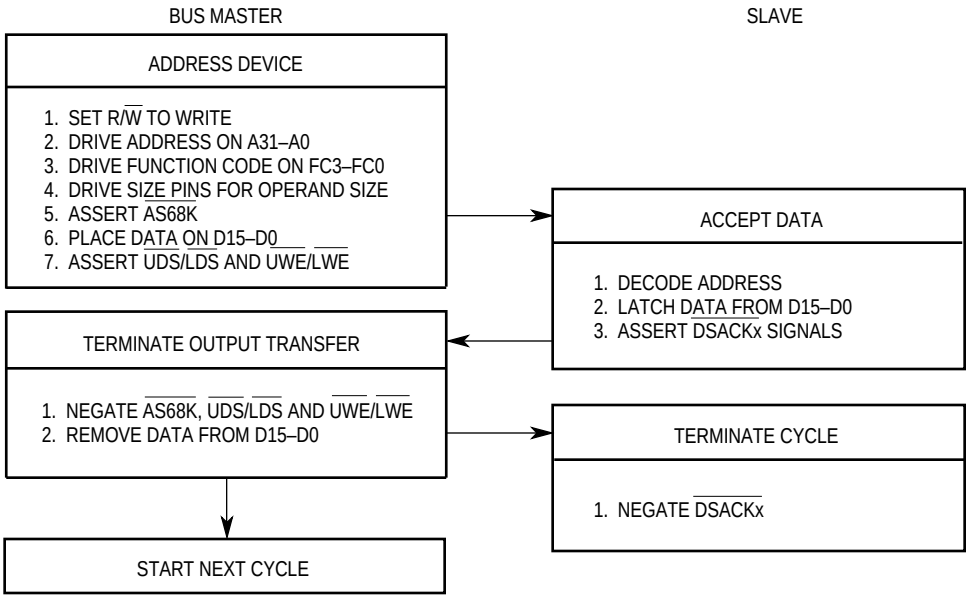

Figure 3-13. 68000 Word Write Cycle Flowchart

State 0—The write cycle starts in S0. During S0, the MC68341 places a valid address on A31–A0 and valid function codes on FC3–FC0. The function codes select the address space for the cycle. The MC68341 drives R/W low for a write cycle. SIZ1/SIZ0 become valid, indicating the number of bytes to be transferred.

State 1—The MC68341 issues no new control signals during S1.

State 2—In S2, the MC68341 asserts AS68K indicating a valid address on the address bus. During S2, the MC68341 places the data to be written onto D15–D0, and samples DSACKx at the end of S2.

State 3—The MC68341 asserts UDS/LDS after the rising edge of S3, indicating that data is stable on the data bus. Write enable strobes UWE and LWE for the active bytes of the data bus are also asserted after the rising edge of S3. As long as DSACKx is recognized by the end of S2 (meeting the asynchronous input setup time requirement), the cycle terminates one clock later. If DSACKx is not recognized by the start of S3, the MC68341 inserts wait states instead of proceeding to S4 and S5. To ensure that wait states are

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inserted, both $\overline{\text{DSACK1}}$ and $\overline{\text{DSACK0}}$ must remain negated throughout the asynchronous input setup and hold times around the end of S2. If wait states are added, the MC68341 continues to sample $\overline{\text{DSACKx}}$ on the falling edges of the clock until one is recognized. The selected device uses R/$\overline{\text{W}}$, $\overline{\text{UDS}}$, and $\overline{\text{LDS}}$ (or $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$) to latch data from the appropriate byte(s) of D15–D8 and D7–D0. If it has not already done so, the device asserts $\overline{\text{DSACKx}}$ to signal that it has successfully stored the data.

State 4—$\overline{\text{DTC}}$ asserts during S4 to indicate the end of the current bus cycle.

State 5—The MC68341 negates $\overline{\text{AS68K}}$ and $\overline{\text{UDS}}$/$\overline{\text{LDS}}$ during S5, and negates $\overline{\text{DTC}}$ after the rising edge of S5. It holds the address and data valid during S5 to provide address hold time for memory systems. R/$\overline{\text{W}}$, SIZ1/SIZ0, and FC3–FC0 also remain valid throughout S5. The external device must keep $\overline{\text{DSACKx}}$ asserted until it detects the negation of $\overline{\text{AS68K}}$ or $\overline{\text{UDS}}$/$\overline{\text{LDS}}$ (whichever it detects first). The device must negate $\overline{\text{DSACKx}}$ within approximately one clock period after sensing the negation of $\overline{\text{AS68K}}$ or $\overline{\text{UDS}}$/$\overline{\text{LDS}}$. $\overline{\text{DSACKx}}$ signals that remain asserted beyond this limit may be prematurely detected for the next bus cycle.

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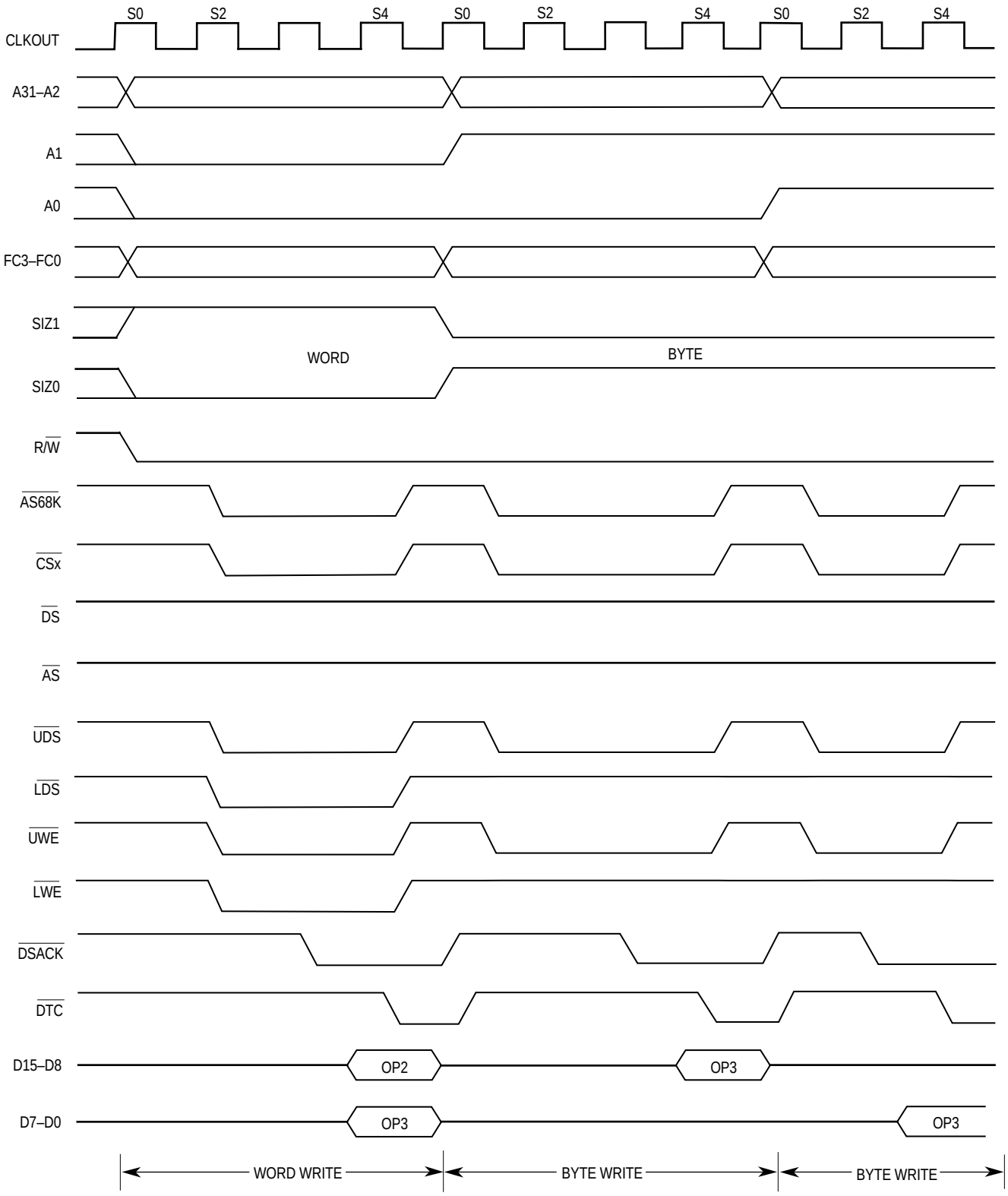

Figure 3-14. 68000 Write Cycle Timing

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3.4.5 Read-Modify-Write Cycle

The read-modify-write cycle performs a read, conditionally modifies the data in the arithmetic logic unit, and may write the data out to memory. In the MC68341, this operation is indivisible, providing semaphore capabilities for multiprocessor systems. During the entire read-modify-write sequence, the MC68341 asserts $\overline{RMC}$ to indicate that an indivisible operation is occurring. The MC68341 does not issue a $\overline{BG}$ signal in response to a $\overline{BR}$ signal during this operation. Figure 3-15 is an example of a functional timing diagram of an M68300 read-modify-write instruction specified in terms of clock periods.

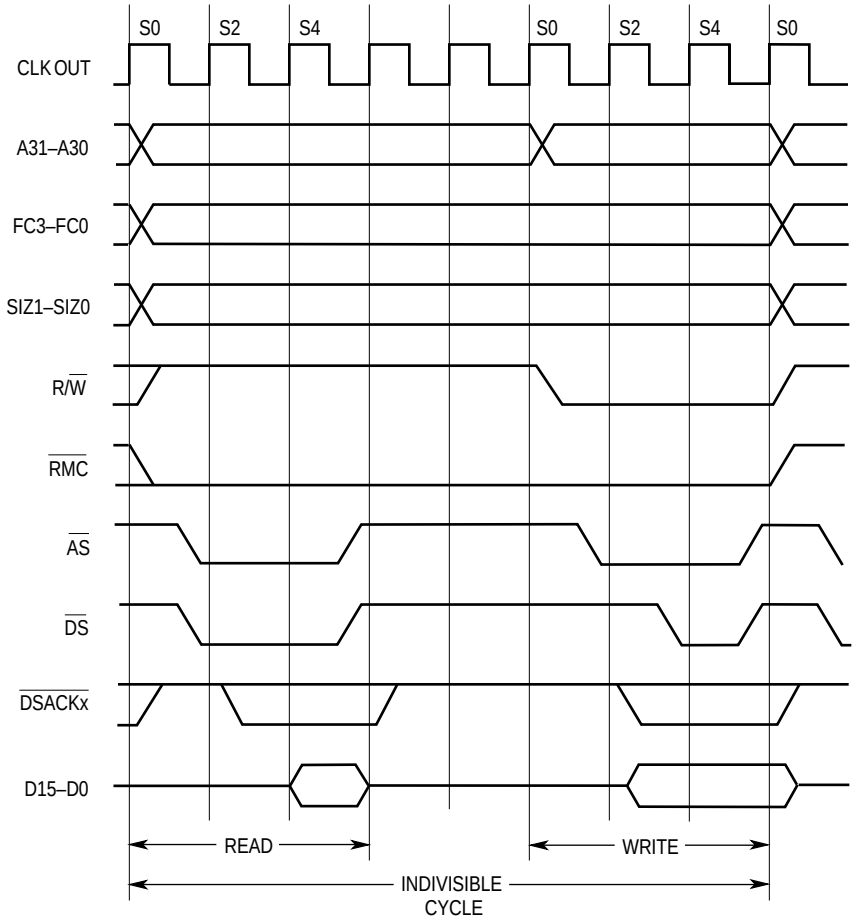

Figure 3-15. Read-Modify-Write Cycle Timing

State 0—The MC68341 asserts $\overline{RMC}$ in S0 to identify a read-modify-write cycle. The MC68341 places a valid address on A31–A0 and valid function codes on FC3–FC0. The function codes select the address space for the operation. SIZ1/SIZ0 become valid in S0 to indicate the operand size. The MC68341 drives R/$\overline{W}$ high for the read cycle.

State 1—One-half clock later during S1, the MC68341 asserts $\overline{AS}$ indicating a valid address on the address bus. The MC68341 also asserts $\overline{DS}$ during S1.

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State 2—The selected device uses R/$\overline{W}$, SIZ1/SIZ0, A0, and $\overline{DS}$ to place information on the data bus. Either or both of the bytes (D15–D8 and D7–D0) are selected by SIZ1/SIZ0 and A0. Concurrently, the selected device may assert $\overline{DSACKx}$.

State 3—As long as at least one of the $\overline{DSACKx}$ signals is recognized by the end of S2 (meeting the asynchronous input setup time requirement), data is latched on the next falling edge of the clock, and the cycle terminates. If $\overline{DSACKx}$ is not recognized by the start of S3, the MC68341 inserts wait states instead of proceeding to S4 and S5. To ensure that wait states are inserted, both $\overline{DSACK1}$ and $\overline{DSACK0}$ must remain negated throughout the asynchronous input setup and hold times around the end of S2. If wait states are added, the MC68341 continues to sample the $\overline{DSACKx}$ signals on the falling edges of the clock until one is recognized.

State 4—At the end of S4, the MC68341 latches the incoming data.

State 5—The MC68341 negates $\overline{AS}$ and $\overline{DS}$ during S5. If more than one read cycle is required to read in the operand(s), S0–S5 are repeated for each read cycle. When finished reading, the MC68341 holds the address, R/$\overline{W}$, and FC3–FC0 valid in preparation for the write portion of the cycle. The external device keeps its data and $\overline{DSACKx}$ signals asserted until it detects the negation of $\overline{AS}$ or $\overline{DS}$ (whichever it detects first). The device must remove the data and negate $\overline{DSACKx}$ within approximately one clock period after sensing the negation of $\overline{AS}$ or $\overline{DS}$. $\overline{DSACKx}$ signals that remain asserted beyond this limit may be prematurely detected for the next portion of the operation.

Idle States—The MC68341 does not assert any new control signals during the idle states, but it may internally begin the modify portion of the cycle at this time. S0–S5 are omitted if no write cycle is required. If a write cycle is required, R/$\overline{W}$ remains in the read mode until S0 to prevent bus conflicts with the preceding read portion of the cycle; the data bus is not driven until S2.

State 0—The MC68341 drives R/$\overline{W}$ low for a write cycle. Depending on the write operation to be performed, the address lines may change during S0.

State 1—In S1, the MC68341 asserts $\overline{AS}$, indicating a valid address on the address bus.

State 2—During S2, the MC68341 places the data to be written onto D15–D0.

State 3—The MC68341 asserts $\overline{DS}$ during S3, indicating stable data on the data bus. As long as at least one of the $\overline{DSACKx}$ signals is recognized by the end of S2 (meeting the asynchronous input setup time requirement), the cycle terminates one clock later. If $\overline{DSACKx}$ is not recognized by the start of S3, the MC68341 inserts wait states instead of proceeding to S4 and S5. To ensure that wait states are inserted, both $\overline{DSACK1}$ and $\overline{DSACK0}$ must remain negated throughout the asynchronous input setup and hold times around the end of S2. If wait states are added, the MC68341 continues to sample $\overline{DSACKx}$ on the falling edges of the clock until one is recognized. The selected device uses R/$\overline{W}$, $\overline{DS}$, SIZ1/SIZ0, and A0 to latch data from the appropriate section(s) of D15–D8 and D7–D0. SIZ1/SIZ0 and A0 select the data bus sections. If it has not already done so, the device asserts $\overline{DSACKx}$ when it has successfully stored the data.

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State 4—The MC68341 issues no new control signals during S4.

State 5—The MC68341 negates $\overline{AS}$ and $\overline{DS}$ during S5. It holds the address and data valid during S5 to provide address hold time for memory systems. R/$\overline{W}$ and FC3–FC0 also remain valid throughout S5. If more than one write cycle is required, states S0–S5 are repeated for each write cycle. The external device keeps $\overline{DSACKx}$ asserted until it detects the negation of $\overline{AS}$ or $\overline{DS}$ (whichever it detects first). The device must remove its data and negate $\overline{DSACKx}$ within approximately one clock period after sensing the negation of $\overline{AS}$ or $\overline{DS}$.

3.5 CPU SPACE CYCLES

FC3–FC0 select user and supervisor program and data areas. The area selected by FC3–FC0 = $7 is classified as the CPU space. The breakpoint acknowledge, LPSTOP broadcast, module base address register access, and interrupt acknowledge cycles described in the following paragraphs use CPU space. The CPU space type, which is encoded on A19–A16 during a CPU space operation, indicates the function that the MC68341 is performing. On the MC68341, four of the encodings are implemented as shown in Figure 3-16. All unused values are reserved by Motorola for additional CPU space types.

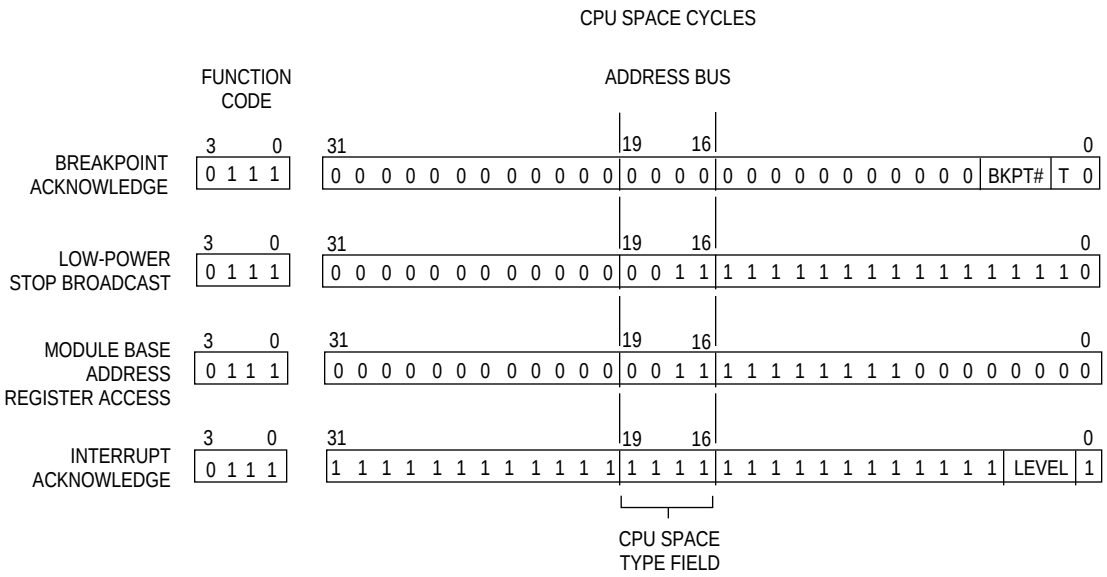

Figure 3-16. CPU Space Address Encoding

3.5.1 Breakpoint Acknowledge Cycle

The breakpoint acknowledge cycle allows external hardware to insert an instruction directly into the instruction pipeline as the program executes. The breakpoint acknowledge cycle is generated by the execution of a breakpoint instruction (BKPT) or the assertion of the $\overline{BKPT}$ pin. The T-bit state (shown in Figure 3-16) differentiates a software breakpoint cycle (T = 0) from a hardware breakpoint cycle (T = 1).

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When a BKPT instruction is executed (software breakpoint), the MC68341 performs a word read from CPU space, type 0, at an address corresponding to the breakpoint number (bits [2–0] of the BKPT opcode) on A4–A2, and the T-bit (A1) is cleared. If this bus cycle is terminated with $\overline{\text{BERR}}$ (i.e., no instruction word is available), the MC68341 then performs illegal instruction exception processing. If the bus cycle is terminated by $\overline{\text{DSACKx}}$, the MC68341 uses the data on D15–D0 (for 16-bit ports) or two reads from D15–D8 (for 8-bit ports) to replace the BKPT instruction in the internal instruction pipeline and then begins execution of that instruction.

When the CPU32 acknowledges a $\overline{\text{BKPT}}$ pin assertion (hardware breakpoint) with background mode disabled, the CPU32 performs a word read from CPU space, type 0, at an address corresponding to all ones on A4–A2 (BKPT#7), and the T-bit (A1) is set. If this bus cycle is terminated by $\overline{\text{BERR}}$, the MC68341 performs hardware breakpoint exception processing. If this bus cycle is terminated by $\overline{\text{DSACKx}}$, the MC68341 ignores data on the data bus and continues execution of the next instruction.

NOTE

The $\overline{\text{BKPT}}$ pin is sampled on the same clock phase as data and is latched with data as it enters the CPU32 pipeline. If $\overline{\text{BKPT}}$ is asserted for only one bus cycle and a pipeline flush occurs before $\overline{\text{BKPT}}$ is detected by the CPU32, $\overline{\text{BKPT}}$ is ignored. To ensure detection of $\overline{\text{BKPT}}$ by the CPU32, $\overline{\text{BKPT}}$ can be asserted until a breakpoint acknowledge cycle is recognized.

The breakpoint operation flowchart is shown in Figure 3-17. Figures 3-18 and 3-19 show the timing diagrams for the breakpoint acknowledge cycle with instruction opcodes supplied on the cycle and with an exception signaled, respectively.

3.5.2 LPSTOP Broadcast Cycle

The low power stop (LPSTOP) broadcast cycle is generated by the CPU32 executing the LPSTOP instruction. Since the external bus interface must get a copy of the interrupt mask level from the CPU32, the CPU32 performs a CPU space type 3 write with the mask level encoded on the data bus, as shown in the following figure. The CPU space type 3 cycle waits for the bus to be available, and is shown externally to indicate to external devices that the MC68341 is going into LPSTOP mode. If an external device requires additional time to prepare for entry into LPSTOP mode, entry can be delayed by asserting $\overline{\text{HALT}}$. The SIM41 provides internal $\overline{\text{DSACKx}}$ response to this cycle. For more information on how the SIM41 responds to LPSTOP mode, see **Section 4 System Integration Module**.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—	—	—	—	—	—	I2	I1	I0

I2–I0—Interrupt Mask Level

The interrupt mask level is encoded on bits 2–0 of the data bus during an LPSTOP broadcast.

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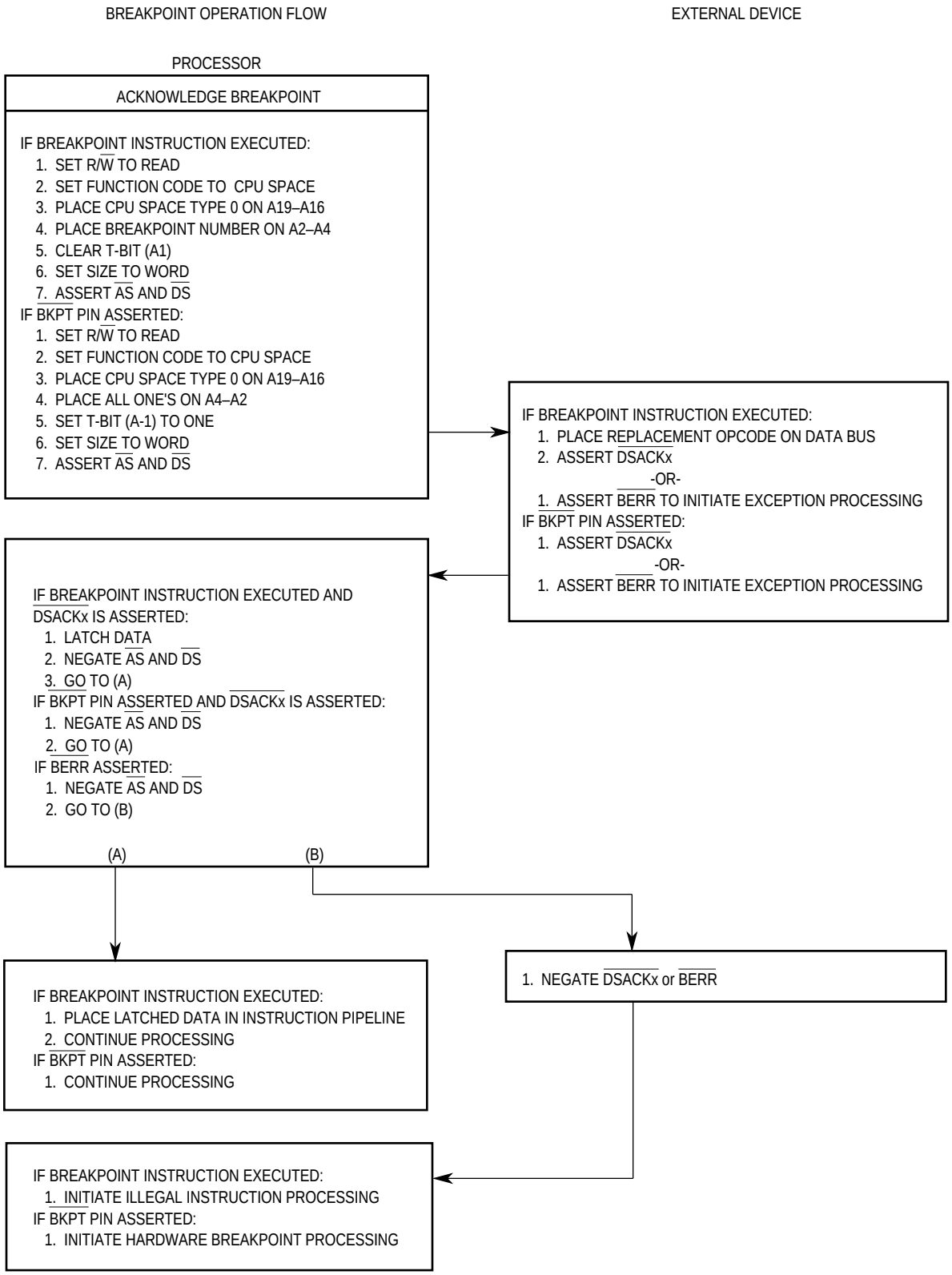

Figure 3-17. Breakpoint Operation Flowchart

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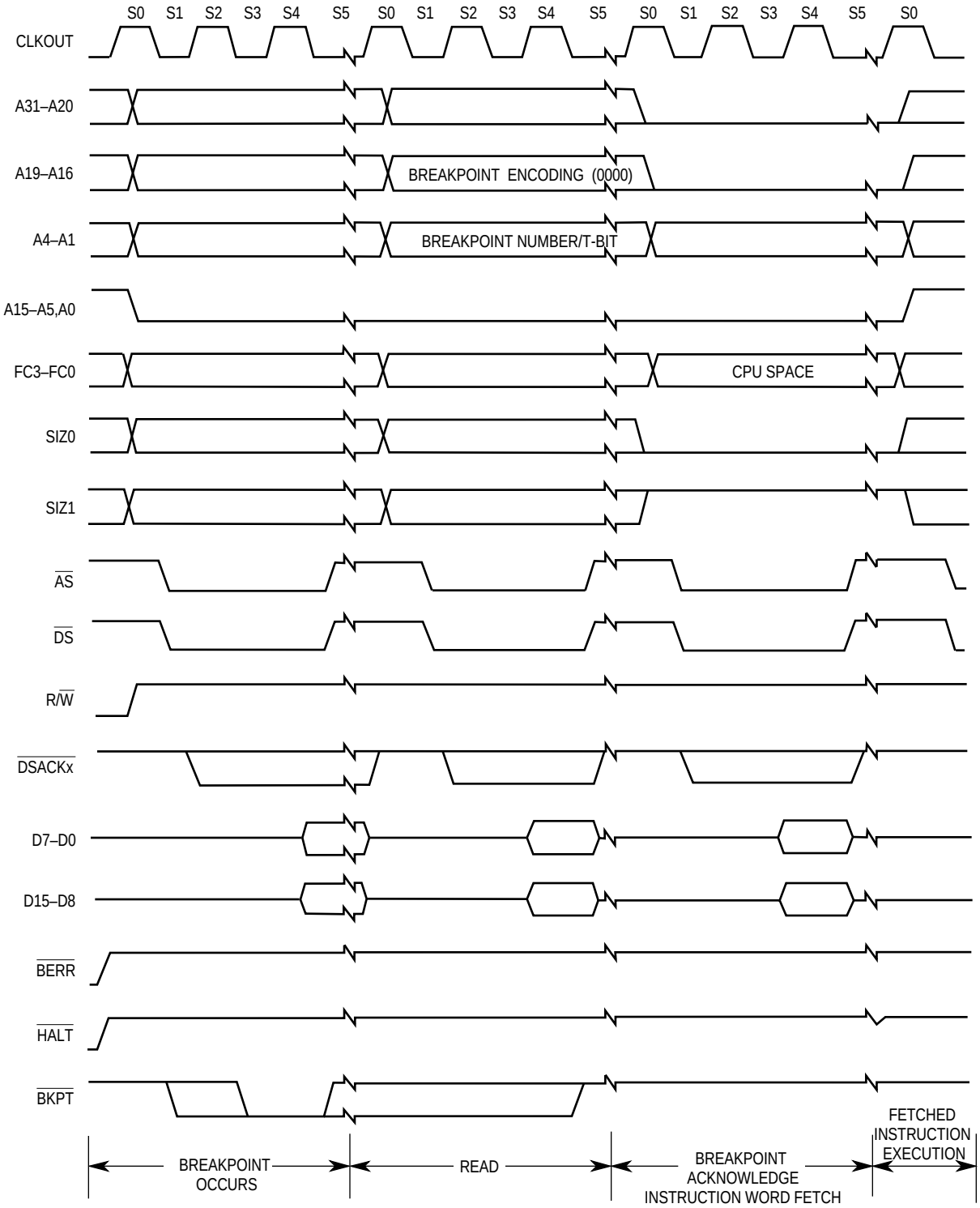

Figure 3-18. Breakpoint Acknowledge Cycle Timing (Opcode Returned)

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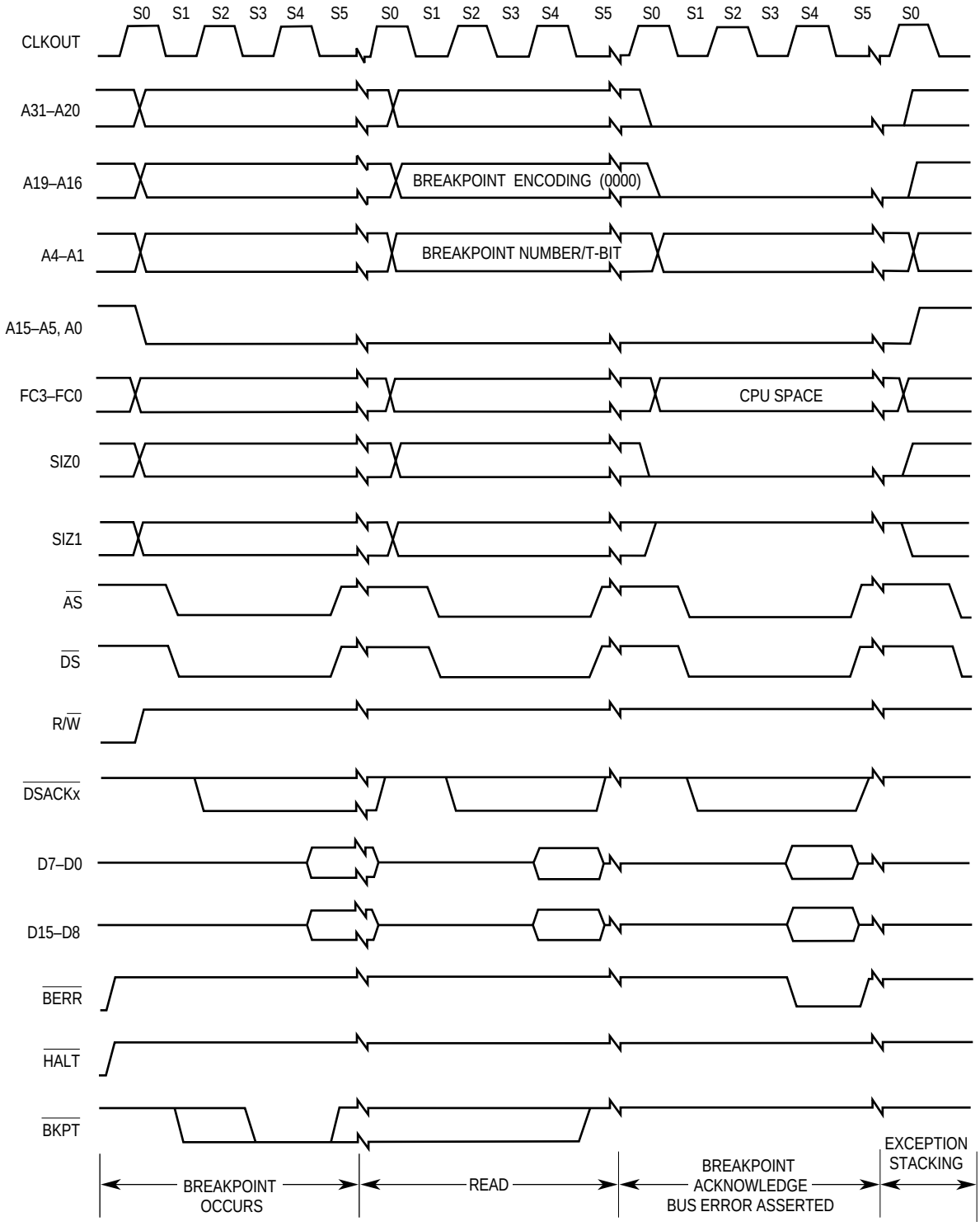

Figure 3-19. Breakpoint Acknowledge Cycle Timing (Exception Signaled)

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3.5.3 Module Base Address Register Access

All internal module registers, including the SIM41, occupy a single 4-Kbyte block that is relocatable along 4-Kbyte boundaries. The location is fixed by writing the desired base address of the SIM41 block to the module base address register using the MOVES instruction. The module base address register is only accessible in CPU space at address $0003FF00. The SFC or DFC register must indicate CPU space (FC3–FC0 = $7), using the MOVEC instruction, before accessing the module base address register. Refer to **Section 4 System Integration Module** for additional information on the module base address register.

3.5.4 Interrupt Acknowledge Bus Cycles

The CPU32 makes an interrupt pending in three cases. The first case occurs when a peripheral device signals the CPU32 (with $\overline{\text{IRQ7}}$–$\overline{\text{IRQ1}}$) that the device requires service and the internally synchronized value on these signals indicates a higher priority than the interrupt mask in the status register. The second case occurs when a transition has occurred in the case of a level 7 interrupt. A recognized level 7 interrupt must be removed for one clock cycle before a second level 7 can be recognized. The third case occurs if, upon returning from servicing a level 7 interrupt, the request level stays at 7 and the processor mask level changes from 7 to a lower level, a second level 7 is recognized. The CPU32 takes an interrupt exception for a pending interrupt within one instruction boundary (after processing any other pending exception with a higher priority). The following paragraphs describe the types of interrupt acknowledge bus cycles that can be executed as part of interrupt exception processing.

3.5.4.1 INTERRUPT ACKNOWLEDGE CYCLE—TERMINATED NORMALLY. When the CPU32 processes an interrupt exception, it performs an interrupt acknowledge cycle to obtain the number of the vector that contains the starting location of the interrupt service routine. Some interrupting devices have programmable vector registers that contain the interrupt vectors for the routines they use. The following paragraphs describe the interrupt acknowledge cycle for these devices. Other interrupting conditions or devices that cannot supply a vector number will use the autovector cycle described in **3.5.4.2 Autovector Interrupt Acknowledge Cycle**.

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The interrupt acknowledge cycle is a read cycle. It differs from the read cycle described in **3.4.1 Read Cycle** in that it accesses the CPU address space. Specifically, the differences are as follows:

1. FC3–FC0 are set to $7 (FC3/FC2/FC1/FC0 = 0111) for CPU address space.
2. A3, A2, and A1 are set to the interrupt request level, and the $\overline{\text{IACKx}}$ strobe corresponding to the current interrupt level is asserted. (Either the function codes and address signals or the $\overline{\text{IACKx}}$ strobes can be monitored to determine that an interrupt acknowledge cycle is in progress and the current interrupt level.)
3. The CPU32 space type field (A19–A16) is set to $F (interrupt acknowledge).
4. Other address signals (A31–A20, A15–A4, and A0) are set to one.
5. The SIZ0/SIZ1 and R/$\overline{\text{W}}$ signals are driven to indicate a single-byte read cycle. The responding device places the vector number on the least significant byte of its data port (for an 8-bit port, the vector number must be on D15–D8; for a 16-bit port, the vector must be on D7–D0) during the interrupt acknowledge cycle. The cycle is then terminated normally with $\overline{\text{DSACKx}}$.

Figure 3-20 is a flowchart of the interrupt acknowledge cycle; Figure 3-21 shows the timing for an interrupt acknowledge cycle terminated with $\overline{\text{DSACKx}}$.

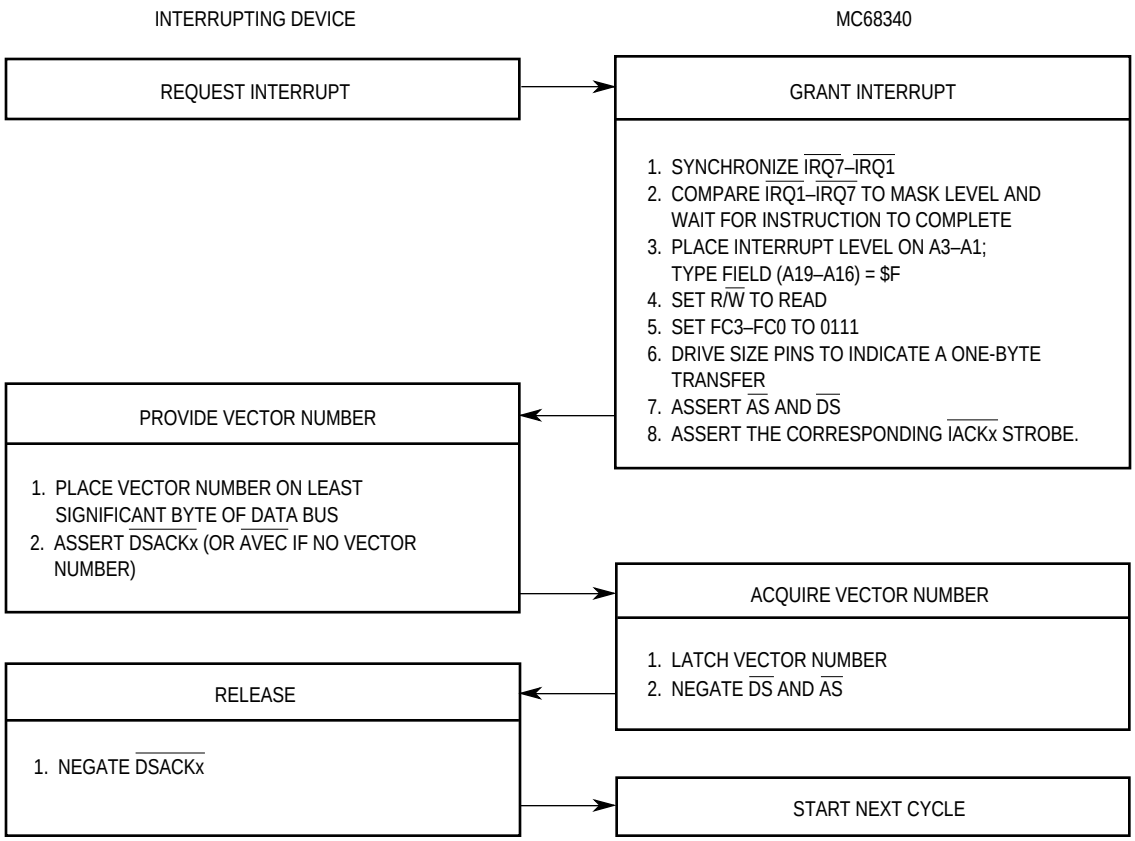

Figure 3-20. Interrupt Acknowledge Cycle Flowchart

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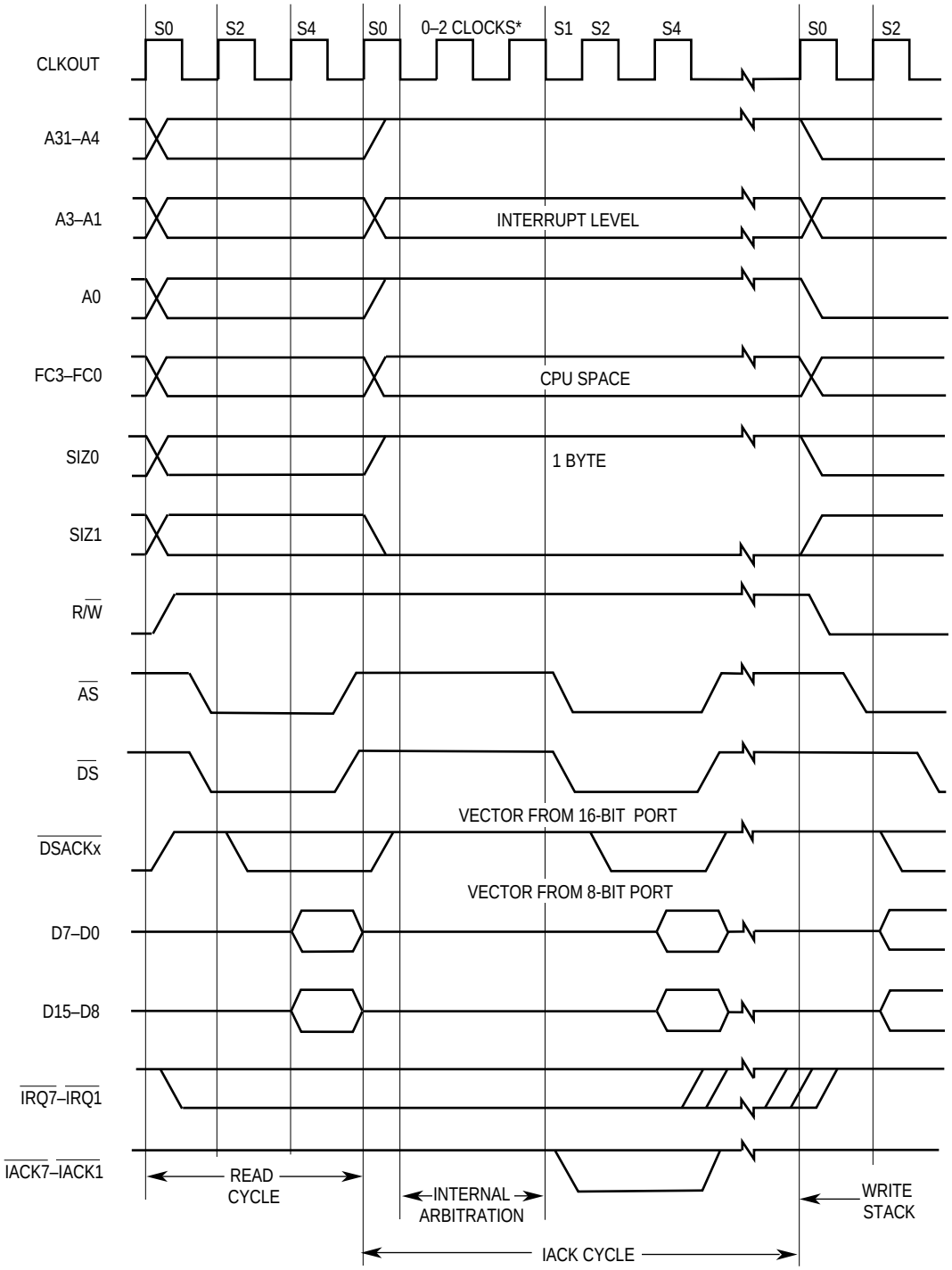

*Internal Arbitration may take between 0–2 clock cycles.

Figure 3-21. Interrupt Acknowledge Cycle Timing

3.5.4.2 AUTOVECTOR INTERRUPT ACKNOWLEDGE CYCLE. When the interrupting device cannot supply a vector number, it requests an automatically generated vector (autovector). Instead of placing a vector number on the data bus and asserting $\overline{\text{DSACKx}}$, the device asserts $\overline{\text{AVEC}}$ to terminate the cycle. If the $\overline{\text{DSACKx}}$ signals are asserted during an interrupt acknowledge cycle terminated by $\overline{\text{AVEC}}$, the $\overline{\text{DSACKx}}$ signals and data

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will be ignored if $\overline{AVEC}$ is asserted before or at the same time as the $\overline{DSACKx}$ signals. The vector number supplied in an autovector operation is derived from the interrupt level of the current interrupt. When $\overline{AVEC}$ is asserted instead of $\overline{DSACKx}$ during an interrupt acknowledge cycle, the MC68341 ignores the state of the data bus and internally generates the vector number (the sum of the interrupt level plus 24 ($18)).

$\overline{AVEC}$ is multiplexed with $\overline{CS0}$. The FIRQ bit in the SIM41 module configuration register controls whether the $\overline{AVEC}/\overline{CS0}$ pin is used as an autovector input or as $\overline{CS0}$ (refer to **Section 4 System Integration Module** for additional information). $\overline{AVEC}$ is only sampled during an interrupt acknowledge cycle. During all other cycles, $\overline{AVEC}$ is ignored. Additionally, $\overline{AVEC}$ can be internally generated for external devices by programming the autovector register. Seven distinct autovectors can be used, corresponding to the seven levels of interrupt available with signals $\overline{IRQ7}$–$\overline{IRQ1}$. Figure 3-22 shows the timing for an autovector operation.

3.5.4.3 SPURIOUS INTERRUPT CYCLE. Requested interrupts, whether internal or external, are arbitrated internally. When no internal module (including the SIM41, which responds for external requests) responds during an interrupt acknowledge cycle by arbitrating for the interrupt acknowledge cycle internally, the spurious interrupt monitor generates an internal bus error signal to terminate the vector acquisition. The MC68341 automatically generates the spurious interrupt vector number (24) instead of the interrupt vector number in this case. When an external device does not respond to an interrupt acknowledge cycle with $\overline{AVEC}$ or $\overline{DSACKx}$, a bus monitor must assert $\overline{BERR}$, which results in the CPU32 taking the spurious interrupt vector. If $\overline{HALT}$ is also asserted, the MC68341 retries the interrupt acknowledge cycle instead of using the spurious interrupt vector.

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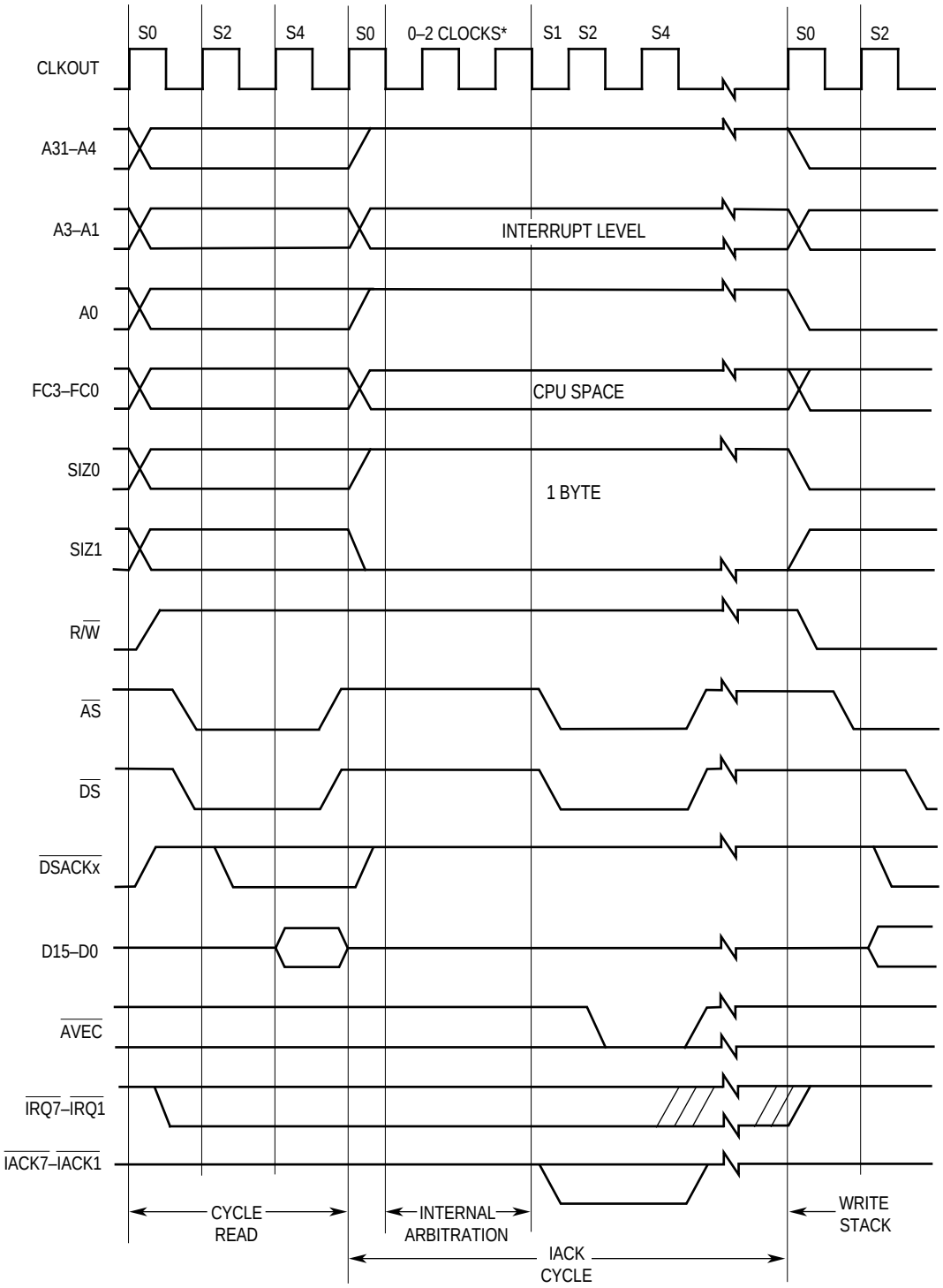

* Internal Arbitration may take between 0–2 clocks.

Figure 3-22 Autovector Operation Timing

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3.6 BUS EXCEPTION CONTROL CYCLES

The bus architecture requires assertion of $\overline{\text{DSACKx}}$ from an external device to signal that a bus cycle is complete. Neither $\overline{\text{DSACKx}}$ nor $\overline{\text{AVEC}}$ is asserted in the following cases:

- $\overline{\text{DSACKx}}$/$\overline{\text{AVEC}}$ is programmed to respond internally.
- The external device does not respond.
- Various other application-dependent errors occur.

The MC68341 provides $\overline{\text{BERR}}$ when no device responds by asserting $\overline{\text{DSACKx}}$/$\overline{\text{AVEC}}$ within an appropriate period of time after the MC68341 asserts $\overline{\text{AS}}$. This mechanism allows the cycle to terminate and the MC68341 to enter exception processing for the error condition. $\overline{\text{HALT}}$ is also used for bus exception control. This signal can be asserted by an external device for debugging purposes to cause single bus cycle operation, or, in combination with $\overline{\text{BERR}}$, a retry of a bus cycle in error. To properly control termination of a bus cycle for a retry or a bus error condition, $\overline{\text{DSACKx}}$, $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ can be asserted and negated with the rising edge of the MC68341 clock. This assures that when two signals are asserted simultaneously, the required setup and hold time for both is met for the same falling edge of the MC68341 clock. This or an equivalent precaution should be designed into the external circuitry to provide these signals. Alternatively, the internal bus monitor could be used. The acceptable bus cycle terminations for asynchronous cycles are summarized in relation to $\overline{\text{DSACKx}}$ assertion as follows (case numbers refer to Table 3-4):

- Normal Termination: $\overline{\text{DSACKx}}$ is asserted; $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ remain negated (case 1).
- Halt Termination: $\overline{\text{HALT}}$ is asserted at the same time as or before $\overline{\text{DSACKx}}$, and $\overline{\text{BERR}}$ remains negated (case 2).
- Bus Error Termination: $\overline{\text{BERR}}$ is asserted in lieu of, at the same time as, or before $\overline{\text{DSACKx}}$ (case 3) or after $\overline{\text{DSACKx}}$ (case 4), and $\overline{\text{HALT}}$ remains negated; $\overline{\text{BERR}}$ is negated at the same time as or after $\overline{\text{DSACKx}}$.
- Retry Termination: $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are asserted in lieu of, at the same time as, or before $\overline{\text{DSACKx}}$ (case 5) or after $\overline{\text{DSACKx}}$ (case 6); $\overline{\text{BERR}}$ is negated at the same time as or after $\overline{\text{DSACKx}}$, and $\overline{\text{HALT}}$ may be negated at the same time as or after $\overline{\text{BERR}}$.

Table 3-4 lists various combinations of control signal sequences and the resulting bus cycle terminations. To ensure predictable operation, $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ should be negated according to the specifications given in **Section 12 Electrical Characteristics**. $\overline{\text{DSACKx}}$ $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ may be negated after $\overline{\text{AS}}$. If $\overline{\text{DSACKx}}$ or $\overline{\text{BERR}}$ remain asserted into S2 of the next bus cycle, that cycle may be terminated prematurely.

EXAMPLE A: A system uses a bus monitor timer to terminate accesses to an unpopulated address space. The timer asserts $\overline{\text{BERR}}$ after timeout (case 3).

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EXAMPLE B: A system uses error detection and correction on RAM contents. The designer may:

1. Delay $\overline{\text{DSACKx}}$ until data is verified and assert $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ simultaneously to indicate to the MC68341 to automatically retry the error cycle (case 5), or if data is valid, assert $\overline{\text{DSACKx}}$ (case 1).
2. Delay $\overline{\text{DSACKx}}$ until data is verified and assert $\overline{\text{BERR}}$ with or without $\overline{\text{DSACKx}}$ if data is in error (case 3). This initiates exception processing for software handling of the condition.
3. Return $\overline{\text{DSACKx}}$ prior to data verification; if data is invalid, $\overline{\text{BERR}}$ is asserted on the next clock cycle (case 4). This initiates exception processing for software handling of the condition.
4. Return $\overline{\text{DSACKx}}$ prior to data verification; if data is invalid, assert $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ on the next clock cycle (case 6). The memory controller can then correct the RAM prior to or during the automatic retry.

Table 3-4. $\overline{\text{DSACKx}}$, $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ Assertion Results

Case Num	Control Signal	Asserted on Rising Edge of State		Result
		N	N + 2	
1	$\overline{\text{DSACKx}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA NA	S NA X	Normal cycle terminate and continue.
2	$\overline{\text{DSACKx}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA A/S	S NA S	Normal cycle terminate and halt; continue when $\overline{\text{HALT}}$ negated.
3	$\overline{\text{DSACKx}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA/A A NA	X S X	Terminate and take bus error exception, possibly deferred.
4	$\overline{\text{DSACKx}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA NA	X A NA	Terminate and take bus error exception, possibly deferred.
5	$\overline{\text{DSACKx}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	NA/A A A/S	X S S	Terminate and retry when $\overline{\text{HALT}}$ negated.
6	$\overline{\text{DSACKx}}$ $\overline{\text{BERR}}$ $\overline{\text{HALT}}$	A NA NA	X A A	Terminate and retry when $\overline{\text{HALT}}$ negated.

NOTES:

N — Number of the current even bus state (e.g., S2, S4, etc.)
A — Signal is asserted in this bus state
NA — Signal is not asserted in this state
X — Don't care
S — Signal was asserted in previous state and remains asserted in this state

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3.6.1 Bus Errors

$\overline{\text{BERR}}$ can be used to abort the bus cycle and the instruction being executed. $\overline{\text{BERR}}$ takes precedence over $\overline{\text{DSACKx}}$ provided it meets the timing constraints described in **Section 12 Electrical Characteristics**. If $\overline{\text{BERR}}$ does not meet these constraints, it may cause unpredictable operation of the MC68341. If $\overline{\text{BERR}}$ remains asserted into the next bus cycle, it may cause incorrect operation of that cycle. When $\overline{\text{BERR}}$ is issued to terminate a bus cycle, the MC68341 can enter exception processing immediately following the bus cycle, or it can defer processing the exception.

The instruction prefetch mechanism requests instruction words from the bus controller before it is ready to execute them. If a bus error occurs on an instruction fetch, the MC68341 does not take the exception until it attempts to use that instruction word. Should an intervening instruction cause a branch or should a task switch occur, the bus error exception does not occur. The bus error condition is recognized during a bus cycle in any of the following cases:

- $\overline{\text{DSACKx}}$ and $\overline{\text{HALT}}$ are negated, and $\overline{\text{BERR}}$ is asserted.
- $\overline{\text{HALT}}$ and $\overline{\text{BERR}}$ are negated, and $\overline{\text{DSACKx}}$ is asserted. $\overline{\text{BERR}}$ is then asserted within one clock cycle ($\overline{\text{HALT}}$ remains negated).
- $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ are asserted simultaneously, indicating a retry.

When the MC68341 recognizes a bus error condition, it terminates the current bus cycle in the normal way. Figure 3-23 shows the timing of a bus error for the case in which $\overline{\text{DSACKx}}$ is not asserted. Figure 3-24 shows the timing for a bus error that is asserted after $\overline{\text{DSACKx}}$. Exceptions are taken in both cases. Refer to **Section 5 CPU32** for details of bus error exception processing.

In the second case, in which $\overline{\text{BERR}}$ is asserted after $\overline{\text{DSACKx}}$ is asserted, $\overline{\text{BERR}}$ must be asserted within the time specified for purely asynchronous operation, or it must be asserted and remain stable during the sample window around the next falling edge of the clock after $\overline{\text{DSACKx}}$ is recognized. If $\overline{\text{BERR}}$ is not stable at this time, the MC68341 may exhibit erratic behavior. $\overline{\text{BERR}}$ has priority over $\overline{\text{DSACKx}}$. In this case, data may be present on the bus, but it may not be valid. This sequence can be used by systems that have memory error detection and correction logic and by external cache memories.

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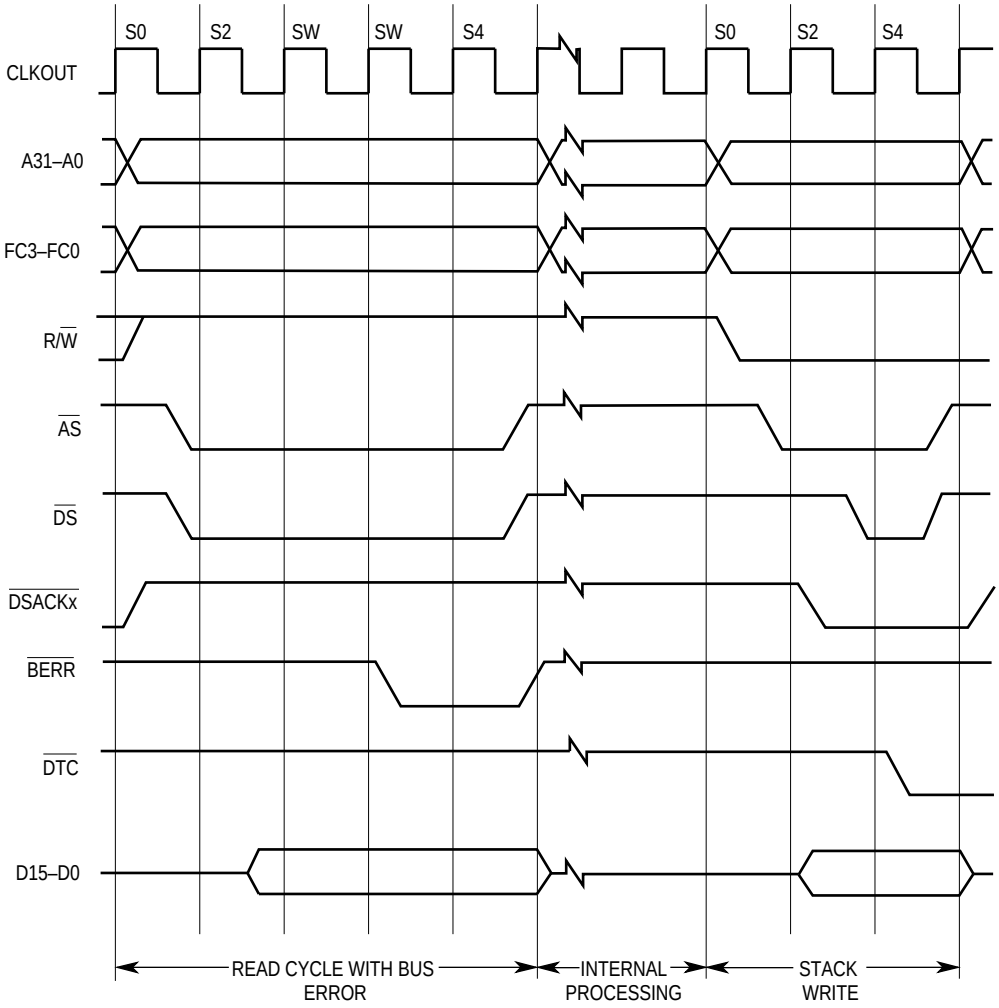

Figure 3-23. Bus Error without DSACKÅ

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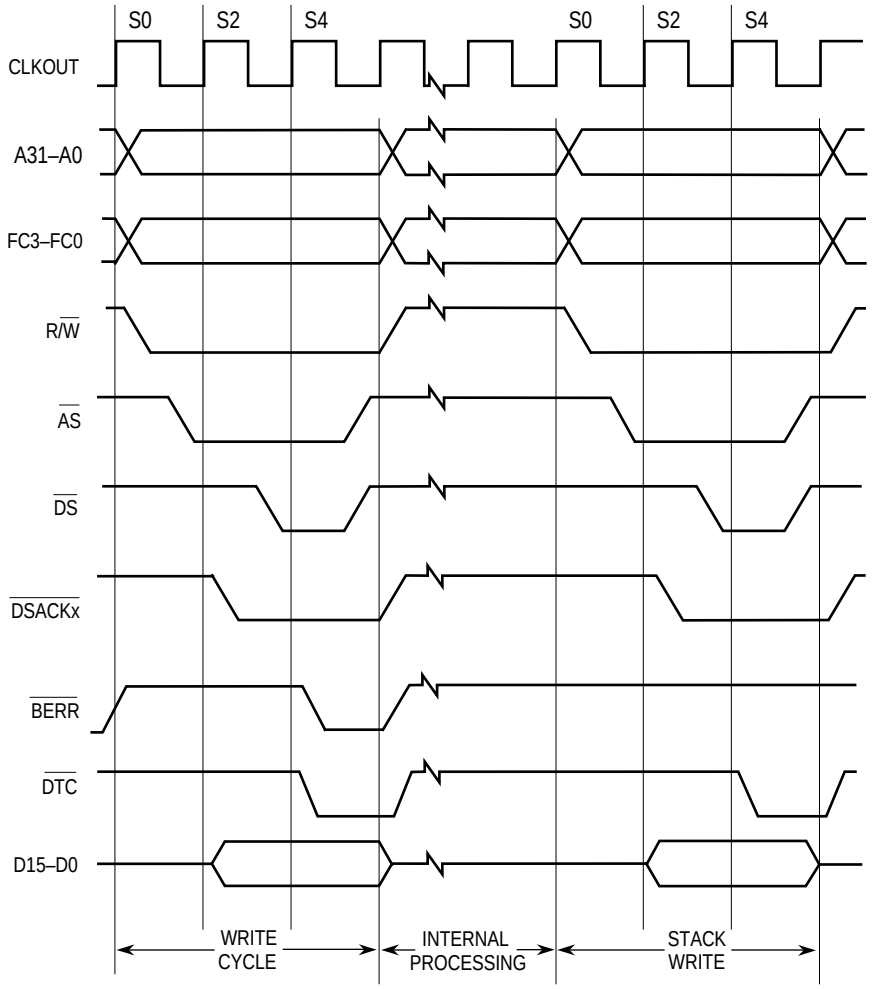

Figure 3-24. Late Bus Error with $\overline{\text{DSACKx}}$

3.6.2 Retry Operation

When both $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ are asserted by an external device during a bus cycle, the MC68341 enters the retry sequence shown in Figure 3-25. A delayed retry, which is similar to the delayed $\overline{\text{BERR}}$ signal described previously, can also occur (see Figure 3-26). The MC68341 terminates the bus cycle, places the control signals in their inactive state, and does not begin another bus cycle until the $\overline{\text{BERR}}$ and $\overline{\text{HALT}}$ signals are negated by external logic. After a synchronization delay, the MC68341 retries the previous cycle using the same access information (address, function code, size, etc.). $\overline{\text{BERR}}$ should be negated before S2 of the retried cycle to ensure correct operation of the retried cycle.

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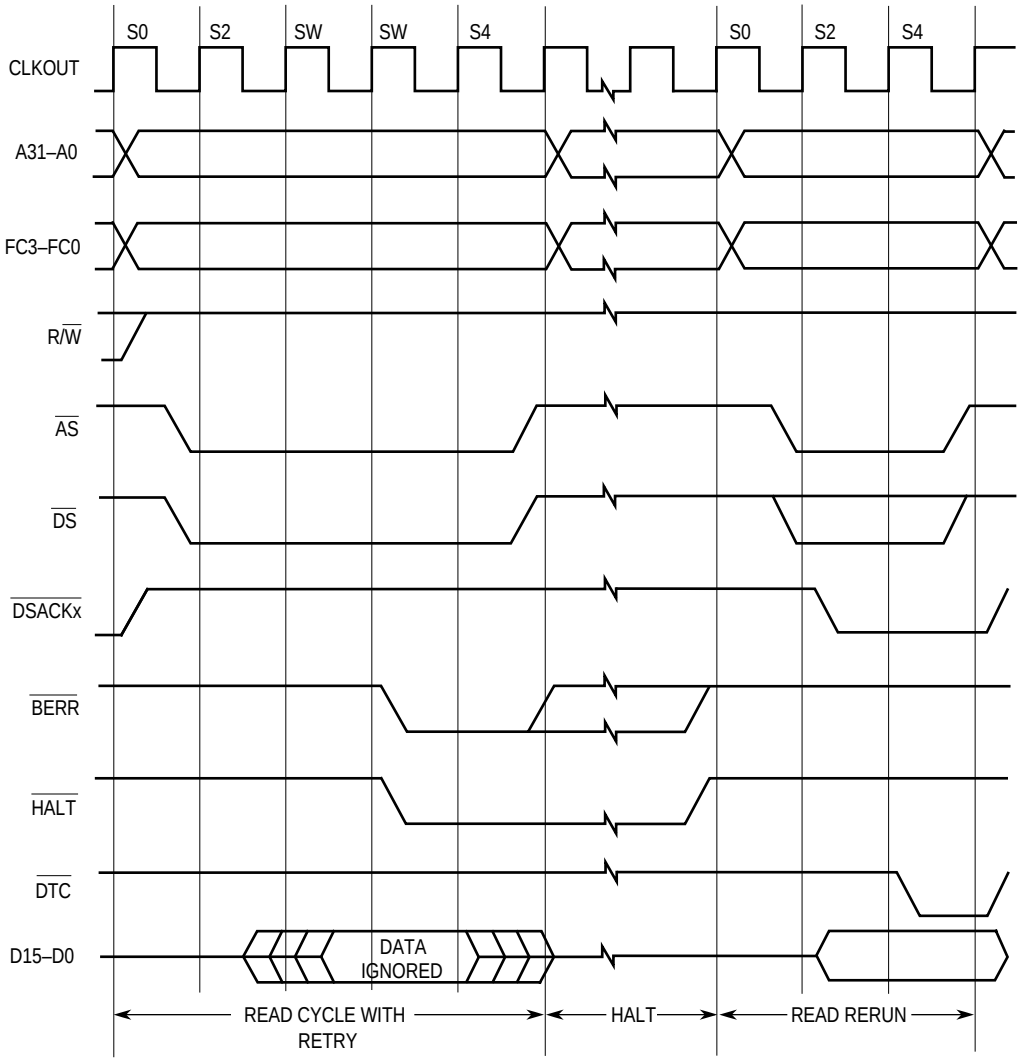

Figure 3-25. Retry Sequence

The MC68341 retries any read or write cycle of a read-modify-write operation separately; RMC remains asserted during the entire retry sequence. Asserting BR along with BERR and HALT provides a relinquish and retry operation. The MC68341 does not relinquish the bus during a read-modify-write operation. Any device that requires the MC68341 to give up the bus and retry a bus cycle during a read-modify-write cycle must assert only BERR and BR (HALT must not be included). The bus error handler software should examine the read-modify-write bit in the special status word (see **Section 5 CPU32**) and take the appropriate action to resolve this type of fault when it occurs.

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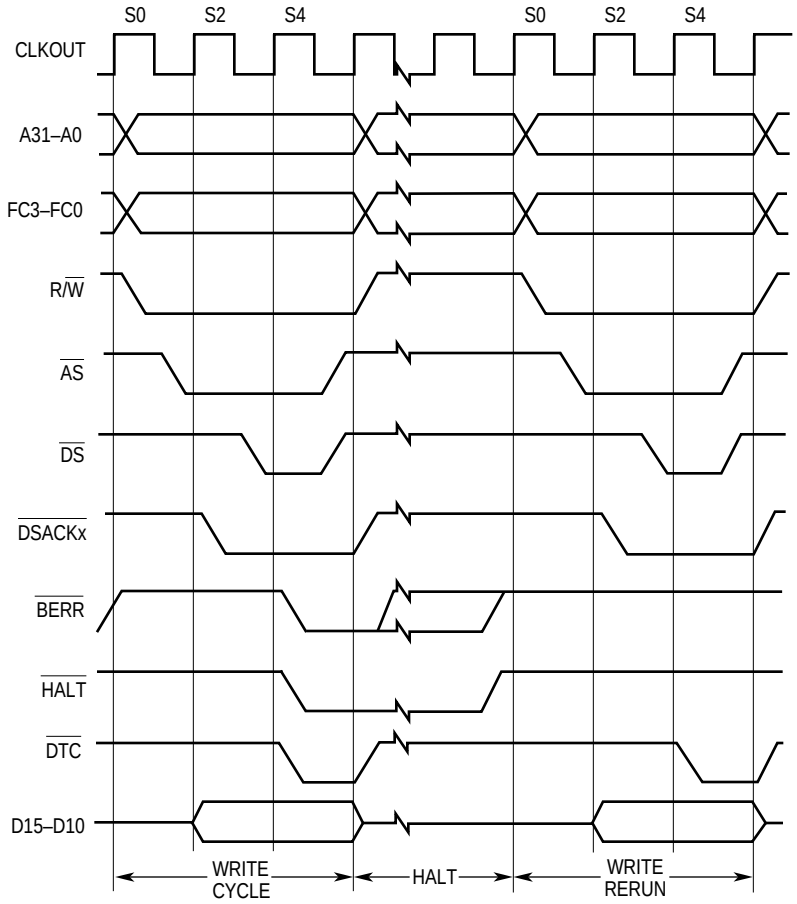

Figure 3-26. Late Retry Sequence

3.6.3 Halt Operation

When $\overline{\text{HALT}}$ is asserted and $\overline{\text{BERR}}$ is not asserted, the MC68341 halts external bus activity at the next bus cycle boundary (see Figure 3-27). $\overline{\text{HALT}}$ by itself does not terminate a bus cycle. Negating and reasserting $\overline{\text{HALT}}$ in accordance with the correct timing requirements provides a single-step (bus cycle to bus cycle) operation. Since $\overline{\text{HALT}}$ affects external bus cycles only, a program that does not require use of the external bus may continue executing. The single-cycle mode allows the user to proceed through (and debug) external MC68341 operations, one bus cycle at a time. Since the occurrence of a bus error while $\overline{\text{HALT}}$ is asserted causes a retry operation, the user must anticipate retry cycles while debugging in the single-cycle mode. The single-step operation and the software trace capability allow the system debugger to trace single bus cycles, single instructions, or changes in program flow.

When the MC68341 completes a bus cycle with $\overline{\text{HALT}}$ asserted, D15–D0 is placed in the high-impedance state, and bus control signals are negated (not high-impedance state); the A31–A0, FCx, SIZx, and R/$\overline{\text{W}}$ signals remain in the same state. The halt operation has no effect on bus arbitration (see **3.7 Bus Arbitration**). When bus arbitration occurs while the MC68341 is halted, the address and control signals are also placed in the high-impedance state. Once bus mastership is returned to the MC68341, if $\overline{\text{HALT}}$ is still

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asserted, the A31–A0, FCx, SIZx, and R/$\overline{W}$ signals are again driven to their previous states. The MC68341 does not service interrupt requests while it is halted.

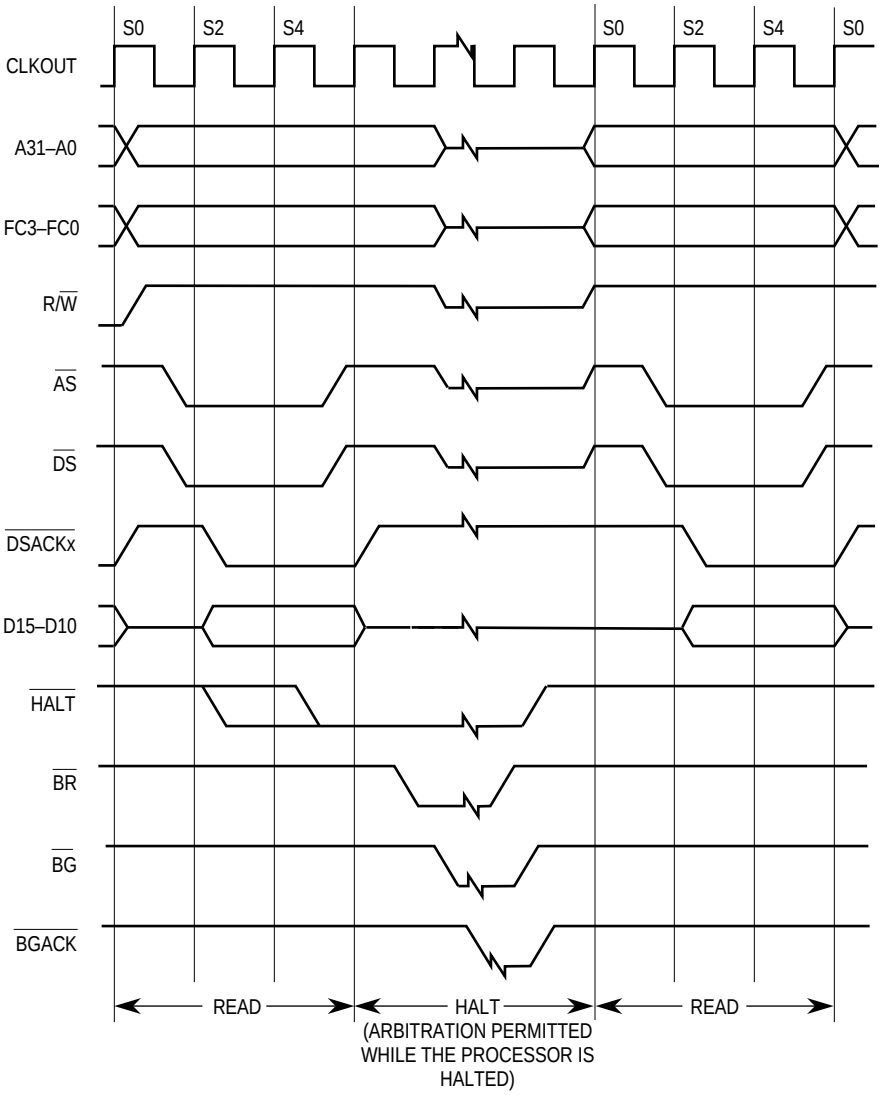

Figure 3-27. $\overline{HALT}$ Timing

3.6.4 Double Bus Fault

A double bus fault results when a bus error or an address error occurs during the exception processing sequence for any of the following:

- A previous bus error
- A previous address error
- A reset

For example, the MC68341 attempts to stack several words containing information about the state of the machine while processing a bus error exception. If a bus error exception

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occurs during the stacking operation, the second error is considered a double bus fault. When a double bus fault occurs, the MC68341 halts and asserts $\overline{\text{HALT}}$. Only a reset operation can restart a halted MC68341. However, bus arbitration can still occur (see **3.7 Bus Arbitration**). A second bus error or address error that occurs after exception processing has completed (during the execution of the exception handler routine or later) does not cause a double bus fault. A bus cycle that is retried does not constitute a bus error or contribute to a double bus fault. The MC68341 continues to retry the same bus cycle as long as the external hardware requests it.

Reset can also be generated internally by the halt monitor (see **Section 5 CPU32**).

3.7 BUS ARBITRATION

The bus design of the MC68341 provides for a single bus master at any one time, either the MC68341 or an external device. One or more of the external devices on the bus can have the capability of becoming bus master for the external bus, but not the MC68341 internal bus. Bus arbitration is the protocol by which an external device becomes bus master; the bus controller in the MC68341 manages the bus arbitration signals so that the MC68341 has the lowest priority. External devices that need to obtain the bus must assert the bus arbitration signals in the sequences described in the following paragraphs. Systems having several devices that can become bus master require external circuitry to assign priorities to the devices so that, when two or more external devices attempt to become bus master at the same time, the one having the highest priority becomes bus master first. The sequence of the protocol is as follows:

1. An external device asserts $\overline{\text{BR}}$.
2. The MC68341 asserts $\overline{\text{BG}}$ to indicate that the bus is available.
3. The external device asserts $\overline{\text{BGACK}}$ to indicate that it has assumed bus mastership.

NOTE

The MC68341 does not place $\overline{\text{CS3}}$–$\overline{\text{CS0}}$ in a high-impedance state after reset or when the bus is granted to an external master.

$\overline{\text{BR}}$ may be issued any time during a bus cycle or between cycles. $\overline{\text{BG}}$ is asserted in response to $\overline{\text{BR}}$. To guarantee operand coherency, $\overline{\text{BG}}$ is only asserted at the end of an operand transfer. Additionally, $\overline{\text{BG}}$ is not asserted until the end of a read-modify-write operation (when $\overline{\text{RMC}}$ is negated) in response to a $\overline{\text{BR}}$ signal. When the requesting device receives $\overline{\text{BG}}$ and more than one external device can be bus master, the requesting device should begin whatever arbitration is required. When the external device assumes bus mastership, it asserts $\overline{\text{BGACK}}$ and maintains $\overline{\text{BGACK}}$ during the entire bus cycle (or cycles) for which it is bus master. The following conditions must be met for an external device to assume mastership of the bus through the normal bus arbitration procedure: 1) it must have received $\overline{\text{BG}}$ through the arbitration process, and 2) $\overline{\text{BGACK}}$ must be inactive, indicating that no other bus master has claimed ownership of the bus.

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Figure 3-28 is a flowchart showing bus arbitration for a single device. This technique allows processing of bus requests during data transfer cycles. Refer to Figures 3-29 and 3-30 for bus arbitration timing diagrams.

$\overline{BR}$ is negated at the time that $\overline{BGACK}$ is asserted. This type of operation applies to a system consisting of the MC68341 and one device capable of bus mastership. In a system having a number of devices capable of bus mastership, $\overline{BR}$ from each device can be wire-ORed to the MC68341. In such a system, more than one bus request could be asserted simultaneously. $\overline{BG}$ is negated a few clock cycles after the transition of $\overline{BGACK}$. However, if bus requests are still pending after the negation of $\overline{BG}$, the MC68341 asserts another $\overline{BG}$ within a few clock cycles after it was negated. This additional assertion of $\overline{BG}$ allows external arbitration circuitry to select the next bus master before the current bus master has finished using the bus. The following paragraphs provide additional information about the three steps in the arbitration process. Bus arbitration requests are recognized during normal processing, $\overline{HALT}$ assertion, and a CPU32 halt caused by a double bus fault.

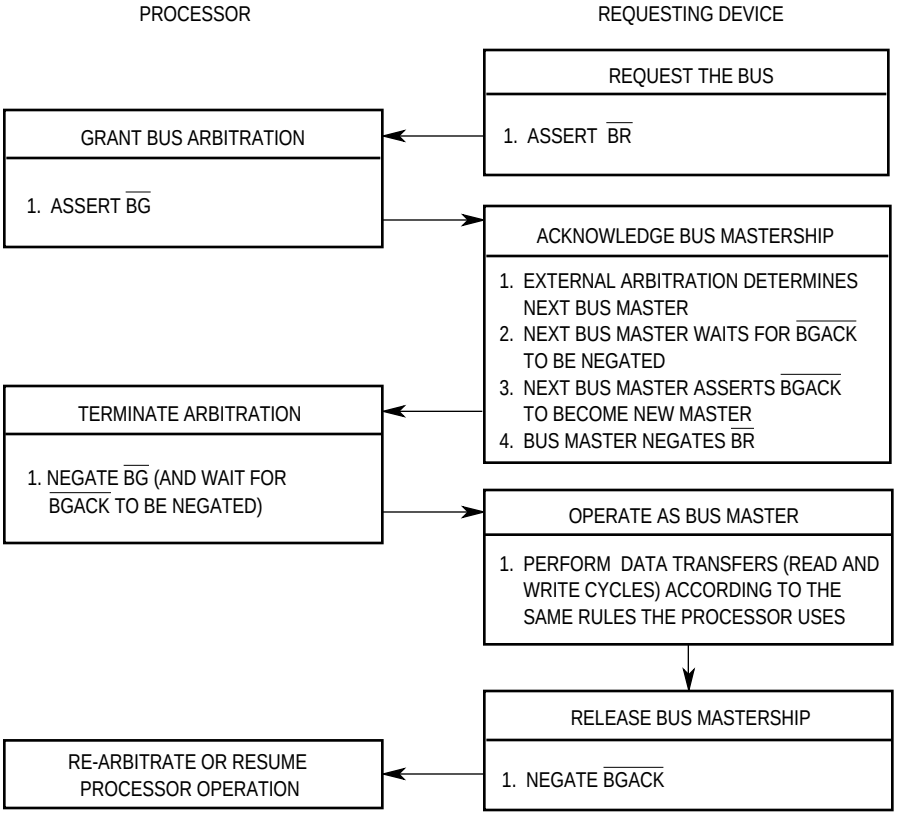

Figure 3-28. Bus Arbitration Flowchart for Single Request

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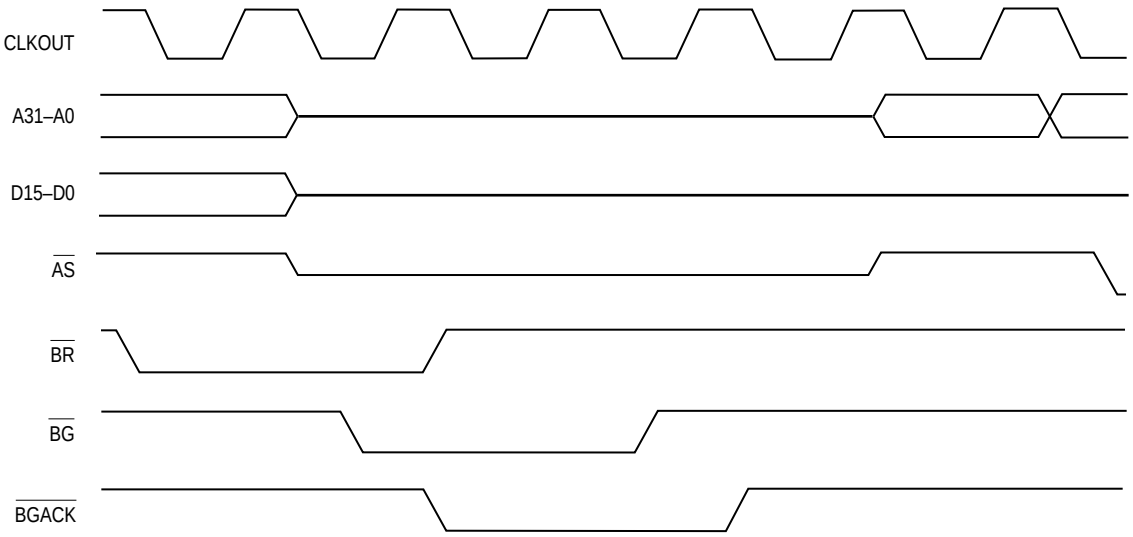

Figure 3-29. Bus Arbitration Timing Diagram—Idle Bus Case

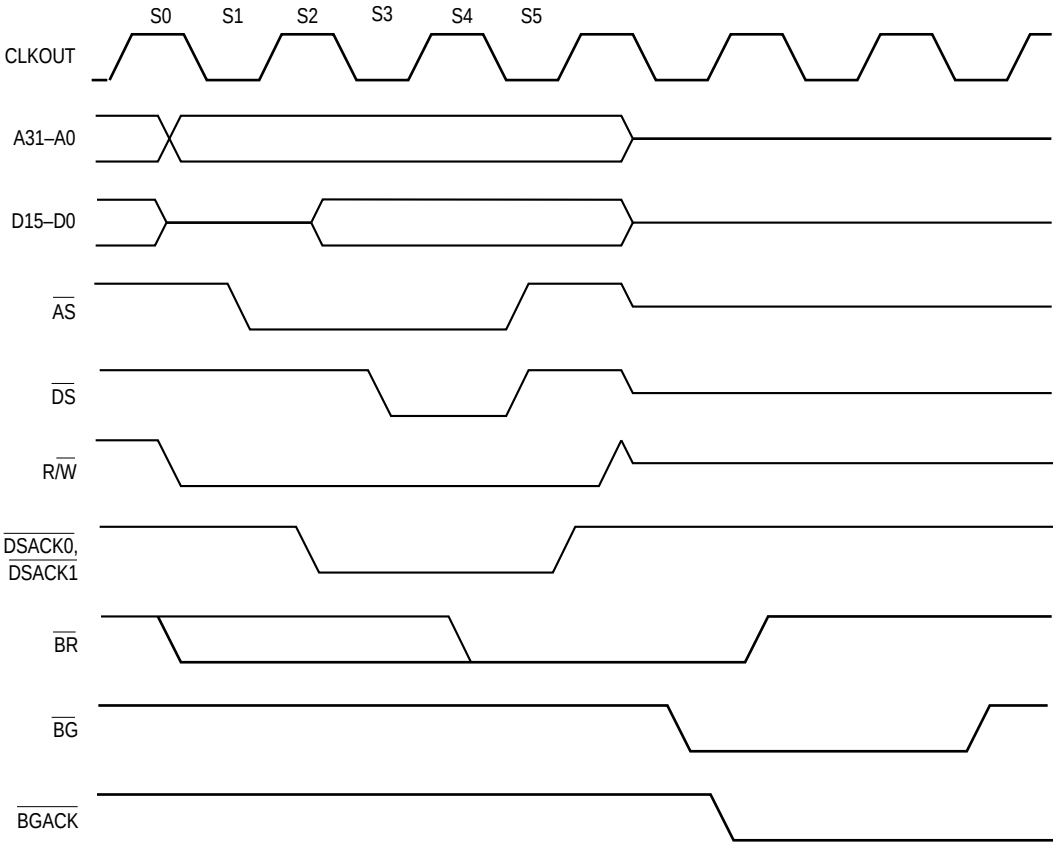

Figure 3-30. Bus Arbitration Timing Diagram—Active Bus Case

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3.7.1 Bus Request

External devices capable of becoming bus masters request the bus by asserting $\overline{BR}$. This signal can be wire-ORed to indicate to the MC68341 that some external device requires control of the bus. The MC68341 is effectively at a lower bus priority level than the external device and relinquishes the bus after it has completed the current bus cycle (if one has started). If no $\overline{BGACK}$ is received while the $\overline{BR}$ is active, the MC68341 remains bus master once $\overline{BR}$ is negated. This prevents unnecessary interference with ordinary processing if the arbitration circuitry inadvertently responds to noise or if an external device determines that it no longer requires use of the bus before it has been granted mastership.

3.7.2 Bus Grant

The MC68341 supports operand coherency; thus, if an operand transfer requires multiple bus cycles, the MC68341 does not release the bus until the entire transfer is complete. Therefore, assertion of $\overline{BG}$ is subject to the following constraints:

- The minimum time for $\overline{BG}$ assertion after $\overline{BR}$ is asserted depends on internal synchronization (see **Section 12 Electrical Characteristics**).
- During an external operand transfer, the MC68341 does not assert $\overline{BG}$ until after the last cycle of the transfer (determined by SIZx and $\overline{DSACKx}$).
- During an external operand transfer, the MC68341 does not assert $\overline{BG}$ as long as $\overline{RMC}$ is asserted.
- If the show cycle bits SHEN1–SHEN0 = 01, the MC68341 does not assert $\overline{BG}$ to an external master.

Externally, the $\overline{BG}$ signal can be routed through a daisy-chained network or a priority-encoded network. The MC68341 is not affected by the method of arbitration as long as the protocol is obeyed.

3.7.3 Bus Grant Acknowledge

An external device cannot request and be granted the external bus while another device is the active bus master. A device that asserts $\overline{BGACK}$ remains the bus master until it negates $\overline{BGACK}$. $\overline{BGACK}$ should not be negated until all required bus cycles are completed. Bus mastership is terminated at the negation of $\overline{BGACK}$.

Once an external device receives the bus and asserts $\overline{BGACK}$, it should negate $\overline{BR}$. If $\overline{BR}$ remains asserted after $\overline{BGACK}$ is asserted, the MC68341 assumes that another device is requesting the bus and prepares to issue another $\overline{BG}$.

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3.7.4 Bus Arbitration Control

The bus arbitration control unit in the MC68341 is implemented with a finite state machine. As discussed previously, all asynchronous inputs to the MC68341 are internally synchronized in a maximum of two cycles of the clock. As shown in Figure 3-31 input signals labeled R and A are internally synchronized versions of $\overline{BR}$ and $\overline{BGACK}$ respectively. The $\overline{BG}$ output is labeled G, and the internal high-impedance control signal is labeled T. If T is true, the address, data, and control buses are placed in the high-impedance state after the next rising edge following the negation of $\overline{AS}$ and $\overline{RMC}$. All signals are shown in positive logic (active high) regardless of their true active voltage level. The state machine shown in Figure 3-31 does not have a state 1 or state 4.

State changes occur on the next rising edge of the clock after the internal signal is valid. The $\overline{BG}$ signal transitions on the falling edge of the clock after a state is reached during which G changes. The bus control signals (controlled by T) are driven by the MC68341 immediately following a state change, when bus mastership is returned to the MC68341. State 0, in which G and T are both negated, is the state of the bus arbiter while the MC68341 is bus master. R and A keep the arbiter in state 0 as long as they are both negated.

The MC68341 does not allow arbitration of the external bus during the $\overline{RMC}$ sequence. For the duration of this sequence, the MC68341 ignores the $\overline{BR}$ input. If mastership of the bus is required during an $\overline{RMC}$ operation, $\overline{BERR}$ must be used to abort the $\overline{RMC}$ sequence.

3.7.5 Show Cycles

The MC68341 can perform data transfers with its internal modules without using the external bus, but, when debugging, it is desirable to have address and data information appear on the external bus. These external bus cycles, called show cycles, are distinguished by the fact that $\overline{AS}$ is not asserted externally. $\overline{DS}$ is used to signal address strobe timing in show cycles.

After reset, show cycles are disabled and must be enabled by writing to the SHEN bits in the module configuration register (see **4.3.2.1 Module Configuration Register (MCR)**). When show cycles are disabled, the A31–A0, FCx, SIZx, and R/$\overline{W}$ signals continue to reflect internal bus activity. However, $\overline{AS}$ and $\overline{DS}$ are not asserted externally, and the external data bus remains in a high-impedance state. When show cycles are enabled, $\overline{DS}$ indicates address strobe timing and the external data bus contains data. The following paragraphs are a state-by-state description of show cycles, and Figure 3-32 illustrates a show cycle timing diagram. Refer to **Section 12 Electrical Characteristics** for specific timing information.

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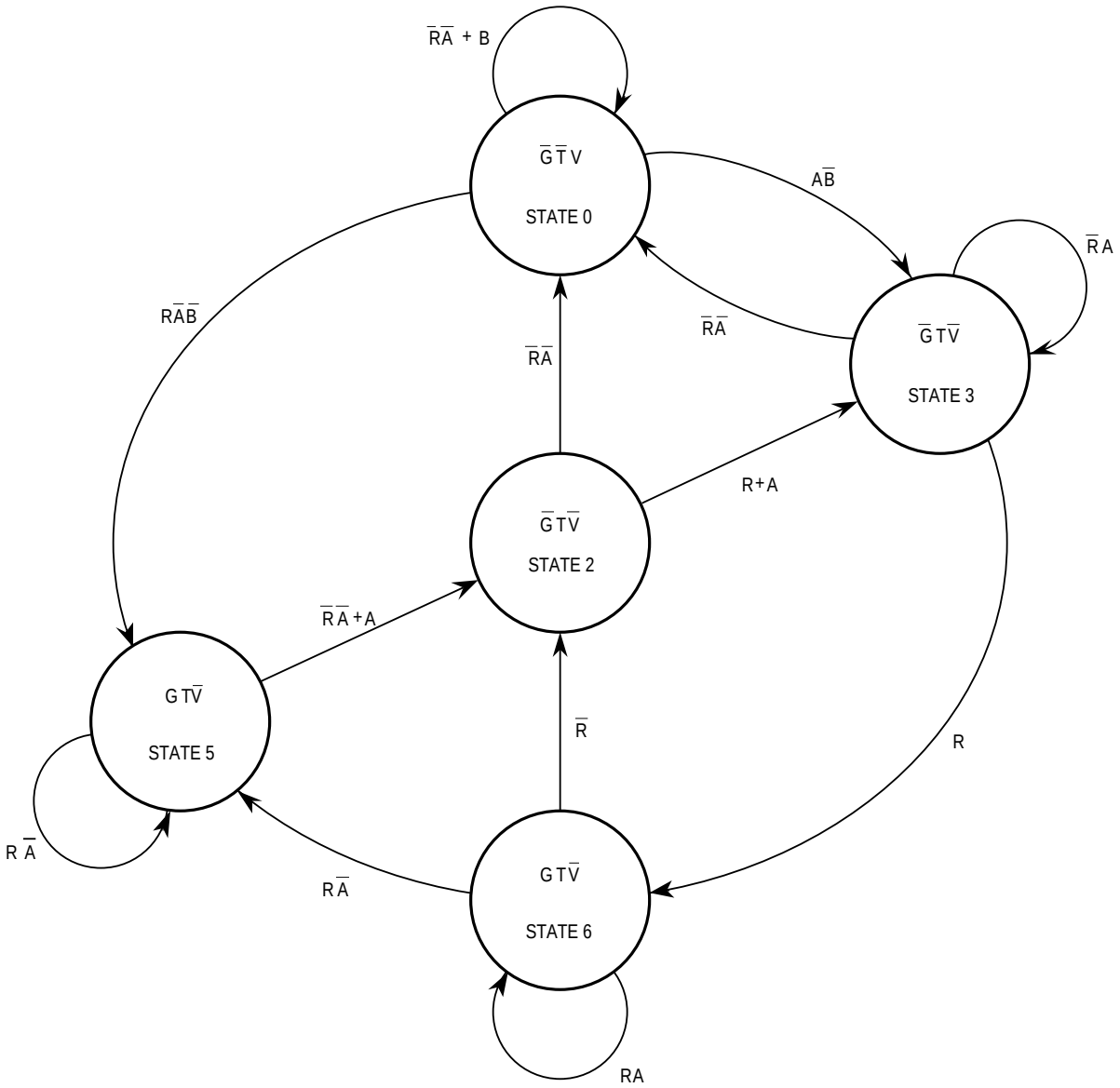

R - BUS REQUEST
A - BUS GRANT ACKNOWLEDGE
B - BUS CYCLE IN PROGRESS

G - BUS GRANT
T - THREE-STATE SIGNAL TO BUS CONTROL
V - BUS AVAILABLE TO BUS CONTROL

Figure 3-31. Bus Arbitration State Diagram

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State 0—During state 0, the A31–A0 and FCx become valid, R/$\overline{W}$ is driven to indicate a show read or write cycle, and the SIZx pins indicate the number of bytes to transfer. During a read, the addressed peripheral is driving the data bus, and the user must take care to avoid bus conflicts.

State 41—One-half clock cycle later, $\overline{DS}$ (rather than $\overline{AS}$) is asserted to indicate that address information is valid.

State 42—No action occurs in state 42. The bus controller remains in state 42 (wait states will be inserted) until the internal read cycle is complete.

State 43—When $\overline{DS}$ is negated, show data is valid on the next falling edge of the system clock. The external data bus drivers are enabled so that data becomes valid on the external bus as soon as it is available on the internal bus.

State 0—The A31–A0, FCx, R/$\overline{W}$, and SIZx pins change to begin the next cycle. Data from the preceding cycle is valid through state 0.

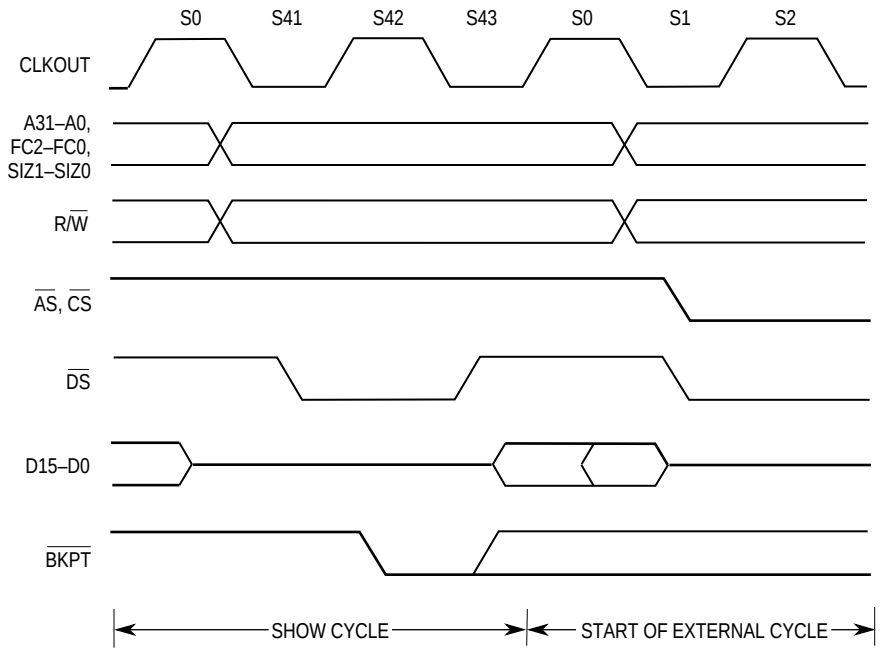

Figure 3-32. Show Cycle Timing Diagram

3.8 RESET OPERATION

The MC68341 has reset control logic to determine the cause of reset, synchronize it if necessary, and assert the appropriate reset lines. The reset control logic can independently drive three different lines:

1. EXTRST (external reset) drives the external $\overline{RESET}$ pin.
2. CLKRST (clock reset) resets the clock module.
3. INTRST (internal reset) goes to all other internal circuits.

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Synchronous reset sources are not asserted until the end of the current bus cycle, whether or not $\overline{RMC}$ is asserted. The internal bus monitor is automatically enabled for synchronous resets; therefore, if the current bus cycle does not terminate normally, the bus monitor terminates it. Only single-byte or word transfers are guaranteed valid for synchronous resets. An external or clock reset is a synchronous reset source.

Asynchronous reset sources indicate a catastrophic failure, and the reset controller logic immediately resets the system. Resetting the MC68341 causes any bus cycle in progress to terminate as if $\overline{DSACKx}$ or $\overline{BERR}$ had been asserted. In addition, the MC68341 appropriately initializes registers for a reset exception. Asynchronous reset sources include power-up, software watchdog, double bus fault resets, and execution of the $\overline{RESET}$ instruction.

If an external device drives $\overline{RESET}$ low, $\overline{RESET}$ should be asserted for at least 590 clock periods to ensure that the MC68341 resets. The reset control logic holds reset asserted internally until the external $\overline{RESET}$ is released. When the reset control logic detects that external $\overline{RESET}$ is no longer being driven, it drives both internal and external reset low for an additional 512 cycles to guarantee this length of reset to the entire system. Figure 3-33 shows the $\overline{RESET}$ timing.

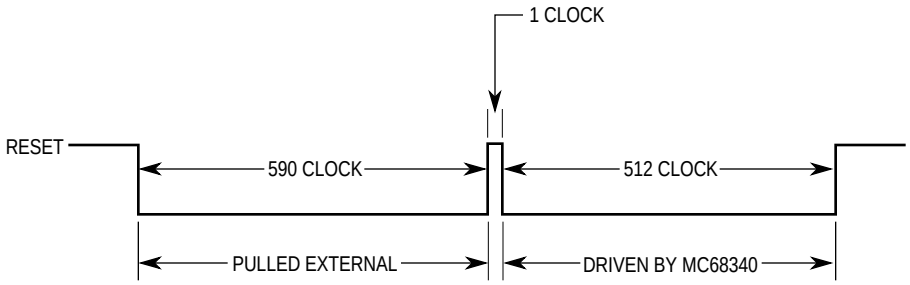

Figure 3-33. Timing for External Devices Driving $\overline{RESET}$

If reset is asserted from any other source, the reset control logic asserts $\overline{RESET}$ for 328 input clock periods plus 512 output clock periods, and until the source of reset is negated.

After any internal reset occurs, a 14-cycle rise time is allowed before testing for the presence of an external reset. If no external reset is detected, the CPU32 begins its vector fetch.

Figure 3-34 is a timing diagram of the power-up reset operation, showing the relationships between $\overline{RESET}$, V_{CC}, and bus signals. During the reset period, the entire bus three-states except for non-three-statable signals, which are driven to their inactive state. Once $\overline{RESET}$ negates, all control signals are driven to their inactive state, the data bus is in read mode, and the address bus is driven. After this, the first bus cycle for $\overline{RESET}$ exception processing begins.

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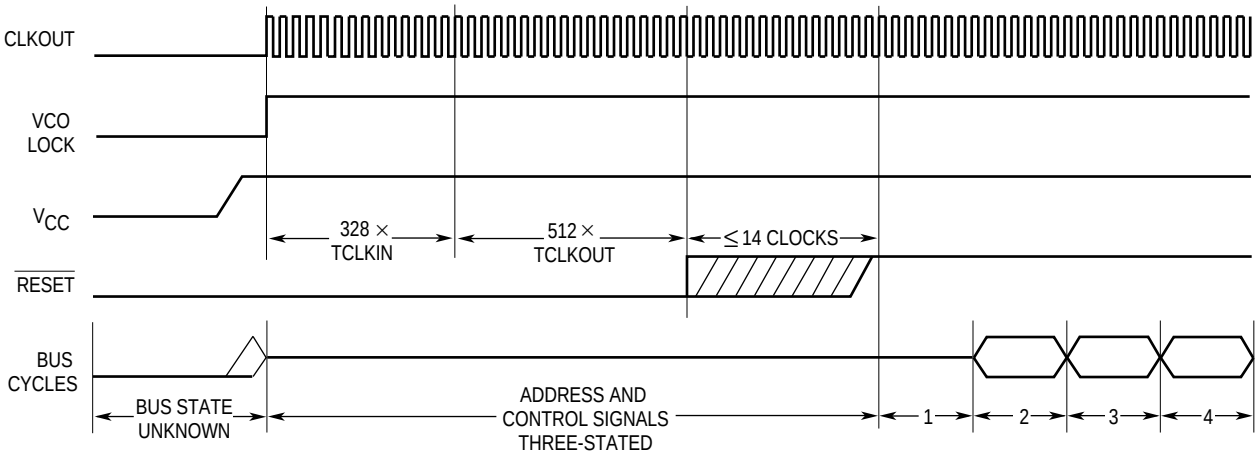

NOTES:
1. Internal start-up time.
2. SSP read here.
3. PC read here.
4. First instruction fetched here.

Figure 3-34. Power-Up Reset Timing Diagram

When a RESET instruction is executed, the MC68341 drives the $\overline{\text{RESET}}$ signal for 512 clock cycles. The SIM41 registers and the module control registers in each internal peripheral module (DMA, timers, and serial modules) are not affected. All other peripheral module registers are reset the same as for a hardware reset. The external devices connected to the $\overline{\text{RESET}}$ signal are reset at the completion of the RESET instruction.

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SECTION 4
SYSTEM INTEGRATION MODULE

The MC68341 system integration module (SIM41) consists of several functions that control the system start-up, initialization, configuration, and the external bus with a minimum of external devices. It also provides the IEEE 1149.1 boundary scan capabilities. The SIM41 includes the following functions:

- System Configuration and Protection
- Clock Synthesizer
- Real-Time Clock
- Chip Selects and Wait States
- 68300/68000 External Bus Interface
- Bus Arbitration
- Dynamic Bus Sizing
- IEEE 1149.1 Test Access Port

4.1 MODULE OVERVIEW

The SIM41 has similar features to the SIM in the MC68330 and MC68340. The periodic interrupt timer, double bus fault monitor, software watchdog, and spurious interrupt monitor are identical. However, many of the other features in the SIM differ in their use and details.

The system configuration and protection function controls system configuration and provides various monitors and timers, including the internal bus monitor, double bus fault monitor, spurious interrupt monitor, software watchdog timer, and the periodic interrupt timer.

The clock synthesizer generates the clock signals used by the SIM41 and the other on-chip modules, as well as CLKOUT used by external devices.

The real-time clock function has internal interrupt generation capability, and a programmable output pin that can provide an interrupt on an alarm or time-matching function.

The programmable chip select function provides eight chip select signals that can enable external memory and peripheral circuits, providing all handshaking and timing signals. Each chip select signal has an associated base address register and an address mask register that contain the programmable characteristics of that chip select. Up to six wait

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states can be programmed by setting bits in the address mask register and base address register.

The 68300/68000 external bus interface (EBI) handles the transfer of information between the internal CPU32 and memory, peripherals, or other processing elements in the external address space. See **Section 3 Bus Operation** for further information.

The MC68341 dynamically interprets the port size of an addressed device during each bus cycle in 68300 bus mode, allowing operand transfers to or from 8-, 16-, and 32-bit ports. The device signals its port size and indicates completion of the bus cycle through the use of the $\overline{\text{DSACKx}}$ inputs. Dynamic bus sizing allows a programmer to write code that is not bus-width specific. For a discussion on dynamic bus sizing, see **Section 3 Bus Operation.**

The MC68341 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 *Standard Test Access Port and Boundary Scan Architecture*. Problems associated with testing high-density circuit boards have led to the development of this standard under the sponsorship of the IEEE Test Technology Committee and Joint Test Action Group (JTAG). The MC68341 implementation supports circuit-board test strategies based on this standard. Refer to **Section 10 IEEE 1149.1 Test Access Port** for additional information.

4.2 MODULE OPERATION

The following paragraphs describe the operation of the module base address register, system configuration and protection, clock synthesizer, chip select functions, and the external bus interface.

NOTE

The terms *assert* and *negate* are used throughout this section to avoid confusion when dealing with a mixture of active-low and active-high signals. The term *assert* or *assertion* indicates that a signal is active or true independent of the level represented by a high or low voltage. The term *negate* or *negation* indicates that a signal is inactive or false.

4.2.1 Module Base Address Register Operation

The module base address register (MBAR) controls the location of all internal module registers (see **4.3.1 Module Base Address Register (MBAR)**). The address stored in this register is the base address (starting location) for all internal registers. All internal module registers are contained in a single 4-Kbyte block (see Figure 4-1) that is relocatable along 4-Kbyte boundaries.

The location of the internal registers is fixed by writing the desired base address of the 4-Kbyte block to the MBAR using the MOVES instruction to address $0003FF00 in CPU space. The source function code (SFC) and destination function code (DFC) registers contain the address space values (FC3–FC0) for the read or write operand of the MOVES

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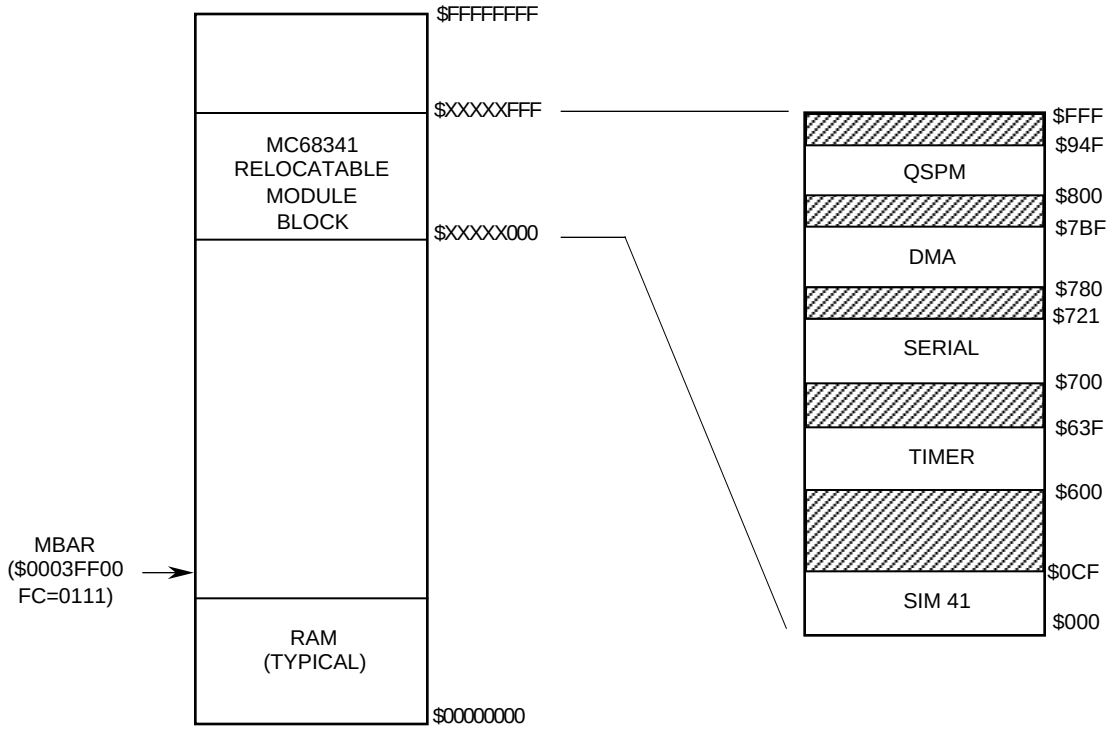
instruction (see **Section 5 CPU32** or M68000PM/AD, *Programmer's Reference Manual*). Therefore, the SFC or DFC register must indicate CPU space (FC3–FC0 = $7), using the MOVEC instruction, before accessing MBAR. The offset from the base address is shown above each register diagram.



NOTE: $XXXXX is the value contained in the MBAR bits BA31-BA12.

Figure 4-1. SIM41 Module Register Block

4.2.2 System Configuration and Protection Operation

The SIM41 allows the user to control certain features of system configuration by writing bits in the module configuration register (MCR). This register also contains read-only status bits that show the state of the SIM41.

All M68000 family members are designed to provide maximum system safeguards. As an extension of the family, the MC68341 promotes the same basic concepts of safeguarded design present in all M68000 members. In addition, many functions that normally must be provided by external circuits are incorporated in this device. The following features are provided in the system configuration and protection function:

SIM41 Module Configuration

The SIM41 allows the user to configure the system to the particular requirements. The functions include control of FREEZE and show cycle operation, the function of the $\overline{\text{CSx}}$ signals, the access privilege of the supervisor/user registers, the level of interrupt arbitration, and automatic vectoring for external interrupts.

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Reset Status

The reset status register provides the user with information on the cause of the most recent reset. The possible causes of reset include: external, power-up, software watchdog, double bus fault, loss of clock, and RESET instruction.

Internal Bus Monitor

The SIM41 provides an internal bus monitor to monitor the $\overline{\text{DSACKx}}$ response time for all internal bus accesses. An option allows the monitoring of external bus accesses. For external bus accesses, four selectable response times are provided to allow for variations in response speed of memory and peripherals used in the system. A bus error signal is asserted internally if the $\overline{\text{DSACKx}}$ response limit is exceeded. $\overline{\text{BERR}}$ is not asserted externally. This monitor can be disabled for external bus cycles only.

Double Bus Fault Monitor

The double bus fault monitor causes a reset to occur if the internal $\overline{\text{HALT}}$ is asserted by the CPU32, indicating a double bus fault. A double bus fault results when a bus or address error occurs during the exception processing sequence for a previous bus or address error, a reset, or while the CPU32 is loading information from a bus error stack frame during an RTE instruction. This function can be disabled. See **Section 3 Bus Operation** for more information.

Spurious Interrupt Monitor

If no interrupt arbitration occurs during an interrupt acknowledge (IACK) cycle, the bus error signal is asserted internally. This function cannot be disabled.

Software Watchdog

The software watchdog asserts reset or a level 7 interrupt (as selected by the system protection and control register) if the software fails to service the software watchdog for a designated period of time (i.e., because it is trapped in a loop or lost). There are eight selectable timeout periods. This function can be disabled.

Periodic Interrupt Timer

The SIM41 provides a timer to generate periodic interrupts. The periodic interrupt time period can vary from 122 µs to 15.94 s (with a 32.768-kHz crystal used to generate the system clock). This function can be disabled.

Figure 4-2 shows a block diagram of the system configuration and protection function.

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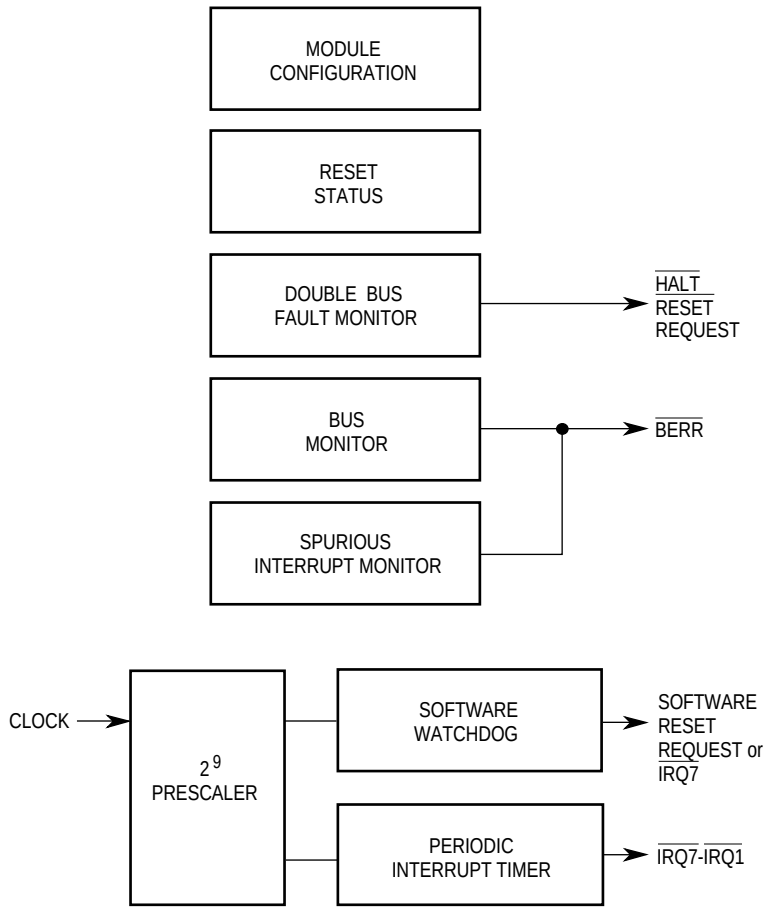

Figure 4-2. System Configuration and Protection Function

4.2.2.1 SYSTEM CONFIGURATION. Aspects of the system configuration are controlled by the MCR and the autovector register (AVR).

The configuration of port B is controlled by the combination of the AVEC bit in the MCR and the port B pin assignment register (PPARB). Port B pins can function as dedicated I/O lines or interrupts.

For debug purposes, internal bus accesses can be shown on the external bus. This function is called show cycles. The SHEN1, SHEN0 bits in the MCR control show cycles. Bus arbitration can be either enabled or disabled during show cycles.

Arbitration for servicing interrupts is controlled by the value programmed into the interrupt arbitration (IARB) field of the MCR. Each module that generates interrupts, including the SIM41, has an IARB field. The value of the IARB field allows arbitration during an IACK cycle among modules that simultaneously generate the same interrupt level. No two modules should share the same IARB value. The IARB must contain a value other than $0 for all modules that can generate interrupts; interrupts with IARB = 0 are discarded as extraneous. The SIM41 arbitrates for both its own interrupts and externally generated interrupts.

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There are eight arbitration levels for access to the intermodule bus (IMB). The SIM41 is fixed at the highest level (above the programmable level 7), and the CPU32 is fixed at the lowest level (below level 0). The direct memory access (DMA) module is the only other module that can become bus master and arbitrate for the bus. It must be initialized with a level other than 0 or 7.

The AVR contains bits that correspond to external interrupt levels that require an autovector response. The SIM41 supports up to seven discrete external interrupt requests. If the bit corresponding to an interrupt level is set in the AVR, the SIM41 returns an autovector in response to the IACK cycle servicing that external interrupt request. Otherwise, external circuitry must either return an interrupt vector or assert the external $\overline{\text{AVEC}}$ signal.

4.2.2.2 INTERNAL BUS MONITOR. The internal bus monitor continually checks for the bus cycle termination response time by checking the $\overline{\text{DSACKx}}$, $\overline{\text{BERR}}$, and $\overline{\text{HALT}}$ status or the $\overline{\text{AVEC}}$ status during an IACK cycle. The monitor initiates a bus error if the response time is excessive. The bus monitor feature cannot be disabled for internal accesses to an internal module. The internal bus monitor cannot check the $\overline{\text{DSACKx}}$ response on the external bus unless the MC68341 is the bus master. The BME bit in the system protection control register (SYPCR) enables the internal bus monitor for internal-to-external bus cycles. If the system contains external bus masters whose bus cycles must be monitored, an external bus monitor must be implemented. In this case, the internal-to-external bus monitor option must be disabled.

The bus cycle termination response time is measured in clock cycles, and the maximum-allowable response time is programmable. The bus monitor response time period ranges from 64 to 512 system clocks (see Table 4-9). These options are provided to allow for different response times of peripherals that might be used in the system.

4.2.2.3 DOUBLE BUS FAULT MONITOR. A double bus fault is caused by a bus error or address error during the exception processing sequence. The double bus fault monitor responds to an assertion of $\overline{\text{HALT}}$ on the internal bus. Refer to **Section 3 Bus Operation** for more information. The DBF bit in the reset status register (RSR) indicates that the last reset was caused by the double bus fault monitor. The double bus fault monitor reset can be enabled by the DBFE bit in the SYPCR.

4.2.2.4 SPURIOUS INTERRUPT MONITOR. The spurious interrupt monitor issues $\overline{\text{BERR}}$ if no interrupt arbitration occurs during an IACK cycle. Normally, during an IACK cycle, one or more internal modules recognize that the CPU32 is responding to interrupt request(s) and arbitrate for the privilege of returning a vector or asserting $\overline{\text{AVEC}}$. (The SIM41 reports and arbitrates for externally generated interrupts.) This feature cannot be disabled.

4.2.2.5 SOFTWARE WATCHDOG. The SIM41 provides a software watchdog option to prevent system lock-up in case the software becomes trapped in loops with no controlled exit. Once enabled by the SWE bit in the SYPCR, the software watchdog requires a special service sequence to be executed on a periodic basis. If this periodic servicing action does not occur, the software watchdog times out and issues a reset or a level 7

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interrupt (as programmed by the SWRI bit in the SYPCR). The address of the interrupt service routine for the software watchdog interrupt is stored in the software interrupt vector register (SWIV). Figure 4-3 shows a block diagram of the software watchdog as well as the clock control circuits for the periodic interrupt timer.

The watchdog clock rate is determined by the SWP bit in the periodic interrupt timer register (PITR) and the SWT bits in the SYPCR. See Table 4-8 for a list of watchdog timeout periods.

The software watchdog service sequence consists of the following steps: 1) write $55 to the software service register (SWSR) and 2) write $AA to the SWSR. Both writes must occur in the order listed prior to the watchdog timeout, but any number of instructions or accesses to the SWSR can be executed between the two writes.

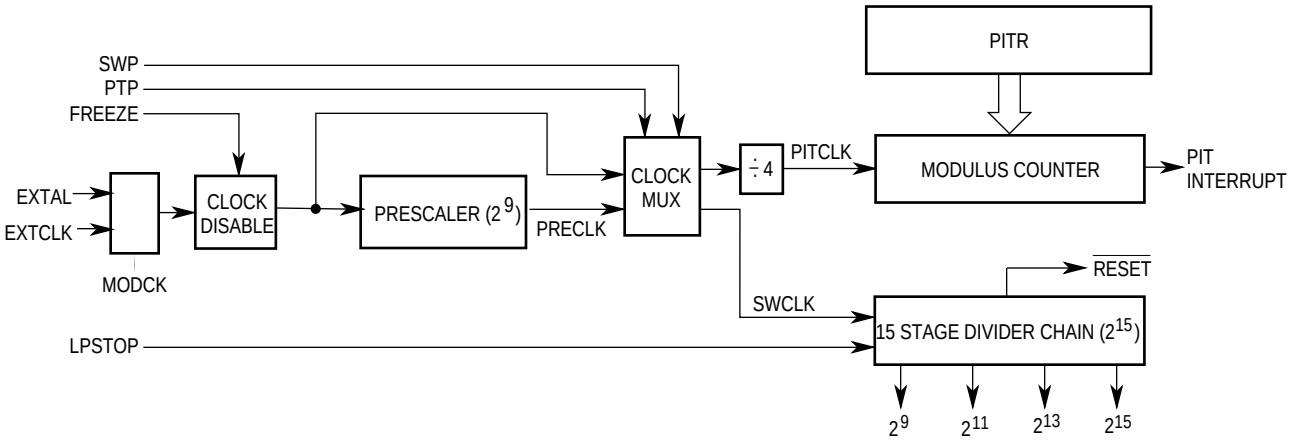

Figure 4-3. Software Watchdog Block Diagram

4.2.2.6 PERIODIC INTERRUPT TIMER. The periodic interrupt timer consists of an 8-bit modulus counter that is loaded with the value contained in the PITR (see Figure 4-3). The modulus counter is clocked by a signal derived from the EXTAL input pin unless an external frequency source from the EXTCLK pin is used. When an external frequency source is used (MODCK low during reset), the default state of the prescaler control bits (SWP and PTP) in the PITR should be changed to enable both prescalers.

Either clock source (EXTAL or EXTCLK or either divided by 512) is divided by 4 before driving the modulus counter (PITCLK). When the modulus counter value reaches zero, an interrupt is generated. The level of the generated interrupt is programmed into the PIRQL bits in the periodic interrupt control register (PICR). During the IACK cycle, the SIM41 places the periodic interrupt vector, programmed into the PIV bits in the PICR, onto the internal bus. The value of bits 7–0 in the PITR is then loaded again into the modulus counter, and the counting process starts over. If a new value is written to the PITR, this value is loaded into the modulus counter when the current count is completed.

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4.2.2.6.1 Periodic Timer Period Calculation. The period of the periodic timer can be calculated using the following equation:

$$\text{periodic interrupt timer period} = \frac{\text{PITR count value}}{\dfrac{\text{EXTAL (or EXTCLK) frequency/prescaler value}}{2^2}}$$

Solving the equation using a crystal frequency of 32.768-kHz with the prescaler disabled gives:

$$\text{periodic interrupt timer period} = \frac{\text{PITR count value}}{\dfrac{32768/1}{2^2}}$$

$$\text{periodic interrupt timer period} = \frac{\text{PITR count value}}{8192}$$

This gives a range from 122 µs, with a PITR value of $01 (00000001 binary), to 31.128 ms, with a PITR value of $FF (11111111 binary).

Solving the equation with the prescaler enabled (PTP=1 in the PITR) gives the following values:

$$\text{periodic interrupt timer period} = \frac{\text{PITR count value}}{\dfrac{32768/512}{2^2}}$$

$$\text{periodic interrupt timer period} = \frac{\text{PITR count value}}{16}$$

This gives a range from 62.5 ms, with a PITR value of $01, to 15.94 s, with a PITR value of $FF.

For fast calculation of periodic timer period using a 32.768-kHz crystal, the following equations can be used:

With prescaler disabled:

$$\text{programmable interrupt timer period} = \text{PITR (122 µs)}$$

With prescaler enabled:

$$\text{programmable interrupt timer period} = \text{PITR (62.5 ms)}$$

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4.2.2.6.2 Using the Periodic Timer as a Real-Time Clock. The periodic interrupt timer can be used as a real-time clock interrupt by setting it up to generate an interrupt with a one-second period. Rearranging the periodic timer period equation to solve for the desired count value:

$$\text{PITR count value} = \frac{\text{(PIT period) (EXTAL (or EXTCLK) frequency)}}{\text{(Prescaler value) } (2^2)}$$

$$\text{PITR count value} = \frac{(1)\ (32768)}{(512)\ (2^2)}$$

$$\text{PITR count value} = 16 \text{ (decimal)}$$

Therefore, when using a 32.768-kHz crystal, the PITR should be loaded with a value of $10 with the prescaler enabled to generate interrupts at a one-second rate.

4.2.2.7 SIMULTANEOUS INTERRUPTS BY SOURCES IN THE SIM41. If multiple interrupt sources at the same interrupt level are simultaneously asserted in the SIM41, it will prioritize and service the interrupts in the following order: 1) software watchdog, 2) periodic interrupt timer, 3) RTC alarm, and 4) external interrupts.

4.2.3 Clock Synthesizer Operation

The clock synthesizer can operate with either an external crystal or an external oscillator for reference, using the internal phase-locked loop (PLL) and voltage-controlled oscillator (VCO), or an external clock can directly drive the external clock input (EXTCLK) at the operating frequency. For RTC operation, 32.768 kHz crystal operation must be used. The four modes of clock operation are listed in Table 4-1.

Table 4-1. Clock Operating Modes

Mode	Description	MODCK Reset Value	V_{CCSYN} Operating Value
Crystal Mode	External crystal used with the on-chip PLL and VCO to generate a system clock and CLKOUT of programmable rates.	1	V_{CC}
External Clock Mode without PLL	The desired operating frequency is driven into EXTCLK resulting in a system clock and CLKOUT of the same frequency, not tightly coupled.	0	0 V
External Clock Mode with PLL	The desired operating frequency is driven into EXTCLK, resulting in a system clock and CLKOUT of the same frequency, with a tight skew between input and output signals.	0	V_{CC}
Limp Mode	Upon input signal loss for either clock mode using the PLL, operation continues at approximately one-half operating speed (affected by the value of the X-bit in the SYNCR).	X	V_{CC}

4.2.3.1 CRYSTAL MODE. In crystal mode (see Figure 4-4), the clock synthesizer can operate from the on-chip PLL and VCO, using a parallel resonant crystal connected between the EXTAL and XTAL pins. An external oscillator can also be connected to EXTCLK as a reference frequency source, as shown in Figure 4-5. A 32.768-kHz watch crystal provides an inexpensive reference, but the reference crystal or external oscillator

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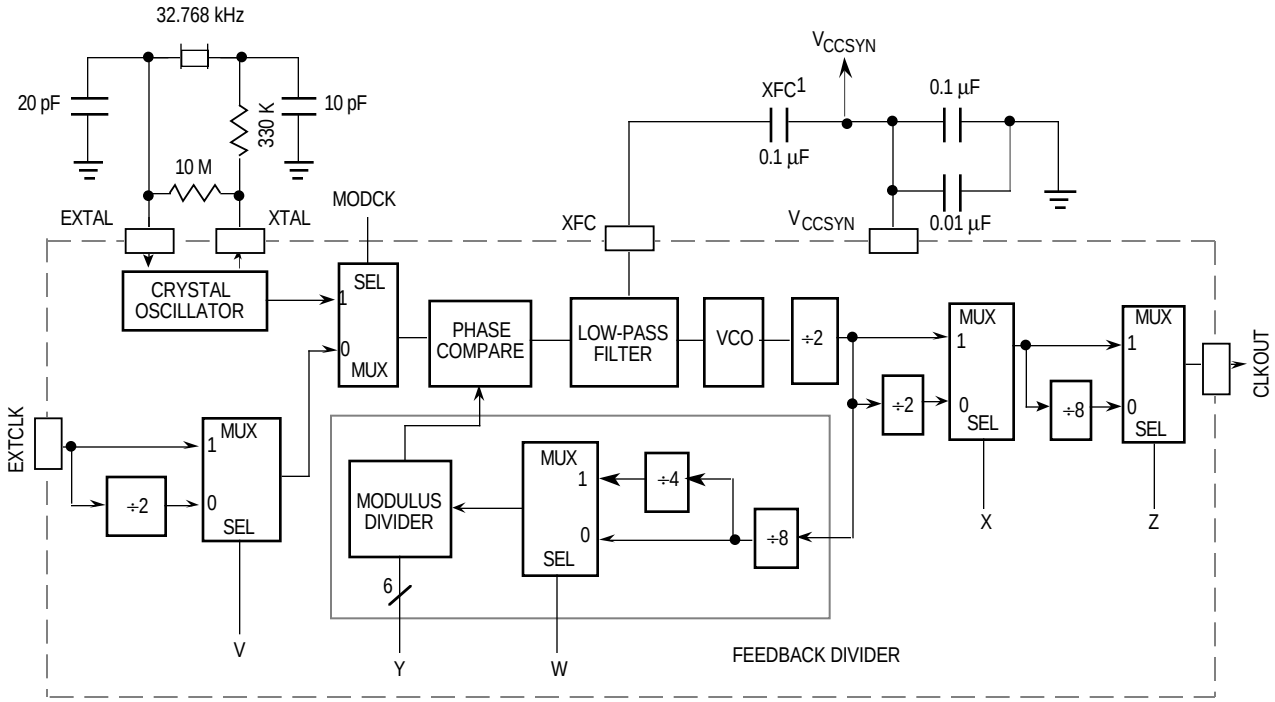
frequency can be any frequency in the range specified in **Section 12 Electrical Characteristics**. When using crystal mode, the system clock frequency is programmable (using the W, X, Y, and Z bits in the SYNCR) over the range specified in **Section 12 Electrical Characteristics** (see Table 4-2.).



1: Must be low-leakage capacitor.

Figure 4-4. Clock Block Diagram for Crystal and EXTCLK Operation

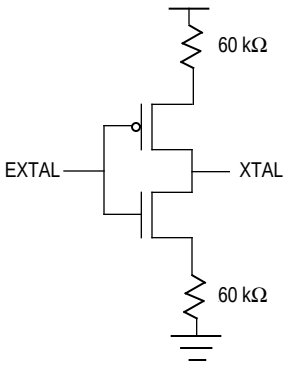


Figure 4-5. MC68341 Crystal Oscillator

A separate power pin (V_{CCSYN}) is used to provide increased noise immunity for the clock circuits. The oscillator Crystal Oscillators always powered if any power is present. If V_{CCSYN} is at V_{CC} it is used. If V_{CCSYN} is at 0V, V_{CC} is used. If $\overline{BSW}$ is asserted, V_{BAT} is used. The source for V_{CCSYN} should be a quiet power supply with adequate external bypass capacitors placed as close as possible to the V_{CCSYN} pin to ensure a stable operating frequency. Figure 4-4 shows typical values for the bypass and PLL external

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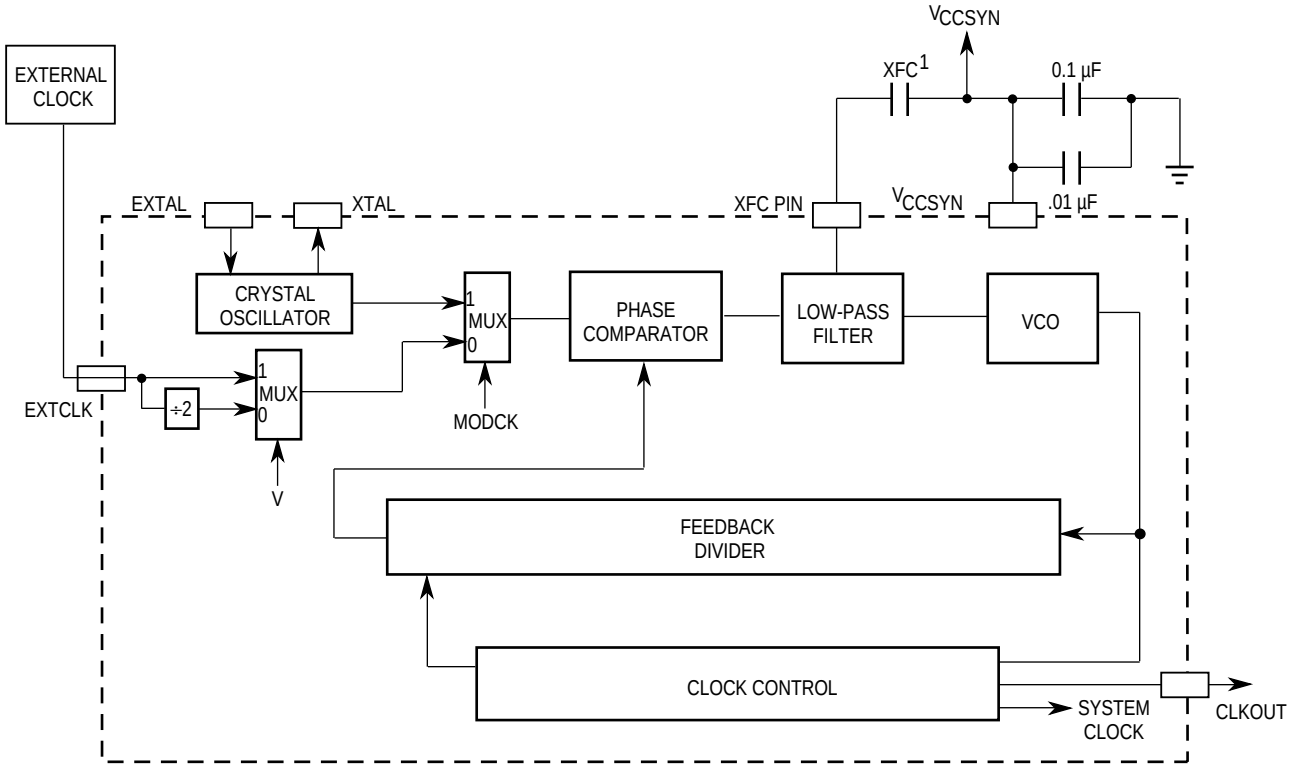
capacitors. The crystal manufacturer's documentation should be consulted for specific recommendations for external components.

4.2.3.2 EXTERNAL CLOCK MODE. To use an external clock source (see Figure 4-6), the operating clock frequency can be driven directly into the EXTCLK pin. The V-bit in the SYNCR allows running the VCO at either the same speed or half the speed of the external clock. This approach results in a system clock and CLKOUT that are the same as the input signal frequency, but not tightly coupled to it. The external clock frequency can optionally be divided by two using the V-bit in SYNCR. To enable this mode, MODCK must be held low during reset, and V_{CCSYN} held at 0 V while the chip is in operation.



NOTES:
1. Must be low-leakage capacitor.

Figure 4-6. Block Diagram for External Clock Operation

Alternatively, an external clock signal can be directly driven into EXTCLK using the on-chip PLL. To enable this mode, MODCK must be held low during reset, and V_{CCSYN} should be connected to a quiet V_{CC} source. (See Table 4-1).

In external clock mode, the V, W, X, Y, and Z bits in the SYNCR can program the system frequency over the range specified in **Section 12 Electrical Characteristics.**

4.2.3.3 LIMP MODE. If an input signal loss for either of the clock modes using the PLL occurs, chip operation can continue in limp mode with the VCO running at approximately one-half the operating speed (affected by the value of the X-bit in the SYNCR), using an internal voltage reference. The SLIMP bit in the SYNCR indicates that a loss of input

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signal reference has been detected. The RSTEN bit in the SYNCR controls whether an input signal loss causes a system reset or causes the device to operate in limp mode. The SLOCK bit in the SYNCR indicates when the VCO has locked onto the desired frequency or if an external clock is being used.

4.2.3.1 PHASE COMPARATOR AND FILTER. The phase comparator takes the output of the frequency divider and compares it to an external input signal reference. The result of this compare is low-pass filtered and used to control the VCO. The comparator also detects when the external crystal or oscillator stops running to initiate the limp mode for the system clock.

The PLL requires an external low-leakage filter capacitor, typically in the range from 0.01 to 0.1 µF, connected between the XFC and V_{CCSYN} pins. The XFC capacitor should provide 50-MΩ insulation but should not be electrolytic. Smaller values of the external filter capacitor provide a faster response time for the PLL, and larger values provide greater frequency stability. For external clock mode without PLL, the XFC pin can be left open.

4.2.3.2 FREQUENCY DIVIDER. The frequency divider circuits divide the VCO frequency down to the reference frequency for the phase comparator. The frequency divider consists of 1) a 2-bit prescaler controlled by the W-bit in the SYNCR and 2) a 6-bit modulo downcounter controlled by the Y-bits in the SYNCR.

The frequency of CLKOUT can additionally be divided by 2 with the X-bit in SYNCR and divided by 8 with the Z-bit in SYNCR.

Several factors are important to the design of the system clock. The resulting system clock frequency must be within the limits specified for the device. The frequency of the system clock is given by the following two equations:

$$F_{SYSTEM} = F_{CRYSTAL}\ [2^{(2W+X+3Z-1)}]\ X\ (Y+1)$$

The maximum VCO frequency limit must also be observed. The VCO frequency is given by the following equation:

$$F_{VCO} = F_{CRYSTAL}[(2)^{(4+2W)}]\ X\ (Y+1) = F_{SYSTEM}[2^{(5-X-3Z)}]$$

The VCO upper frequency limit must be considered when programming the SYNCR. Both the system clock and VCO frequency limits are given in **Section 12 Electrical Characteristics**. Table 4-2 lists some frequencies available from various combinations of SYNCR bits with a reference frequency of 32.768-KHz.

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Table 4-2. System Frequencies from 32.768-kHz Reference

	CLKOUT(kHz)[1]				VCO (kHz)[1]	CLKOUT (kHz)[1]				VCO (kHz)[1]
	W = 0[2]				W = 0[2]	W = 1[2]				W = 1[2]
	Z = 0		Z = 1		Z = x	Z = 0		Z = 1		Z = x
Y[2]	X = 0	X = 1	X = 0	X = 1	X = x	X = 0	X = 1	X = 0	X = 1	X = x
0	16	33	131	262	524	66	1049	524	1049	2097
1	33	66	262	524	1049	131	2097	1049	2097	4194
2	49	98	393	786	1573	197	3146	1573	3146	6291
3	66	131	524	1049	2097	262	4194	2097	4194	8389
4	82	164	655	1311	2621	328	5243	2621	5243	10486
5	98	197	786	1573	3146	393	6291	3146	6291	12583
6	115	229	918	1835	3670	459	7340	3670	7340	14680
7	131	262	1049	2097	4194	524	8389	4194	8389	16777
8	147	295	1180	2359	4719	590	9437	4719	9437	18874
9	164	328	1311	2621	5243	655	10486	5243	10486	20972
10	180	360	1442	2884	5767	721	11534	5767	11534	23069
11	197	393	1573	3146	6291	786	12583	6291	12583	25166
12	213	426	1704	3408	6816	852	13631	6816	13631	27263
13	229	459	1835	3670	7340	918	14680	7340	14680	29360
14	246	492	1966	3932	7864	983	15729	7864	15729	31457
15	262	524	2097	4194	8389	1049	16777	8389	16777	33554
16	279	557	2228	4456	8913	1114	17826	8913	17826	35652
17	295	590	2359	4719	9437	1180	18874	9437	18874	37749
18	311	623	2490	4981	9961	1245	19923	9961	19923	39846
19	328	655	2621	5243	10486	1311	20972	10486	20972	41943
20	344	688	2753	5505	11010	1376	22020	11010	22020	44040
21	360	721	2884	5767	11534	1442	23069	11534	23069	46137
22	377	754	3015	6029	12059	1507	24117	12059	24117	48234
23	393	786	3146	6291	12583	1573	25166	12583	25166	50332
24	410	819	3277	6554	13107	1638	26214	13107	26214	52429
25	426	852	3408	6816	13631	1704	27263	13631	27263	54526
26	442	885	3539	7078	14156	1769	28312	14156	28312	56623
27	459	918	3670	7340	14680	1835	29360	14680	29360	58720
28	475	950	3801	7602	15204	1901	30409	15204	30409	60817
29	492	983	3932	7864	15729	1966	31457	15729	31457	62915
30	508	1016	4063	8126	16253	2032	32506	16253	32506	65012
31	524	1049	4194	8389	16777	2097	33554	16777	33554	67109

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Table 4-2. System Frequencies from 32.768-kHz Reference (Continued)

	CLKOUT (kHz)				VCO (kHz)	CLKOUT (kHz)				VCO (kHz)
	W = 0				W = 0	W = 1				W = 1
	Z = 0		Z = 1		Z = x	Z = 0		Z = 1		Z = x
Y	X = 0	X = 1	X = 0	X = 1	X = x	X = 0	X = 1	X = 0	X = 1	X = x
32	541	1081	4325	8651	17302	2163	34603	17302	34603	69206
33	557	1114	4456	8913	17826	2228	35652	17826	35652	71303
34	573	1147	4588	9175	18350	2294	36700	18350	36700	73400
35	590	1180	4719	9437	18874	2359	37749	18874	37749	75497
36	606	1212	4850	9699	19399	2425	38797	19399	38797	77595
37	623	1245	4981	9961	19923	2490	39846	19923	39846	79692
38	639	1278	5112	10224	20447	2556	40894	20447	40894	81789
39	655	1311	5243	10486	20972	2621	41943	20972	41943	83886
40	672	1343	5374	10748	21496	2687	42992	21496	42992	85983
41	688	1376	5505	11010	22020	2753	44040	22020	44040	88080
42	705	1409	5636	11272	22544	2818	45089	22544	45089	90178
43	721	1442	5767	11534	23069	2884	46137	23069	46137	92275
44	737	1475	5898	11796	23593	2949	47186	23593	47186	94372
45	754	1507	6029	12059	24117	3015	48234	24117	48234	96469
46	770	1540	6160	12321	24642	3080	49283	24642	49283	98566
47	786	1573	6291	12583	25166	3146	50332	25166	50332	100663
48	803	1606	6423	12845	25690	3211	51380	25690	51380	102760
49	819	1638	6554	13107	26214	3277	52429	26214	52429	104858
50	836	1671	6685	13369	26739	3342	53477	26739	53477	106955
51	852	1704	6816	13631	27263	3408	54526	27263	54526	109052
52	868	1737	6947	13894	27787	3473	55575	27787	55575	111149
53	885	1769	7078	14156	28312	3539	56623	28312	56623	113246
54	901	1802	7209	14418	28836	3604	57672	28836	57672	115343
55	918	1835	7340	14680	29360	3670	58720	29360	58720	117441
56	934	1868	7471	14942	29884	3736	59769	29884	59769	119538
57	950	1901	7602	15204	30409	3801	60817	30409	60817	121635
58	967	1933	7733	15466	30933	3867	61866	30933	61866	123732
59	983	1966	7864	15729	31457	3932	62915	31457	62915	125829
60	999	1999	7995	15991	31982	3998	63963	31982	63963	127926
61	1016	2032	8126	16253	32506	4063	65012	32506	65012	130023
62	1032	2064	8258	16515	33030	4129	66060	33030	66060	132121
63	1049	2097	8389	16777	33554	4194	67109	33554	67109	134218

NOTES:

1. Some W/X/Y/Z bit combinations shown may select a CLKOUT or VCO frequency higher than spec. Refer to **Section 11 Electrical Characteristics** for CLKOUT and VCO frequency limits.
2. Any change to W or Y results in a change in the VCO frequency - the VCO should be allowed to relock if necessary

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4.2.3.3 CLOCK CONTROL. The clock control circuits determine the source used for both internal and external clocks during special circumstances, such as low-power stop (LPSTOP) execution.

Table 4-3 summarizes the clock activity during LPSTOP in crystal mode operation. Any clock in the off state is held low. The STEXT and STSIM bits in the SYNCR control clock activity during LPSTOP. Refer to **4.2.6 Low-Power Stop** for additional information.

Table 4-3. Clock Control Signals

Control Bits		Clock Outputs	
STSIM	**STEXT**	**SIMCLK**	**CLKOUT**
0	0	EXTAL	Off
0	1	EXTAL	EXTAL
1	0	VCO	Off
1	1	VCO	VCO

NOTE: SIMCLK runs the periodic interrupt $\overline{\text{RESET}}$ and $\overline{\text{IRQx}}$ pin synchronizers in LPSTOP mode.

4.2.4 Chip Select Operation

Typical microprocessor systems require external hardware to provide select signals to external memory and peripherals. The MC68341 integrates these functions on chip to provide the cost, speed, and reliability benefits of a higher level of integration. The chip select function contains register pairs for each external chip select signal. The pair consists of a base address register and an address mask register that define the characteristics of a single chip select. The register pair provides flexibility for a wide variety of chip select functions.

There are also two registers associated with each chip select to support 68000 bus operation. The bus select register defines the type of bus cycle for each chip select. The map select register defines the 68000 bus byte peripherals.

4.2.4.1 PROGRAMMABLE FEATURES. The chip select function supports the following programmable features:

Eight Programmable Chip Select Circuits

All eight chip select circuits are independently programmable from the same list of selectable features. Each chip select circuit has an individual base address register and address mask register that contain the programmed characteristics of that chip select. The base address register selects the starting address for the address block in 256-byte increments. The address mask register specifies the size of the address block range. The base address register V-bit indicates that the register information for that chip select is valid. A global chip select ($\overline{\text{CS0}}$) allows address decode for a boot ROM before system initialization occurs.

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Variable Block Sizes

The block size, starting from the specified base address, can vary in size from 256 bytes up to 4 Gbytes in 2^n increments. The specified base address must be on a multiple of the block size. The block size is specified in the address mask register.

Both 8- and 16-Bit Ports Supported in M68300 Bus Cycle Mode

The 8-bit ports are accessible on both odd and even addresses when connected to data bus bits 15–8; the 16-bit ports can be accessed as odd bytes, even bytes, or even words in M68300 bus mode. The port size is specified by the PS bits in the address mask register.

Write Protect Capability

The WP bit in each base address register can restrict write access to its range of addresses.

Fast Termination Option (M68300 Bus Mode Only)

Programming the FTE, EDS, and DD bits in the base address register for the fast termination option causes the chip select to terminate the cycle by asserting the internal $\overline{\text{DSACKx}}$ early, providing a two-cycle external access in M68300 mode.

Internal $\overline{\text{DSACKx}}$ Generation for External Accesses with Programmable Wait States

$\overline{\text{DSACKx}}$ can be generated internally with up to six wait states for a particular device using the EDS and DD bits in the address mask register.

Full 32-Bit Address Decode with Address Space Checking

The FC bits in the base address register and FCM bits in the address mask register are used to select address spaces for which the chip selects will be asserted.

4.2.4.2 GLOBAL CHIP SELECT OPERATION. Global chip select operation allows address decode for a boot ROM before system initialization occurs. $\overline{\text{CS0}}$ is the global chip select output, and its operation differs from the other external chip select outputs following reset. When the CPU32 begins fetching after reset, $\overline{\text{CS0}}$ is asserted for every address until the V-bit is set in the $\overline{\text{CS0}}$ base address register.

NOTE

If an access matches multiple chip selects, the lowest numbered chip select will have priority. For example, if $\overline{\text{CS0}}$ and $\overline{\text{CS2}}$ "overlap" for a certain range, $\overline{\text{CS0}}$ will assert when accessing the "overlapped" address range, and $\overline{\text{CS2}}$ will not.

Global chip select provides a 16-bit port with six wait states, which allows a boot ROM to be located in any address space and still provide the stack pointer and program counter values at $00000000 and $00000004, respectively. Global chip select does not provide write protection and responds to all function codes. While $\overline{\text{CS0}}$ is a global chip select, no other chip select ($\overline{\text{CS7}}$–$\overline{\text{CS1}}$) can be used. $\overline{\text{CS0}}$ operates in this manner until the V-bit is set in the $\overline{\text{CS0}}$ base address register, which will then allow the use of $\overline{\text{CS7}}$–$\overline{\text{CS1}}$. Provided

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the desired address range is first loaded into the $\overline{CS0}$ base address register, $\overline{CS0}$ can be programmed to continue decode for a range of addresses after the V-bit is set. After the V-bit is set for $\overline{CS0}$, global chip select can only be restarted with a system reset.

After the V-bit is set, the $\overline{CS0}$ pin can alternately be used as the AVEC input. The AVEC bit in the MCR controls the function of this pin, as shown in Table 4-4.

Table 4-4. Port B Pin Assignment Register

Signal	Pin Function	
	AVEC Bit = 0	AVEC Bit = 1
$\overline{CS0}$	$\overline{CS0}$	$\overline{AVEC}$

A system can use an 8-bit boot ROM if an external 8-bit $\overline{DSACKx}$ that responds in five or less wait states is generated. The 8-bit $\overline{DSACKx}$ must respond in five or less wait states so that the global chip select, which responds with six wait states, will not be used. See **Section 11 Applications** for a detailed discussion.

4.2.5 External Bus Interface Operation

This section describes port A and port B functions. Refer to **Section 3 Bus Operation** for more information about the EBI.

4.2.5.1 PORT A. Port A pins can be independently programmed to function as either addresses A31–A24, discrete I/O pins, or $\overline{IACKx}$ pins. The port A pin assignment registers (PPARA1 and PPARA2) control the function of the port A pins as listed in Table 4-5. Upon reset, port A is configured as input pins. If the system uses these signals as addresses, pulldowns should be put on these signals to avoid indeterminate values until the port A registers can be programmed.

Table 4-5 Port A Pin Assignment Register

Signal	Pin Function		
	PPARA1 = 0 PPARA2 = 0	PPARA1 = 1 PPARA2 = X	PPARA1 = 0 PPARA2 = 1
A31	A31	PORT A7	$\overline{IACK7}$
A30	A30	PORT A6	$\overline{IACK6}$
A29	A29	PORT A5	$\overline{IACK5}$
A28	A28	PORT A4	$\overline{IACK4}$
A27	A27	PORT A3	$\overline{IACK3}$
A26	A26	PORT A2	$\overline{IACK2}$
A25	A25	PORT A1	$\overline{IACK1}$
A24	A24	PORT A0	—

4.2.5.2 PORT B. Port B pins can be independently programmed to function as $\overline{IRQx}$ or discrete I/O pins. Selection of a pin function is accomplished by the port B pin assignment register (PPARB). See Table 4-6 for port B selections. By changing the value of the

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corresponding bits in the PPARB for a particular signal, the port B pins can be configured for different pin functions. Upon reset, port B is configured as $\overline{IRQ7}$–$\overline{IRQ1}$, MODCK.

Table 4-6. Port B Pin Assignment Register

Signal	Pin Function	
	PPARB = 0	PPARB = 1
$\overline{IRQ7}$	PORTB7	$\overline{IRQ7}$
$\overline{IRQ6}$	PORTB6	$\overline{IRQ6}$
$\overline{IRQ5}$	PORTB5	$\overline{IRQ5}$
$\overline{IRQ4}$	PORTB4	$\overline{IRQ4}$
$\overline{IRQ3}$	PORTB3	$\overline{IRQ3}$
$\overline{IRQ2}$	PORTB2	$\overline{IRQ2}$
$\overline{IRQ1}$	PORTB1	$\overline{IRQ1}$
$\overline{IRQ0}$	PORTB0	MODCK

NOTE: MODCK has no function after reset.

4.2.6 Low-Power Stop

Executing the LPSTOP instruction provides reduced power consumption when the MC68341 is idle; only the SIM41 remains active. Operation of the SIM41 clock and CLKOUT during LPSTOP is controlled by the STSIM and STEXT bits in the SYNCR (see Table 4-3). LPSTOP disables the clock to the software watchdog in the low state. The software watchdog remains stopped until the LPSTOP mode ends; it begins to run again on the next rising clock edge.

NOTE

When the CPU32 executes the STOP instruction (as opposed to LPSTOP), the software watchdog continues to run. If the software watchdog is enabled, it issues a reset or interrupt when timeout occurs.

The periodic interrupt timer and real time clock do not respond to an LPSTOP instruction; thus, they can be used to exit LPSTOP as long as their interrupt request level is higher than the CPU32 interrupt mask level. To stop the periodic interrupt timer while in LPSTOP, the PITR must be loaded with a zero value before LPSTOP is executed. The bus monitor, double bus fault monitor, and spurious interrupt monitor are all inactive during LPSTOP.

The STP bit in the MCR of each on-chip module (DMA, timer, and serial modules) should be set prior to executing the LPSTOP instruction. Setting the STP bit stops all clocks within each of the modules, except for the clock from the IMB. The clock from the IMB remains active to allow the CPU32 access to the MCR of each module. The system clock stops on the low phase of the clock and remains stopped until the STP bit is cleared by the CPU32 or until reset. For more information, see the description of the MCR STP bit for each module.

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If an external device requires additional time to prepare for entry into LPSTOP mode, entry can be delayed by asserting $\overline{\text{HALT}}$ (see **3.4.2 LPSTOP Broadcast Cycle**).

4.2.7 Freeze

FREEZE is asserted by the CPU32 if a breakpoint is encountered with background mode enabled. Refer to **Section 5 CPU32** for more information on the background mode. When FREEZE is asserted, the double bus fault monitor and spurious interrupt monitor continue to operate normally. However, the software watchdog, the periodic interrupt timer and the internal bus monitor will be affected. When FREEZE is asserted, setting the FRZ1 bit in the MCR disables the software watchdog and periodic interrupt timer, and setting the FRZ0 bit in the MCR disables the bus monitor.

4.3 PROGRAMMING MODEL

Figure 4-8 is a programming model (register map) of all registers in the SIM41. For more information about a particular register, refer to the description of the module or function indicated in the right column. The ADDR (address) column indicates the offset of the register from the address stored in the module base address register. The FC (function code) column indicates whether a register is restricted to supervisor access (S) or programmable to exist in either supervisor or user space (S/U).

For the registers discussed in the following pages, the number in the upper right-hand corner indicates the offset of the register from the address stored in the module base address register. The numbers on the top line of the register represent the bit position in the register. The second line contains the mnemonic for the bit. The numbers below the register represent the bit values after a hardware reset. The access privilege is indicated in the lower right-hand corner.

NOTE:

A CPU32 RESET instruction will not affect any of the SIM41 registers.

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ADDR	FC	15 8	7 0	
000	S	MODULE CONFIGURATION REGISTER (MCR)		SYS PROTECT
004	S	CLOCK SYNTHESIZER CONTROL REGISTER (SYNCR)		CLOCK
006	S	AUTOVECTOR REGISTER (AVR)	RESET STATUS REGISTER (RSR)	SYS PROTECT
008	S	PROGRAMMABLE INTERRUPT (PIR)		EBI
010	S/U	RESERVED	PORT A DATA (PORTA)	EBI
012	S/U	RESERVED	PORT A DATA DIRECTION (DDRA)	EBI
014	S	RESERVED	PORT A PIN ASSIGNMENT 1 (PPRA1)	EBI
016	S	RESERVED	PORT A PIN ASSIGNMENT 2 (PPRA2)	EBI
018	S/U	RESERVED	PORT B DATA (PORTB)	EBI
01A	S/U	RESERVED	PORT B DATA (PORTB1)	EBI
01C	S/U	RESERVED	PORT B DATA DIRECTION (DDRB)	EBI
01E	S	RESERVED	PORT B PIN ASSIGNMENT (PPARB)	EBI
020	S	SW INTERRUPT VECTOR (SWIV)	SYSTEM PROTECTION CONTROL (SYPCR)	SYS PROTECT
022	S	PERIODIC INTERRUPT CONTROL (PICR)	PERIODIC INTERRUPT VECTOR (PICR)	SYS PROTECT
024	S	SCALE SELECT (SSR)	PERIODIC INTERRUPT TIMING PITR)	SYS PROTECT
026	S	RESERVED	SOFTWARE SERVICE (SWSR)	SYS PROTECT
028	S	RESERVED	PORT C PIN ASSIGNMENT (PPARC)	EBI
03C	S	BUS SELECT (BSR)		CHIP SELECT
03E	S	MAP SELECT (MSR)		CHIP SELECT
040	S	ADDRESS MASK 1 CS0		CHIP SELECT
042	S	ADDRESS MASK 2 CS0		CHIP SELECT
044	S	BASE ADDRESS 1 CS0		CHIP SELECT
046	S	BASE ADDRESS 2 CS0		CHIP SELECT
048	S	ADDRESS MASK 1 CS1		CHIP SELECT
04A	S	ADDRESS MASK 2 CS1		CHIP SELECT
04C	S	BASE ADDRESS 1 CS1		CHIP SELECT
04E	S	BASE ADDRESS 2 CS1		CHIP SELECT
050	S	ADDRESS MASK 1 CS2		CHIP SELECT
052	S	ADDRESS MASK 2 CS2		CHIP SELECT
054	S	BASE ADDRESS 1 CS2		CHIP SELECT
056	S	BASE ADDRESS 2 CS2		CHIP SELECT
058	S	ADDRESS MASK 1 CS3		CHIP SELECT
05A	S	ADDRESS MASK 2 CS3		CHIP SELECT
05C	S	BASE ADDRESS 1 CS3		CHIP SELECT
05E	S	BASE ADDRESS 2 CS3		CHIP SELECT
060	S	ADDRESS MASK 1 CS4		CHIP SELECT
062	S	ADDRESS MASK 2 CS4		CHIP SELECT
064	S	BASE ADDRESS 1 CS4		CHIP SELECT
066	S	BASE ADDRESS 2 CS4		CHIP SELECT

Figure 4-8. SIM41 Programming Model

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068	S	ADDRESS MASK 1 CS5	CHIP SELECT
06A	S	ADDRESS MASK 2 CS5	CHIP SELECT
06C	S	BASE ADDRESS 1 CS5	CHIP SELECT
06E	S	BASE ADDRESS 2 CS5	CHIP SELECT
070	S	ADDRESS MASK 1 CS6	CHIP SELECT
072	S	ADDRESS MASK 2 CS6	CHIP SELECT
074	S	BASE ADDRESS 1 CS6	CHIP SELECT
076	S	BASE ADDRESS 2 CS6	CHIP SELECT
078	S	ADDRESS MASK 1 CS7	CHIP SELECT
07A	S	ADDRESS MASK 2 CS7	CHIP SELECT
07C	S	BASE ADDRESS 1 CS7	CHIP SELECT
07E	S	BASE ADDRESS 2 CS7	CHIP SELECT

0C0	S	MINUTES (MIN)	SECONDS (SEC)	RTC
0C2	S/U	DATE	HOUR	RTC
0C4	S/U	MONTH	YEAR	RTC
0C6	S/U	RTC CONTROL (RCR)	DAY	RTC
0C8	S/U	MINUTES ALARM (MINA)	SECONDS ALARM (SECA)	RTC
0CA	S/U	DATE ALARM (DATEA)	HOURS ALARM (HOURA)	RTC
0CE	S/U	RESERVED	CALIBRATION (RCCR)	RTC

FF	S	RESERVED

Figure 4-8. SIM41 Programming Model (Continued)

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4.3.1 Module Base Address Register (MBAR)

MBAR 1 $0003FF00

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24	BA23	BA22	BA21	BA20	BA19	IBA18	BA17	BA16
RESET: 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CPU Space Only

MBAR 2 $0003FF02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA15	BA14	BA13	BA12	0	0	AS8	AS7	AS6	AS5	AS4	AS3	AS2	AS1	AS0	V
RESET 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CPU Space Only

BA31–BA12—Base Address Bits 31–12

The base address field is the upper 20 bits of the MBAR that provides for block starting locations in increments of 4-Kbytes.

Bits 11, 10—Reserved

AS8–AS0—Address Space Bits 8–0

The address space field allows particular address spaces to be masked, placing the 4K module block into a particular address space(s). If an address space is masked, an access to the register block location in that address space becomes an external access. The module block is not accessed. The address space bits are as follows:

AS8—mask DMA Space	address space (FC3–FC0 = 1xxx)
AS7—mask CPU Space	address space (FC3–FC0 = 0111)
AS6—mask Supervisor Program	address space (FC3–FC0 = 0110)
AS5—mask Supervisor Data	address space (FC3–FC0 = 0101)
AS4—mask Reserved [Motorola]	address space (FC3–FC0 = 0100)
AS3—mask Reserved [User]	address space (FC3–FC0 = 0011)
AS2—mask User Program	address space (FC3–FC0 = 0010)
AS1—mask User Data	address space (FC3–FC0 = 0001)
AS0—mask Reserved [Motorola]	address space (FC3–FC0 = 0000)

For each address space bit:

1 = Mask this address space from the internal module selection. The bus cycle goes external.
0 = Decode for the internal module block.

V—Valid Bit

This bit indicates when the contents of the MBAR are valid. The base address value is not used; therefore, all internal module registers are not accessible until the V-bit is set.

1 = Contents are valid.
0 = Contents are not valid.

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NOTE

An access to this register does not affect external space since the cycle is not run externally.

Example code for accessing the MBAR is as follows:

Register D0 will contain the value of MBAR. MBAR can be read using the following code:

```
MOVE.L      #7,D0          load D0 with the CPU space function code
MOVEC.L     D0,SFC         load SFC to indicate CPU space
LEA.L       $0003FF00,A0   load A0 with the address of MBAR
MOVES.L     (A0),D0        lread MBAR
```

Address $0003FF00 in CPU space (MBAR) will be loaded with the value $FFFFF101. This value will set the base address of the internal registers to $FFFFF000. MBAR can be written to using the following code:

```
MOVE.L      #7,D0          load D0 with the CPU space function code
MOVEC.L     D0,DFC         load DFC to indicate CPU space
LEA.L       $0003FF00,A0   load A0 with the address of MBAR
MOVE.L      #$FFFFF101,D0  base=FFFFF000, AS7=no CPU space, validate
MOVES.L     D0,(A0)        write MBAR
```

4.3.2 System Configuration and Protection Registers

The following paragraphs provide descriptions of the system configuration and protection registers.

4.3.2.1 MODULE CONFIGURATION REGISTER (MCR). The MCR, which controls the SIM41 configuration, can be read or written at any time.

MCR $000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FRZ1	FRZ0	AVEC	0	0	SHEN1	SHEN0	SUPV	0	0	0	IARB3	IARB2	IARB1	IARB0
RESET:															
0	1	1	0	0	0	0	0	1	0	0	0	1	1	1	1

Supervisor Only

Bits 15, 11, 10, 6–4—Reserved

FRZ1—Freeze Software Enable

1 = When FREEZE is asserted, the software watchdog and periodic interrupt timer counters are disabled, preventing interrupts from occurring during software debug.

0 = When FREEZE is asserted, the software watchdog and periodic interrupt timer counters continue to run. See **4.2.7 Freeze** for more information.

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FRZ0—Freeze Bus Monitor Enable

1 = When FREEZE is asserted, the bus monitor is disabled.
0 = When FREEZE is asserted, the bus monitor continues to operate as programmed.

AVEC—Automatic Vector Response

1 = Automatic vector response enabled.
0 = Automatic vector response disabled.

SHEN1, SHEN0—Show Cycle Enable

These two control bits determine what the EBI does with the external bus during internal transfer operations (see Table 4-7). A show cycle allows internal transfers to be externally monitored. The address, data, and control signals (except for $\overline{AS}$) are driven externally. $\overline{DS}$ is used to signal address strobe timing for show cycles. Data is valid on the next falling clock edge after $\overline{DS}$ is negated. However, data is not driven externally, and $\overline{AS}$ and $\overline{DS}$ are not asserted externally for internal accesses unless show cycles are enabled.

If external bus arbitration is disabled, the EBI will not recognize an external bus request until arbitration is enabled again. To prevent bus conflicts, external peripherals must not attempt to initiate cycles during show cycles with arbitration disabled.

Table 4-7. SHENx Control Bits

SHEN1	SHEN0	ACTION
0	0	Show cycles disabled, external arbitration enabled
0	1	Show cycles enabled, external arbitration disabled
1	X	Show cycles enabled, external arbitration enabled

SUPV—Supervisor/User Data Space

The SUPV bit defines the SIM41 registers as either supervisor data space or user (unrestricted) data space.

1 = The SIM41 registers defined as supervisor/user are restricted to supervisor data access (FC3–FC0 = $5). An attempted user-space write is ignored and returns $\overline{BERR}$.
0 = The SIM41 registers defined as supervisor/user data are unrestricted (FC2 is a don't care).

IARB3–IARB0—Interrupt Arbitration Bits 3–0

These bits are used to arbitrate for the bus in the case that two or more modules simultaneously generate an interrupt at the same priority level. No two modules can share the same IARB value. The reset value of IARB is $F, allowing the SIM41 to arbitrate during an IACK cycle immediately after reset. The system software should initialize the IARB field to a value from $F (highest priority) to $1 (lowest priority). A value of $0 prevents arbitration and causes all SIM41 interrupts, including external interrupts, to be discarded as extraneous.

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4.3.2.2 AUTOVECTOR REGISTER (AVR). The AVR contains bits that correspond to external interrupt levels that require an autovector response. Setting a bit allows the SIM41 to assert an internal $\overline{\text{AVEC}}$ during the IACK cycle in response to the specified interrupt request level. This register can be read and written at any time.

AVR $006

7	6	5	4	3	2	1	0
AV7	AV6	AV5	AV4	AV3	AV2	AV1	0
RESET:							
0	0	0	0	0	0	0	0

Supervisor Only

NOTE:

The IARB field in the MCR must contain a value other than $0 for the SIM41 to autovector for external interrupts.

4.3.2.3 RESET STATUS REGISTER (RSR). The RSR contains a bit for each reset source to the SIM41. A set bit indicates the last type of reset that occurred, and only one bit can be set in the register. The RSR is updated by the reset control logic when the SIM41 comes out of reset. This register can be read at any time; a write has no effect. For more information, see **Section 3 Bus Operation.**

RSR $007

7	6	5	4	3	2	1	0
EXT	POW	SW	DBF	0	LOC	SYS	0

Supervisor Only

EXT—External Reset

1 = The last reset was caused by an external signal driving $\overline{\text{RESET}}$.

POW—Power-Up Reset

1 = The last reset was caused by the power-up reset circuit.

SW—Software Watchdog Reset

1 = The last reset was caused by the software watchdog circuit.

DBF—Double Bus Fault Monitor Reset

1 = The last reset was caused by the double bus fault monitor.

Bits 3, 0—Reserved

LOC—Loss of Clock Reset

1 = The last reset was caused by a loss of frequency reference to the clock synthesizer. This reset can only occur if the RSTEN bit in the SYNCR is set and the VCO is enabled.

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SYS—System Reset

1 = The last reset was caused by the CPU32 executing a RESET instruction. The system reset does not load a reset vector or affect any internal CPU32 registers, SIM41 configuration registers, or the MCR in each internal peripheral module (DMA, timers, and serial modules). It will, however, reset external devices and all other registers in the peripheral modules.

4.3.2.4 SOFTWARE INTERRUPT VECTOR REGISTER (SWIV). The SWIV contains the 8-bit vector that is returned by the SIM41 during an IACK cycle in response to an interrupt generated by the software watchdog. This register can be read or written at any time. This register is set to the uninitialized vector, $0F, at reset.

SWIV $020

7	6	5	4	3	2	1	0
SWIV7	SWIV6	SWIV5	SWIV4	SWIV3	SWIV2	SWIV1	SWIV0
RESET:							
0	0	0	0	1	1	1	1

Supervisor Only

4.3.2.5 SYSTEM PROTECTION CONTROL REGISTER (SYPCR). The SYPCR controls the system monitors, the prescaler for the software watchdog, and the bus monitor timing. This register can be read at any time, but can be written only once after reset.

SYPCR $021

7	6	5	4	3	2	1	0
SWE	SWRI	SWT1	SWT0	DBFE	BME	BMT1	BMT0
RESET:							
0	0	0	0	0	0	0	0

Supervisor Only

SWE—Software Watchdog Enable

1 = Software watchdog is enabled.
0 = Software watchdog is disabled.

See **4.2.2.5 Software Watchdog** for more information.

SWRI—Software Watchdog Reset/Interrupt Select

1 = Software watchdog causes a system reset.
0 = Software watchdog causes a level 7 interrupt to the CPU32.

SWT1, SWT0—Software Watchdog Timing

These bits, along with the SWP bit in the PITR, control the divide ratio used to establish the timeout period for the software watchdog. The software watchdog timeout period is given by the following formula:

$$\frac{\text{divide count}}{\text{EXTAL frequency}}$$

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The software watchdog timeout period, listed in Table 4-8, gives the formula to derive the software watchdog timeout for any clock frequency. The timeout periods are listed for a 32.768-kHz crystal used with the VCO and for a 16.777-MHz external oscillator with divide by one selected by the V-bit of the SYNCR.

Table 4-8. Deriving Software Watchdog Timeout

SWP	SWT1	SWT0	Software Timeout Period	32.768-kHz Crystal Period	16.777-MHz External Clock Period
0	0	0	2^9/EXTAL Input Frequency	15.6 ms	30 µs
0	0	1	2^{11}/EXTAL Input Frequency	62.5 ms	122 µs
0	1	0	2^{13}/EXTAL Input Frequency	250 ms	488 µs
0	1	1	2^{15}/EXTAL Input Frequency	1 s	1.95 ms
1	0	0	2^{18}/EXTAL Input Frequency	8 s	15.6 ms
1	0	1	2^{20}/EXTAL Input Frequency	32 s	62.5 ms
1	1	0	2^{22}/EXTAL Input Frequency	128 s	250 ms
1	1	1	2^{24}/EXTAL Input Frequency	512 s	1 s

NOTE: When the SWP and SWT bits are modified to select a software timeout other than the default, the software service sequence ($55 followed by $AA written to the software service register) must be performed before the new timeout period takes effect. Refer to **4.2.2.5 Software Watchdog** for more information.

DBFE—Double Bus Fault Monitor Enable

1 = Enable double bus fault monitor function.
0 = Disable double bus fault monitor function.

For more information, see **4.2.2.3 Double Bus Fault Monitor** and **Section 5 CPU32**.

BME—Bus Monitor External Enable

1 = Enable bus monitor function for an internal-to-external bus cycle.
0 = Disable bus monitor function for an internal-to-external bus cycle.

For more information see **4.2.2.2 Internal Bus Monitor**.

BMT1, BMT0—Bus Monitor Timing

These bits select the timeout period for the bus monitor (see Table 4-9). Upon reset, the bus monitor is set to 512 system clocks.

Table 4-9. BMTx Encoding

BMT1	BMT0	Bus Monitor Timeout Period
0	0	512 system clocks (CLKOUT)
0	1	256 system clocks
1	0	128 system clocks
1	1	64 system clocks

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4.3.2.6 PERIODIC INTERRUPT CONTROL REGISTER (PICR). The PICR contains the interrupt level and the vector number for the periodic interrupt request. This register can be read or written at any time. Bits 15–11 are unimplemented and always return zero; a write to these bits has no effect.

PICR $022

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	PIRQL2	PIRQL1	PIRQL0	PIV7	PIV6	PIV5	PIV4	PIV3	PIV2	PIV1	PIV0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Supervisor Only

Bits 15–11—Reserved

PIRQL2–PIRQL0—Periodic Interrupt Request Level

These bits contain the periodic interrupt request level. Table 4-10 lists which interrupt request level is asserted during an IACK cycle when a periodic interrupt is generated. The periodic timer continues to run when the interrupt is disabled.

Table 4-10. PIRQL Encoding

PIRQL2	PIRQL1	PIRQL0	Interrupt Request Level
0	0	0	Periodic Interrupt Disabled
0	0	1	Interrupt Request Level 1
0	1	0	Interrupt Request Level 2
0	1	1	Interrupt Request Level 3
1	0	0	Interrupt Request Level 4
1	0	1	Interrupt Request Level 5
1	1	0	Interrupt Request Level 6
1	1	1	Interrupt Request Level 7

NOTE:

Use caution with a level 7 interrupt encoding due to the SIM41's interrupt servicing order. See **4.2.2.7 Simultaneous Interrupts by Sources in the SIM41** for the servicing order.

PIV7–PIV0—Periodic Interrupt Vector Bits 7–0

These bits contain the value of the vector generated during an IACK cycle in response to an interrupt from the periodic timer. When the SIM41 responds to the IACK cycle, the periodic interrupt vector from the PICR is placed on the bus. This vector number is multiplied by four to form the vector offset, which is added to the vector base register to obtain the address of the vector.

4.3.2.7 PERIODIC INTERRUPT TIMER REGISTER (PITR). The PITR contains control for prescaling the software watchdog and periodic timer as well as the count value for the

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periodic timer. This register can be read or written at any time. Bits 15–10 are not implemented and always return zero when read. A write does not affect these bits.

PITR $024

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	SWP	PTP	PITR7	PITR6	PITR5	PITR4	PITR3	PITR2	PITR1	PITR0
RESET:															
0	0	0	0	0	0	$\overline{\text{MODCK}}$	$\overline{\text{MODCK}}$	0	0		0	0	0	0	0

Supervisor Only

Bits 15–10—Reserved

SWP—Software Watchdog Prescale

This bit controls the software watchdog clock source as shown in **4.3.2.5 System Protection Control Register (SYPCR)**.

1 = Software watchdog clock prescaled by a value of 512.
0 = Software watchdog clock not prescaled.

The SWP reset value is the inverse of the MODCK bit state on the rising edge of reset.

PTP—Periodic Timer Prescaler Control

This bit contains the prescaler control for the periodic timer.

1 = Periodic timer clock prescaled by a value of 512.
0 = Periodic timer clock not prescaled.

The PTP reset value is the inverse of the MODCK bit state on the rising edge of reset.

PITR7–PITR0—Periodic Interrupt Timer Register Bits 7–0

The remaining bits of the PITR contain the count value for the periodic timer. A zero value turns off the periodic timer.

4.3.2.8 SOFTWARE SERVICE REGISTER (SWSR). The SWSR is the location to which the software watchdog servicing sequence is written. The software watchdog can be enabled or disabled by the SWE bit in the SYPCR. SWSR can be written at any time, but returns all zeros when read.

SWSR $027

7	6	5	4	3	2	1	0
SWSR7	SWSR6	SWSR5	SWSR4	SWSR3	SWSR2	SWSR1	SWSR0
RESET:							
0	0	0	0	0	0	0	0

Supervisor Only

4.3.3 Clock Synthesizer Control Register (SYNCR)

The SYNCR can be read or written only in supervisor mode. The reset state of SYNCR produces an operating frequency of 8.39 MHz when the PLL is referenced to a 32.768-

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kHz reference signal. The system frequency is controlled by the frequency control bits in the upper byte of the SYNCR as follows:

$$F_{SYSTEM} = F_{CRYSTAL}\,[2^{(2W+X+3Z-1)}] \times (Y+1)$$

SYNCR $004

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
W	X	Y5	Y4	Y3	Y2	Y1	Y0	Z	V	0	SLIMP	SLOCK	RSTEN	STSIM	STEXT
RESET:															
0	0	1	1	1	1	1	1	1	0	0	U	U	0	0	0

U = Unaffected by reset Supervisor Only

W—Frequency Control Bit

This bit controls the prescaler tap in the synthesizer feedback loop. Setting the bit increases the VCO frequency by a factor of 4, requiring a time delay for the VCO to relock (see equation for determining system frequency).

X—Frequency Control Bit

This bit controls a divide-by-two prescaler, which is not in the synthesizer feedback loop. Setting the bit doubles the system clock speed without changing the VCO speed, as specified in the equation for determining system frequency; therefore, no delay is incurred to relock the VCO.

Y5–Y0—Frequency Control Bits

The Y-bits, with a value from 0–63, control the modulus downcounter in the synthesizer feedback loop, causing it to divide by the value of Y+1 (see the equation for determining system frequency). Changing these bits requires a time delay for the VCO to relock.

Z—Frequency Control Bit

This bit controls a divide-by-eight. Setting the bit increases the system clock frequency by a factor of eight, without changing the VCO speed.

V—Frequency Control Bit

This bit controls a divide-by-two on the external clock input (EXTCLK). Clearing the bit allows the VCO to run at half the speed of the external clock. Changing the bit value requires a time delay for the VCO to relock.

Bits 5—Reserved

Bit 5 is reserved.

SLIMP—Limp Mode

1 = A loss of input signal reference has been detected, and the VCO is running at approximately one-half the maximum speed (affected by the X-bit), determined from an internal voltage reference.

0 = External input signal frequency is at VCO reference.

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SLOCK—Synthesizer Lock

1 = VCO has locked onto the desired frequency (or system clock is driven externally).
0 = VCO is enabled, but has not yet locked.

RSTEN—Reset Enable

1 = Loss of input signal causes a system reset.
0 = Loss of input signal causes the VCO to operate at a nominal speed without external reference (limp mode), and the device continues to operate at that speed.

STSIM—Stop Mode System Integration Clock

1 = When LPSTOP is executed, the SIM41 clock is driven from the VCO.
0 = When LPSTOP is executed, the SIM41 clock is driven from an external crystal or oscillator, and the VCO is turned off to conserve power.

STEXT—Stop Mode External Clock

1 = When the LPSTOP instruction is executed, the external clock pin (CLKOUT) is driven from the SIM41 clock as determined by the STSIM bit.
0 = When the LPSTOP instruction is executed, the external clock (CLKOUT) is held low to conserve power. No external clock will be driven in LPSTOP mode.

4.3.4 Chip Select Registers

The following paragraphs provide descriptions of the registers in the chip select function, and an example of how to program the registers. The chip select registers cannot be used until the V-bit in the MBAR is set.

4.3.4.1 BASE ADDRESS REGISTERS. There are eight 32-bit base address registers in the chip select function, one for each chip select signal.

Base Address 1 $044, $04C, $054, $05C, $064, $06C, $074, $07C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA31	BA30	BA29	BA28	BA27	BA26	BA25	BA24	BA23	BA22	BA21	BA20	BA19	BA18	BA17	BA16
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

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Base Address 2 $046, $04E, $056, $05E, $066, $06E, $076, $07E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8	BFC3	BFC2	BFC1	BFC0	WP	EDS	NCS	V
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	0	0

U = Unaffected by reset Supervisor Only

BA31–BA8—Base Address Bits 31–8

The base address field, the upper 24 bits of each base address register, selects the starting address for the chip select. The specified base address must be on a multiple of

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the selected block size. The corresponding bits, AM31–AM8, in the address mask register define the size of the block for the chip select. The base address field (and the base function code field) is compared to the address on the address bus to determine if a chip select should be generated.

BFC3–BFC0—Base Function Code Bits 3–0

The value programmed into this field causes a chip select to be asserted for a certain address space type. There are nine function code address spaces (see **Section 3 Bus Operation**) specified as either user or supervisor, program or data, CPU, and DMA. These bits should be used to allow access to one type of address space. If access to more than one type of address space is desired, the FCMx bits should be used in addition to the BFCx bits. To prevent access to CPU space, set the NCS bit.

WP—Write Protect

This bit can restrict write accesses to the address range in a base address register. An attempt to write to the range of addresses specified in a base address register that has this bit set returns $\overline{\text{BERR}}$.

1 = Only read accesses are allowed.
0 = Either read or write accesses are allowed.

EDS—Extended Delay Select

This bit is used in combination with the DD bits in the Address Mask registers to select the number of wait states added before an internal $\overline{\text{DSACKx}}$ is supplied. See Table 4-11.

1 = Extended delay enabled .
0 = Extended delay disabled.

NCS—No CPU Space

This bit specifies whether or not a chip select will assert on a CPU space access cycle (FC3–FC0 = $7 or $F). If both supervisor data and program accesses are desired, while ignoring CPU space accesses, then this bit should be set. The NCS bit is cleared at reset.

1 = Suppress the chip select on a CPU space access.
0 = Assert the chip select on a CPU space access.

V—Valid Bit

This bit indicates that the contents of its base address register and address mask register pair are valid. The programmed chip selects do not assert until the V-bit is set. A reset clears the V-bit in each base address register, but does not change any other bits in the base address and address mask registers ($\overline{\text{CS0}}$ is a special case, see **4.2.4.2 Global Chip Select Operation**).

1 = Contents are valid.
0 = Contents are not valid.

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4.3.4.2 ADDRESS MASK REGISTERS. There are eight 32-bit address mask registers in the chip select function, one for each chip select signal.

Address Mask 1 — $040, $048, $050, $058, $060, $068, $070, $078

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AM31	AM30	AM29	AM28	AM27	AM26	AM25	AM24	AM23	AM22	AM21	AM20	AM19	AM18	AM17	AM16
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

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Address Mask 2 — $042, $04A, $052, $05A, $062, $06A, $072, $07A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AM15	AM14	AM13	AM12	AM11	AM10	AM9	AM8	FCM3	FCM2	FCM1	FCM0	DD1	DD0	PS1	PS0
RESET:															
U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

U = Unaffected by reset — Supervisor Only

AM31–AM8—Address Mask Bits 31–8

The address mask field, the upper 24 bits of each address mask register, defines the chip select block size. The block size is equal to 2^n, where n = (number of bits set in the address mask field) + 8.

Any set bit masks the corresponding base address register bit (the base address register bit becomes a don't care). By masking the address bits independently, external devices of different size address ranges can be used. Address mask bits can be set or cleared in any order in the field, allowing a resource to reside in more than one area of the address map. This field can be read or written at any time.

FCM3–FCM0—Function Code Mask Bits 3–0

This field can be used to mask certain function code bits, allowing more than one address space type to be assigned to a chip select. Any set bit masks the corresponding function code bit.

DD1, DD0—DSACK Delay Bits 1 and 0

This field, in combination with the EDS bit determines the number of wait states added before an internal $\overline{\text{DSACKx}}$ is returned for that entry. Table 4-11 lists the encoding for the DD and EDS bits.

NOTE:

The port size field must be programmed for an internal $\overline{\text{DSACKx}}$ response for the DDx bits to have significance. If external $\overline{\text{DSACKx}}$ signals are returned earlier than indicated by the DDx and EDS bits, the cycle will terminate sooner than programmed.

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Table 4-11. DDx Encoding

EDS	DD1	DD0	Response	Cycle Duration
0	0	0	Zero Wait State	Three Clocks
0	0	1	One Wait State	Four Clocks
0	1	0	Two Wait States	Five Clocks
0	1	1	Three Wait States	Six Clocks
1	0	0	Four Wait State	Seven Clocks
1	0	1	Five Wait State	Eight Clocks
1	1	0	Six Wait States	Nine Clocks
1	1	1	Fast Termination	Two Clocks

PS1, PS0—Port Size Bits 1 and 0

This field determines whether a given chip select responds with $\overline{\text{DSACKx}}$ and, if so, what port size is returned. Table 4-12 lists the encoding for the PSx bits.

Table 4-12. PSx Encoding

PS1	PS0	Mode
0	0	Reserved*
0	1	16-Bit Port
1	0	8-Bit Port
1	1	External $\overline{\text{DSACKx}}$ Response

*Use only for 32-bit DMA transfers.

To use the external $\overline{\text{DSACKx}}$ response, PS1–PS0 = 11 should be selected to suppress internal $\overline{\text{DSACKx}}$ generation. The DDx and EDS bits then have no significance.

4.3.4.3 BUS SELECT REGISTER. Each chip select can be programmed to select either M68000 bus or M68300 bus address space using the bus select register. An access that does not address internal resources or match one of the external chip select address spaces defaults to an MC68300 bus access. The chip selects are gated out with $\overline{\text{AS}}$ or $\overline{\text{68KAS}}$ timing for accesses to M68300 or 68000 bus address spaces respectively.

Bus Select Register $03C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								BSR7	BSR6	BSR5	BSR4	BSR3	BSR2	BSR1	BSR0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Setting a bit in the BSR defines the corresponding chip select to be an M68000 bus access and use $\overline{\text{68KAS}}$ timing for accesses within the defined address range. This register can be read or written at any time.

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4.3.4.4 MAP SELECT REGISTER. The map select register can map byte wide peripherals on the M68000 bus to either the upper or lower half of the data bus (even or odd address space).

Map Select Register $03E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED								MSR7	MSR6	MSR5	MSR4	MSR3	MSR2	MSR1	MSR0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Setting a bit in the MSR defines the corresponding $\overline{CSx}$ bit to be a byte-wide peripheral. Even/odd select capability is provided by pairing of chip selects, so the base address for an even/odd pair is specified in the even chip select register ($\overline{CS2}$ provides base address and range for $\overline{CS2}$ and $\overline{CS3}$ if MSR3 is set). The base address and range information is combined with the size and A0 information drive the corresponding chip select pins for an even/odd pair of chip selects. If an access addresses both even and odd bytes, then the corresponding even and odd chip select pins are asserted.

The chip select implementation requires that odd byte chip selects used for M68000 byte peripherals be paired with even byte chip selects of similar address, but does not restrict even byte peripheral chip selects. For example, if $\overline{CS2}$ is used for an M68000 byte peripheral, but there is no byte peripheral in that address range on the lower half of the data bus, then $\overline{CS3}$ can be used as a general purpose chip select for any address range, bus type, or port size.

4.3.4.5 CHIP SELECT REGISTERS PROGRAMMING EXAMPLE. The following listing is an example of programming a chip select at starting address $00040000, for a block size of 256 Kbytes, accessing supervisor and user data spaces with a 16-bit port requiring two wait states. There will be no write protection, no fast termination, and no CPU space accesses.

base address 1 = $0004
base address 2 = $0013
address mask 1 = $0003
address mask 2 = $FF49

NOTE

If an access matches multiple chip selects, the lowest numbered chip select will have priority. For example, if $\overline{CS0}$ and $\overline{CS2}$ "overlap" for a certain range, $\overline{CS0}$ will assert when accessing the "overlapped" address range, and $\overline{CS2}$ will not.

4.3.5 External Bus Interface Control

The following paragraphs describe the registers that control the I/O pins used with the EBI. Refer to the **Section 3 Bus Operation** for more information about the EBI. For a list of pin numbers used with port A and port B, see the pinout diagram in **Section 13**

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Ordering Information and Mechanical Data. Section 2 Signal Descriptions shows a block diagram of the port control circuits.

4.3.5.1 PORT A PIN ASSIGNMENT REGISTER 1 (PPARA1). PPARA1 selects between an address and discrete I/O function for the port A pins. Any set bit defines the corresponding pin to be an I/O pin, controlled by the port A data and data direction registers. Any cleared bit defines the corresponding pin to be an address bit as defined in the following register diagram. Bits set in this register override the configuration setting of PPARA2. The $FF reset value of PPARA1 configures port A as an input port. This register can be read or written at any time.

PPARA1 $015

7	6	5	4	3	2	1	0
PRTA7 (A31)	PRTA6 (A30)	PRTA5 (A29)	PRTA4 (A28)	PRTA3 (A27)	PRTA2 (A26)	PRTA1 (A25)	PRTA0 (A24)
RESET: 1	1	1	1	1	1	1	1

Supervisor Only

4.3.5.2 PORT A PIN ASSIGNMENT REGISTER 2 (PPARA2). PPARA2 selects between an address and $\overline{\text{IACKx}}$ function for the port A pins. Any set bit defines the corresponding pin to be an $\overline{\text{IACKx}}$ output pin. Any cleared bit defines the corresponding pin to be an address bit as defined in the register diagram. Any set bits in PPARA1 override the configuration set in PPARA2. Bit 0 has no function in this register because there is no level 0 interrupt. This register can be read or written at any time.

PPARA2 $017

7	6	5	4	3	2	1	0
IACK7 (A31)	IACK6 (A30)	IACK5 (A29)	IACK4 (A28)	IACK3 (A27)	IACK2 (A26)	IACK1 (A25)	0
RESET: 0	0	0	0	0	0	0	0

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The $\overline{\text{IACKx}}$ signals are asserted if a bit in PPARA2 is set and the CPU32 services an external interrupt at the corresponding level. $\overline{\text{IACKx}}$ signals have the same timing as address strobes.

4.3.5.3 PORT A DATA DIRECTION REGISTER (DDRA). DDRA controls the direction of the pin drivers when the pins are configured as I/O. Any set bit configures the corresponding pin as an output. Any cleared bit configures the corresponding pin as an input. This register affects only pins configured as discrete I/O. This register can be read or written at any time.

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DDRA $013

7	6	5	4	3	2	1	0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET:							
0	0	0	0	0	0	0	0

Supervisor/User

4.3.5.4 PORT A DATA REGISTER (PORTA). PORTA affects only pins configured as discrete I/O. A write to PORTA is stored in the internal data latch, and if any port A pin is configured as an output, the value stored for that bit is driven on the pin. A read of PORTA returns the value at the pin only if the pin is configured as discrete input. Otherwise, the value read is the value stored in the internal data latch. This register can be read or written at any time.

PORTA $011

7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0
RESET:							
U	U	U	U	U	U	U	U

Supervisor/User

4.3.5.5 PORT B PIN ASSIGNMENT REGISTER (PPARB). PPARB controls the function of each port B pin. Any set bit defines the corresponding pin to be an $\overline{\text{IRQx}}$ input as defined in Table 4-6. Any cleared bit defines the corresponding pin to be a discrete I/O pin controlled by the port B data and data direction registers. The MODCK signal has no function after reset. PPARB is configured to all ones at reset to provide for MODCK, $\overline{\text{IRQ7}}$–$\overline{\text{IRQ1}}$. This register can be read or written at any time.

PPARB $01F

7	6	5	4	3	2	1	0
PPARB7 (IRQ7)	PPARB6 (IRQ6)	PPARB5 (IRQ5)	PPARB4 (IRQ4)	PPARB3 (IRQ3)	PPARB2 (IRQ2)	PPARB1 (IRQ1)	PPARB0 (MODCK)
RESET:							
1	1	1	1	1	1	1	1

Supervisor Only

4.3.5.6 PORT B DATA DIRECTION REGISTER (DDRB). DDRB controls the direction of the pin drivers when the pins are configured as I/O. Any set bit configures the corresponding pin as an output; any cleared bit configures the corresponding pin as an input. This register affects only pins configured as discrete I/O. This register can be read or written at any time.

DDRB $01D

7	6	5	4	3	2	1	0
DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET:							
0	0	0	0	0	0	0	0

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4.3.5.7 PORT B DATA REGISTER (PORTB, PORTB1). This is a single register that can be accessed at two different addresses. This register affects only those pins configured as discrete I/O. A write is stored in the internal data latch, and if any port B pin is configured as an output, the value stored for that bit is driven on the pin. A read of this register returns the value stored in the register only if the pin is configured as a discrete output. Otherwise, the value read is the value of the pin. This register can be read or written at any time.

PORTB, PORTB1 $019, 01B

7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0
RESET:							
U	U	U	U	U	U	U	U

Supervisor/User

4.3.5.8 PORT C PIN ASSIGNMENT REGISTER (PPARC). The MC68341 has multiplexed functions on several pins that had a dedicated function on the MC68340. Five new signals have been added to the DMA module, and the RTCOUT signal is multiplexed with $\overline{\text{RMC}}$. These new alternate functions are selected by setting the appropriate bit in PPARC.

PPARC $029

7	6	5	4	3	2	1	0
TIN / $\overline{\text{RDY2}}$	$\overline{\text{TGATE}}$ / $\overline{\text{RDY1}}$	$\overline{\text{DACK2}}$ / $\overline{\text{DDACK2}}$	$\overline{\text{DACK1}}$ / $\overline{\text{DDACK1}}$	FC3 / $\overline{\text{DTC}}$	$\overline{\text{RMC}}$ / RTCOUT	0	0
RESET:							
0	0	0	0	0	0	0	0

Supervisor Only

4.4 REAL TIME CLOCK

The SIM41 includes a real time clock and calendar function (RTC), that counts seconds, minutes, hours, days, day of the week, date of the month, month, and year with leap year compensation. The RTC can generate both an internal interrupt and an external output (RTCOUT) based on an alarm or time matching function.

The 32.768kHz oscillator and the RTC can continue to operate from the V_{BATT} power pin when VCC is turned off. In typical applications V_{BATT} is connected to a 3V lithium battery to provide backup of the RTC time function. If the $\overline{\text{RMC}}$/RTCOUT signal is configured as RTCOUT before VCC is powered down, the output drivers for RTCOUT are also powered from V_{BATT} to allow the alarm output to be seen by other system devices. During initial system debug, or for systems which do not require the time function to be non-volatile, V_{BATT} and $\overline{\text{BSW}}$ can be connected to VCC to eliminate the need for a separate power supply source.

4.4.1 Reset

Hardware $\overline{\text{RESET}}$ does not affect the clock or calendar functions of the RTC. When $\overline{\text{RESET}}$ is asserted, the following occurs:

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1. The Alarm Indicator Enable/Clear (AIE/$\overline{C}$) bit is cleared.
2. The Alarm Indicator (ALARM) bit is cleared.
3. Interrupt control register (RICR) is cleared.

4.4.2 RTC Interrupt Control Register (RICR)

The RICR contains the interrupt level and the vector number for the RTC alarm interrupt request.

RTC Interrupt Control Register $0C0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	RIRQ2	RIRQ1	RIRQ0	RIV7	RIV6	RIV5	RIV4	RIV3	RIV2	RIV1	RIV0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Supervisor Only

RIRQ2–RIRQ0—RTC Interrupt Request Level

These bits contain the real time clock alarm interrupt request level. Table 4-13 lists the interrupt request level asserted during an IACK cycle when an RTC alarm interrupt occurs. The RTC shares the interrupt arbitration bits with the other sub-modules of the SIM41. The relative priority of the SIM41 interrupt sources is:

1. Watchdog timer
2. Periodic timer
3. RTC alarm interrupt
4. External interrupts

Table 4-13. RIRQL Encoding

RIRQ2	RIRQ1	RIRQ0	Interrupt Request Level
0	0	0	RTC Interrupt Disabled
0	0	1	Interrupt Request Level 1
0	1	0	Interrupt Request Level 2
0	1	1	Interrupt Request Level 3
1	0	0	Interrupt Request Level 4
1	0	1	Interrupt Request Level 5
1	1	0	Interrupt Request Level 6
1	1	1	Interrupt Request Level 7

RIV7–RIV0—RTC Interrupt Vector Bits 7–0

These bits contain the value of the vector generated during an IACK cycle in response to an interrupt from the RTC alarm. When the SIM41 responds to an IACK cycle, the RTC interrupt vector is placed on the bus.

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4.4.3 RTC Control/Status Register (RCR)

The RCR contains the control bits for the RTC.

RCR $0C8

7	6	5	4	3	2	1	0
WR_ERR	ALARM	ERRMUX	ROS1	ROS0	AIE/ C	RCK_HT	SET
RESET:							
U	0	0	0	0	0	0	0

Supervisor Only

WR_ERR—RTC Write Error Indicator

1 = An error has occurred in the contents of the time registers.
0 = No error in the contents of the time registers.

Any illegal combination in the time registers sets this bit, e.g., seconds greater than 59, hours greater than 23, non-BCD data, or day exceeding the maximum for the month selected.

ALARM—RTC Alarm Indicator

1 = Alarm has occurred. In alarm indicator latched mode, this bit remains set until AIE/$\overline{C}$ is cleared. In alarm indicator pulsed mode, this bit clears on reading the RCR.
0 = No alarm condition.

ERRMK—RTC Write Error Mask

1 = Enables the interrupt output from the WR_ERR indicator.Masks the interrupt output from the WR_ERR indicator.
0 = Masks the interrupt output from the WR_ERR indicator.

ROS1, ROS0—RTC Output Select

00 = Alarm indicator latched. RTCOUT is asserted high when the alarm register matches the time, and negated low by clearing the AIE/C bit.
01 = Alarm indicator pulsed. RTCOUT is asserted high when the alarm register matches the time, and negated low one RTC clock (30.5 µS) later. RTCOUT can also be negated by clearing the AIE/C bit.
10 = Square wave. RTCOUT drives a 1.024 KHz square wave (RTC clock ÷ 32)
11 = Alarm indicator latched inverted. RTCOUT is asserted low when the alarm register matches the time, and negated high by clearing the AIE/C bit.

AIE/$\overline{C}$—Alarm Indicator Enable/Clear

1 = Alarm indicator bit can assert
0 = Alarm indicator bit cannot assert. Clearing this bit clears the alarm condition and negates RTCOUT if programmed as an alarm indicator.

RCK_HT—RTC Clock Halt

1 = RTC clock is stopped
0 = RTC clock runs.

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SET—RTC Initialization

1 = Update cycles are inhibited so that time and calendar bytes can be written without an update occurring.
0 = Update cycle functions normally.

4.4.3 RTC Calibration Control Register (RCCR)

The RCCR contains the calibration data and sign bit for the RTC, used to compensate for crystal frequency error. The calibration circuits add or subtract counts at the divide-by-128 stage in the oscillator divide circuit. Positive value adds counts and speeds up the clock; negative values subtract counts and slow the clock down.

RCCR $0CF

7	6	5	4	3	2	1	0
0	RDCLR	RCSN	RCD4	RCD3	RCD2	RCD1	RCD0
RESET:							
U	U	U	U	U	U	U	U

Supervisor Only

RDCLR—RTC Divider Clear

1 = Clears 15-bit RTC clock divider used to generate the 1Hz seconds clock.
0 = Normal divider operation

RCSN—RTC Calibration Sign Bit

1 = Positive calibration (adds to clock count)
0 = Negative calibration (subtracts from clock count)

RCD4–RCD0—RTC Calibration Data

This bit field contains the value (times 128 clock cycles) to be added to the clock count each hour.

RCD4–RCD0—RTC Calibration Data

This bit field contains the value (times 128 clock cycles) to be added to the clock count each hour. Valid range is 0 to 31 ($1F hex). Operation with values from $20-3F is undefined.

At the start of each hour, the value in the calibration data field RCDx is loaded into a counter. If the count is non-zero, the first minute is either shortened or lengthened by 128 clocks (as indicated by the RCSN sign bit), and the count is decremented. This correction process is repeated each successive minute, until the count is exhausted. Each calibration step has the effect of adding or subtracting 128 oscillator cycles every 117,964,800 (32768Hz × 60 sec/min × 60 min/hr) oscillator cycles, or 1.085 PPM of adjustment per calibration step. The 31 steps positive and negative support a total crystal frequency adjustment range of ±33.6 PPM.

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The following procedure may be used to calibrate the RTC:

1. Program the 1.024 kHz signal to be output on RTCOUT.
   a. Set Port C pIn assignment register PPARC bit 2 to a one to select RTCOUT.
   b. Set RCR bits 4:3 to 1:0 to select square wave output.
2. A 1.024 kHz signal can be observed on the RTCOUT pin. Any deviation from 1.024 kHz indicates the degree and direction of the oscillator error. Measure the RTCOUT frequency and use the following formula, substituting the measured frequency in Hz for M. COM is the resulting compensation value.

$$COM = \frac{\left(\frac{M}{1024}\right) - 1}{1.085 \times 10^{-6}}$$

3. Round COM to the nearest integer. The RCSN sign bit should be zero if COM is positive, one if COM is negative. The RCDx data field should be set to the absolute value of COM, converted to hex.

For example, if 1023.9834 Hz is measured on RTCOUT, COM would equal –14.9, or -15 after rounding. Since COM is negative, the RCSN bit should be one. Fifteen equals F hex, so the required RCCR value is 2F. The correctable RTCOUT frequency range is 1024.034 to 1023.966 Hz. The RTCOUT frequency is not affected by the current correction value programmed in the RCCR.

4.4.4 RTC Time of Day Registers

These registers contain the time of day in BCD format.

MIN $0C2

7	6	5	4	3	2	1	0
0	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

SEC $0C3

7	6	5	4	3	2	1	0
0	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

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DATE $0C4

7	6	5	4	3	2	1	0
0	0	DATE5	DATE4	DATE3	DATE2	DATE1	DATE0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

The date counter is a 6-bit BCD counter with a range of 1 to 31 decimal. The date counter and month counter compensate for leap years.

HOUR $0C5

7	6	5	4	3	2	1	0
0	0	HOUR5	HOUR4	HOUR3	HOUR2	HOUR1	HOUR0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

The hours counter is a 24-hour clock only.

MONTH $0C6

7	6	5	4	3	2	1	0
0	0	0	MNT4	MNT3	MNT2	MNT1	MNT0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

YEAR $0C7

7	6	5	4	3	2	1	0
YR7	YR6	YR5	YR4	YR3	YR2	YR1	YR0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

DAY $0C9

7	6	5	4	3	2	1	0
0	0	0	0	0	DOW2	DOW1	DOW0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

The day of the week counter is a 3-bit count-up counter with a range from 0 to 6. The user defines the set value and day-of-week definition for the counter.

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4.4.5 RTC ALARM Registers

These registers contain the time of day alarm registers. Bit 7 of each register is the mask bit for the register, described in Table 4-14. Setting the mask bit in a register makes its match a don't care. The alarm registers are written and read in the same format as the time of day registers.

MINA $0CA

7	6	5	4	3	2	1	0
MX	MIN6	MIN5	MIN4	MIN3	MIN2	MIN1	MIN0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

SECA $0CB

7	6	5	4	3	2	1	0
SX	SEC6	SEC5	SEC4	SEC3	SEC2	SEC1	SEC0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

DATEA $0CC

7	6	5	4	3	2	1	0
DX	0	DATE5	DATE4	DATE3	DATE2	DATE1	DATE0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

HOURA $0CD

7	6	5	4	3	2	1	0
HX	0	HOUR5	HOUR4	HOUR3	HOUR2	HOUR1	HOUR0
RESET:							
U	U	U	U	U	U	U	U

User—Read Only
Supervisor—Read and Write

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Table 4-14 Alarm Bit Setting

SECA	MINA	HOURA	DATEA	Alarm Activated
1	1	1	1	Alarm once per second
0	1	1	1	Alarm when seconds match
0	0	1	1	Alarm when minutes and seconds match
0	0	0	1	Alarm when hours, minutes and seconds match
0	0	0	0	Alarm when date, hours, minutes and seconds match

4.4.6 RTC Power Up Operation

Figure 4-9 is a timing diagram of the power up operation, showing the relationships between $\overline{RESET}$, V_{CC}, CLKOUT, and $\overline{BSW}$. $\overline{BSW}$ is sampled as an asynchronous input by CLKOUT. After V_{CC} has reached the minimum spec operating voltage, $\overline{BSW}$ and $\overline{RESET}$ must remain asserted for at least four system clock cycles before $\overline{BSW}$ is negated. Negation of $\overline{BSW}$ switches the RTC and oscillator power connection from V_{BATT} to either V_{CCSYN} (in crystal mode) or to V_{CC} (in external clock mode). $\overline{BSW}$ should not remain asserted for extended periods of time when V_{CC} voltage is at or above V_{BATT}.

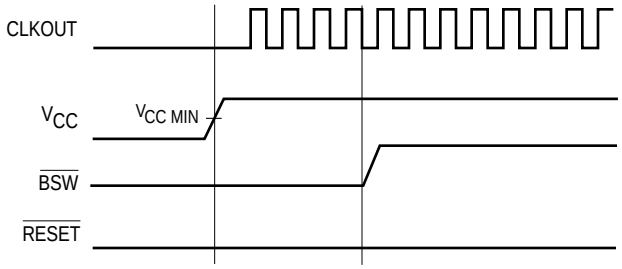

Figure 4-9. Power-Up Reset Timing

4.4.7 RTC Power Down Operation

Figure 4-10 is a timing diagram of the power down operation, showing the relationships between V_{CC}, CLKOUT, and $\overline{BSW}$. $\overline{BSW}$ must be asserted at least three system clock cycles before V_{CC} has reached the minimum spec operating voltage.

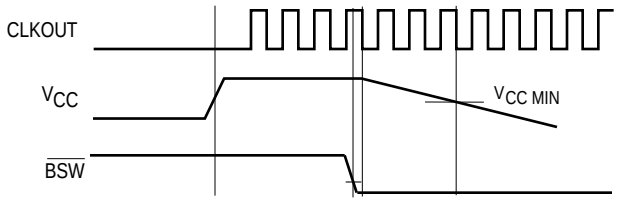

Figure 4-10. Power-Down Timing

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4.5 MC68340 INITIALIZATION SEQUENCE

The following paragraphs discuss a suggested method for initializing the MC68341 after power-up.

4.5.1 Startup

$\overline{\text{RESET}}$ is asserted by the MC68341 during the time in which V_{CC} is ramping up, the VCO is locking onto the frequency, and the MC68341 is going through the reset operation. After $\overline{\text{RESET}}$ is negated, four bus cycles are run, with global $\overline{\text{CS0}}$ being asserted to fetch the 32-bit supervisor stack pointer (SSP) and the 32-bit program counter (PC) from the boot ROM. Until programmed, $\overline{\text{CS0}}$ is a global, 16-bit port, six-wait-state chip select. $\overline{\text{CS0}}$ can be programmed to continue decode for a range of addresses after the V-bit is set, provided the desired address range is first loaded into the $\overline{\text{CS0}}$ base address register. After the V-bit is set for $\overline{\text{CS0}}$, global chip select can only be restarted with a system reset.

After the SSP and the PC are fetched, the module base address register (MBAR) should be initialized, and the MBAR V-bit should be set (CPU space address $0003FF00) with the desired base address for the internal modules.

4.5.2 SIM41 Module Configuration

The order of the following SIM41 register initializations is not important; however, time can be saved by initializing the SYNCR first to quickly increase to the desired processor operating frequency. The module base address register must be initialized prior to any of following steps.

Clock Synthesizer Control Register (SYNCR):

- Set frequency control bits (W, X, Y, Z) to specify frequency.
- Select action taken during loss of crystal (RSTEN bit): activate a system reset or operate in limp mode.
- Select system clock and CLKOUT during LPSTOP (STSIM and STEXT bits).

Module Configuration Register (MCR)

- If using the software watchdog, periodic interrupt timer, and/or the bus monitor, select action taken when FREEZE is asserted (FRZx bits).
- Select AVEC/CS0 configuration (AVEC bit).
- Select the access privilege for the supervisor/user registers (SUPV bit).
- Select the interrupt arbitration level for the SIM41 (IARBx bits).

Autovector Register (AVR)

- Select the desired external interrupt levels for internal autovectoring.

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System Protection Control Register (SYPCR) (Note that this register can only be written once after reset.)

- Enable the software watchdog, if desired (SWE bit).
- If the watchdog is enabled, select whether a system reset or a level 7 interrupt is desired at timeout (SWRI bit).
- If the watchdog is enabled, select the timeout period (SWTx bits).
- Enable the double bus fault monitor, if desired (DBFE bit).
- Enable the external bus monitor, if desired (BME bit).
- Select timeout period for bus monitor (BMTx bits).

Software Watchdog Interrupt Vector Register (SWIV)

- If using the software watchdog, program the vector number for a software watchdog interrupt.

Periodic Interrupt Timer Register (PITR)

- If using the software watchdog, select whether or not to prescale (SWP bit).
- If using the periodic interrupt timer, select whether or not to prescale (PTP bit).
- Program the count value for the periodic timer, or program a zero value to turn off the periodic timer (PITRx bits).

Periodic Interrupt Control Register (PICR)

- If using the periodic timer, program the desired interrupt level for the periodic interrupt timer (PIRQLx bits).
- If using the periodic timer, program the vector number for a periodic timer interrupt.

Chip Select Base Address and Address Mask Registers

- Initialize and set the V-bits in the necessary chip select base address and address mask registers. Following this step, other system resources requiring the $\overline{CSx}$ signals can be accessed. Care must be exercised when changing the address for $\overline{CS0}$. The address of the instruction following the MOVE instruction to the $\overline{CS0}$ base address register must match the value of the PC at that time. $\overline{CS0}$ must be taken out of global chip select mode by setting the V-bit in the base address register before $\overline{CS7}$–$\overline{CS1}$ can be used.

Port A and B Registers

- Program the desired function of the port A signals (PPARA1 and PPARA2 registers).
- Program the desired function of the port B signals (PPARB register).

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4.5.3 SIM41 Example Configuration Code

The following code is an example configuration sequence for the SIM41 module.

```
*****************************************************************************
* MC68341 basic SIM41 register initialization example code:
* This code is used to initialize the MC68341's internal SIM41 registers,
* providing basic functions for operation.
* It includes chip select programming for external devices.
* This code would be programmed beginning at offset $0 into ROM which is
* relocated to address $60000 by the initialization code.
* The SSP_VEC and RST_VEC vectors used to initialize the system stack
* pointer and initial PC, respectively, are located at offset $0 after
* reset.
*****************************************************************************
* equates
*****************************************************************************
SSP_INIT EQU      $10000            Stack pointer initial value - top of RAM
MBAR     EQU      $0003FF00         Address of Module Base Address Reg.
MODBASE  EQU      $FFFFF000         Default Module Base address value

****************************************
* SIM41 register offsets from MBAR base address
MCR      EQU      $00
SYNCR    EQU      $04
SYPCR    EQU      $21
CSAM0    EQU      $40
*****************************************************************************
* Reset vectors
* These two vectors should be located at offset $0 in the boot ROM.
*****************************************************************************
         ORG      $60000
SSP_VEC  DC.L     SSP_INIT          Supervisor stack pointer - initial value
RST_VEC  DC.L     INIT340           Reset vector pointing to init code

*****************************************************************************
* Initialization code
*****************************************************************************
INIT340  MOVE.W   #$2700,SR         Init SR - interrupts masked

*****************************************************************************
* Set up default module base address value
         MOVEQ.L  #7,D0             MBAR is in CPU space
         MOVEC.L  D0,DFC            Load DFC to indicate CPU space
         MOVE.L   #MODBASE+$1BB,D0  Allow DMA, supervisor/user data accesses
         MOVES.L  D0,MBAR           Write to MBAR

*****************************************************************************
```


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```
* Set up system protection register:
* Software watchdog disabled, double bus fault monitor disabled, bus
* monitor BERR after 128 clocks.
        MOVE.B   #6,SYPCR+MODBASE

*************************************************************************
* Clock synthesizer control register:
* Switch from 8.3 to 16.7 MHZ
        MOVE.W   #$7F80,SYNCR+MODBASE       X-bit doubles the default speed

*************************************************************************
* Module configuration register:
* When FREEZE is asserted, software watchdog and periodic interrupt timer
* are disabled, bus monitor is enabled. Show Cycles enabled, external
* arbitration enabled. Supervisor/user SIM registers unrestricted,
* Interrupt Arbitration at priority $F
        MOVE.W   #$420F,MCR+MODBASE

*************************************************************************
* Set up address masks and base addresses for the first 4 chip selects:
        LEA      CSAM0+MODBASE,A0  Point to CS0 addr. mask location.
        MOVEQ    #8-1,D0           Set up loop counter for 2 regs * 4 CSx
        LEA      CSAM0$,A1         Point to init table location.
LOOP    MOVE.L   (A1)+,(A0)+       Init. addr mask and base addr reg
        DBRA     D0,LOOP

*************************************************************************
* Data table for chip select initialization
*************************************************************************
* CS0 - EPROM - 00060000-0007ffff, 3-wait states, 16-bit, write protect, NCS
CSAM0$   DC.L     $0001FFFD
CSBAR0$  DC.L     $0006000B
* CS1 - RAM - 00000000-0000ffff, fast termination, NCS
CSAM1$   DC.L     $0000FFFC
CSBAR1$  DC.L     $00000007
* CS2 - external device - 00FFE8xx, external termination, NCS
CSAM2$   DC.L     $000000F3
CSBAR2$  DC.L     $00FFE803
* CS3 - secondary memory - 00000000-0003ffff, 1-wait state, 8-bit, NCS
CSAM3$   DC.L     $0003FFF6
CSBAR3$  DC.L     $00000003
* CS4-8 unused. Reset invalidates these registers, so initialization
* is not specifically required
CS4$     DC.L     $0,$0
CS5$     DC.L     $0,$0
CS6$     DC.L     $0,$0
CS7$     DC.L     $0,$0
*************************************************************************
         END
```


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SECTION 5
CPU32

The CPU32, the first-generation instruction processing module of the M68300 family, is based on the industry-standard MC68000 core processor. It has many features of the MC68010 and MC68020 as well as unique features suited for high-performance processor applications. The CPU32 provides a significant performance increase over the MC68000 CPU, yet maintains source-code and binary-code compatibility with the M68000 family.

5.1 OVERVIEW

The CPU32 is designed to interface to the intermodule bus (IMB), allowing interaction with other IMB submodules. In this manner, integrated processors can be developed that contain useful peripherals on chip. This integration provides high-speed accesses among the IMB submodules, increasing system performance.

Another advantage of the CPU32 is low power consumption. The CPU32 is implemented in high-speed complementary metal-oxide semiconductor (HCMOS) technology, providing low power use during normal operation. During periods of inactivity, the low-power stop (LPSTOP) instruction can be executed, shutting down the CPU32 and other IMB modules, greatly reducing power consumption.

Ease of programming is an important consideration when using an integrated processor. The CPU32 instruction format reflects a predominant register-memory interaction philosophy. All data resources are available to operations that require them. The programming model includes eight multifunction data registers and seven general-purpose addressing registers. The data registers support 8-bit (byte), 16-bit (word), and 32-bit (long-word) operand lengths for all operations. Address manipulation is supported by word and long-word operations. Although the program counter (PC) and stack pointers (SP) are special-purpose registers, they are also available for most data addressing activities. Ease of program checking and diagnosis is enhanced by trace and trap capabilities at the instruction level.

As processor applications become more complex and programs become larger, high-level languages (HLLs) will become the system designer's choice in programming languages. HLLs aid in the rapid development of complex algorithms with less error and are readily portable. The CPU32 instruction set efficiently supports HLLs.

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5.1.1 Features

Features of the CPU32 are as follows:

- Fully Upward Object-Code Compatible with M68000 Family
- Virtual Memory Implementation
- Loop Mode of Instruction Execution
- Fast Multiply, Divide, and Shift Instructions
- Fast Bus Interface with Dynamic Bus Port Sizing
- Improved Exception Handling for Embedded Control Applications
- Additional Addressing Modes
  - — Scaled Index
  - — Address Register Indirect with Base Displacement and Index
  - — Expanded PC Relative Modes
  - — 32-Bit Branch Displacements
- Instruction Set Additions
  - — High-Precision Multiply and Divide
  - — Trap on Condition Codes
  - — Upper and Lower Bounds Checking
- Enhanced Breakpoint Instruction
- Trace on Change of Flow
- Table Lookup and Interpolate (TBL) Instruction
- LPSTOP Instruction
- Hardware $\overline{\text{BKPT}}$ Signal, Background Mode
- Fully Static Implementation

A block diagram of the CPU32 is shown in Figure 5-1. The major blocks depicted operate in a highly independent fashion that maximizes concurrences of operation while managing the essential synchronization of instruction execution and bus operation. The bus controller loads instructions from the data bus into the decode unit. The sequencer and control unit provide overall chip control by managing the internal buses, registers, and functions of the execution unit.

5.1.2 Virtual Memory

A system that supports virtual memory has a limited amount of high-speed physical memory that can be accessed directly by the processor and maintains an image of a much larger virtual memory on a secondary storage device. When the processor attempts to access a location in the virtual memory map that is not resident in physical memory, a page fault occurs. The access to that location is temporarily suspended while the necessary data is fetched from secondary storage and placed in physical memory. The

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CPU32 uses instruction restart, which requires that only a small portion of the internal machine state be saved. After correcting the page fault, the machine state is restored, and the instruction is refetched and restarted. This process is completely transparent to the application program.

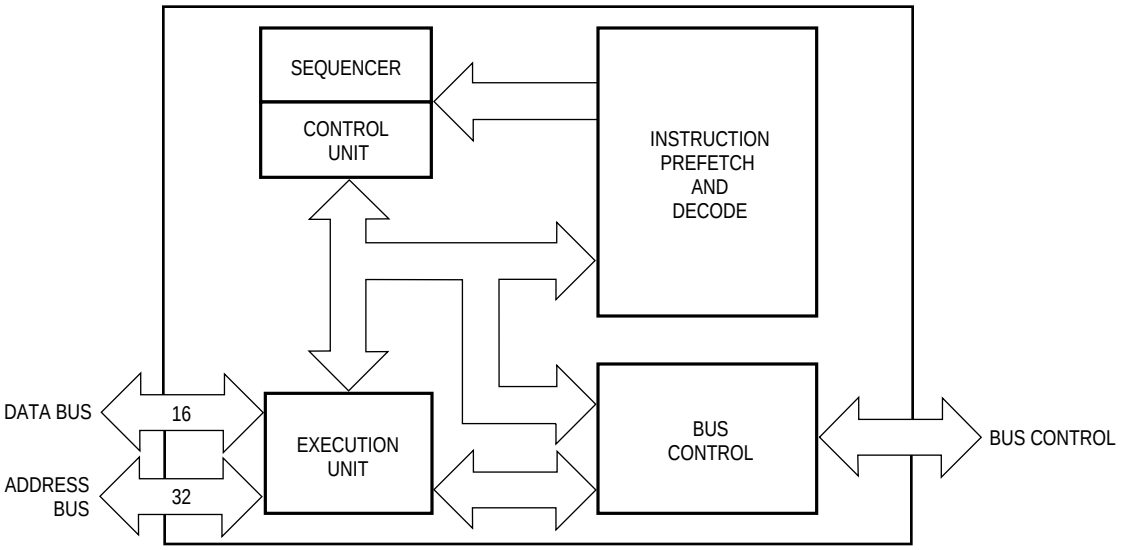

Figure 5-1. CPU32 Block Diagram

5.1.3 Loop Mode Instruction Execution

The CPU32 has several features that provide efficient execution of program loops. One of these features is the DBcc looping primitive instruction. To increase the performance of the CPU32, a loop mode has been added to the processor. The loop mode is used by any single-word instruction that does not change the program flow. Loop mode is implemented in conjunction with the DBcc instruction. Figure 5-2 shows the required form of an instruction loop for the processor to enter loop mode.

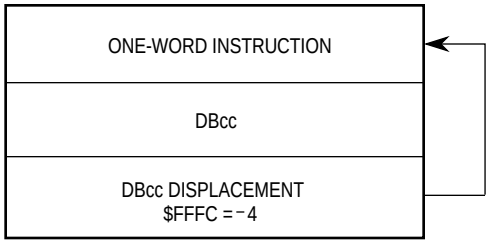

Figure 5-2. Loop Mode Instruction Sequence

The loop mode is entered when the DBcc instruction is executed and the loop displacement is –4. Once in loop mode, the processor performs only the data cycles associated with the instruction and suppresses all instruction fetches. The termination

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condition and count are checked after each execution of the data operations of the looped instruction. The CPU32 automatically exits the loop mode during interrupts or other exceptions.

5.1.4 Vector Base Register

The vector base register (VBR) contains the base address of the 1024-byte exception vector table, which consists of 256 exception vectors. Exception vectors contain the memory addresses of routines that begin execution at the completion of exception processing. These routines perform a series of operations appropriate for the corresponding exceptions. Because the exception vectors contain memory addresses, each consists of one long word, except the reset vector. The reset vector consists of two long words: the address used to initialize the supervisor stack pointer (SSP) and the address used to initialize the PC.

The address of an interrupt exception vector is derived from an 8-bit vector number and the VBR. The vector numbers for some exceptions are obtained from an external device; other numbers are supplied automatically by the processor. The processor multiplies the vector number by 4 to calculate the vector offset, which is added to the VBR. The sum is the memory address of the vector. All exception vectors are located in supervisor data space, except the reset vector, which is located in supervisor program space. Only the initial reset vector is fixed in the processor's memory map; once initialization is complete, there are no fixed assignments. Since the VBR provides the base address of the vector table, the vector table can be located anywhere in memory; it can even be dynamically relocated for each task that is executed by an operating system. Refer to **5.5 Exception Processing** for additional details.

31	0
VECTOR BASE REGISTER (VBR)	

5.1.5 Exception Handling

The processing of an exception occurs in four steps, with variations for different exception causes. During the first step, a temporary internal copy of the status register (SR) is made, and the SR is set for exception processing. During the second step, the exception vector is determined. During the third step, the current processor context is saved. During the fourth step, a new context is obtained, and the processor then proceeds with instruction processing.

Exception processing saves the most volatile portion of the current context by pushing it on the supervisor stack. This context is organized in a format called the exception stack frame. This information always includes the SR and PC context of the processor when the exception occurred. To support generic handlers, the processor places the vector offset in the exception stack frame. The processor also marks the frame with a frame format. The format field allows the return-from-exception (RTE) instruction to identify what information is on the stack so that it may be properly restored.

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5.1.6 Addressing Modes

Addressing in the CPU32 is register oriented. Most instructions allow the results of the specified operation to be placed either in a register or directly in memory; this flexibility eliminates the need for extra instructions to store register contents in memory.

The seven basic addressing modes are as follows:

- Register Direct
- Register Indirect
- Register Indirect with Index
- Program Counter Indirect with Displacement
- Program Counter Indirect with Index
- Absolute
- Immediate

Included in the register indirect addressing modes are the capabilities to postincrement, predecrement, and offset. The PC relative mode also has index and offset capabilities. In addition to these addressing modes, many instructions implicitly specify the use of the SR, SP and/or PC. Addressing is explained fully in the M68000PM/AD, *M68000 Family Programmer's Reference Manual*.

5.2 ARCHITECTURE SUMMARY

The CPU32 is upward source- and object-code compatible with the MC68000 and MC68010. It is downward source- and object-code compatible with the MC68020. Within the M68000 family, architectural differences are limited to the supervisory operating state. User state programs can be executed unchanged on upward-compatible devices.

The major CPU32 features are as follows:

- 32-Bit Internal Data Path and Arithmetic Hardware
- 32-Bit Address Bus Supported by 32-Bit Calculations
- Rich Instruction Set
- Eight 32-Bit General-Purpose Data Registers
- Seven 32-Bit General-Purpose Address Registers
- Separate User and Supervisor Stack Pointers (USP and SSP)
- Separate User and Supervisor Address Spaces
- Separate Program and Data Address Spaces
- Many Data Types
- Flexible Addressing Modes
- Full Interrupt Processing
- Expansion Capability

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5.2.1 Programming Model

The CPU32 programming model consists of two groups of registers that correspond to the user and supervisor privilege levels. User programs can only use the registers of the user model. The supervisor programming model, which supplements the user programming model, is used by CPU32 system programmers who wish to protect sensitive operating system functions. The supervisor model is identical to that of MC68010 and later processors.

The CPU32 has eight 32-bit data registers, seven 32-bit address registers, a 32-bit PC, separate 32-bit SSP and USP, a 16-bit SR, two alternate function code registers, and a 32-bit VBR (see Figures 5-3 and 5-4).

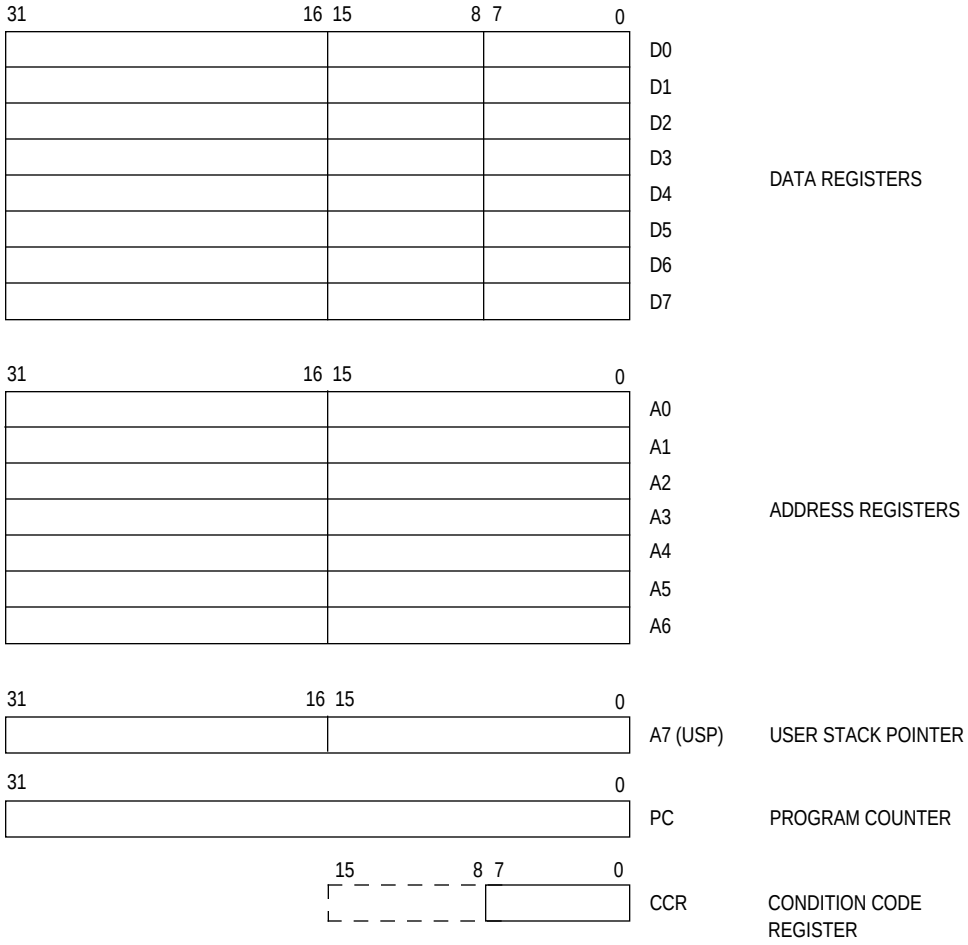

Figure 5-3. User Programming Model

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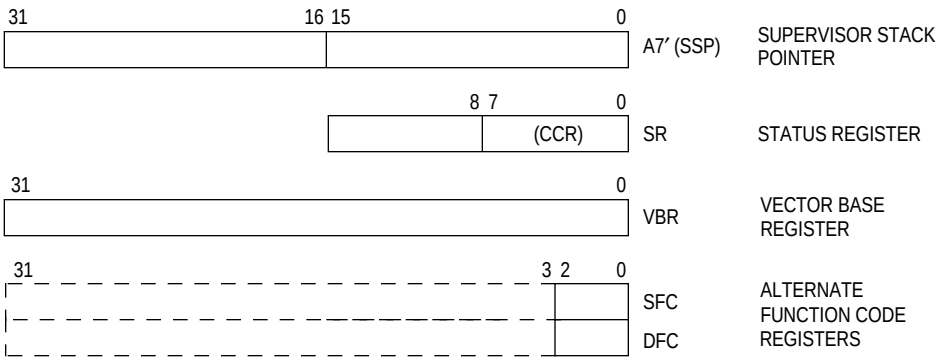

Figure 5-4. Supervisor Programming Model Supplement

5.2.2 Registers

Registers D7–D0 are used as data registers for bit, byte (8-bit), word (16-bit), long-word (32-bit), and quad-word (64-bit) operations. Registers A6 to A0 and the USP and SSP are address registers that may be used as software SPs or base address registers. Register A7 (shown as A7 and A7' in Figures 5-3 and 5-4) is a register designation that applies to the USP in the user privilege level and to the SSP in the supervisor privilege level. In addition, address registers may be used for word and long-word operations. All 16 general-purpose registers (D7–D0, A7–A0) may be used as index registers.

The PC contains the address of the next instruction to be executed by the CPU32. During instruction execution and exception processing, the processor automatically increments the contents of the PC or places a new value in the PC, as appropriate.

The SR (see Figure 5-5) contains condition codes, an interrupt priority mask (three bits), and three control bits. Condition codes reflect the results of a previous operation. The codes are contained in the low byte (CCR) of the SR. The interrupt priority mask determines the level of priority an interrupt must have to be acknowledged. The control bits determine trace mode and privilege level. At user privilege level, only the CCR is available. At supervisor privilege level, software can access the full SR.

The VBR contains the base address of the exception vector table in memory. The displacement of an exception vector is added to the value in this register to access the vector table.

Alternate source and destination function code registers (SFC and DFC) contain 3-bit function codes. The CPU32 generates a function code each time it accesses an address. Specific codes are assigned to each type of access. The codes can be used to select eight dedicated 4-Gbyte address spaces. The MOVEC instruction can use registers SFC and DFC to specify the function code of a memory address.

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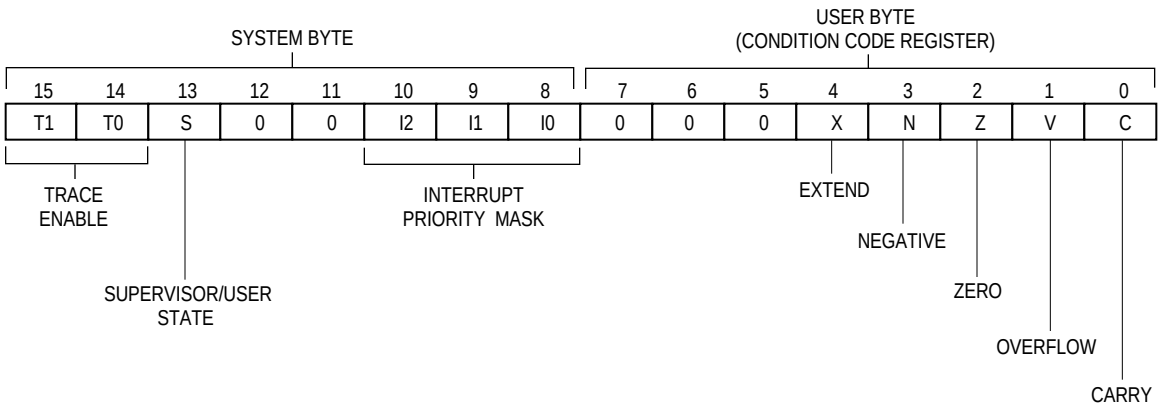

Figure 5-5. Status Register

5.3 INSTRUCTION SET

The following paragaphs describe the CPU32 instruction set. A description of the instruction format, the operands used by the instructions, and a summary of the instructions by category are included. Complete programming information is provided in the M68000PM/AD, *M68000 Family Programmer's Reference Manual.*

The CPU32 instructions include machine functions for all the following operations:

- Data Movement
- Arithmetic Operations
- Logical Operations
- Shifts and Rotates
- Bit Manipulation
- Conditionals and Branches
- System Control

The large instruction set encompasses a complete range of capabilities and, combined with the enhanced addressing modes, provides a flexible base for program development.

The instruction set of the CPU32 is very similar to that of the MC68020 (see Table 5-1). The following M68020 instructions are not implemented on the CPU32:

BFxxx	—	Bit Field Instructions (BFCHG, BFCLR, BFEXTS, BFEXTU, BFFFO, BFINS, BFSET, BFTST)
CALLM, RTM	—	Call Module, Return Module
CAS, CAS2	—	Compare and Set (Read-Modify-Write Instructions)
cpxxx	—	Coprocessor Instructions (cpBcc, cpDBcc, cpGEN, cpRESTORE, cpSAVE, cpScc, cpTRAPcc)
PACK, UNPK	—	Pack, Unpack BCD Instructions

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The CPU32 traps on unimplemented instructions or illegal effective addressing modes, allowing user-supplied code to emulate unimplemented capabilities or to define special-purpose functions. However, Motorola reserves the right to use all currently unimplemented instruction operation codes for future M68000 core enhancements.

Table 5-1. Instruction Set

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
ADDA	Add Address
ADDI	Add Immediate
ADDQ	Add Quick
AND	Logical AND
ANDI	Logical AND Immediate
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally (16 Tests)
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BGND	Enter Background Mode
BKPT	Breakpoint
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register against Bounds
CHK2	Check Register against Upper and Lower Bounds
CLR	Clear Operand
CMP	Compare
CMPA	Compare Address
CMPI	Compare Immediate
CMPM	Compare Memory
CMP2	Compare Register against Upper and Lower Bounds
DBcc	Test Condition, Decrement and Branch (16 Tests)
DIVS, DIVSL	Signed Divide
DIVU, DIVUL	Unsigned Divide
EOR	Logical Exclusive OR
EORI	Logical Exclusive OR Immediate
EXG	Exchange Registers
EXT, EXTB	Sign Extend
ILLEGAL	Take Illegal Instruction Trap
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link and Allocate
LPSTOP	Low-Power Stop
LSL, LSR	Logical Shift Left and Right
MOVE	Move

Mnemonic	Description
MOVEA	Move Address
MOVE CCR	Move Condition Code Register
MOVE SR	Move to/from Status Register
MOVE USP	Move User Stack Pointer
MOVEC	Move Control Register
MOVEM	Move Multiple Registers
MOVEP	Move Peripheral Data
MOVEQ	Move Quick
MOVES	Move Alternate Address Space
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NEGX	Negate with Extend
NOP	No Operation
NOT	Ones Complement
OR	Logical Inclusive OR
ORI	Logical Inclusive OR Immediate
PEA	Push Effective Address
RESET	Reset External Devices
ROL, ROR	Rotate Left and Right
ROXL, ROXR	Rotate with Extend Left and Right
RTD	Return and Deallocate
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditionally
STOP	Stop
SUB	Subtract
SUBA	Subtract Address
SUBI	Subtract Immediate
SUBQ	Subtract Quick
SUBX	Subtract with Extend
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TBLS, TBLSN	Table Lookup and Interpolate, Signed
TBLU, TBLUN	Table Lookup and Interpolate, Unsigned
TRAPcc	Trap Conditionally (16 Tests)
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

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5.3.1 M68000 Family Compatibility

It is the philosophy of the M68000 Family that all user-mode programs should execute unchanged on a more advanced processor and that supervisor-mode programs and exception handlers should require only minimal alteration.

The CPU32 can be thought of as an intermediate member of the M68000 family. Object code from an MC68000 or MC68010 may be executed on the CPU32, and many of the instruction and addressing mode extensions of the MC68020 are also supported.

5.3.1.1 NEW INSTRUCTIONS. Two instructions have been added to the M68000 instruction set for use in embedded control applications: LPSTOP and table lookup and interpolation (TBL).

5.3.1.1.1 Low-Power Stop (LPSTOP). In applications where power consumption is a consideration, the CPU32 can force the device into a low-power standby mode when immediate processing is not required. The low-power mode is entered by executing the LPSTOP instruction. The processor remains in this mode until a user-specified or higher level interrupt or a reset occurs.

5.3.1.1.2 Table Lookup and Interpolate (TBL). To maximize throughput for real-time applications, reference data is often precalculated and stored in memory for quick access. The storage of sufficient data points can require an inordinate amount of memory. The TBL instruction uses linear interpolation to recover intermediate values from a sample of data points, thus conserving memory.

When the TBL instruction is executed, the CPU32 looks up two table entries bounding the desired result and performs a linear interpolation between them. Byte, word, and long-word operand sizes are supported. The result can be rounded according to a round-to-nearest algorithm or returned unrounded along with the fractional portion of the calculated result (byte and word results only). This extra precision can be used to reduce cumulative error in complex calculations. See **5.3.4 Using the TBL Instructions** for examples.

5.3.1.2 UNIMPLEMENTED INSTRUCTIONS. The ability to trap on unimplemented instructions allows user-supplied code to emulate unimplemented capabilities or to define special-purpose functions. However, Motorola reserves the right to use all currently unimplemented instruction operation codes for future M68000 enhancements. See **5.5.2.8 Illegal or Unimplemented Instructions** for more details.

5.3.2 Instruction Format and Notation

All instructions consist of at least one word. Some instructions can have as many as seven words, as shown in Figure 5-6. The first word of the instruction, called the operation word, specifies instruction length and the operation to be performed. The remaining words, called extension words, further specify the instruction and operands. These words may be immediate operands, extensions to the effective address mode specified in the operation word, branch displacements, bit number, special register specifications, trap operands, or argument counts.

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15	0
OPERATION WORD (ONE WORD, SPECIFIES OPERATION AND MODES)	
SPECIAL OPERAND SPECIFIERS (IF ANY, ONE OR TWO WORDS)	
IMMEDIATE OPERAND OR SOURCE ADDRESS EXTENSION (IF ANY, ONE TO THREE WORDS)	
DESTINATION EFFECTIVE ADDRESS EXTENSION (IF ANY, ONE TO THREE WORDS)	

Figure 5-6. Instruction Word General Format

Besides the operation code, which specifies the function to be performed, an instruction defines the location of every operand for the function. Instructions specify an operand location in one of three ways:

- Register Specification — A register field of the instruction contains the number of the register.
- Effective Address — An effective address field of the instruction contains address mode information.
- Implicit Reference — The definition of an instruction implies the use of specific registers.

The register field within an instruction specifies the register to be used. Other fields within the instruction specify whether the register is an address or data register and how it is to be used. The M68000PM/AD, *M68000 Family Programmer's Reference Manual*, contains detailed register information.

Except where noted, the following notation is used in this section:

Data	Immediate data from an instruction
Destination	Destination contents
Source	Source contents
Vector	Location of exception vector
An	Any address register (A7–A0)
Ax, Ay	Address registers used in computation
Dn	Any data register (D7–D0)
Rc	Control register (VBR, SFC, DFC)
Rn	Any address or data register
Dh, Dl	Data registers, high- and low-order 32 bits of product
Dr, Dq	Data registers, division remainder, division quotient
Dx, Dy	Data registers, used in computation
Dym, Dyn	Data registers, table interpolation values
Xn	Index register
[An]	Address extension

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cc	Condition code
d#	Displacement
	Example: d_{16} is a 16-bit displacement
⟨ea⟩	Effective address
#⟨data⟩	Immediate data; a literal integer
label	Assembly program label
list	List of registers
	Example: D3–D0
[...]	Bits of an operand
	Examples: [7] is bit 7; [31:24] are bits 31–24
(...)	Contents of a referenced location
	Example: (Rn) refers to the contents of Rn
CCR	Condition code register (lower byte of SR)
	X—extend bit
	N—negative bit
	Z—zero bit
	V—overflow bit
	C—carry bit
PC	Program counter
SP	Active stack pointer
SR	Status register
SSP	Supervisor stack pointer
USP	User stack pointer
FC	Function code
DFC	Destination function code register
SFC	Source function code register
+	Arithmetic addition or postincrement
–	Arithmetic subtraction or predecrement
/	Arithmetic division or conjunction symbol
×	Arithmetic multiplication
=	Equal to
≠	Not equal to
>	Greater than
≥	Greater than or equal to
<	Less than
≤	Less than or equal to
Λ	Logical AND
V	Logical OR
⊕	Logical exclusive OR
~	Invert; operand is logically complemented

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BCD	Binary-coded decimal, indicated by subscript Example: $Source_{10}$ is a BCD source operand.
LSW	Least significant word
MSW	Most significant word
{R/W}	Read/write indicator

In a description of an operation, a destination operand is placed to the right of source operands and is indicated by an arrow (⇒).

5.3.3 Instruction Summary

The instructions form a set of tools to perform the following operations:

Data Movement	Bit Manipulation
Integer Arithmetic	Binary-Coded Decimal Arithmetic
Logic	Program Control
Shift and Rotate	System Control

The complete range of instruction capabilities combined with the addressing modes described previously provide flexibility for program development. All CPU32 instructions are summarized in Table 5-2.

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Table 5-2. Instruction Set Summary

Opcode	Operation	Syntax
ABCD	$Source_{10}$ + $Destination_{10}$ + X ⇒ Destination	ABCD Dy,Dx ABCD –(Ay),–(Ax)
ADD	Source + Destination ⇒ Destination	ADD ⟨ea⟩,Dn ADD Dn,⟨ea⟩
ADDA	Source + Destination ⇒ Destination	ADDA ⟨ea⟩,An
ADDI	Immediate Data + Destination ⇒ Destination	ADDI #⟨data⟩,⟨ea⟩
ADDQ	Immediate Data + Destination ⇒ Destination	ADDQ #⟨data⟩,⟨ea⟩
ADDX	Source + Destination + X ⇒ Destination	ADDX Dy,Dx ADDX –(Ay),–(Ax)
AND	Source Λ Destination ⇒ Destination	AND ⟨ea⟩, Dn AND Dn,⟨ea⟩
ANDI	Immediate Data Λ Destination ⇒ Destination	ANDI #⟨data⟩,⟨ea⟩
ANDI to CCR	Source Λ CCR ⇒ CCR	ANDI #⟨data⟩,CCR
ANDI to SR	If supervisor state the Source Λ SR ⇒ SR else TRAP	ANDI #⟨data⟩,SR
ASL,ASR	Destination Shifted by ⟨count⟩ ⇒ Destination	ASd Dx,Dy ASd #⟨data⟩,Dy ASd ⟨ea⟩
Bcc	If (condition true) then PC + d ⇒ PC	Bcc ⟨label⟩
BCHG	~(⟨number⟩ of Destination) ⇒ Z; ~(⟨number⟩ of Destination) ⇒ ⟨bit number⟩ of Destination	BCHG Dn,⟨ea⟩ BCHG #⟨data⟩,⟨ea⟩
BCLR	~(⟨number⟩ of Destination) ⇒ Z; 0 ⇒ ⟨bit number⟩ of Destination	BCLR Dn, ⟨ea⟩ BCLR #⟨data⟩,⟨ea⟩
BGND	If (background mode enabled) then enter background mode else Format/Vector offset ⇒ –(SSP) PC ⇒ –(SSP) SR ⇒ –(SSP) (Vector) ⇒ PC	BGND
BKPT	Run breakpoint acknowledge cycle; TRAP as illegal instruction	BKPT #⟨data⟩
BRA	PC + d ⇒ PC	BRA ⟨label⟩
BSET	~(⟨number⟩ of Destination) ⇒ Z; 1 ⇒ ⟨bit number⟩ of Destination	BSET Dn,⟨ea⟩ BSET #⟨data⟩,⟨ea⟩
BSR	SP – 4 ⇒ SP; PC ⇒ (SP); PC + d ⇒ PC	BSR ⟨label⟩
BTST	– (⟨number⟩ of Destination) ⇒ Z;	BTST Dn, ⟨ea⟩ BTST #⟨data⟩,⟨ea⟩
CHK	If Dn < 0 or Dn > Source then TRAP	CHK ⟨ea⟩,Dn
CHK2	If Rn < lower bound or If Rn > upper bound then TRAP	CHK2 ⟨ea⟩,Rn
CLR	0 ⇒ Destination	CLR ⟨ea⟩
CMP	Destination — Source ⇒ cc	CMP ⟨ea⟩,Dn
CMPA	Destination — Source	CMPA ⟨ea⟩,An
CMPI	Destination — Immediate Data	CMPI #⟨data⟩,⟨ea⟩
CMPM	Destination — Source ⇒ cc	CMPM (Ay)+,(Ax)+

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Table 5-2. Instruction Set Summary (Continued)

Opcode	Operation	Syntax
CMP2	Compare Rn < lower-bound or Rn > upper-bound and Set Condition Codes	CMP2 ⟨ea⟩,Rn
DBcc	If condition false then (Dn – 1 ⇒ Dn; If Dn ≠ –1 then PC + d ⇒ PC)	DBcc Dn,⟨label⟩
DIVS DIVSL	Destination/Source ⇒ Destination	DIVS.W ⟨ea⟩,Dn 32/16 ⇒ 16r:16q DIVS.L ⟨ea⟩,Dq 32/32 ⇒ 32q DIVS.L ⟨ea⟩,Dr:Dq 64/32 ⇒ 32r:32q DIVSL.L ⟨ea⟩,Dr:Dq 32/32 ⇒ 32r:32q
DIVU DIVUL	Destination/Source ⇒ Destination	DIVU.W ⟨ea⟩,Dn 32/16 ⇒ 16r:16q DIVU.L ⟨ea⟩,Dq 32/32 ⇒ 32q DIVU.L ⟨ea⟩,Dr:Dq 64/32 ⇒ 32r:32q DIVUL.L ⟨ea⟩,Dr:Dq 32/32 ⇒ 32r:32q
EOR	Source ⊕ Destination ⇒ Destination	EOR Dn,⟨ea⟩
EORI	Immediate Data ⊕ Destination ⇒ Destination	EORI #⟨data⟩,⟨ea⟩
EORI to CCR	Source ⊕ CCR ⇒ CCR	EORI #⟨data⟩,CCR
EORI to SR	If supervisor state the Source ⊕ SR ⇒ SR else TRAP	EORI #⟨data⟩,SR
EXG	Rx ⇔ Ry	EXG Dx,Dy EXG Ax,Ay EXG Dx,Ay EXG Ay,Dx
EXT EXTB	Destination Sign-Extended ⇒ Destination	EXT.W Dn extend byte to word EXT.L Dn extend word to long word EXTB.L Dn extend byte to long word
LLEGAL	SSP – 2 ⇒ SSP; Vector Offset ⇒ (SSP); SSP – 4 ⇒ SSP; PC ⇒ (SSP); SSp – 2 ⇒ SSP; SR ⇒ (SSP); Illegal Instruction Vector Address ⇒ PC	ILLEGAL
JMP	Destination Address ⇒ PC	JMP ⟨ea⟩
JSR	SP – 4 ⇒ SP; PC ⇒ (SP) Destination Address ⇒ PC	JSR ⟨ea⟩
LEA	⟨ea⟩ ⇒ An	LEA ⟨ea⟩,An
LINK	SP – 4 ⇒ SP; An ⇒ (SP) SP ⇒ An, SP + d ⇒ SP	LINK An,#⟨displacement⟩
LPSTOP	If supervisor state Immediate Data ⇒ SR Interrupt Mask ⇒ External Bus Interface (EBI) STOP else TRAP	LPSTOP #⟨data⟩
LSL,LSR	Destination Shifted by ⟨count⟩ ⇒ Destination	LSd[1] Dx,Dy LSd[1] #⟨data⟩,Dy LSd[1] ⟨ea⟩
MOVE	Source ⇒ Destination	MOVE ⟨ea⟩,⟨ea⟩
MOVEA	Source ⇒ Destination	MOVEA ⟨ea⟩,An
MOVE from CCR	CCR ⇒ Destination	MOVE CCR,⟨ea⟩

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Table 5-2. Instruction Set Summary (Continued)

Opcode	Operation	Syntax
MOVE to CCR	Source ⇒ CCR	MOVE ⟨ea⟩,CCR
MOVE from SR	If supervisor state then SR ⇒ Destination else TRAP	MOVE SR,⟨ea⟩
MOVE to SR	If supervisor state then Source ⇒ SR else TRAP	MOVE ⟨ea⟩,SR
MOVE USP	If supervisor state then USP ⇒ An or An ⇒ USP else TRAP	MOVE USP,An MOVE An,USP
MOVEC	If supervisor state then Rc ⇒ Rn or Rn ⇒ Rc else TRAP	MOVEC Rc,Rn MOVEC Rn,Rc
MOVEM	Registers ⇒ Destination Source ⇒ Registers	MOVEM register list,⟨ea⟩ MOVEM ⟨ea⟩,register list
MOVEP	Source ⇒ Destination	MOVEP Dx,(d,Ay) MOVEP (d,Ay),Dx
MOVEQ	Immediate Data ⇒ Destination	MOVEQ #⟨data⟩,Dn
MOVES	If supervisor state then Rn ⇒ Destination [DFC] or Source [SFC]⇒Rn else TRAP	MOVES Rn,⟨ea⟩ MOVES ⟨ea⟩,Rn
MULS	Source × Destination ⇒ Destination	MULS.W ⟨ea⟩,Dn 16 × 16 ⇒ 32 MULS.L ⟨ea⟩,Dl 32 × 32 ⇒ 32 MULS.L ⟨ea⟩,Dh:Dl 32 × 32 ⇒ 64
MULU	Source × Destination ⇒ Destination	MULU.W ⟨ea⟩,Dn 16 × 16 ⇒ 32 MULU.L ⟨ea⟩,Dl 32 × 32 ⇒ 32 MULU.L ⟨ea⟩,Dh:Dl 32 × 32 ⇒ 64
NBCD	0 – (Destination$_{10}$) – X ⇒ Destination	NBCD ⟨ea⟩
NEG	0 – (Destination) ⇒ Destination	NEG ⟨ea⟩
NEGX	0 – (Destination) – X ⇒ Destination	NEGX ⟨ea⟩
NOP	None	NOP
NOT	~Destination ⇒ Destination	NOT ⟨ea⟩
OR	Source V Destination ⇒ Destination	OR ⟨ea⟩,Dn OR Dn,⟨ea⟩
ORI	Immediate Data V Destination ⇒ Destination	ORI #⟨data⟩,⟨ea⟩
ORI to CCR	Source V CCR ⇒ CCR	ORI #⟨data⟩,CCR
ORI to SR	If supervisor state then Source V SR ⇒ SR else TRAP	ORI #⟨data⟩,SR
PEA	Sp – 4 ⇒ SP; ⟨ea⟩ ⇒ (SP)	PEA ⟨ea⟩
RESET	If supervisor state then Assert RESET else TRAP	RESET
ROL,ROR	Destination Rotated by ⟨count⟩ ⇒ Destination	ROd^1 Rx,Dy ROd^1 #⟨data⟩,Dy ROd^1 ⟨ea⟩

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Table 5-2. Instruction Set Summary (Concluded)

Opcode	Operation	Syntax
ROXL,ROXR	Destination Rotated with X by ⟨count⟩ ⇒ Destination	ROXd[1] Rx,Dy ROXd[1] #⟨data⟩,Dy ROXd[1] ⟨ea⟩
RTD	(SP) ⇒ PC; SP + 4 + d ⇒ SP	RTD #⟨displacement⟩
RTE	If supervisor state the (SP) ⇒ SR; SP + 2 ⇒ SP; (SP) ⇒ PC; SP + 4 ⇒ SP; restore state and deallocate stack according to (SP) else TRAP	RTE
RTR	(SP) ⇒ CCR; SP + 2 ⇒ SP; (SP) ⇒ PC; SP + 4 ⇒ SP	RTR
RTS	(SP) ⇒ PC; SP + 4 ⇒ SP	RTS
SBCD	Destination_{10} – Source_{10} – X ⇒ Destination	SBCD Dx,Dy SBCD –(Ax),–(Ay)
Scc	If Condition True then 1s ⇒ Destination else 0s ⇒ Destination	Scc ⟨ea⟩
STOP	If supervisor state then Immediate Data ⇒ SR; STOP else TRAP	STOP #⟨data⟩
SUB	Destination – Source ⇒ Destination	SUB ⟨ea⟩,Dn SUB Dn,⟨ea⟩
SUBA	Destination – Source ⇒ Destination	SUBA ⟨ea⟩,An
SUBI	Destination – Immediate Data ⇒ Destination	SUBI #⟨data⟩,⟨ea⟩
SUBQ	Destination – Immediate Data ⇒ Destination	SUBQ #⟨data⟩,⟨ea⟩
SUBX	Destination – Source – X ⇒ Destination	SUBX Dx,Dy SUBX –(Ax),–(Ay)
SWAP	Register [31:16] ⇔ Register [15:0]	SWAP Dn
TAS	Destination Tested ⇒ Condition Codes; 1 ⇒ bit 7 of Destination	TAS ⟨ea⟩
TBLS	ENTRY(n) + {(ENTRY(n + 1) – ENTRY(n)) × Dx[7:0]} / 256 ⇒ Dx	TBLS.⟨size⟩ ⟨ea⟩, Dx TBLS.⟨size⟩ Dym:Dyn, Dx
TBLSN	ENTRY(n) × 256 + {(ENTRY(n + 1) – ENTRY(n)) × Dx [7:0]} ⇒ Dx	TBLSN.⟨size⟩ ⟨ea⟩,Dx TBLSN.⟨size⟩ Dym:Dyn, Dx
TBLU	ENTRY(n) + {(ENTRY(n + 1) – ENTRY(n)) × Dx[7:0]} / 256 ⇒ Dx	TBLU.⟨size⟩ ⟨ea⟩,Dx TBLU.⟨size⟩ Dym:Dyn, Dx
TBLUN	ENTRY(n) × 256 + {(ENTRY(n + 1) – ENTRY(n)) × Dx[7:0]} ⇒ Dx	TBLUN.⟨size⟩ ⟨ea⟩,Dx TBLUN.⟨size⟩ Dym:Dyn,Dx
TRAP	SSP – 2 ⇒ SSP; Format/Offset ⇒ (SSP); SSP – 4 ⇒ SSP; PC ⇒ (SSP); SSP – 2 ⇒ SSP; SR ⇒ (SSP); Vector Address ⇒ PC	TRAP #⟨vector⟩
TRAPcc	If cc then TRAP	TRAPcc TRAPcc.W #⟨data⟩ TRAPcc.L #⟨data⟩
TRAPV	If V then TRAP	TRAPV
TST	Destination Tested ⇒ Condition Codes	TST ⟨ea⟩
UNLK	An ⇒ SP; (SP) ⇒ An; SP + 4 ⇒ SP	UNLK An

NOTE 1: d is direction, L or R.

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5.3.3.1 CONDITION CODE REGISTER. The CCR portion of the SR contains five bits that indicate the result of a processor operation. Table 5-3 lists the effect of each instruction on these bits. The carry bit and the multiprecision extend bit are separate in the M68000 Family to simplify programming techniques that use them. Refer to Table 5-7 as an example.

Table 5-3. Condition Code Computations

Operations	X	N	Z	V	C	Special Definition
ABCD	*	U	?	U	?	C = Decimal Carry $Z = Z \wedge \overline{Rm} \wedge \ldots \wedge \overline{R0}$
ADD, ADDI, ADDQ	*	*	*	?	?	$V = Sm \wedge Dm \wedge \overline{Rm} \vee \overline{Sm} \wedge \overline{Dm} \wedge Rm$ $C = Sm \wedge Dm \vee \overline{Rm} \wedge Dm \vee Sm \wedge \overline{Rm}$
ADDX	*	*	?	?	?	$V = Sm \wedge Dm \wedge \overline{Rm} \vee \overline{Sm} \wedge \overline{Dm} \wedge Rm$ $C = Sm \wedge Dm \vee \overline{Rm} \wedge Dm \vee Sm \wedge \overline{Rm}$ $Z = Z \wedge \overline{Rm} \wedge \ldots \wedge \overline{R0}$
AND, ANDI, EOR, EORI, MOVEQ, MOVE, OR, ORI, CLR, EXT, NOT, TAS, TST	—	*	*	0	0	
CHK	—	*	U	U	U	
CHK2, CMP2	—	U	?	U	?	Z = (R = LB) V (R = UB) C = (LB < UB) $\wedge$ (IR < LB) V (R > UB) V (UB < LB) $\wedge$ (R > UB) $\wedge$ (R < LB)
SUB, SUBI, SUBQ	*	*	*	?	?	$V = \overline{Sm} \wedge Dm \wedge \overline{Rm} \vee Sm \wedge \overline{Dm} \wedge Rm$ $C = Sm \wedge \overline{Dm} \vee Rm \wedge \overline{Dm} \vee Sm \wedge Rm$
SUBX	*	*	?	?	?	$V = \overline{Sv} \wedge Dm \wedge \overline{Rv} \vee Sm \wedge \overline{Dv} \wedge Rm$ $C = Sm \wedge \overline{Dv} \vee Rm \wedge \overline{Dv} \vee Sm \wedge Rm$ $Z = Z \wedge \overline{Rv} \wedge \ldots \wedge \overline{R0}$
CMP, CMPI, CMPM	—	*	*	?	?	$V = \overline{Sv} \wedge Dm \wedge \overline{Rv} \vee Sm \wedge \overline{Dv} \wedge Rm$ $C = Sm \wedge \overline{Dv} \vee Rm \wedge \overline{Dv} \vee Sm \wedge Rm$
DIVS, DIVU	—	*	*	?	0	V = Division Overflow
MULS, MULU	—	*	*	?	0	V = Multiplication Overflow
SBCD, NBCD	*	U	?	U	?	C = Decimal Borrow $Z = Z \wedge \overline{Rm} \wedge \ldots \wedge \overline{R0}$
NEG	*	*	*	?	?	$V = Dm \wedge Rm$ $C = Dm \vee Rm$
NEGX	*	*	?	?	?	$V = Dm \wedge Rm$ $C = Dm \vee Rm$ $Z = Z \wedge \overline{Rm} \wedge \ldots \wedge \overline{R0}$
ASL	*	*	*	?	?	$V = Dm \wedge (\overline{Dm-1} \vee \ldots \vee \overline{Dm-r}) \vee \overline{Dm} \wedge$ $(Dm-1 \vee \ldots + Dm-r)$ $C = \overline{Dm-r+1}$
ASL (r = 0)	—	*	*	0	0	
LSL, ROXL	*	*	*	0	?	C = Dm – r + 1
LSR (r = 0)	—	*	*	0	0	
ROXL (r = 0)	—	*	*	0	?	C = X
ROL	—	*	*	0	?	C = Dm – r + 1
ROL (r = 0)	—	*	*	0	0	
ASR, LSR, ROXR	*	*	*	0	?	C = Dr – 1
ASR, LSR (r = 0)	—	*	*	0	0	
ROXR (r = 0)	—	*	*	0	?	C = X

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Table 5-3. Condition Code Computations (Continued)

Operations	X	N	Z	V	C	Special Definition
ROR	—	*	*	0	?	C = Dr – 1
ROR (r = 0)	—	*	*	0	0	

NOTE: The following notations apply to this table only.

—	=	Not affected	Sm	=	Source operand MSB
U	=	Undefined	Dm	=	Destination operand MSB
?	=	See special definition	Rm	=	Result operand MSB
*	=	General case	R	=	Register tested
X	=	C	n	=	Bit Number
N	=	Rm	r	=	Shift count
Z	=	$\overline{Rm} \wedge ... \wedge \overline{R0}$	LB	=	Lower bound
$\wedge$	=	Boolean AND	UB	=	Upper bound
V	=	Boolean OR	$\overline{Rm}$	=	NOT Rm

5.3.3.2 DATA MOVEMENT INSTRUCTIONS. The MOVE instruction is the basic means of transferring and storing address and data. MOVE instructions transfer byte, word, and long-word operands from memory to memory, memory to register, register to memory, and register to register. Address movement instructions (MOVE or MOVEA) transfer word and long-word operands and ensure that only valid address manipulations are executed.

In addition to the general MOVE instructions, there are several special data movement instructions—move multiple registers (MOVEM), move peripheral data (MOVEP), move quick (MOVEQ), exchange registers (EXG), load effective address (LEA), push effective address (PEA), link stack (LINK), and unlink stack (UNLK). Table 5-4 is a summary of the data movement operations.

Table 5-4. Data Movement Operations

Instruction	Operand Syntax	Operand Size	Operation
EXG	Rn, Rn	32	Rn ⇒ Rn
LEA	⟨ea⟩, An	32	⟨ea⟩ ⇒ An
LINK	An, #⟨d⟩	16, 32	SP – 4 ⇒ SP, An ⇒ (SP); SP ⇒ An, SP + d ⇒ SP
MOVE	⟨ea⟩, ⟨ea⟩	8, 16, 32	Source ⇒ Destination
MOVEA	⟨ea⟩, An	16, 32 ⇒ 32	Source ⇒ Destination
MOVEM	list, ⟨ea⟩ ⟨ea⟩, list	16, 32 16, 32 ⇒ 32	Listed registers ⇒ Destination Source ⇒ Listed registers
MOVEP	Dn, (d_{16}, An) (d_{16}, An), Dn	16, 32	Dn [31:24] ⇒ (An + d); Dn [23:16] ⇒ (An + d + 2); Dn [15:8] ⇒ (An + d + 4); Dn [7:0] ⇒ (An + d + 6) (An + d) ⇒ Dn [31:24]; (An + d + 2) ⇒ Dn [23:16]; (An + d + 4) ⇒ Dn [15:8]; (An + d + 6) ⇒ Dn [7:0]
MOVEQ	#⟨data⟩, Dn	8 ⇒ 32	Immediate Data ⇒ Destination
PEA	⟨ea⟩	32	SP – 4 ⇒ SP; ⟨ea⟩ ⇒ SP
UNLK	An	32	An ⇒ SP; (SP) ⇒ An, SP + 4 ⇒ SP

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5.3.3.3 INTEGER ARITHMETIC OPERATIONS. The arithmetic operations include the four basic operations of add (ADD), subtract (SUB), multiply (MUL), and divide (DIV) as well as arithmetic compare (CMP, CMPM, CMP2), clear (CLR), and negate (NEG). The instruction set includes ADD, CMP, and SUB instructions for both address and data operations with all operand sizes valid for data operations. Address operands consist of 16 or 32 bits. The clear and negate instructions apply to all sizes of data operands.

Signed and unsigned MUL and DIV instructions include:

- Word multiply to produce a long-word product
- Long-word multiply to produce a long-word or quad-word product
- Division of a long-word dividend by a word divisor (word quotient and word remainder)
- Division of a long-word or quad-word dividend by a long-word divisor (long-word quotient and long-word remainder)

A set of extended instructions provides multiprecision and mixed-size arithmetic. These instructions are add extended (ADDX), subtract extended (SUBX), sign extend (EXT), and negate binary with extend (NEGX). Refer to Table 5-5 for a summary of the integer arithmetic operations.

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Table 5-5. Integer Arithmetic Operations

Instruction	Operand Syntax	Operand Size	Operation
ADD	Dn, ⟨ea⟩ ⟨ea⟩, Dn	8, 16, 32 8, 16, 32	Source + Destination ⇒ Destination
ADDA	⟨ea⟩, An	16, 32	Source + Destination ⇒ Destination
ADDI	#⟨data⟩, ⟨ea⟩	8, 16, 32	Immediate Data + Destination ⇒ Destination
ADDQ	#⟨data⟩, ⟨ea⟩	8, 16, 32	Immediate Data + Destination ⇒ Destination
ADDX	Dn, Dn – (An), – (An)	8, 16, 32 8, 16, 32	Source + Destination + X ⇒ Destination
CLR	⟨ea⟩	8, 16, 32	0 ⇒ Destination
CMP	⟨ea⟩, Dn	8, 16, 32	(Destination – Source), CCR shows results
CMPA	⟨ea⟩, An	16, 32	(Destination – Source), CCR shows results
CMPI	#⟨data⟩, ⟨ea⟩	8, 16, 32	(Destination – Immediate Data), CCR shows results
CMPM	(An) +, (An) +	8, 16, 32	(Destination – Source), CCR shows results
CMP2	⟨ea⟩, Rn	8, 16, 32	Lower bound ≤ Rn ≤ Upper Bound, CCR shows results
DIVS/DIVU DIVSL/DIVUL	⟨ea⟩, Dn ⟨ea⟩, Dr:Dq ⟨ea⟩, Dq ⟨ea⟩, Dr:Dq	32/16 ⇒ 16:16 64/32 ⇒ 32:32 32/32 ⇒ 32 32/32 ⇒ 32:32	Destination/Source ⇒ Destination (signed or unsigned)
EXT	Dn Dn	8 ⇒ 16 16 ⇒ 32	Sign Extended Destination ⇒ Destination
EXTB	Dn	8 ⇒ 32	Sign Extended Destination ⇒ Destination
MULS/MULU	⟨ea⟩, Dn ⟨ea⟩, Dl ⟨ea⟩, Dh:Dl	16 × 16 ⇒ 32 32 × 32 ⇒ 32 32 × 32 ⇒ 64	Source × Destination ⇒ Destination (signed or unsigned)
NEG	⟨ea⟩	8, 16, 32	0 – Destination ⇒ Destination
NEGX	⟨ea⟩	8, 16, 32	0 – Destination – X ⇒ Destination
SUB	⟨ea⟩, Dn Dn, ⟨ea⟩	8, 16, 32	Destination – Source ⇒ Destination
SUBA	⟨ea⟩, An	16, 32	Destination – Source ⇒ Destination
SUBI	#⟨data⟩, ⟨ea⟩	8, 16, 32	Destination – Immediate Data ⇒ Destination
SUBQ	#⟨data⟩, ⟨ea⟩	8, 16, 32	Destination – Immediate Data ⇒ Destination
SUBX	Dn, Dn – (An), – (An)	8, 16, 32 8, 16, 32	Destination – Source – X ⇒ Destination
TBLS/TBLU	⟨ea⟩, Dn Dym:Dyn, Dn	8, 16, 32	Dyn – Dym ⇒ Temp (Temp × Dn [7:0]) ⇒ Temp (Dym × 256) + Temp ⇒ Dn
TBLSN/TBLUN	⟨ea⟩, Dn Dym:Dyn, Dn	8, 16, 32	Dyn – Dym ⇒ Temp (Temp × Dn [7:0]) / 256 ⇒ Temp Dym + Temp ⇒ Dn

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5.3.3.4 LOGIC INSTRUCTIONS. The logical operation instructions (AND, OR, EOR, and NOT) perform logical operations with all sizes of integer data operands. A similar set of immediate instructions (ANDI, ORI, and EORI) provide these logical operations with all sizes of immediate data. The test (TST) instruction arithmetically compares the operand with zero, placing the result in the CCR. Table 5-6 summarizes the logical operations.

Table 5-6. Logic Operations

Instruction	Operand Syntax	Operand Size	Operation
AND	⟨ea⟩, Dn Dn, ⟨ea⟩	8, 16, 32 8, 16, 32	Source Λ Destination ⇒ Destination
ANDI	#⟨data⟩, ⟨ea⟩	8, 16, 32	Immediate Data Λ Destination ⇒ Destination
EOR	Dn, ⟨ea⟩	8, 16, 32	Source ⊕ Destination ⇒ Destination
EORI	#⟨data⟩, ⟨ea⟩	8, 16, 32	Immediate Data ⊕ Destination ⇒ Destination
NOT	⟨ea⟩	8, 16, 32	$\overline{\text{Destination}}$ ⇒ Destination
OR	⟨ea⟩, Dn Dn, ⟨ea⟩	8, 16, 32 8, 16, 32	Source V Destination ⇒ Destination
ORI	#⟨data⟩, ⟨ea⟩	8, 16, 32	Immediate Data V Destination ⇒ Destination
TST	⟨ea⟩	8, 16, 32	Source – 0, to set condition codes

5.3.3.5 SHIFT AND ROTATE INSTRUCTIONS. The arithmetic shift instructions, ASR and ASL, and logical shift instructions, LSR and LSL, provide shift operations in both directions. The ROR, ROL, ROXR, and ROXL instructions perform rotate (circular shift) operations, with and without the extend bit. All shift and rotate operations can be performed on either registers or memory.

Register shift and rotate operations shift all operand sizes. The shift count may be specified in the instruction operation word (to shift from 1 to 8 places) or in a register (modulo 64 shift count).

Memory shift and rotate operations shift word-length operands one bit position only. The SWAP instruction exchanges the 16-bit halves of a register. Performance of shift/rotate instructions is enhanced so that use of the ROR and ROL instructions with a shift count of eight allows fast byte swapping. Table 5-7 is a summary of the shift and rotate operations.

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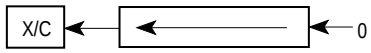
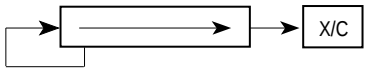
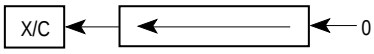
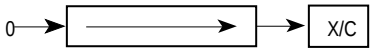
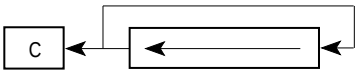
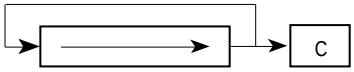
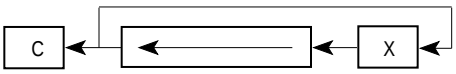
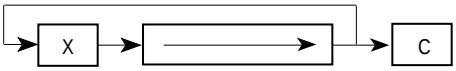
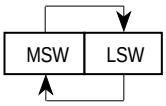
Table 5-7. Shift and Rotate Operations

Instruction	Operand Syntax	Operand Size	Operation
ASL	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
ASR	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
LSL	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
LSR	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
ROL	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
ROR	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
ROXL	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
ROXR	Dn, Dn #⟨data⟩, Dn ⟨ea⟩	8, 16, 32 8, 16, 32 16	
SWAP	Dn	16	

5.3.3.6 BIT MANIPULATION INSTRUCTIONS. Bit manipulation operations are accomplished using the following instructions: bit test (BTST), bit test and set (BSET), bit test and clear (BCLR), and bit test and change (BCHG). All bit manipulation operations can be performed on either registers or memory. The bit number is specified as immediate data or in a data register. Register operands are 32 bits, and memory operands are 8 bits. Table 5-8 is a summary of bit manipulation instructions.

Table 5-8. Bit Manipulation Operations

Instruction	Operand Syntax	Operand Size	Operation
BCHG	Dn, ⟨ea⟩ #⟨data⟩, ⟨ea⟩	8, 32 8, 32	~(⟨bit number⟩ of destination) ⇒ Z ⇒ bit of destination
BCLR	Dn, ⟨ea⟩ #⟨data⟩, ⟨ea⟩	8, 32 8, 32	~(⟨bit number⟩ of destination) ⇒ Z; 0 ⇒ bit of destination
BSET	Dn, ⟨ea⟩ #⟨data⟩, ⟨ea⟩	8, 32 8, 32	~(⟨bit number⟩ of destination) ⇒ Z; 1 ⇒ bit of destination
BTST	Dn, ⟨ea⟩ #⟨data⟩, ⟨ea⟩	8, 32 8, 32	~(⟨bit number⟩ of destination) ⇒ Z

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5.3.3.7 BINARY-CODED DECIMAL (BCD) INSTRUCTIONS. Five instructions support operations on BCD numbers. The arithmetic operations on packed BCD numbers are add decimal with extend (ABCD), subtract decimal with extend (SBCD), and negate decimal with extend (NBCD). Table 5-9 is a summary of the BCD operations.

Table 5-9. Binary-Coded Decimal Operations

Instruction	Operand Syntax	Operand Size	Operation
ABCD	Dn, Dn – (An), – (An)	8 8	$\text{Source}_{10} + \text{Destination}_{10} + X \Rightarrow \text{Destination}$
NBCD	⟨ea⟩	8 8	$0 - \text{Destination}_{10} - X \Rightarrow \text{Destination}$
SBCD	Dn, Dn – (An), – (An)	8 8	$\text{Destination}_{10} - \text{Source}_{10} - X \Rightarrow \text{Destination}$

5.3.3.8 PROGRAM CONTROL INSTRUCTIONS. A set of subroutine call and return instructions and conditional and unconditional branch instructions perform program control operations. Table 5-10 summarizes these instructions.

Table 5-10. Program Control Operations

Instruction	Operand Syntax	Operand Size	Operation
Conditional			
Bcc	⟨label⟩	8, 16, 32	If condition true, then PC + d ⇒ PC
DBcc	Dn, ⟨label⟩	16	If condition false, then Dn – 1 ⇒ PC; if Dn ≠ (– 1), then PC + d ⇒ PC
Scc	⟨ea⟩	8	If condition true, then destination bits are set to 1; else destination bits are cleared to 0
Unconditional			
BRA	⟨label⟩	8, 16, 32	PC + d ⇒ PC
BSR	⟨label⟩	8, 16, 32	SP – 4 ⇒ SP; PC ⇒ (SP); PC + d ⇒ PC
JMP	⟨ea⟩	none	Destination ⇒ PC
JSR	⟨ea⟩	none	SP – 4 ⇒ SP; PC ⇒ (SP); destination ⇒ PC
NOP	none	none	PC + 2 ⇒ PC
Returns			
RTD	#⟨d⟩	16	(SP) ⇒ PC; SP + 4 + d ⇒ SP
RTR	none	none	(SP) ⇒ CCR; SP + 2 ⇒ SP; (SP) ⇒ PC; SP + 4 ⇒ SP
RTS	none	none	(SP) ⇒ PC; SP + 4 ⇒ SP

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To specify conditions for change in program control, condition codes must be substituted for the letters "cc" in conditional program control opcodes. Condition test mnemonics are given below. Refer to **5.3.3.10 Condition Tests** for detailed information on condition codes.

CC	—	Carry clear	LS	—	Low or same
CS	—	Carry set	LT	—	Less than
EQ	—	Equal	MI	—	Minus
F	—	False*	NE	—	Not equal
GE	—	Greater or equal	PL	—	Plus
GT	—	Greater than	T	—	True
HI	—	High	VC	—	Overflow clear
LE	—	Less or equal	VS	—	Overflow set

*Not applicable to the Bcc instruction

5.3.3.9 SYSTEM CONTROL INSTRUCTIONS. Privileged instructions, trapping instructions, and instructions that use or modify the CCR provide system control operations. All of these instructions cause the processor to flush the instruction pipeline. Table 5-11 summarizes the instructions. The preceding list of condition tests also applies to the TRAPcc instruction. Refer to **5.3.3.10 Condition Tests** for detailed information on condition codes.

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Table 5-11. System Control Operations

Instruction	Operand Syntax	Operand Size	Operation
Privileged			
ANDI	#⟨data⟩, SR	16	Immediate Data Λ SR ⇒ SR
EORI	#⟨data⟩, SR	16	Immediate Data ⊕ SR ⇒ SR
MOVE	⟨ea⟩, SR SR, ⟨ea⟩	16 16	Source ⇒ SR SR ⇒ Destination
MOVEA	USP, An An, USP	32 32	USP ⇒ An An ⇒ USP
MOVEC	Rc, Rn Rn, Rc	32 32	Rc ⇒ Rn Rn ⇒ Rc
MOVES	Rn, ⟨ea⟩ ⟨ea⟩, Rn	8, 16, 32	Rn ⇒ Destination using DFC Source using SFC ⇒ Rn
ORI	#⟨data⟩, SR	16	Immediate Data V SR ⇒ SR
RESET	none	none	Assert $\overline{\text{RESET}}$ line
RTE	none	none	(SP) ⇒ SR; SP + 2 ⇒ SP; (SP) ⇒ PC; SP + 4 ⇒ SP; restore stack according to format
STOP	#⟨data⟩	16	Immediate Data ⇒ SR; STOP
LPSTOP	#⟨data⟩	none	Immediate Data ⇒ SR; interrupt mask ⇒ EBI; STOP
Trap Generating			
BKPT	#⟨data⟩	none	If breakpoint cycle acknowledged, then execute returned operation word, else trap as illegal instruction.
BGND	none	none	If background mode enabled, then enter background mode, else format/vector offset ⇒ – (SSP); PC ⇒ – (SSP); SR ⇒ – (SSP); (vector) ⇒ PC
CHK	⟨ea⟩, Dn	16, 32	If Dn < 0 or Dn < (ea), then CHK exception
CHK2	⟨ea⟩, Rn	8, 16, 32	If Rn < lower bound or Rn > upper bound, then CHK exception
ILLEGAL	none	none	SSP – 2 ⇒ SSP; vector offset ⇒ (SSP); SSP – 4 ⇒ SSP; PC ⇒ (SSP); SSP – 2 ⇒ SSP; SR ⇒ (SSP); llegal instruction vector address ⇒ PC
TRAP	#⟨data⟩	none	SSP – 2 ⇒ SSP; format/vector offset ⇒ (SSP); SSP – 4 ⇒ SSP; PC ⇒ (SSP); SR ⇒ (SSP); vector address ⇒ PC
TRAPcc	none #⟨data⟩	none 16, 32	If cc true, then TRAP exception
TRAPV	none	none	If V set, then overflow TRAP exception
Condition Code Register			
ANDI	#⟨data⟩, CCR	8	Immediate Data Λ CCR ⇒ CCR
EORI	#⟨data⟩, CCR	8	Immediate Data ⊕ CCR ⇒ CCR
MOVE	⟨ea⟩, CCR CCR, ⟨ea⟩	16 16	Source ⇒ CCR CCR ⇒ Destination
ORI	#⟨data⟩, CCR	8	Immediate Data V CCR ⇒ CCR

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5.3.3.10 CONDITION TESTS. Conditional program control instructions and the TRAPcc instruction execute on the basis of condition tests. A condition test is the evaluation of a logical expression related to the state of the CCR bits. If the result is 1, the condition is true. If the result is 0, the condition is false. For example, the T condition is always true, and the EQ condition is true only if the Z-bit condition code is true. Table 5-12 lists each condition test.

Table 5-12. Condition Tests

Mnemonic	Condition	Encoding	Test
T	True	0000	1
F*	False	0001	0
HI	High	0010	C • Z
LS	Low or Same	0011	C + Z
CC	Carry Clear	0100	C
CS	Carry Set	0101	C
NE	Not Equal	0110	Z
EQ	Equal	0111	Z
VC	Overflow Clear	1000	V
VS	Overflow Set	1001	V
PL	Plus	1010	N
MI	Minus	1011	N
GE	Greater or Equal	1100	N • V + N • V
LT	Less Than	1101	N • V + N • V
GT	Greater Than	1110	N • V • Z + N • V • Z
LE	Less or Equal	1111	Z + N • V + N • V

* Not available for the Bcc instruction.
• = Boolean AND
\+ = Boolean OR
N = Boolean NOT

5.3.4 Using the TBL Instructions

There are four TBL instructions. TBLS returns a signed, rounded byte, word, or long-word result. TBLSN returns a signed, unrounded byte, word, or long-word result. TBLU returns an unsigned, rounded byte, word, or long-word result. TBLUN returns an unsigned, unrounded byte, word, or long-word result. All four instructions support two types of interpolation data: an n-element table stored in memory and a two-element range stored in a pair of data registers. The latter form provides a means of performing surface (3D) interpolation between two previously calculated linear interpolations.

The following examples show how to compress tables and use fewer interpolation levels between table entries. Example 1 (see Figure 5-7) demonstrates TBL for a 257-entry table, allowing up to 256 interpolation levels between entries. Example 2 (see Figure 5-8) reduces table length for the same data to four entries. Example 3 (see Figure 5-9) demonstrates use of an 8-bit independent variable with an instruction.

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Two additional examples show how TBLSN can reduce cumulative error when multiple table lookup and interpolation operations are used in a calculation. Example 4 demonstrates addition of the results of three table interpolations. Example 5 illustrates use of TBLSN in surface interpolation.

5.3.4.1 TABLE EXAMPLE 1: STANDARD USAGE. The table consists of 257 word entries. As shown in Figure 5-7, the function is linear within the range 32768 ≤ X ≤ 49152. Table entries within this range are as given in Table 5-13 .

Table 5-13. Standard Usage Entries

Entry Number	X-Value	Y-Value
128*	32768	1311
162	41472	1659
163	41728	1669
164	41984	1679
165	42240	1690
192*	49152	1966

*These values are the end points of the range.
All entries between these points fall on the line.

Figure 5-7. Table Example 1

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The table instruction is executed with the following bit pattern in Dx:

31 … 16	15															0
NOT USED	1	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0

Table Entry Offset ⇒ Dx [8:15] = $A3 = 163

Interpolation Fraction ⇒ Dx [0:7] = $80 = 128

Using this information, the table instruction calculates dependent variable Y:

$$Y = 1669 + (128\ (1679 - 1669))\ /\ 256 = 1674$$

5.3.4.2 TABLE EXAMPLE 2: COMPRESSED TABLE. In Example 2 (see Figure 5-8), the data from Example 1 has been compressed by limiting the maximum value of the independent variable. Instead of the range $0 \leq X = 65535$, X is limited to $0 \leq X \leq 1023$. The table has been compressed to only five entries, but up to 256 levels of interpolation are allowed between entries.

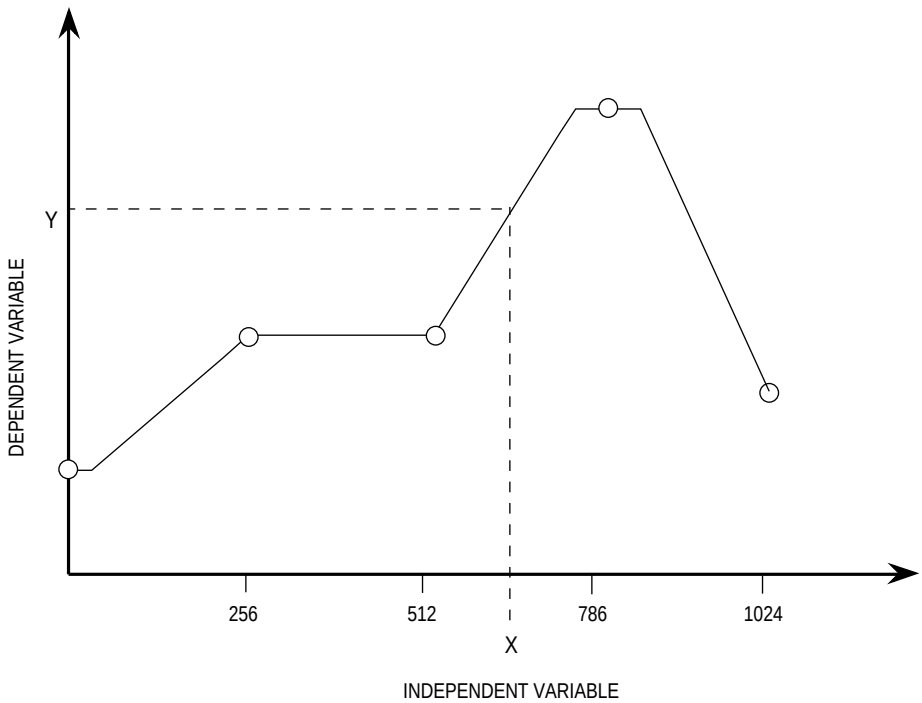

Figure 5-8. Table Example 2

NOTE

Extreme table compression with many levels of interpolation is possible only with highly linear functions. The table entries within the range of interest are listed in Table 5-14.

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Table 5-14. Compressed Table Entries

Entry Number	X-Value	Y-Value
2	512	1311
3	786	1966

Since the table is reduced from 257 to 5 entries, independent variable X must be scaled appropriately. In this case the scaling factor is 64, and the scaling is done by a single instruction:

LSR.W #6,Dx

Thus, Dx now contains the following bit pattern:

31 … 16	15															0
NOT USED	0	0	0	0	0	0	1	0	1	0	0	0	1	1	1	0

Table Entry Offset ⇒ Dx [8:15] = $02 = 2

Interpolation Fraction ⇒ Dx [0:7] = $8E = 142

Using this information, the table instruction calculates dependent variable Y:

$$Y = 1331 + (142\ (1966 - 1311))\ /\ 256 = 1674$$

The function chosen for Examples 1 and 2 is linear between data points. If another function had been used, interpolated values might not have been identical.

5.3.4.3 TABLE EXAMPLE 3: 8-BIT INDEPENDENT VARIABLE. This example shows how to use a table instruction within an interpolation subroutine. Independent variable X is calculated as an 8-bit value, allowing 16 levels of interpolation on a 17-entry table. X is passed to the subroutine, which returns an 8-bit result. The subroutine uses the data listed in Table 5-15, based on the function shown in Figure 5-9.

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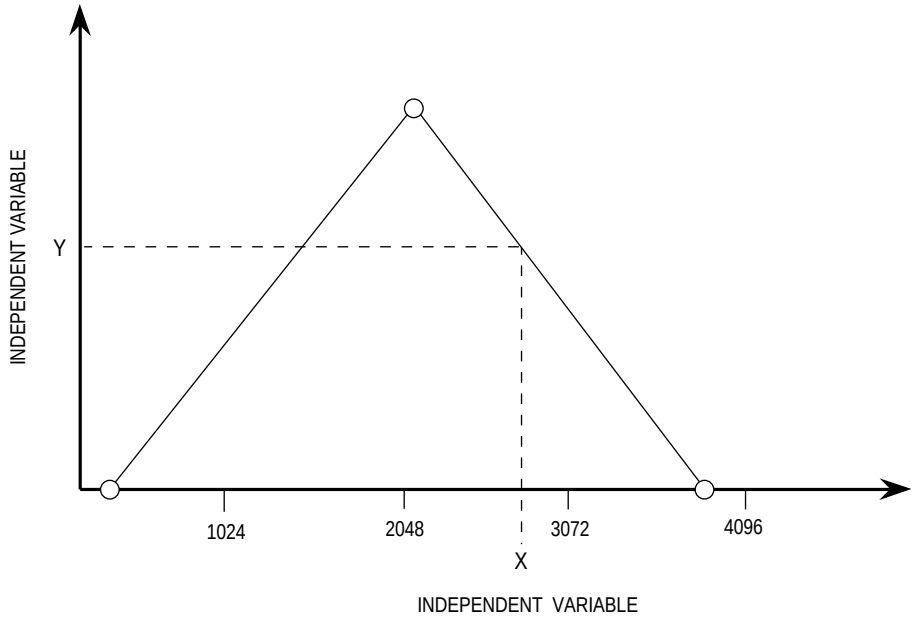

Figure 5-9. Table Example 3

Table 5-15. 8-Bit Independent Variable Entries

X (Subroutine)	X (Instruction)	Y
0	0	0
1	256	16
2	512	32
3	768	48
4	1024	64
5	1280	80
6	1536	96
7	1792	112
8	2048	128
9	2304	112
10	2560	96
11	2816	80
12	3072	64
13	3328	48
14	3584	32
15	3840	16
16	4096	0

The first column is the value passed to the subroutine, the second column is the value expected by the table instruction, and the third column is the result returned by the subroutine.

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The following value has been calculated for independent variable X:

31 … 16	15															0
NOT USED	0	0	0	0	0	0	0	0	1	0	1	1	1	1	0	1

Since X is an 8-bit value, the upper four bits are used as a table offset, and the lower four bits are used as an interpolation fraction. The following results are obtained from the subroutine:

$$\text{Table Entry Offset} \Rightarrow \text{Dx [4:7]} = \$B = 11$$

$$\text{Interpolation Fraction} \Rightarrow \text{Dx [0:3]} = \$D = 13$$

Thus, Y is calculated as follows:

$$Y = 80 + (13\ (64 - 80))\ /\ 16 = 67$$

If the 8-bit value for X were used directly by the table instruction, interpolation would be incorrectly performed between entries 0 and 1. Data must be shifted to the left four places before use:

LSL.W #4, Dx

The new range for X is $0 \leq X \leq 4096$; however, since a left shift fills the least significant digits of the word with zeros, the interpolation fraction can only have one of 16 values.

After the shift operation, Dx contains the following value:

31 … 16	15															0
NOT USED	0	0	0	0	1	0	1	1	1	1	0	1	0	0	0	0

Execution of the table instruction using the new value in Dx yields:

$$\text{Table Entry Offset} \Rightarrow \text{Dx [8:15]} = \$0B = 11$$

$$\text{Interpolation Fraction} \Rightarrow \text{Dx [0:7]} = \$D0 = 208$$

Thus, Y is calculated as follows:

$$Y = 80 + (208\ (64 - 80))\ /\ 256 = 67$$

5.3.4.4 TABLE EXAMPLE 4: MAINTAINING PRECISION. In this example, three TBL operations are performed and the results are summed. The calculation is done once with the result of each TBL rounded before addition and once with only the final result rounded. Assume that the result of the three interpolations are as follows (a "." indicates the binary radix point).

TBL # 1	0010 0000 . 0111 0000
TBL# 2	0011 1111 . 0111 0000
TBL # 3	0000 0001 . 0111 0000

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First, the results of each TBL are rounded with the TBLS round-to-nearest-even algorithm. The following values would be returned by TBLS:

TBL # 1	0010 0000 .
TBL # 2	0011 1111 .
TBL # 3	0000 0001 .

Summing, the following result is obtained:

```
0010 0000 .
0011 1111 .
0000 0001 .
0110 0000 .
```

Now, using the same TBL results, the sum is first calculated and then rounded according to the same algorithm:

```
0010 0000 . 0111 0000
0011 1111 . 0111 0000
0000 0001 . 0111 0000
0110 0001 . 0101 0000
```

Rounding yields:

```
0110 0001 .
```

The second result is preferred. The following code sequence illustrates how addition of a series of table interpolations can be performed without loss of precision in the intermediate results:

```
L0:
    TBLSN.B     ⟨ea⟩, Dx
    TBLSN.B     ⟨ea⟩, Dx
    TBLSN.B     ⟨ea⟩, Dl
    ADD.L       Dx, Dm      Long addition avoids problems with carry
    ADD.L       Dm, Dl
    ASR.L       #8, Dl      Move radix point
    BCC.B       L1          Fraction MSB in carry
    ADDQ.B      #1, Dl
L1: . . .
```


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5.3.4.5 Table Example 5: Surface Interpolations. The various forms of table can be used to perform surface (3D) TBLs. However, since the calculation must be split into a series of 2D TBLs, it is possible to lose precision in the intermediate results. The following code sequence, incorporating both TBLS and TBLSN, eliminates this possibility.

```
L0:
    MOVE.W      Dx, Dl          Copy entry number and fraction number
    TBLSN.B     ⟨ea⟩, Dx
    TBLSN.B     ⟨ea⟩, Dl
    TBLS.W      Dx:Dl, Dm       Surface interpolation, with round
    ASR.L       #8, Dm          Read just the result
    BCC.B       L1              No round necessary
    ADDQ.B      #1, Dl          Half round up
L1: . . .
```

Before execution of this code sequence, Dx must contain fraction and entry numbers for the two TBL, and Dm must contain the fraction for surface interpolation. The ⟨ea⟩ fields in the TBLSN instructions point to consecutive columns in a 3D table. The TBLS size parameter must be word if the TBLSN size parameter is byte, and must be long word if TBLSN is word. Increased size is necessary because a larger number of significant digits is needed to accommodate the scaled fractional results of the 2D TBL.

5.3.5 Nested Subroutine Calls

The LINK instruction pushes an address onto the stack, saves the stack address at which the address is stored, and reserves an area of the stack for use. Using this instruction in a series of subroutine calls will generate a linked list of stack frames.

The UNLK instruction removes a stack frame from the end of the list by loading an address into the SP and pulling the value at that address from the stack. When the instruction operand is the address of the link address at the bottom of a stack frame, the effect is to remove the stack frame from both the stack and the linked list.

5.3.6 Pipeline Synchronization with the NOP Instruction

Although the no operation (NOP) instruction performs no visible operation, it does force synchronization of the instruction pipeline, since all previous instructions must complete execution before the NOP begins.

5.4 PROCESSING STATES

This section describes the processing states of the CPU32. It includes a functional description of the bits in the supervisor portion of the SR and an overview of actions taken by the processor in response to exception conditions.

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5.4.1 State Transitions

The processor is always in one of four processing states: normal, background, exception, or halted.

When the processor fetches instructions and operands or executes instructions, it is in the normal processing state. The stopped condition, which the processor enters when a STOP or LPSTOP instruction is executed, is a variation of the normal state in which no further bus cycles are generated.

Background state is an alternate operational mode used for system debugging. Refer to **5.6 Development Support** for more information.

Exception processing refers specifically to the transition from normal processing of a program to normal processing of system routines, interrupt routines, and other exception handlers. Exception processing includes the stack operations, the exception vector fetch, and the filling of the instruction pipeline caused by an exception. Exception processing ends when execution of an exception handler routine begins. Refer to **5.5 Exception Processing** for comprehensive information.

A catastrophic system failure occurs if the processor detects a bus error or generates an address error while in the exception processing state. This type of failure halts the processor. For example, if a bus error occurs during exception processing caused by another bus error, the CPU32 assumes that the system is not operational and halts.

The halted condition should not be confused with the stopped condition. After the processor executes a STOP or LPSTOP instruction, execution of instructions can resume when a trace, interrupt, or reset exception occurs.

5.4.2 Privilege Levels

To protect system resources, the processor can operate with either of two levels of access—user or supervisor. Supervisor level is more privileged than user level. All instructions are available at the supervisor level, but execution of some instructions is not permitted at the user level. There are separate SPs for each level. The S-bit in the SR indicates privilege level and determines which SP is used for stack operations. The processor identifies each bus access (supervisor or user mode) via function codes to enforce supervisor and user access levels.

In a typical system, most programs execute at the user level. User programs can access only their own code and data areas and are restricted from accessing other information. The operating system executes at the supervisor privilege level, has access to all resources, performs the overhead tasks for the user level programs, and coordinates their activities.

5.4.2.1 SUPERVISOR PRIVILEGE LEVEL. If the S-bit in the SR is set, supervisor privilege level applies, and all instructions are executable. The bus cycles generated for instructions executed in supervisor level are normally classified as supervisor references, and the values of the function codes on FC2–FC0 refer to supervisor address spaces.

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All exception processing is performed at the supervisor level. All bus cycles generated during exception processing are supervisor references, and all stack accesses use the SSP.

Instructions that have important system effects can only be executed at supervisor level. For instance, user programs are not permitted to execute STOP, LPSTOP, or RESET instructions. To prevent a user program from gaining privileged access, except in a controlled manner, instructions that can alter the S-bit in the SR are privileged. The TRAP #n instruction provides controlled user access to operating system services.

5.4.2.2 USER PRIVILEGE LEVEL. If the S-bit in the SR is cleared, the processor executes instructions at the user privilege level. The bus cycles for an instruction executed at the user privilege level are classified as user references, and the values of the function codes on FC2–FC0 specify user address spaces. While the processor is at the user level, implicit references to the system SP and explicit references to address register seven (A7) refer to the USP.

5.4.2.3 CHANGING PRIVILEGE LEVEL. To change from user privilege level to supervisor privilege level, a condition that causes exception processing must occur. When exception processing begins, the current values in the SR, including the S-bit, are saved on the supervisor stack, and then the S-bit is set to enable supervisor access. Execution continues at supervisor privilege level until exception processing is complete.

To return to user access level, a system routine must execute one of the following instructions: MOVE to SR, ANDI to SR, EORI to SR, ORI to SR, or RTE. These instructions execute only at supervisor privilege level and can modify the S-bit of the SR. After these instructions execute, the instruction pipeline is flushed, then refilled from the appropriate address space.

The RTE instruction causes a return to a program that was executing when an exception occurred. When RTE is executed, the exception stack frame saved on the supervisor stack can be restored in either of two ways.

If the frame was generated by an interrupt, breakpoint, trap, or instruction exception, the SR and PC are restored to the values saved on the supervisor stack, and execution resumes at the restored PC address, with access level determined by the S-bit of the restored SR.

If the frame was generated by a bus error or an address error exception, the entire processor state is restored from the stack.

5.5 EXCEPTION PROCESSING

An exception is a special condition that pre-empts normal processing. Exception processing is the transition from normal mode program execution to execution of a routine that deals with an exception. The following paragraphs discuss system resources related to exception handling, exception processing sequence, and specific features of individual exception processing routines.

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5.5.1 Exception Vectors

An exception vector is the address of a routine that handles an exception. The VBR contains the base address of a 1024-byte exception vector table, which consists of 256 exception vectors. Sixty-four vectors are defined by the processor, and 192 vectors are reserved for user definition as interrupt vectors. Except for the reset vector, which is two long words, each vector in the table is one long word. Refer to Table 5-16 for information on vector assignment.

Table 5-16. Exception Vector Assignments

Vector Number	Vector Offset			Assignment
	Dec	Hex	Space	
0	0	000	SP	Reset: Initial Stack Pointer
1	4	004	SP	Reset: Initial Program Counter
2	8	008	SD	Bus Error
3	12	00C	SD	Address Error
4	16	010	SD	Illegal Instruction
5	20	014	SD	Zero Division
6	24	018	SD	CHK, CHK2 Instructions
7	28	01C	SD	TRAPcc, TRAPV Instructions
8	32	020	SD	Privilege Violation
9	36	024	SD	Trace
10	40	028	SD	Line 1010 Emulator
11	44	02C	SD	Line 1111 Emulator
12	48	030	SD	Hardware Breakpoint
13	52	034	SD	(Reserved for Coprocessor Protocol Violation)
14	56	038	SD	Format Error
15	60	03C	SD	Uninitialized Interrupt
16–23	64 92	040 05C	SD	(Unassigned, Reserved) —
24	96	060	SD	Spurious Interrupt
25	100	064	SD	Level 1 Interrupt Autovector
26	104	068	SD	Level 2 Interrupt Autovector
27	108	06C	SD	Level 3 Interrupt Autovector
28	112	070	SD	Level 4 Interrupt Autovector
29	116	074	SD	Level 5 Interrupt Autovector
30	120	078	SD	Level 6 Interrupt Autovector
31	124	07C	SD	Level 7 Interrupt Autovector
32–47	128 188	080 0BC	SD	Trap Instruction Vectors (0–15) —
48–58	192 232	0C0 0E8	SD	(Reserved for Coprocessor) —
59–63	236 252	0EC 0FC	SD	(Unassigned, Reserved) —
64–255	256 1020	100 3FC	SD	User-Defined Vectors (192)

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CAUTION

Because there is no protection on the 64 processor-defined vectors, external devices can access vectors reserved for internal purposes. This practice is strongly discouraged.

All exception vectors, except the reset vector, are located in supervisor data space. The reset vector is located in supervisor program space. Only the initial reset vector is fixed in the processor memory map. When initialization is complete, there are no fixed assignments. Since the VBR stores the vector table base address, the table can be located anywhere in memory. It can also be dynamically relocated for each task executed by an operating system.

Each vector is assigned an 8-bit number. Vector numbers for some exceptions are obtained from an external device; others are supplied by the processor. The processor multiplies the vector number by 4 to calculate vector offset, then adds the offset to the contents of the VBR. The sum is the memory address of the vector.

5.5.1.1 TYPES OF EXCEPTIONS. An exception can be caused by internal or external events.

An internal exception can be generated by an instruction or by an error. The TRAP, TRAPcc, TRAPV, BKPT, CHK, CHK2, RTE, and DIV instructions can cause exceptions during normal execution. Illegal instructions, instruction fetches from odd addresses, word or long-word operand accesses from odd addresses, and privilege violations also cause internal exceptions.

Sources of external exception include interrupts, breakpoints, bus errors, and reset requests. Interrupts are peripheral device requests for processor action. Breakpoints are used to support development equipment. Bus error and reset are used for access control and processor restart.

5.5.1.2 EXCEPTION PROCESSING SEQUENCE. For all exceptions other than a reset exception, exception processing occurs in the following sequence. Refer to **5.5.2.1 Reset** for details of reset processing.

As exception processing begins, the processor makes an internal copy of the SR. After the copy is made, the processor state bits in the SR are changed—the S-bit is set, establishing supervisor access level, and bits T1 and T0 are cleared, disabling tracing. For reset and interrupt exceptions, the interrupt priority mask is also updated.

Next, the exception number is obtained. For interrupts, the number is fetched from CPU space $F (the bus cycle is an interrupt acknowledge). For all other exceptions, internal logic provides a vector number.

Next, current processor status is saved. An exception stack frame is created and placed on the supervisor stack. All stack frames contain copies of the SR and the PC for use by RTE. The type of exception and the context in which the exception occurs determine what other information is stored in the stack frame.

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Finally, the processor prepares to resume normal execution of instructions. The exception vector offset is determined by multiplying the vector number by 4, and the offset is added to the contents of the VBR to determine displacement into the exception vector table. The exception vector is loaded into the PC. If no other exception is pending, the processor will resume normal execution at the new address in the PC.

5.5.1.3 EXCEPTION STACK FRAME. During exception processing, the most volatile portion of the current context is saved on the top of the supervisor stack. This context is organized in a format called the exception stack frame.

The exception stack frame always includes the contents of SR and PC at the time the exception occurred. To support generic handlers, the processor also places the vector offset in the exception stack frame and marks the frame with a format code. The format field allows an RTE instruction to identify stack information so that it can be properly restored.

The general form of the exception stack frame is illustrated in Figure 5-10. Although some formats are peculiar to a particular M68000 Family processor, format 0000 is always legal and always indicates that only the first four words of a frame are present. See **5.5.4 CPU32 Stack Frames** for a complete discussion of exception stack frames.

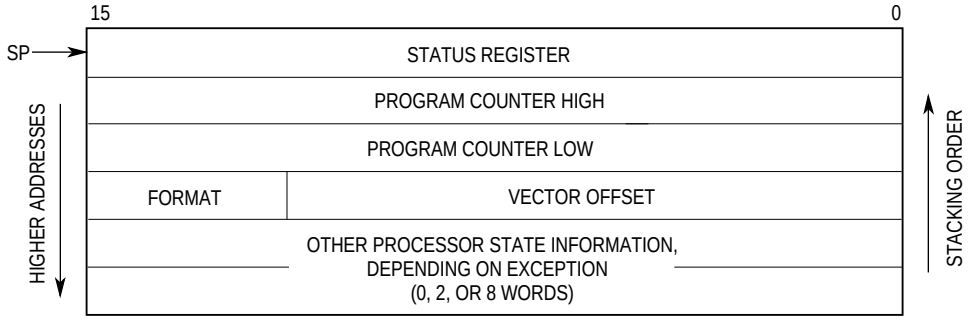

Figure 5-10. Exception Stack Frame

5.5.1.4 MULTIPLE EXCEPTIONS. Each exception has been assigned a priority based on its relative importance to system operation. Priority assignments are shown in Table 5-17. Group 0 exceptions have the highest priorities; group 4 exceptions have the lowest priorities. Exception processing for exceptions that occur simultaneously is done by priority, from highest to lowest.

It is important to be aware of the difference between exception processing mode and execution of an exception handler. Each exception has an assigned vector that points to an associated handler routine. Exception processing includes steps described in **5.5.1.2 Exception Processing Sequence**, but does not include execution of handler routines, which is done in normal mode.

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When the CPU32 completes exception processing, it is ready to begin either exception processing for a pending exception or execution of a handler routine. Priority assignment governs the order in which exception processing occurs, not the order in which exception handlers are executed.

Table 5-17. Exception Priority Groups

Group/ Priority	Exception and Relative Priority	Characteristics
0	Reset	Aborts all processing (instruction or exception); does not save old context.
1.1 1.2	Address Error Bus Error	Suspends processing (instruction or exception); saves internal context.
2	BKPT#n, CHK, CHK2, Division by Zero, RTE, TRAP#n, TRAPcc, TRAPV	Exception processing is a part of instruction execution.
3	Illegal Instruction, Line A, Unimplemented Line F, Privilege Violation	Exception processing begins before instruction execution.
4.1 4.2 4.3	Trace Hardware Breakpoint Interrupt	Exception processing begins when current instruction or previous exception processing is complete.

As a general rule, when simultaneous exceptions occur, the handler routines for lower priority exceptions are executed before the handler routines for higher priority exceptions. For example, consider the arrival of an interrupt during execution of a TRAP instruction while tracing is enabled. Trap exception processing (2) is done first, followed immediately by exception processing for the trace (4.1), and then by exception processing for the interrupt (4.3). Each exception places a new context on the stack. When the processor resumes normal instruction execution, it is vectored to the interrupt handler, which returns to the trace handler that returns to the trap handler.

There are special cases to which the general rule does not apply. The reset exception will always be the first exception handled since reset clears all other exceptions. It is also possible for high-priority exception processing to begin before low-priority exception processing is complete. For example, if a bus error occurs during trace exception processing, the bus error will be processed and handled before trace exception processing has completed.

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5.5.2 Processing of Specific Exceptions

The following paragraphs provide details concerning sources of specific exceptions, how each arises, and how each is processed.

5.5.2.1 RESET. Assertion of $\overline{\text{RESET}}$ by external hardware or assertion of the internal $\overline{\text{RESET}}$ signal by an internal module causes a reset exception. The reset exception has the highest priority of any exception. Reset is used for system initialization and for recovery from catastrophic failure. When the reset exception is recognized, it aborts any processing in progress, and that processing cannot be recovered. Reset performs the following operations:

1. Clears T0 and T1 in the SR to disable tracing
2. Sets the S-bit in the SR to establish supervisor privilege
3. Sets the interrupt priority mask to the highest priority level (%111)
4. Initializes the VBR to zero ($00000000)
5. Generates a vector number to reference the reset exception vector
6. Loads the first long word of the vector into the interrupt SP
7. Loads the second long word of the vector into the PC
8. Fetches and initiates decode of the first instruction to be executed

Figure 5-11 is a flowchart of the reset exception

After initial instruction prefetches, normal program execution begins at the address in the PC. The reset exception does not save the value of either the PC or the SR.

If a bus error or address error occurs during reset exception processing, a double bus fault occurs, the processor halts, and the $\overline{\text{HALT}}$ signal is asserted to indicate the halted condition.

Execution of the RESET instruction does not cause a reset exception nor does it affect any internal CPU register. The SIM40 registers and the module control register in each internal peripheral module (DMA, timers, and serial modules) are not affected. All other internal peripheral module registers are reset the same as for a hardware reset. The external devices connected to the $\overline{\text{RESET}}$ signal are reset at the completion of the RESET instruction.

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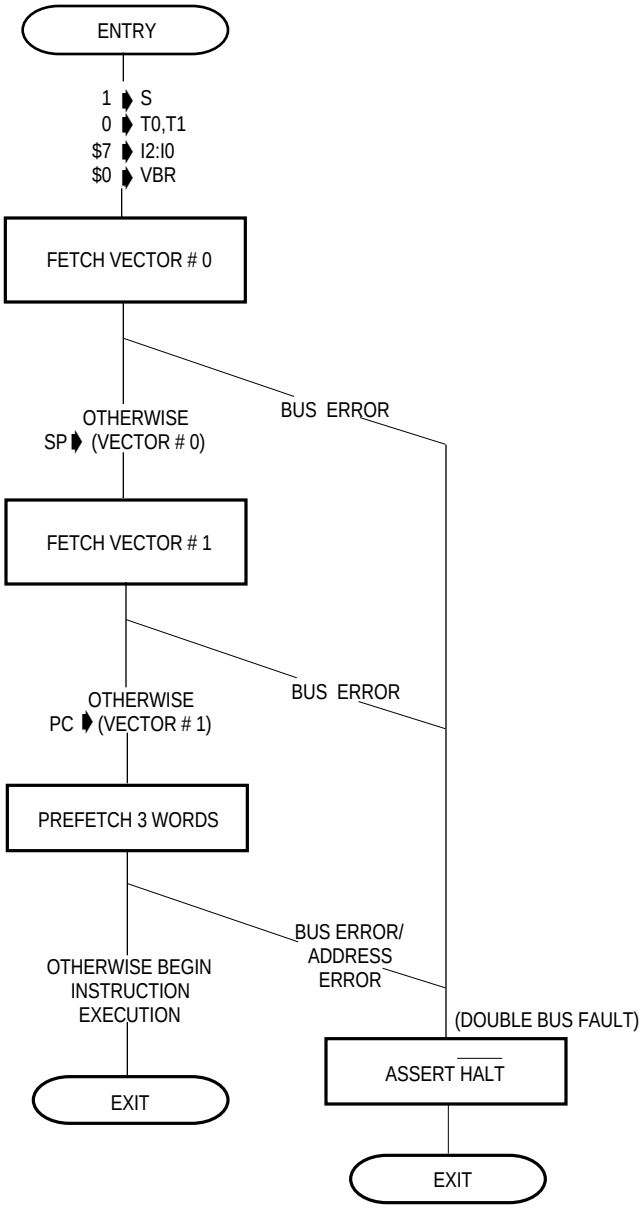

Figure 5-11. Reset Operation Flowchart

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5.5.2.2 BUS ERROR. A bus error exception occurs when an assertion of the BERR signal is acknowledged. The $\overline{\text{BERR}}$ signal can be asserted by one of three sources:

1. External logic by assertion of the $\overline{\text{BERR}}$ input pin
2. Direct assertion of the internal $\overline{\text{BERR}}$ signal by an internal module
3. Direct assertion of the internal $\overline{\text{BERR}}$ signal by the on-chip hardware watchdog after detecting a no-response condition

Bus error exception processing begins when the processor attempts to use information from an aborted bus cycle.

When the aborted bus cycle is an instruction prefetch, the processor will not initiate exception processing unless the prefetched information is used. For example, if a branch instruction flushes an aborted prefetch, that word is not accessed, and no exception occurs.

When the aborted bus cycle is a data access, the processor initiates exception processing immediately, except in the case of released operand writes. Released write bus errors are delayed until the next instruction boundary or until another operand access is attempted.

Exception processing for bus error exceptions follows the regular sequence, but context preservation is more involved than for other exceptions because a bus exception can be initiated while an instruction is executing. Several bus error stack format organizations are utilized to provide additional information regarding the nature of the fault.

First, any register altered by a faulted-instruction EA calculation is restored to its initial value. Then a special status word (SSW) is placed on the stack. The SSW contains specific information about the aborted access—size, type of access (read or write), bus cycle type, and function code. Finally, fault address, bus error exception vector number, PC value, and a copy of the SR are saved.

If a bus error occurs during exception processing for a bus error, an address error, a reset, or while the processor is loading stack information during RTE execution, the processor halts. This simplifies isolation of catastrophic system failure by preventing processor interaction with stacks and memory. Only assertion of $\overline{\text{RESET}}$ can restart a halted processor.

5.5.2.3 ADDRESS ERROR. Address error exceptions occur when the processor attempts to access an instruction, word operand, or long-word operand at an odd address. The effect is much the same as an internally generated bus error. The exception processing sequence is the same as that for bus error, except that the vector number refers to the address error exception vector.

Address error exception processing begins when the processor attempts to use information from the aborted bus cycle. If the aborted cycle is a data space access, exception processing begins when the processor attempts to use the data, except in the

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case of a released operand write. Released write exceptions are delayed until the next instruction boundary or attempted operand access.

An address exception on a branch to an odd address is delayed until the PC is changed. No exception occurs if the branch is not taken. In this case, the fault address and return PC value placed in the exception stack frame are the odd address, and the current instruction PC points to the instruction that caused the exception.

If an address error occurs during exception processing for a bus error, another address error, or a reset, the processor halts.

5.5.2.4 INSTRUCTION TRAPS. Traps are exceptions caused by instructions. They arise from either processor recognition of abnormal conditions during instruction execution or from use of specific trapping instructions. Traps are generally used to handle abnormal conditions that arise in control routines.

The TRAP instruction, which always forces an exception, is useful for implementing system calls for user programs. The TRAPcc, TRAPV, CHK, and CHK2 instructions force exceptions when a program detects a run-time error. The DIVS and DIVU instructions force an exception if a division operation is attempted with a divisor of zero.

Exception processing for traps follows the regular sequence. If tracing is enabled when an instruction that causes a trap begins execution, a trace exception will be generated by the instruction, but the trap handler routine will not be traced. (The trap exception will be processed first, then the trace exception.)

The vector number for the TRAP instruction is internally generated—part of the number comes from the instruction itself. The trap vector number, PC value, and a copy of the SR are saved on the supervisor stack. The saved PC value is the address of the instruction that follows the instruction that generated the trap. For all instruction traps other than TRAP, a pointer to the instruction causing the trap is also saved in the fifth and sixth words of the exception stack frame.

5.5.2.5 SOFTWARE BREAKPOINTS. To support hardware emulation, the CPU32 must provide a means of inserting breakpoints into target code and of announcing when a breakpoint is reached.

The MC68000 and MC68008 can detect an illegal instruction inserted at a breakpoint when the processor fetches from the illegal instruction exception vector location. Since the VBR on the CPU32 allows relocation of exception vectors, the exception vector address is not a reliable indication of a breakpoint. CPU32 breakpoint support is provided by extending the function of a set of illegal instructions ($4848–$484F).

When a breakpoint instruction is executed, the CPU32 performs a read from CPU space $0, at a location corresponding to the breakpoint number. If this bus cycle is terminated by $\overline{\text{BERR}}$, the processor performs illegal instruction exception processing. If the bus cycle is terminated by $\overline{\text{DSACKx}}$, the processor uses the data returned to replace the breakpoint in the instruction pipeline and begins execution of that instruction. See **Section 3 Bus Operation** for a description of CPU space operations.

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5.5.2.6 HARDWARE BREAKPOINTS. The CPU32 recognizes hardware breakpoint requests. Hardware breakpoint requests do not force immediate exception processing, but are left pending. An instruction breakpoint is not made pending until the instruction corresponding to the request is executed.

A pending breakpoint can be acknowledged between instructions or at the end of exception processing. To acknowledge a breakpoint, the CPU performs a read from CPU space $0 at location $1E (see **Section 3 Bus Operation)**.

If the bus cycle terminates normally, instruction execution continues with the next instruction as if no breakpoint request occurred. If the bus cycle is terminated by $\overline{\text{BERR}}$, the CPU begins exception processing. Data returned during this bus cycle is ignored.

Exception processing follows the regular sequence. Vector number 12 (offset $30) is internally generated. The PC of the executing instruction, the PC of the next instruction to be executed, and a copy of the SR are saved on the supervisor stack.

5.5.2.7 FORMAT ERROR. The processor checks certain data values for control operations. The validity of the stack format code and, in the case of a bus cycle fault format, the version number of the processor that generated the frame are checked during execution of the RTE instruction. This check ensures that the program does not make erroneous assumptions about information in the stack frame.

If the format of the control data is improper, the processor generates a format error exception. This exception saves a four-word format exception frame and then vectors through vector table entry number 14. The stacked PC is the address of the RTE instruction that discovered the format error.

5.5.2.8 ILLEGAL OR UNIMPLEMENTED INSTRUCTIONS. An instruction is illegal if it contains a word bit pattern that does not correspond to the bit pattern of the first word of a legal CPU32 instruction, if it is a MOVEC instruction that contains an undefined register specification field in the first extension word, or if it contains an indexed addressing mode extension word with bits 5–4 = 00 or bits 3–0 ≠ 0000.

If an illegal instruction is fetched during instruction execution, an illegal instruction exception occurs. This facility allows the operating system to detect program errors or to emulate instructions in software.

Word patterns with bits 15–12 = 1010 (referred to as A-line opcodes) are unimplemented instructions. A separate exception vector (vector 10, offset $28) is given to unimplemented instructions to permit efficient emulation.

Word patterns with bits 15–12 = 1111 (referred to as F-line opcodes) are used for M68000 family instruction set extensions. They can generate an unimplemented instruction exception caused by the first extension word of the instruction or by the addressing mode extension word. A separate F-line emulation vector (vector 11, offset $2C) is used for the exception vector.

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All unimplemented instructions are reserved for use by Motorola for enhancements and extensions to the basic M68000 architecture. Opcode pattern $4AFC is defined to be illegal on all M68000 family members. Those customers requiring the use of an unimplemented opcode for synthesis of "custom instructions," operating system calls, etc., should use this opcode.

Exception processing for illegal and unimplemented instructions is similar to that for traps. The instruction is fetched and decoding is attempted. When the processor determines that execution of an illegal instruction is being attempted, exception processing begins. No registers are altered.

Exception processing follows the regular sequence. The vector number is generated to refer to the illegal instruction vector or in the case of an unimplemented instruction, to the corresponding emulation vector. The illegal instruction vector number, current PC, and a copy of the SR are saved on the supervisor stack, with the saved value of the PC being the address of the illegal or unimplemented instruction.

5.5.2.9 PRIVILEGE VIOLATIONS. To provide system security, certain instructions can be executed only at the supervisor access level. An attempt to execute one of these instructions at the user level will cause an exception. The privileged exceptions are as follows:

- AND Immediate to SR
- EOR Immediate to SR
- LPSTOP
- MOVE from SR
- MOVE to SR
- MOVE USP
- MOVEC
- MOVES
- OR Immediate to SR
- RESET
- RTE
- STOP

Exception processing for privilege violations is nearly identical to that for illegal instructions. The instruction is fetched and decoded. If the processor determines that a privilege violation has occurred, exception processing begins before instruction execution.

Exception processing follows the regular sequence. The vector number (8) is generated to reference the privilege violation vector. Privilege violation vector offset, current PC, and SR are saved on the supervisor stack. The saved PC value is the address of the first word of the instruction causing the privilege violation.

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5.5.2.10 TRACING. To aid in program development, M68000 processors include a facility to allow tracing of instruction execution. CPU32 tracing also has the ability to trap on changes in program flow. In trace mode, a trace exception is generated after each instruction executes, allowing a debugging program to monitor the execution of a program under test. The T1 and T0 bits in the supervisor portion of the SR are used to control tracing.

When T1–T0 = 00, tracing is disabled, and instruction execution proceeds normally (see Table 5-18).

Table 5-18. Tracing Control

T1	T0	Tracing Function
0	0	No tracing
0	1	Trace on change of flow
1	0	Trace on instruction execution
1	1	Undefined; reserved

When T1–T0 = 01 at the beginning of instruction execution, a trace exception will be generated if the PC changes sequence during execution. All branches, jumps, subroutine calls, returns, and SR manipulations can be traced in this way. No exception occurs if a branch is not taken.

When T1–T0 = 10 at the beginning of instruction execution, a trace exception will be generated when execution is complete. If the instruction is not executed, either because an interrupt is taken or because the instruction is illegal, unimplemented, or privileged, an exception is not generated.

At the present time, T1–T0 = 11 is an undefined condition. It is reserved by Motorola for future use.

Exception processing for trace starts at the end of normal processing for the traced instruction and before the start of the next instruction. Exception processing follows the regular sequence; tracing is disabled so that the trace exception itself is not traced. A vector number is generated to reference the trace exception vector. The address of the instruction that caused the trace exception, the trace exception vector offset, the current PC, and a copy of the SR are saved on the supervisor stack. The saved value of the PC is the address of the next instruction to be executed.

A trace exception can be viewed as an extension to the function of any instruction. If a trace exception is generated by an instruction, the execution of that instruction is not complete until the trace exception processing associated with it is also complete.

If an instruction is aborted by a bus error or address error exception, trace exception processing is deferred until the suspended instruction is restarted and completed normally. An RTE from a bus error or address error will not be traced because of the possibility of continuing the instruction from the fault.

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If an instruction is executed and an interrupt is pending on completion, the trace exception is processed before the interrupt exception.

If an instruction forces an exception, the forced exception is processed before the trace exception.

If an instruction is executed and a breakpoint is pending upon completion of the instruction, the trace exception is processed before the breakpoint.

If an attempt is made to execute an illegal, unimplemented, or privileged instruction while tracing is enabled, no trace exception will occur because the instruction is not executed. This is particularly important to an emulation routine that performs an instruction function, adjusts the stacked PC to beyond the unimplemented instruction, and then returns. The SR on the stack must be checked to determine if tracing is on before the return is executed. If tracing is on, trace exception processing must be emulated so that the trace exception handler can account for the emulated instruction.

Tracing also affects normal operation of the STOP and LPSTOP instructions. If either instruction begins execution with T1 set, a trace exception will be taken after the instruction loads the SR. Upon return from the trace handler routine, execution will continue with the instruction following STOP (LPSTOP), and the processor will not enter the stopped condition.

5.5.2.11 INTERRUPTS. There are seven levels of interrupt priority and 192 assignable interrupt vectors within each exception vector table. Careful use of multiple vector tables and hardware chaining will permit a virtually unlimited number of peripherals to interrupt the processor.

Interrupt recognition and subsequent processing are based on internal interrupt request signals ($\overline{IRQ7}$–$\overline{IRQ1}$) and the current priority set in SR priority mask I2–I0. Interrupt request level 0 ($\overline{IRQ7}$–$\overline{IRQ1}$ negated) indicates that no service is requested. When an interrupt of level 1 through 6 is requested via $\overline{IRQ6}$–$\overline{IRQ1}$, the processor compares the request level with the interrupt mask to determine whether the interrupt should be processed. Interrupt requests are inhibited for all priority levels less than or equal to the current priority. Level 7 interrupts are nonmaskable.

$\overline{IRQ7}$–$\overline{IRQ1}$ are synchronized and debounced by input circuitry on consecutive rising edges of the processor clock. To be valid, an interrupt request must be held constant for at least two consecutive clock periods.

Interrupt requests do not force immediate exception processing, but are left pending. A pending interrupt is detected between instructions or at the end of exception processing—all interrupt requests must be held asserted until they are acknowledged by the CPU. If the priority of the interrupt is greater than the current priority level, exception processing begins.

Exception processing occurs as follows. First, the processor makes an internal copy of the SR. After the copy is made, the processor state bits in the SR are changed—the S-bit is set, establishing supervisor access level, and bits T1 and T0 are cleared, disabling

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tracing. Priority level is then set to the level of the interrupt, and the processor fetches a vector number from the interrupting device (CPU space $F). The fetch bus cycle is classified as an interrupt acknowledge, and the encoded level number of the interrupt is placed on the address bus.

If an interrupting device requests automatic vectoring, the processor generates a vector number (25 to 31) determined by the interrupt level number.

If the response to the interrupt acknowledge bus cycle is a bus error, the interrupt is taken to be spurious, and the spurious interrupt vector number (24) is generated.

The exception vector number, PC, and SR are saved on the supervisor stack. The saved value of the PC is the address of the instruction that would have executed if the interrupt had not occurred.

Priority level 7 interrupt is a special case. Level 7 interrupts are nonmaskable interrupts (NMI). Level 7 requests are transition sensitive to eliminate redundant servicing and resultant stack overflow. Transition sensitive means that the level 7 input must change state before the CPU will detect an interrupt.

An NMI is generated each time the interrupt request level changes to level 7 (regardless of priority mask value), and each time the priority mask changes from 7 to a lower number while the request level remains at 7.

Many M68000 peripherals provide for programmable interrupt vector numbers to be used in the system interrupt request/acknowledge mechanism. If the vector number is not initialized after reset and if the peripheral must acknowledge an interrupt request, the peripheral should return the uninitialized interrupt vector number (15).

See **Section 3 Bus Operation** for detailed information on interrupt acknowledge cycles.

5.5.2.12 RETURN FROM EXCEPTION. When exception stacking operations for all pending exceptions are complete, the processor begins execution of the handler for the last exception processed. After the exception handler has executed, the processor must restore the system context in existence prior to the exception. The RTE instruction is designed to accomplish this task.

When RTE is executed, the processor examines the stack frame on top of the supervisor stack to determine if it is valid and determines what type of context restoration must be performed. See **5.5.4 CPU32 Stack Frames** for a description of stack frames.

For a normal four-word frame, the processor updates the SR and PC with data pulled from the stack, increments the SSP by 8, and resumes normal instruction execution. For a six-word frame, the SR and PC are updated from the stack, the active SSP is incremented by 12, and normal instruction execution resumes.

For a bus fault frame, the format value on the stack is first checked for validity. In addition, the version number on the stack must match the version number of the processor that is

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attempting to read the stack frame. The version number is located in the most significant byte (bits 15–8) of the internal register word at location SP + $14 in the stack frame. The validity check ensures that stack frame data will be properly interpreted in multiprocessor systems.

If a frame is invalid, a format error exception is taken. If it is inaccessible, a bus error exception is taken. Otherwise, the processor reads the entire frame into the proper internal registers, de-allocates the stack (12 words), and resumes normal processing. Bus error frames for faults during exception processing require the RTE instruction to rewrite the faulted stack frame. If an error occurs during any of the bus cycles required by rewrite, the processor halts.

If a format error occurs during RTE execution, the processor creates a normal four-word fault stack frame below the frame that it was attempting to use. If a bus error occurs, a bus-error stack frame will be created. The faulty stack frame remains intact, so that it may be examined and repaired by an exception handler or used by a different type of processor (e.g., MC68010, MC68020, or future M68000 processor) in a multiprocessor system.

5.5.3 Fault Recovery

There are four phases of recovery from a fault: recognizing the fault, saving the processor state, repairing the fault (if possible), and restoring the processor state. Saving and restoring the processor state are described in the following paragraphs.

The stack contents are identified by the special status word (SSW). In addition to identifying the fault type represented by the stack frame, the SSW contains the internal processor state corresponding to the fault.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TP	MV	0	TR	B1	B0	RR	RM	IN	RW	LG	SIZ		FUNC		

TP—BERR Frame Type

The TP field defines the class of the faulted bus operation. Two bus error exception frame types are defined. One is for faults on prefetch and operand accesses, and the other is for faults during exception frame stacking.

0 = Operand or prefetch bus fault
1 = Exception processing bus fault

MV—MOVEM in Progress

MV is set when the operand transfer portion of the MOVEM instruction is in progress at the time of a bus fault. If a prefetch bus fault occurs while prefetching the MOVEM opcode and extension word, both the MV and IN bits will be set.

0 = MOVEM was not in progress when fault occurred
1 = MOVEM was in progress when fault occurred

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TR—Trace Pending

TR indicates that a trace exception was pending when a bus error exception was processed. The instruction that generated the trace will not be restarted upon return from the exception handler. This includes MOVEM and released write bus errors indicated by the assertion of either MV or RR in the SSW.

0 = Trace not pending
1 = Trace pending

B1—Breakpoint Channel 1 Pending

B1 indicates that a breakpoint exception was pending on channel 1 (external breakpoint source) when a bus error exception was processed. Pending breakpoint status is stacked, regardless of the type of bus error exception.

0 = Breakpoint not pending
1 = Breakpoint pending

B0—Breakpoint Channel 0 Pending

B0 indicates that a breakpoint exception was pending on channel 0 (internal breakpoint source) when the bus error exception was processed. Pending breakpoint status is stacked, regardless of the type of bus error exception.

0 = Breakpoint not pending
1 = Breakpoint pending

RR—Rerun Write Cycle after RTE

RR will be set if the faulted bus cycle was a released write. A released write is one that is overlapped. If the write is completed (rerun) in the exception handler, the RR bit should be cleared before executing RTE. The bus cycle will be rerun if the RR bit is set upon return from the exception handler.

0 = Faulted cycle was read, RMW, or unreleased write
1 = Faulted cycle was a released write

RM—Faulted Cycle Was Read-Modify-Write

Faulted RMW bus cycles set the RM bit. RM is ignored during unstacking.

0 = Faulted cycle was non-RMW cycle
1 = Faulted cycle was either the read or write of an RMW cycle

IN—Instruction/Other

Instruction prefetch faults are distinguished from operand (both read and write) faults by the IN bit. If IN is cleared, the error was on an operand cycle; if IN is set, the error was on an instruction prefetch. IN is ignored during unstacking.

0 = Operand
1 = Prefetch

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RW—Read/Write of Faulted Bus Cycle

Read and write bus cycles are distinguished by the RW bit. Read bus cycles will set this bit, and write bus cycles will clear it. RW is reloaded into the bus controller if the RR bit is set during unstacking.

0 = Faulted cycle was an operand write
1 = Faulted cycle was a prefetch or operand read

SIZ—Remaining Size of Faulted Bus Cycle

The SIZ field shows operand size remaining when a fault was detected. This field does not indicate the initial size of the operand, nor does it necessarily indicate the proper status of a dynamically sized bus cycle. Dynamic sizing occurs on the external bus and is transparent to the CPU. Byte size is shown only when the original operand was a byte. The field is reloaded into the bus controller if the RR bit is set during unstacking. The SIZ field is encoded as follows:

00 = Long word
01 = Byte
10 = Word
11 = Unused, reserved

FUNC—Function Code of Faulted Bus Cycle

The function code for the faulted cycle is stacked in the FUNC field of the SSW, which is a copy of FC2–FC0 for the faulted bus cycle. This field is reloaded into the bus controller if the RR bit is set during unstacking. All unused bits are stacked as zeros and are ignored during unstacking. Further discussion of the SSW is included in **5.5.3.1 Types of Faults**.

5.5.3.1 TYPES OF FAULTS. An efficient implementation of instruction restart dictates that faults on some bus cycles be treated differently than faults on other bus cycles. The CPU32 defines four fault types: released write faults, faults during exception processing, faults during MOVEM operand transfer, and faults on any other bus cycle.

5.5.3.1.1 Type I—Released Write Faults. CPU32 instruction pipelining can cause a final instruction write to overlap the execution of a following instruction. A write that is overlapped is called a released write. A released write fault occurs when a bus error or some other fault occurs on the released write.

Released write faults are taken at the next instruction boundary. The stacked PC is that of the next unexecuted instruction. If a subsequent instruction attempts an operand access while a released write fault is pending, the instruction is aborted and the write fault is acknowledged. This action prevents the instruction from using stale data.

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The SSW for a released write fault contains the following bit pattern:

15	14	13	12	11	10	9	8	7	6	5	4 3	2 0
0	0	0	TR	B1	B0	1	0	0	0	LG	SIZ	FUNC

TR, B1, and B0 are set if the corresponding exception is pending when the bus error exception is taken. Status regarding the faulted bus cycle is reflected in the LG, SIZ, and FUNC fields.

The remainder of the stack contains the PC of the next unexecuted instruction, the current SR, the address of the faulted memory location, and the contents of the data buffer that was to be written to memory. This data is written on the stack in the format depicted in Figure 5-15. When a released write fault exception handler executes, the machine will complete the faulted write and then continue executing instructions wherever the PC indicates.

5.5.3.1.2 Type II—Prefetch, Operand, RMW, and MOVEP Faults. The majority of bus error exceptions are included in this category—all instruction prefetches, all operand reads, all RMW cycles, and all operand accesses resulting from execution of MOVEP (except the last write of a MOVEP Rn,⟨ea⟩ or the last write of MOVEM, which are type I faults). The TAS, MOVEP, and MOVEM instructions account for all operand writes not considered released write faults.

All type II faults cause an immediate exception that aborts the current instruction. Any registers that were altered as the result of an EA calculation (i.e., postincrement or predecrement) are restored prior to processing the bus cycle fault.

The SSW for faults in this category contains the following bit pattern:

15	14	13	12	11	10	9	8	7	6	5	4 3	2 0
0	0	0	0	B1	B0	0	RM	IN	RW	LG	SIZ	FUNC

The trace pending bit is always cleared, since the instruction will be restarted upon return from the handler. Saving a pending exception on the stack causes a trace exception to be taken prior to restarting the instruction. If the exception handler does not alter the stacked SR trace bits, the trace is requeued when the instruction is started.

The breakpoint pending bits are stacked in the SSW, even though the instruction is restarted upon return from the handler. This avoids problems with bus state analyzer equipment that has been programmed to breakpoint only the first access to a specific location or to count accesses to that location. If this response is not desired, the exception handler can clear the bits before return. The RM, IN, RW, LG, FUNC, and SIZ fields all reflect the type of bus cycle that caused the fault. If the bus cycle was an RMW, the RM bit will be set, and the RW bit will show whether the fault was on a read or write.

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5.5.3.1.3 Type III—Faults During MOVEM Operand Transfer. Bus faults that occur as a result of MOVEM operand transfer are classified as type III faults. MOVEM instruction prefetch faults are type II faults.

Type III faults cause an immediate exception that aborts the current instruction. Registers altered during execution of the faulted instruction are not restored prior to execution of the fault handler. This includes any register predecremented as a result of the effective address calculation or any register overwritten during instruction execution. Since postincremented registers are not updated until the end of an instruction, the register retains its pre-instruction value unless overwritten by operand movement.

The SSW for faults in this category contains the following bit pattern:

15	14	13	12	11	10	9	8	7	6	5	4 3	2 0
0	1	0	TR	B1	B0	RR	0	IN	RW	LG	SIZ	FUNC

MV is set, indicating that MOVEM should be continued from the point where the fault occurred upon return from the exception handler. TR, B1, and B0 are set if a corresponding exception is pending when the bus error exception is taken. IN is set if a bus fault occurs while prefetching an opcode or an extension word during instruction restart. RW, LG, SIZ, and FUNC all reflect the type of bus cycle that caused the fault. All write faults have the RR bit set to indicate that the write should be rerun upon return from the exception handler.

The remainder of the stack frame contains sufficient information to continue MOVEM with operand transfer following a faulted transfer. The address of the next operand to be transferred, incremented or decremented by operand size, is stored in the faulted address location ($08). The stacked transfer counter is set to 16 minus the number of transfers attempted (including the faulted cycle). Refer to Figure 5-12 for the stacking format.

5.5.3.1.4 Type IV—Faults During Exception Processing. The fourth type of fault occurs during exception processing. If this exception is a second address or bus error, the machine halts in the double bus fault condition. However, if the exception is one that causes a four- or six-word stack frame to be written, a bus cycle fault frame is written below the faulted exception stack frame.

The SSW for a fault within an exception contains the following bit pattern:

15	14	13	12	11	10	9	8	7	6	5	4 3	2 0
1	0	0	TR	B1	B0	0	0	0	1	LG	SIZ	FUNC

TR, B1, and B0 are set if a corresponding exception is pending when the bus error exception is taken.

The contents of the faulted exception stack frame are included in the bus fault stack frame. The pre-exception SR and the format/vector word of the faulted frame are stacked. The type of exception can be determined from the format/vector word. If the faulted exception stack frame contains six words, the PC of the instruction that caused the initial

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exception is also stacked. This data is placed on the stack in the format shown in Figure 5-13. The return address from the initial exception is stacked for RTE .

5.5.3.2 CORRECTING A FAULT. There are two ways to complete a faulted released write bus cycle. The first is to use a software handler. The second is to rerun the bus cycle via RTE.

Type II fault handlers must terminate with RTE, but specific requirements must also be met before an instruction is restarted.

There are three varieties of type III operand fault recovery. The first is completion of an instruction in software. The second is conversion to type II with restart via RTE. The third is continuation from the fault via RTE.

5.5.3.2.1 Type I—Completing Released Writes via Software. To complete a bus cycle in software, a handler must first read the SSW function code field to determine the appropriate address space, access the fault address pointer on the stack, and then transfer data from the stacked image of the output buffer to the fault address.

Because the CPU32 has a 16-bit internal data bus, long operands require two bus accesses. A fault during the second access of a long operand causes the LG bit in the SSW to be set. The SIZ field indicates remaining operand size. If operand coherency is important, the complete operand must be rewritten. After a long operand is rewritten, the RR bit must be cleared. Failure to clear the RR bit can cause the RTE instruction to rerun the bus cycle. Following rewrite, it is not necessary to adjust the PC (or other stack contents) before executing RTE.

5.5.3.2.2 Type I—Completing Released Writes via RTE. An exception handler can use the RTE instruction to complete a faulted bus cycle. When RTE executes, the fault address, data output buffer, PC, and SR are restored from the stack. Any pending breakpoint or trace exceptions, as indicated by TR, B1, and B0 in the stacked SSW, are requeued during SSW restoration. The RR bit in the SSW is checked during the unstacking operation; if it is set, the RW, FUNC, and SIZ fields are restored and the released write cycle is rerun.

To maintain long-word operand coherence, stack contents must be adjusted prior to RTE execution. The fault address must be decremented by 2 if LG is set and SIZ indicates a remaining byte or word. SIZ must be set to long. All other fields should be left unchanged. The bus controller uses the modified fault address and SIZ field to rerun the complete released write cycle.

Manipulating the stacked SSW can cause unpredictable results because RTE checks only the RR bit to determine if a bus cycle must be rerun. Inadvertent alteration of the control bits could cause the bus cycle to be a read instead of a write or could cause access to a different address space than the original bus cycle. If the rerun bus cycle is a read, returned data will be ignored.

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5.5.3.2.3 Type II—Correcting Faults via RTE. Instructions aborted because of a type II fault are restarted upon return from the exception handler. A fault handler must establish safe restart conditions. If a fault is caused by a nonresident page in a demand-paged virtual memory configuration, the fault address must be read from the stack, and the appropriate page retrieved. An RTE instruction terminates the exception handler. After unstacking the machine state, the instruction is refetched and restarted.

5.5.3.2.4 Type III—Correcting Faults via Software. Sufficient information is contained in the stack frame to complete MOVEM in software. After the cause of the fault is corrected, the faulted bus cycle must be rerun. Perform the following procedures to complete an instruction through software:

A. Set Up for Rerun

1. Read the MOVEM opcode and extension from locations pointed to by stack frame PC and PC + 2. The EA need not be recalculated since the next operand address is saved in the stack frame. However, the opcode EA field must be examined to determine how to update the address register and PC when the instruction is complete.
2. Adjust the mask to account for operands already transferred. Subtract the stacked operand transfer count from 16 to obtain the number of operands transferred. Scan the mask using this count value. Each time a set bit is found, clear it and decrement the counter. When the count is zero, the mask is ready for use.
3. Adjust the operand address. If the predecrement addressing mode is in effect, subtract the operand size from the stacked value; otherwise, add the operand size to the stacked value.

B. Rerun Instruction

1. Scan the mask for set bits. Read/write the selected register from/to the operand address as each bit is found.
2. As each operand is transferred, clear the mask bit and increment (decrement) the operand address. When all bits in the mask are cleared, all operands have been transferred.
3. If the addressing mode is predecrement or postincrement, update the register to complete the execution of the instruction.
4. If TR is set in the stacked SSW, create a six-word stack frame and execute the trace handler. If either B1 or B0 is set in the SSW, create another six-word stack frame and execute the hardware breakpoint handler.
5. De-allocate the stack and return control to the faulted program.

5.5.3.2.5 Type III—Correcting Faults by Conversion and Restart. In some situations, it may be necessary to rerun all the operand transfers for a faulted instruction rather than continue from a faulted operand. Clearing the MV bit in the stacked SSW converts a type III fault into a type II fault. Consequently, MOVEM, like all other type II

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exceptions, will be restarted upon return from the exception handler. When a fault occurs after an operand has transferred, that transfer is not "undone". However, these memory locations are accessed a second time when the instruction is restarted. If a register used in an EA calculation is overwritten before a fault occurs, an incorrect EA is calculated upon instruction restart.

5.5.3.2.6 Type III—Correcting Faults via RTE. The preferred method of MOVEM bus fault recovery is to correct the cause of the fault and then execute an RTE instruction without altering the stack contents.

The RTE recognizes that MOVEM was in progress when a fault occurred, restores the appropriate machine state, refetches the instruction, repeats the faulted transfer, and continues the instruction.

MOVEM is the only instruction continued upon return from an exception handler. Although the instruction is refetched, the EA is not recalculated, and the mask is rescanned the same number of times as before the fault. Modifying the code prior to RTE can cause unexpected results.

5.5.3.2.7 Type IV—Correcting Faults via Software. Bus error exceptions can occur during exception processing while the processor is fetching an exception vector or while it is stacking. The same stack frame and SSW are used in both cases, but each has a distinct fault address. The stacked faulted exception format/vector word identifies the type of faulted exception and the contents of the remainder of the frame. A fault address corresponding to the vector specified in the stacked format/vector word indicates that the processor could not obtain the address of the exception handler.

A bus error exception handler should execute RTE after correcting a fault. RTE restores the internal machine state, fetches the address of the original exception handler, recreates the original exception stack frame, and resumes execution at the exception handler address.

If the fault is intractable, the exception handler should rewrite the faulted exception stack frame at SP + $14 + $06 and then jump directly to the original exception handler. The stack frame can be generated from the information in the bus error frame: the pre-exception SR (SP + $0C), the format/vector word (SP + $0E), and, if the frame being written is a six-word frame, the PC of the instruction causing the exception (SP + $10). The return PC value is available at SP + $02.

A stacked fault address equal to the current SP may indicate that, although the first exception received a bus error while stacking, the bus error exception stacking successfully completed. This occurrence is extremely improbable, but the CPU32 supports recovery from it. Once the exception handler determines that the fault has been corrected, recovery can proceed as described previously. If the fault cannot be corrected, move the supervisor stack to another area of memory, copy all valid stack frames to the new stack, create a faulted exception frame on top of the stack, and resume execution at the exception handler address.

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5.5.4 CPU32 Stack Frames

The CPU32 generates three different stack frames: four-word frames, six-word frames, and twelve-word bus error frames.

5.5.4.1 FOUR-WORD STACK FRAME. This stack frame is created by interrupt, format error, TRAP #n, illegal instruction, A-line and F-line emulator trap, and privilege violation exceptions. Depending on the exception type, the PC value is either the address of the next instruction to be executed or the address of the instruction that caused the exception (see Figure 5-12).

	15				0
SP ⇒	STATUS REGISTER				
+$02	PROGRAM COUNTER HIGH				
	PROGRAM COUNTER LOW				
+$06	0	0	0	0	VECTOR OFFSET

Figure 5-12. Format $0—Four-Word Stack Frame

5.5.4.2 SIX-WORD STACK FRAME. This stack frame (see Figure 5-13) is created by instruction-related traps, which include CHK, CHK2, TRAPcc, TRAPV, and divide-by-zero, and by trace exceptions. The faulted instruction PC value is the address of the instruction that caused the exception. The next PC value (the address to which RTE returns) is the address of the next instruction to be executed.

	15				0
SP ⇒	STATUS REGISTER				
+$02	NEXT INSTRUCTION PROGRAM COUNTER HIGH				
	NEXT INSTRUCTION PROGRAM COUNTER LOW				
+$06	0	0	1	0	VECTOR OFFSET
+$08	FAULTED INSTRUCTION PROGRAM COUNTER HIGH				
	FAULTED INSTRUCTION PROGRAM COUNTER LOW				

Figure 5-13. Format $2—Six-Word Stack Frame

Hardware breakpoints also utilize this format. The faulted instruction PC value is the address of the instruction executing when the breakpoint was sensed. Usually this is the address of the instruction that caused the breakpoint, but, because released writes can overlap following instructions, the faulted instruction PC may point to an instruction following the instruction that caused the breakpoint. The address to which RTE returns is the address of the next instruction to be executed.

5.5.4.3 BUS ERROR STACK FRAME. This stack frame is created when a bus cycle fault is detected. The CPU32 bus error stack frame differs significantly from the equivalent stack frames of other M68000 Family members. The only internal machine state required in the CPU32 stack frame is the bus controller state at the time of the error and a single register.

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Bus operation in progress at the time of a fault is conveyed by the SSW.

15	14	13	12	11	10	9	8	7	6	5	4 3	2 1 0
TP	MV	0	TR	B1	B0	RR	RM	IN	RW	LG	SIZ	FUNC

The bus error stack frame is 12 words in length. There are three variations of the frame, each distinguished by different values in the SSW TP and MV fields.

An internal transfer count register appears at location SP + $14 in all bus error stack frames. The register contains an 8-bit microcode revision number, and, for type III faults, an 8-bit transfer count. Register format is shown in Figure 5-14.

15 8	7 0
MICROCODE REVISION NUMBER	TRANSFER COUNT

Figure 5-14. Internal Transfer Count Register

The microcode revision number is checked before a bus error stack frame is restored via RTE. In a multiprocessor system, this check ensures that a processor using stacked information is at the same revision level as the processor that created it.

The transfer count is ignored unless the MV bit in the stacked SSW is set. If the MV bit is set, the least significant byte of the internal register is reloaded into the MOVEM transfer counter during RTE execution.

For faults occurring during normal instruction execution (both prefetches and non-MOVEM operand accesses), SSW TP,MV = 00. Stack frame format is shown in Figure 5-15.

Faults that occur during the operand portion of the MOVEM instruction are identified by SSW TP,MV = 01. Stack frame format is shown in Figure 5-16.

When a bus error occurs during exception processing, SSW TP,MV = 10. The frame shown in Figure 5-17 is written below the faulting frame. Stacking begins at the address pointed to by SP – 6 (SP value is the value before initial stacking on the faulted frame).

The frame can have either four or six words, depending on the type of error. Four-word stack frames do not include the faulted instruction PC. (The internal transfer count register is located at SP + $10 and the SSW is located at SP + $12.)

The fault address of a dynamically sized bus cycle is the address of the upper byte, regardless of the byte that caused the error.

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	15				0
SP ⇒	STATUS REGISTER				
+$02	RETURN PROGRAM COUNTER HIGH				
	RETURN PROGRAM COUNTER LOW				
+$06	1	1	0	0	VECTOR OFFSET
+$08	FAULTED ADDRESS HIGH				
	FAULTED ADDRESS LOW				
+$0C	DBUF HIGH				
	DBUF LOW				
+$10	CURRENT INSTRUCTION PROGRAM COUNTER HIGH				
	CURRENT INSTRUCTION PROGRAM COUNTER LOW				
+$14	INTERNAL TRANSFER COUNT REGISTER				
+$16	0	0	SPECIAL STATUS WORD		

Figure 5-15. Format $C—BERR Stack for Prefetches and Operands

	15				0
SP ⇒	STATUS REGISTER				
+$02	RETURN PROGRAM COUNTER HIGH				
	RETURN PROGRAM COUNTER LOW				
+$06	1	1	0	0	VECTOR OFFSET
+$08	FAULTED ADDRESS HIGH				
	FAULTED ADDRESS LOW				
+$0C	DBUF HIGH				
	DBUF LOW				
+$10	CURRENT INSTRUCTION PROGRAM COUNTER HIGH				
	CURRENT INSTRUCTION PROGRAM COUNTER LOW				
+$14	INTERNAL TRANSFER COUNT REGISTER				
+$16	0	1	SPECIAL STATUS WORD		

Figure 5-16. Format $C—BERR Stack on MOVEM Operand

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	15				0
SP ⇒	STATUS REGISTER				
+$02	NEXT INSTRUCTION PROGRAM COUNTER HIGH				
	NEXT INSTRUCTION PROGRAM COUNTER LOW				
+$06	1	1	0	0	VECTOR OFFSET
+$08	FAULTED ADDRESS HIGH				
	FAULTED ADDRESS LOW				
+$0C	PRE-EXCEPTION STATUS REGISTER				
	FAULTED EXCEPTION FORMAT/VECTOR WORD				
+$10	FAULTED INSTRUCTION PROGRAM COUNTER HIGH (SIX WORD FRAME ONLY)				
	FAULTED INSTRUCTION PROGRAM COUNTER LOW (SIX WORD FRAME ONLY)				
+$14	INTERNAL TRANSFER COUNT REGISTER				
+$16	1	0	SPECIAL STATUS WORD		

Figure 5-17. Format $C—Four- and Six-Word BERR Stack

5.6 DEVELOPMENT SUPPORT

All M68000 family members have the following special features that facilitate applications development.

Trace on Instruction Execution—All M68000 processors include an instruction-by-instruction tracing facility to aid in program development. The MC68020, MC68030, and CPU32 can also trace those instructions that change program flow. In trace mode, an exception is generated after each instruction is executed, allowing a debugger program to monitor execution of a program under test. See **5.5.2.10 Tracing** for more information.

Breakpoint Instruction—An emulator can insert software breakpoints into target code to indicate when a breakpoint occurs. On the MC68010, MC68020, MC68030, and CPU32, this function is provided via illegal instructions ($4848–$484F) that serve as breakpoint instructions. See **5.5.2.5 Software Breakpoints** for more information.

Unimplemented Instruction Emulation—When an attempt is made to execute an illegal instruction, an illegal instruction exception occurs. Unimplemented instructions (F-line, A-line) utilize separate exception vectors to permit efficient emulation of unimplemented instructions in software. See **5.5.2.8 Illegal or Unimplemented Instructions** for more information.

5.6.1 CPU32 Integrated Development Support

In addition to standard MC68000 family capabilities, the CPU32 has features to support advanced integrated system development. These features include background debug mode, deterministic opcode tracking, hardware breakpoints, and internal visibility in a single-chip environment.

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5.6.1.1 BACKGROUND DEBUG MODE (BDM) OVERVIEW. Microprocessor systems generally provide a debugger, implemented in software, for system analysis at the lowest level. The BDM on the CPU32 is unique because the debugger is implemented in CPU microcode.

BDM incorporates a full set of debug options—registers can be viewed and/or altered, memory can be read or written, and test features can be invoked.

A resident debugger simplifies implementation of an in-circuit emulator. In a common setup (see Figure 5-18), emulator hardware replaces the target system processor. A complex, expensive pod-and-cable interface provides a communication path between target system and emulator.

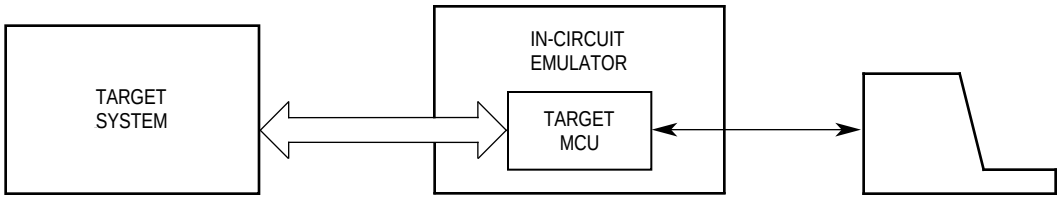

Figure 5-18. In-Circuit Emulator Configuration

By contrast, an integrated debugger supports use of a bus state analyzer (BSA) for in-circuit emulation. The processor remains in the target system (see Figure 5-19), and the interface is simplified. The BSA monitors target processor operation and the on-chip debugger controls the operating environment. Emulation is much closer to target hardware; thus, many interfacing problems (i.e., limitations on high-frequency operation, AC and DC parametric mismatches, and restrictions on cable length) are minimized.

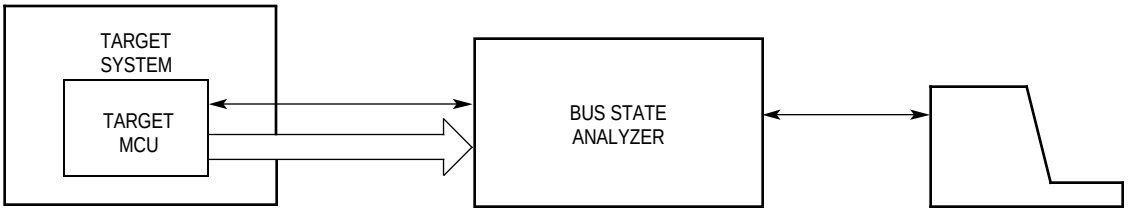

Figure 5-19. Bus State Analyzer Configuration

5.6.1.2 DETERMINISTIC OPCODE TRACKING OVERVIEW. CPU32 function code outputs are augmented by three supplementary signals that monitor the instruction pipeline. The $\overline{\text{IFETCH}}$ output signal identifies bus cycles in which data is loaded into the pipeline and signals pipeline flushes. The $\overline{\text{IPIPE}}$ output signals indicate when each mid-instruction pipeline advance occurs and when instruction execution begins. These signals allow a BSA to synchronize with instruction stream activity. Refer to **5.6.3 Deterministic Opcode Tracking** for complete information.

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5.6.1.3 ON-CHIP HARDWARE BREAKPOINT OVERVIEW. An external breakpoint input and an on-chip hardware breakpoint capability permit breakpoint trap on any memory access. Off-chip address comparators will not detect breakpoints on internal accesses unless show cycles are enabled. Breakpoints on prefetched instructions, which are flushed from the pipeline before execution, are not acknowledged, but operand breakpoints are always acknowledged. Acknowledged breakpoints can initiate either exception processing or BDM. See **5.5.2.6 Hardware Breakpoints** for more information.

5.6.2 Background Debug Mode

BDM is an alternate CPU32 operating mode. During BDM, normal instruction execution is suspended, and special microcode performs debugging functions under external control. Figure 5-20 is a BDM block diagram.

BDM can be initiated in several ways—by externally generated breakpoints, by internal peripheral breakpoints, by the background instruction (BGND), or by catastrophic exception conditions. While in BDM, the CPU32 ceases to fetch instructions via the parallel bus and communicates with the development system via a dedicated, high-speed, SPI-type serial command interface.

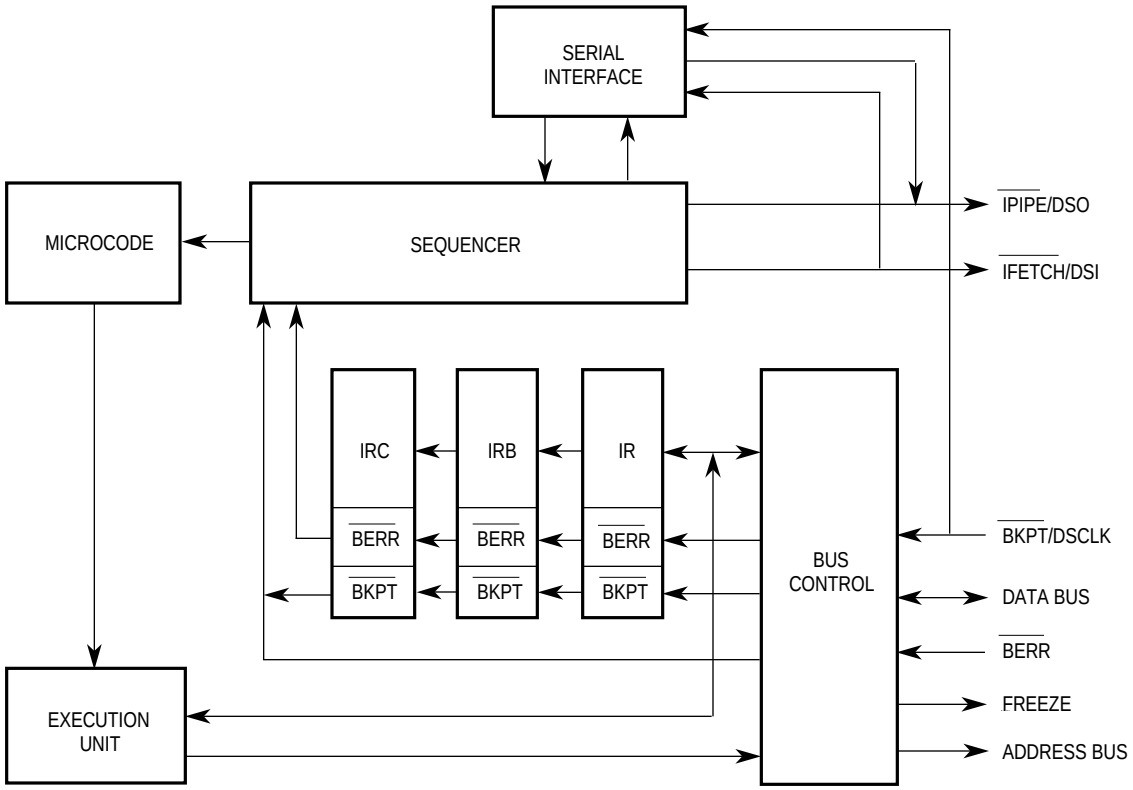

Figure 5-20. BDM Block Diagram

5.6.2.1 ENABLING BDM. Accidentally entering BDM in a nondevelopment environment could lock up the CPU32 since the serial command interface would probably not be available. For this reason, BDM is enabled during reset via the $\overline{\text{BKPT}}$ signal.

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BDM operation is enabled when $\overline{\text{BKPT}}$ is asserted (low) at the rising edge of $\overline{\text{RESET}}$. BDM remains enabled until the next system reset. A high $\overline{\text{BKPT}}$ on the trailing edge of $\overline{\text{RESET}}$ disables BDM. $\overline{\text{BKPT}}$ is relatched on each rising transition of $\overline{\text{RESET}}$. $\overline{\text{BKPT}}$ is synchronized internally and must be held low for at least two clock cycles prior to negation of $\overline{\text{RESET}}$.

BDM enable logic must be designed with special care. If hold time on $\overline{\text{BKPT}}$ (after the trailing edge of $\overline{\text{RESET}}$) extends into the first bus cycle following reset, this bus cycle could be tagged with a breakpoint. Refer to **Section 3 Bus Operation** for timing information.

5.6.2.2 BDM SOURCES. When BDM is enabled, any of several sources can cause the transition from normal mode to BDM. These sources include external $\overline{\text{BKPT}}$ hardware, the BGND instruction, a double bus fault, and internal peripheral breakpoints. If BDM is not enabled when an exception condition occurs, the exception is processed normally. Table 5-19 summarizes the processing of each source for both enabled and disabled cases. Note that the BKPT instruction never causes a transition into BDM.

Table 5-19. BDM Source Summary

Source	BDM Enabled	BDM Disabled
$\overline{\text{BKPT}}$	Background	Breakpoint Exception
Double Bus Fault	Background	Halted
BGND Instruction	Background	Illegal Instruction
BKPT Instruction	Opcode Substitution/ Illegal Instruction	Opcode Substitution/ Illegal Instruction

5.6.2.2.1 External $\overline{\text{BKPT}}$ Signal. Once enabled, BDM is initiated whenever assertion of $\overline{\text{BKPT}}$ is acknowledged. If BDM is disabled, a breakpoint exception (vector $0C) is acknowledged. The $\overline{\text{BKPT}}$ input has the same timing relationship to the data strobe trailing edge as read cycle data. There is no breakpoint acknowledge bus cycle when BDM is entered.

5.6.2.2.2 BGND Instruction. An illegal instruction, $4AFA, is reserved for use by development tools. The CPU32 defines $4AFA (BGND) to be a BDM entry point when BDM is enabled. If BDM is disabled, an illegal instruction trap is acknowledged. Illegal instruction traps are discussed in **5.5.2.8 Illegal or Unimplemented Instructions**.

5.6.2.2.3 Double Bus Fault. The CPU32 normally treats a double bus fault (two bus faults in succession) as a catastrophic system error and halts. When this condition occurs during initial system debug (a fault in the reset logic), further debugging is impossible until the problem is corrected. In BDM, the fault can be temporarily bypassed so that its origin can be isolated and eliminated.

5.6.2.3 ENTERING BDM. When the processor detects a $\overline{\text{BKPT}}$ or a double bus fault or decodes a BGND instruction, it suspends instruction execution and asserts the FREEZE output. FREEZE assertion is the first indication that the processor has entered BDM. Once

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FREEZE has been asserted, the CPU enables the serial communication hardware and awaits a command.

The CPU writes a unique value indicating the source of BDM transition into temporary register A (ATEMP) as part of the process of entering BDM. A user can poll ATEMP and determine the source (see Table 5-20) by issuing a read system register command (RSREG). ATEMP is used in most debugger commands for temporary storage—it is imperative that the RSREG command be the first command issued after transition into BDM.

Table 5-20. Polling the BDM Entry Source

Source	ATEMP 31–16	ATEMP 15–0
Double Bus Fault	SSW*	$FFFF
BGND Instruction	$0000	$0001
Hardware Breakpoint	$0000	$0000

*SSW is described in detail in **5.5.3 Fault Recovery.**

A double bus fault during initial SP/PC fetch sequence is distinguished by a value of $FFFFFFFF in the current instruction PC. At no other time will the processor write an odd value into this register.

5.6.2.4 COMMAND EXECUTION. Figure 5-21 summarizes BDM command execution. Commands consist of one 16-bit operation word and can include one or more 16-bit extension words. Each incoming word is read as it is assembled by the serial interface. The microcode routine corresponding to a command is executed as soon as the command is complete. Result operands are loaded into the output shift register to be shifted out as the next command is read. This process is repeated for each command until the CPU returns to normal operating mode.

5.6.2.5 BDM REGISTERS. BDM processing uses three special-purpose registers to track program context during development. A description of each register follows.

5.6.2.5.1 Fault Address Register (FAR). The FAR contains the address of the faulting bus cycle immediately following a bus or address error. This address remains available until overwritten by a subsequent bus cycle. Following a double bus fault, the FAR contains the address of the last bus cycle. The address of the first fault (if one occurred) is not visible to the user.

5.6.2.5.2 Return Program Counter (RPC). The RPC points to the location where fetching will commence after transition from BDM to normal mode. This register should be accessed to change the flow of a program under development. Changing the RPC to an odd value will cause an address error when normal mode prefetching begins.

5.6.2.5.3 Current Instruction Program Counter (PCC). The PCC holds a pointer to the first word of the last instruction executed prior to transition into BDM. Due to instruction pipelining, the instruction pointed to may not be the instruction that caused the transition. An example is a breakpoint on a released write. The bus cycle may overlap as many as two subsequent instructions before stalling the instruction sequencer. A $\overline{\text{BKPT}}$ asserted

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during this cycle will not be acknowledged until the end of the instruction executing at completion of the bus cycle. PCC will contain $00000001 if BDM is entered via a double bus fault immediately out of reset.

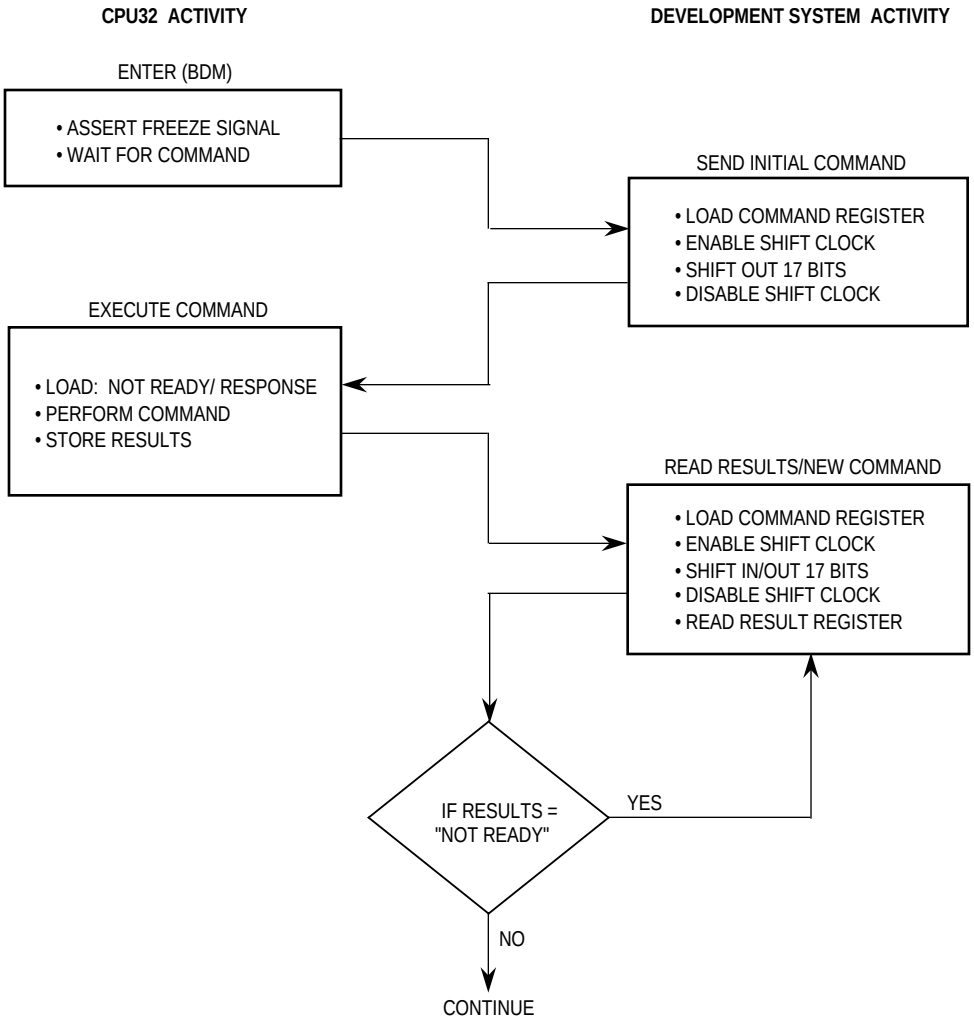

Figure 5-21. BDM Command Execution Flowchart

5.6.2.6 RETURNING FROM BDM. BDM is terminated when a resume execution (GO) or call user code (CALL) command is received. Both GO and CALL flush the instruction pipeline and prefetch instructions from the location pointed to by the RPC.

The return PC and the memory space referred to by the SR SUPV bit reflect any changes made during BDM. FREEZE is negated prior to initiating the first prefetch. Upon negation of FREEZE, the serial subsystem is disabled, and the signals revert to $\overline{\text{IPIPE}}$ and $\overline{\text{IFETCH}}$ functionality.

5.6.2.7 SERIAL INTERFACE. Communication with the CPU32 during BDM occurs via a dedicated serial interface, which shares pins with other development features. The $\overline{\text{BKPT}}$ signal becomes the DSCLK; DSI is received on $\overline{\text{IFETCH}}$, and DSO is transmitted on $\overline{\text{IPIPE}}$.

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The serial interface uses a full-duplex synchronous protocol similar to the serial peripheral interface (SPI) protocol. The development system serves as the master of the serial link since it is responsible for the generation of DSCLK. If DSCLK is derived from the CPU32 system clock, development system serial logic is unhindered by the operating frequency of the target processor. Operable frequency range of the serial clock is from DC to one-half the processor system clock frequency.

The serial interface operates in full-duplex mode—i.e., data is transmitted and received simultaneously by both master and slave devices. In general, data transitions occur on the falling edge of DSCLK and are stable by the following rising edge of DSCLK. Data is transmitted MSB first and is latched on the rising edge of DSCLK.

The serial data word is 17 bits wide—16 data bits and a status/control (S/C) bit.

16	15 … 0
S/C	DATA FIELD

Bit 16 indicates the status of CPU-generated messages as listed in Table 5-21.

Table 5-21. CPU Generated Message Encoding

Encoding	Data	Message Type
0	xxxx	Valid Data Transfer
0	FFFF	Command Complete; Status OK
1	0000	Not Ready with Response; Come Again
1	0001	$\overline{\text{BERR}}$ Terminated Bus Cycle; Data Invalid
1	FFFF	Illegal Command

Command and data transfers initiated by the development system should clear bit 16. The current implementation ignores this bit; however, Motorola reserves the right to use this bit for future enhancements.

5.6.2.7.1 CPU Serial Logic. CPU serial logic, shown in the left-hand portion of Figure 5-22, consists of transmit and receive shift registers and of control logic that includes synchronization, serial clock generation circuitry, and a received bit counter.

Both DSCLK and DSI are synchronized to on-chip clocks, thereby minimizing the chance of propagating metastable states into the serial state machine. Data is sampled during the high phase of CLKOUT. At the falling edge of CLKOUT, the sampled value is made available to internal logic. If there is no synchronization between CPU32 and development system hardware, the minimum hold time on DSI with respect to DSCLK is one full period of CLKOUT.

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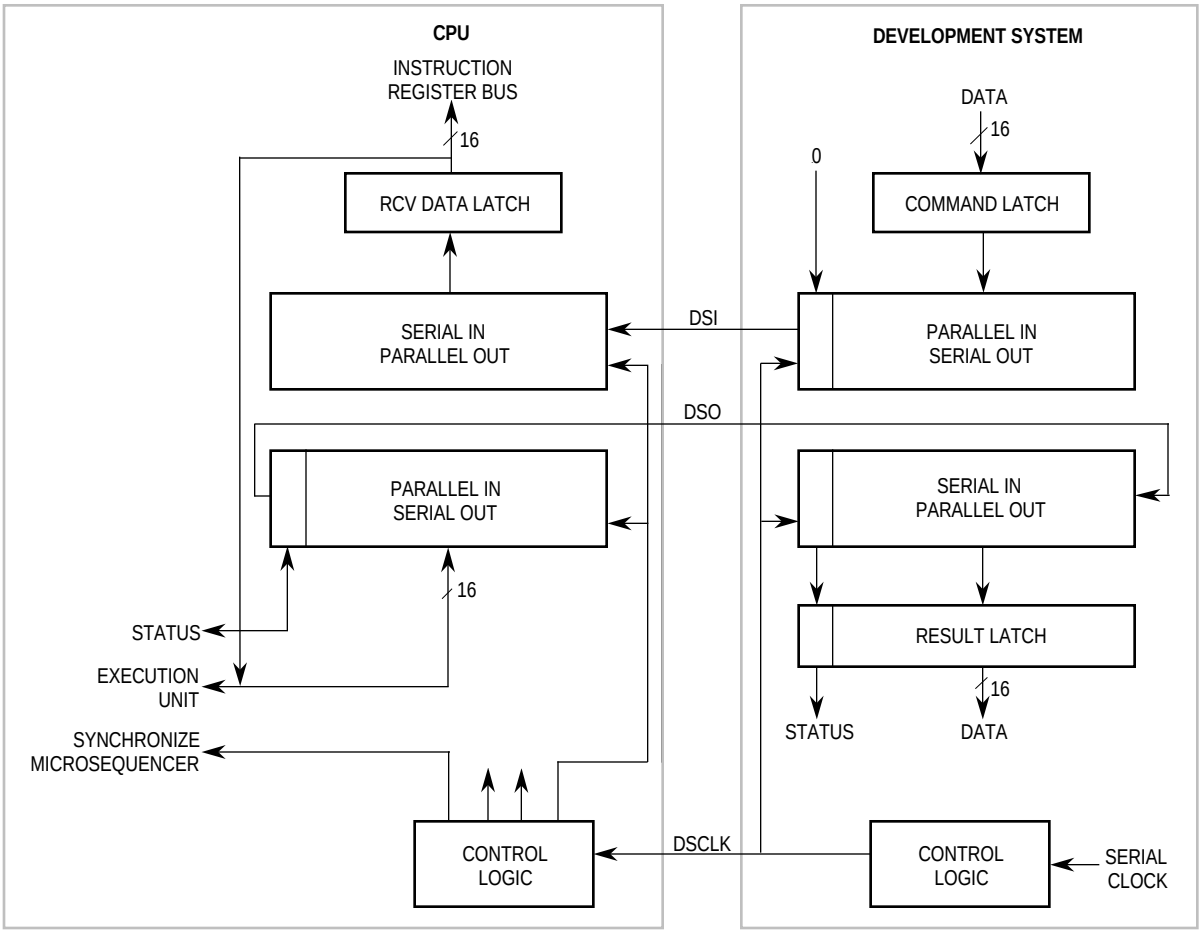

Figure 5-22. Debug Serial I/O Block Diagram

The serial state machine begins a sequence of events based on the rising edge of the synchronized DSCLK (see Figure 5-23). Synchronized serial data is transferred to the input shift register, and the received bit counter is decremented. One-half clock period later, the output shift register is updated, bringing the next output bit to the DSO signal. DSO changes relative to the rising edge of DSCLK and does not necessarily remain stable until the falling edge of DSCLK.

One clock period after the synchronized DSCLK has been seen internally, the updated counter value is checked. If the counter has reached zero, the receive data latch is updated from the input shift register. At this same time, the output shift register is reloaded with the “not ready/come again” response. Once the receive data latch has been loaded, the CPU is released to act on the new data. Response data overwrites the “not ready” response when the CPU has completed the current operation.

Data written into the output shift register appears immediately on the DSO signal. In general, this action changes the state of the signal from a high (“not ready” response status bit) to a low (valid data status bit) logic level. However, this level change only occurs if the command completes successfully. Error conditions overwrite the “not ready” response with the appropriate response that also has the status bit set.

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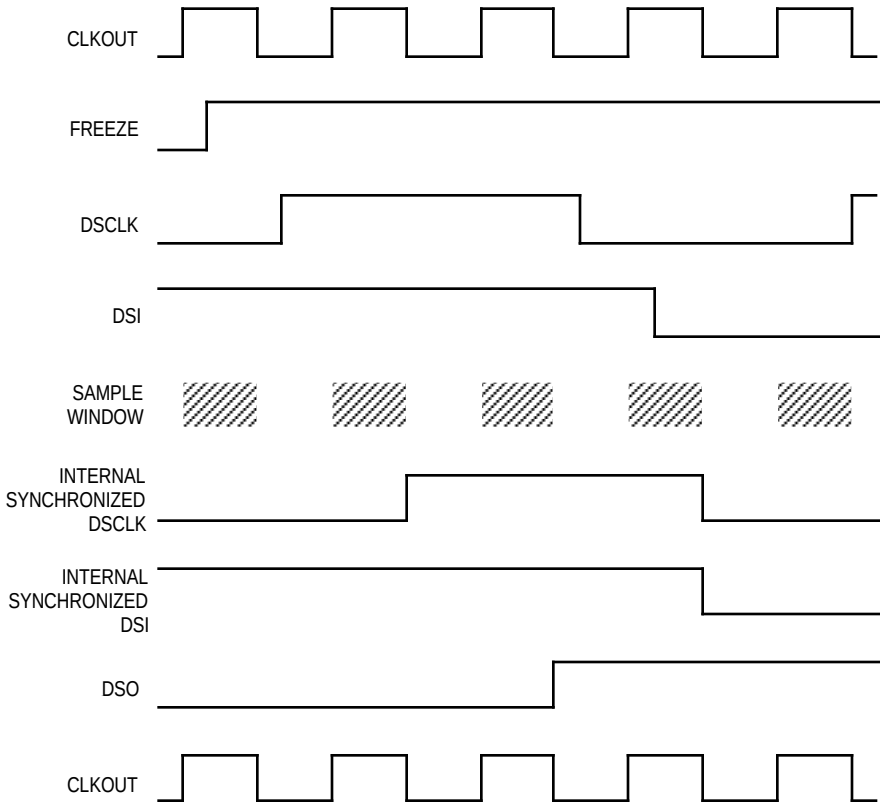

Figure 5-23. Serial Interface Timing Diagram

A user can use the state change on DSO to signal hardware that the next serial transfer may begin. A timeout of sufficient length to trap error conditions that do not change the state of DSO should also be incorporated into the design. Hardware interlocks in the CPU prevent result data from corrupting serial transfers in progress.

5.6.2.7.2 Development System Serial Logic. The development system, as the master of the serial data link, must supply the serial clock. However, normal and BDM operations could interact if the clock generator is not properly designed.

Breakpoint requests are made by asserting $\overline{\text{BKPT}}$ to the low state in either of two ways. The primary method is to assert $\overline{\text{BKPT}}$ during a single bus cycle for which an exception is desired. Another method is to assert $\overline{\text{BKPT}}$, then continue to assert it until the CPU32 responds by asserting FREEZE. This method is useful for forcing a transition into BDM when the bus is not being monitored. Each method requires a slightly different serial logic design to avoid spurious serial clocks.

Figure 5-24 represents the timing required for asserting $\overline{\text{BKPT}}$ during a single bus cycle.

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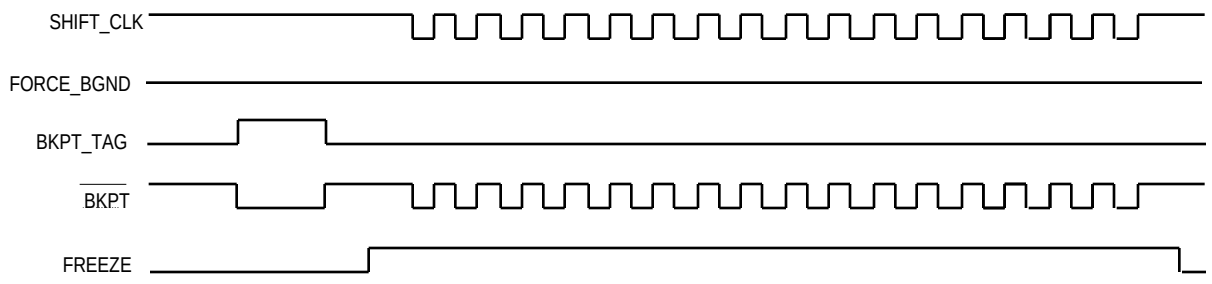

Figure 5-24. $\overline{\text{BKPT}}$ Timing for Single Bus Cycle

Figure 5-25 depicts the timing of the $\overline{\text{BKPT}}$/FREEZE method. In both cases, the serial clock is left high after the final shift of each transfer. This technique eliminates the possibility of accidentally tagging the prefetch initiated at the conclusion of a BDM session. As mentioned previously, all timing within the CPU is derived from the rising edge of the clock; the falling edge is effectively ignored.

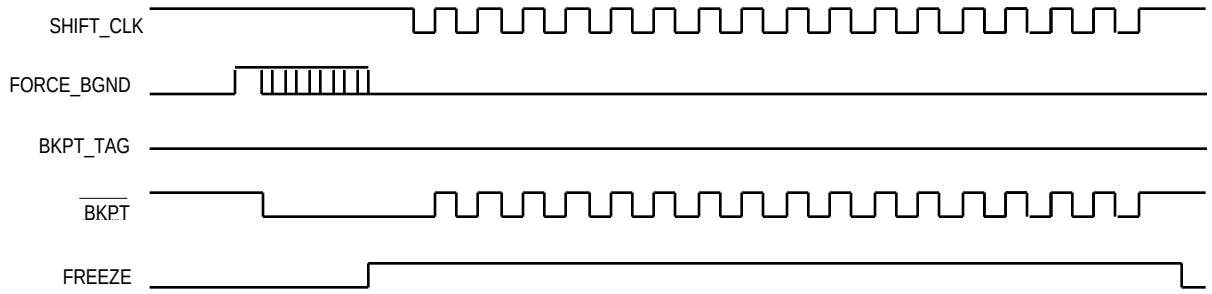

Figure 5-25. $\overline{\text{BKPT}}$ Timing for Forcing BDM

Figure 5-26 represents a sample circuit providing for both $\overline{\text{BKPT}}$ assertion methods. As the name implies, FORCE_BGND is used to force a transition into BDM by the assertion of $\overline{\text{BKPT}}$. FORCE_BGND can be a short pulse or can remain asserted until FREEZE is asserted. Once asserted, the set-reset latch holds $\overline{\text{BKPT}}$ low until the first SHIFT_CLK is applied.

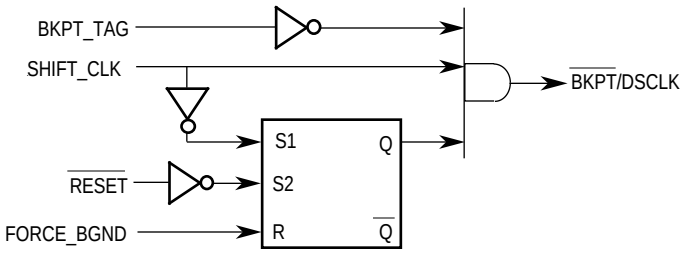

Figure 5-26. $\overline{\text{BKPT}}$/DSCLK Logic Diagram

BKPT_TAG should be timed to the bus cycles since it is not latched. If extended past the assertion of FREEZE, the negation of BKPT_TAG appears to the CPU32 as the first DSCLK.

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DSCLK, the gated serial clock, is normally high, but it pulses low for each bit to be transferred. At the end of the seventeenth clock period, it remains high until the start of the next transmission. Clock frequency is implementation dependent and may range from DC to the maximum specified frequency. Although performance considerations might dictate a hardware implementation, software solutions can be used provided serial bus timing is maintained.

5.6.2.8 COMMAND SET. The following paragraphs describe the command set available in BDM.

5.6.2.8.1 Command Format. The following standard bit command format is utilized by all BDM commands.

15 – 10	9	8	7 – 6	5	4	3	2 – 0
OPERATION	0	R/W	OP SIZE	0	0	A/D	REGISTER
EXTENSION WORD(S)							

Bits 15–10—Operation Field

The operation field specifies the commands. This 6-bit field provides for a maximum of 64 unique commands.

R/W Field

The R/W field specifies the direction of operand transfer. When the bit is set, the transfer is from theCPU to the development system. When the bit is cleared, data is written to the CPU or to memory from the development system.

Operand Size

For sized operations, this field specifies the operand data size. All addresses are expressed as 32-bit absolute values. The size field is encoded as listed in Table 5-22.

Table 5-22. Size Field Encoding

Encoding	Operand Size
00	Byte
01	Word
10	Long
11	Reserved

Address/Data (A/D) Field

The A/D field is used by commands that operate on address and data registers. It determines whether the register field specifies a data or address register. One indicates an address register; zero indicates a data register. For other commands, this field may be interpreted differently.

Register Field:

In most commands, this field specifies the register number for operations performed on an address or data register.

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Extension Word(s) (as required):

At this time, no command requires an extension word to specify fully the operation to be performed, but some commands require extension words for addresses or immediate data. Addresses require two extension words because only absolute long addressing is permitted. Immediate data can be either one or two words in length—byte and word data each require a single extension word; long-word data requires two words. Both operands and addresses are transferred most significant word first.

5.6.2.8.2 Command Sequence Diagram. A command sequence diagram (see Figure 5-27) illustrates the serial bus traffic for each command. Each bubble in the diagram represents a single 17-bit transfer across the bus. The top half in each diagram corresponds to the data transmitted by the development system to the CPU; the bottom half corresponds to the data returned by the CPU in response to the development system commands. Command and result transactions are overlapped to minimize latency.

The cycle in which the command is issued contains the development system command mnemonic (in this example, “read memory location”). During the same cycle, the CPU responds with either the lowest order results of the previous command or with a command complete status (if no results were required).

During the second cycle, the development system supplies the high-order 16 bits of the memory address. The CPU returns a "not ready" response unless the received command was decoded as unimplemented, in which case the response data is the illegal command encoding. If an illegal command response occurs, the development system should retransmit the command.

NOTE

The “not ready” response can be ignored unless a memory bus cycle is in progress. Otherwise, the CPU can accept a new serial transfer with eight system clock periods.

In the third cycle, the development system supplies the low-order 16 bits of a memory address. The CPU always returns the “not ready” response in this cycle. At the completion of the third cycle, the CPU initiates a memory read operation. Any serial transfers that begin while the memory access is in progress return the “not ready” response.

Results are returned in the two serial transfer cycles following the completion of memory access. The data transmitted to the CPU during the final transfer is the opcode for the following command. Should a memory access generate either a bus or address error, an error status is returned in place of the result data.

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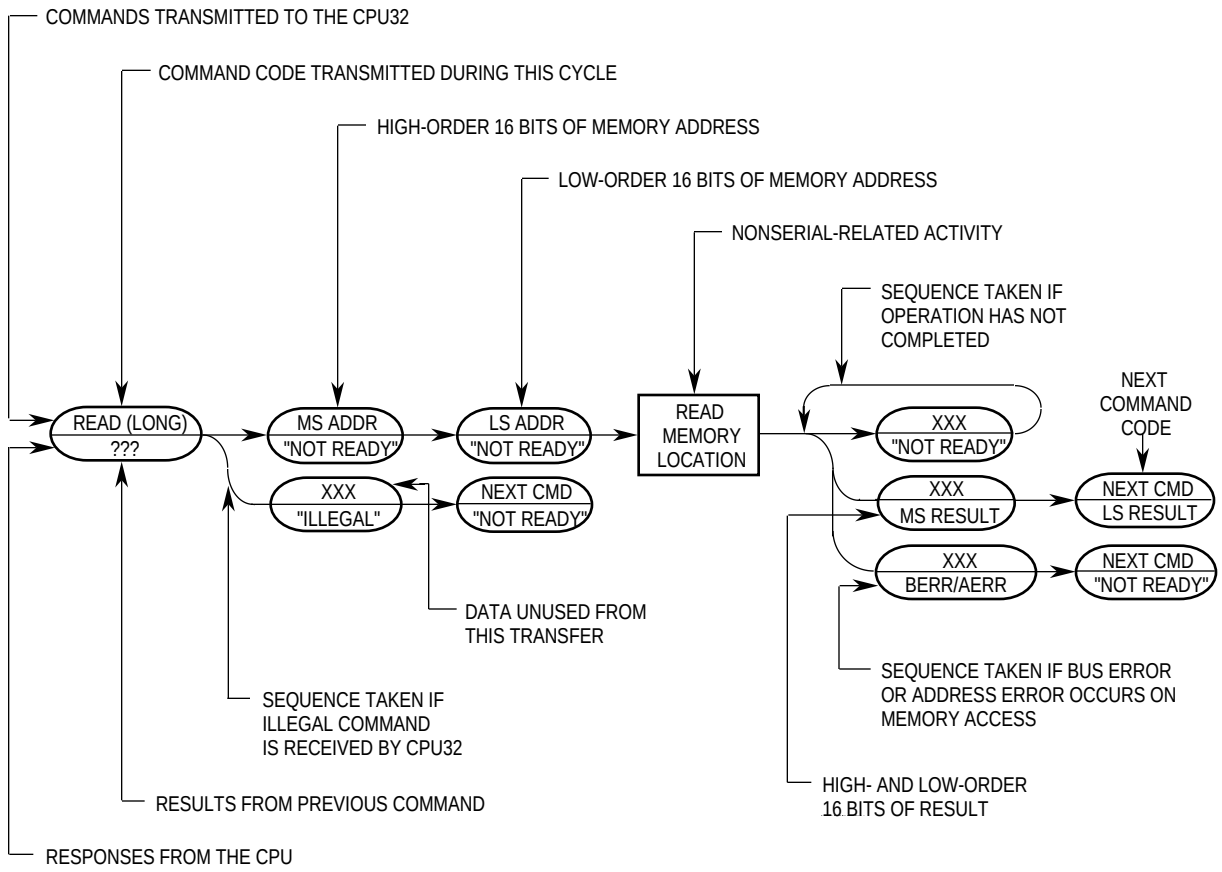

Figure 5-27. Command Sequence Diagram

5.6.2.8.3 Command Set Summary. The BDM command set is summarized in Table 5-23. Subsequent paragraphs contain detailed descriptions of each command.

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Table 5-23. BDM Command Summary

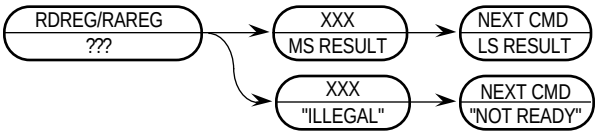
Command	Mnemonic	Description
Read A/D Register	RAREG/RDREG	Read the selected address or data register and return the results via the serial interface.
Write A/D Register	WAREG/WDREG	The data operand is written to the specified address or data register.
Read System Register	RSREG	The specified system control register is read. All registers that can be read in supervisor mode can be read in BDM.
Write System Register	WSREG	The operand data is written into the specified system control register.
Read Memory Location	READ	Read the sized data at the memory location specified by the long-word address. The SFC register determines the address space accessed.
Write Memory Location	WRITE	Write the operand data to the memory location specified by the long-word address. The DFC register determines the address space accessed.
Dump Memory Block	DUMP	Used in conjunction with the READ command to dump large blocks of memory. An initial READ is executed to set up the starting address of the block and to retrieve the first result. Subsequent operands are retrieved with the DUMP command.
Fill Memory Block	FILL	Used in conjunction with the WRITE command to fill large blocks of memory. An initial WRITE is executed to set up the starting address of the block and to supply the first operand. Subsequent operands are written with the FILL command.
Resume Execution	GO	The pipeline is flushed and refilled before resuming instruction execution at the return PC.
Call User Code	CALL	Current PC is stacked at the location of the current SP. Instruction execution begins at user patch code.
Reset Peripherals	RST	Asserts RESET for 512 clock cycles. The CPU is not reset by this command. Synonymous with the CPU RESET instruction.
No Operation	NOP	NOP performs no operation and may be used as a null command.

5.6.2.8.4 Read A/D Register (RAREG/RDREG). Read the selected address or data register and return the results via the serial interface.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	0	0	0	1	1	0	0	0	A/D	REGISTER		

Command Sequence:



Operand Data:
None

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Result Data:

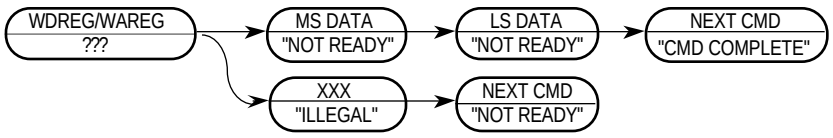
The contents of the selected register are returned as a long-word value. The data is returned most significant word first.

5.6.2.8.5 Write A/D Register (WAREG/WDREG). The operand (long-word) data is written to the specified address or data register. All 32 bits of the register are altered by the write.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2 — 0
0	0	1	0	0	0	0	0	1	0	0	0	A/D	REGISTER

Command Sequence:



Operand Data:

Long-word data is written into the specified address or data register. The data is supplied most significant word first.

Result Data:

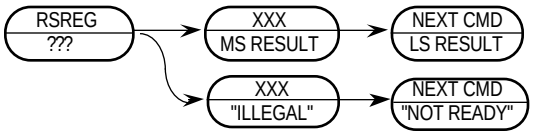
Command complete status ($0FFFF) is returned when register write is complete.

5.6.2.8.6 Read System Register (RSREG). The specified system control register is read. All registers that can be read in supervisor mode can be read in BDM. Several internal temporary registers are also accessible.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3 — 0
0	0	1	0	0	1	0	0	1	0	0	0	REGISTER

Command Sequence:



Operand Data:

None

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Result Data:

Always returns 32 bits of data, regardless of the size of the register being read. If the register is less than 32 bits, the result is returned zero extended.

Register Field:

The system control register is specified by the register field (see Table 5-24).

Table 5-24. Register Field for RSREG and WSREG

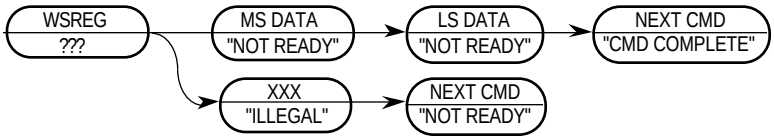
System Register	Select Code
Return Program Counter (RPC)	0000
Current Instruction Program Counter (PCC)	0001
Status Register (SR)	1011
User Stack Pointer (USP)	1100
Supervisor Stack Pointer (SSP)	1101
Source Function Code Register (SFC)	1110
Destination Function Code Register (DFC)	1111
Temporary Register A (ATEMP)	1000
Fault Address Register (FAR)	1001
Vector Base Register (VBR)	1010

5.6.2.8.7 Write System Register (WSREG). Operand data is written into the specified system control register. All registers that can be written in supervisor mode can be written in BDM. Several internal temporary registers are also accessible.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3 — 0
0	0	1	0	0	1	0	0	1	0	0	0	REGISTER

Command Sequence:



Operand Data:

The data to be written into the register is always supplied as a 32-bit long word. If the register is less than 32 bits, the least significant word is used.

Result Data:

“Command complete” status is returned when register write is complete.

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Register Field:

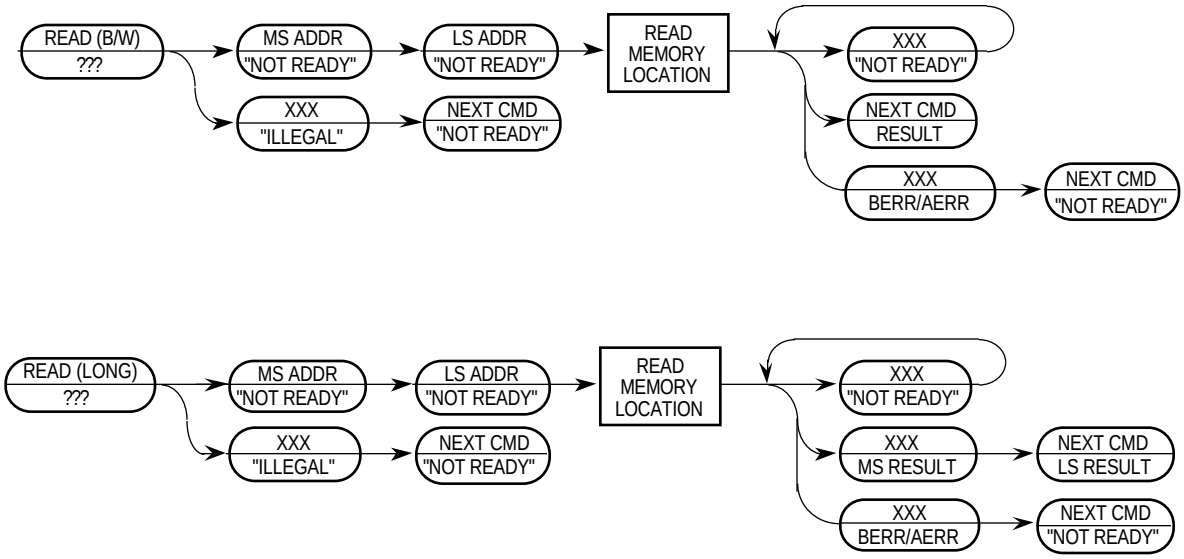
The system control register is specified by the register field (see Table 5-24). The FAR is a read-only register—any write to it is ignored.

5.6.2.8.8 Read Memory Location (READ). Read the sized data at the memory location specified by the long-word address. Only absolute addressing is supported. The SFC register determines the address space accessed. Valid data sizes include byte, word, or long word.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	1	OP SIZE		0	0	0	0	0	0

Command Sequence:



Operand Data:

The single operand is the long-word address of the requested memory location.

Result Data:

The requested data is returned as either a word or long word. Byte data is returned in the least significant byte of a word result, with the upper byte cleared. Word results return 16 bits of significant data; long-word results return 32 bits.

A successful read operation returns data bit 16 cleared. If a bus or address error is encountered, the returned data is $10001.

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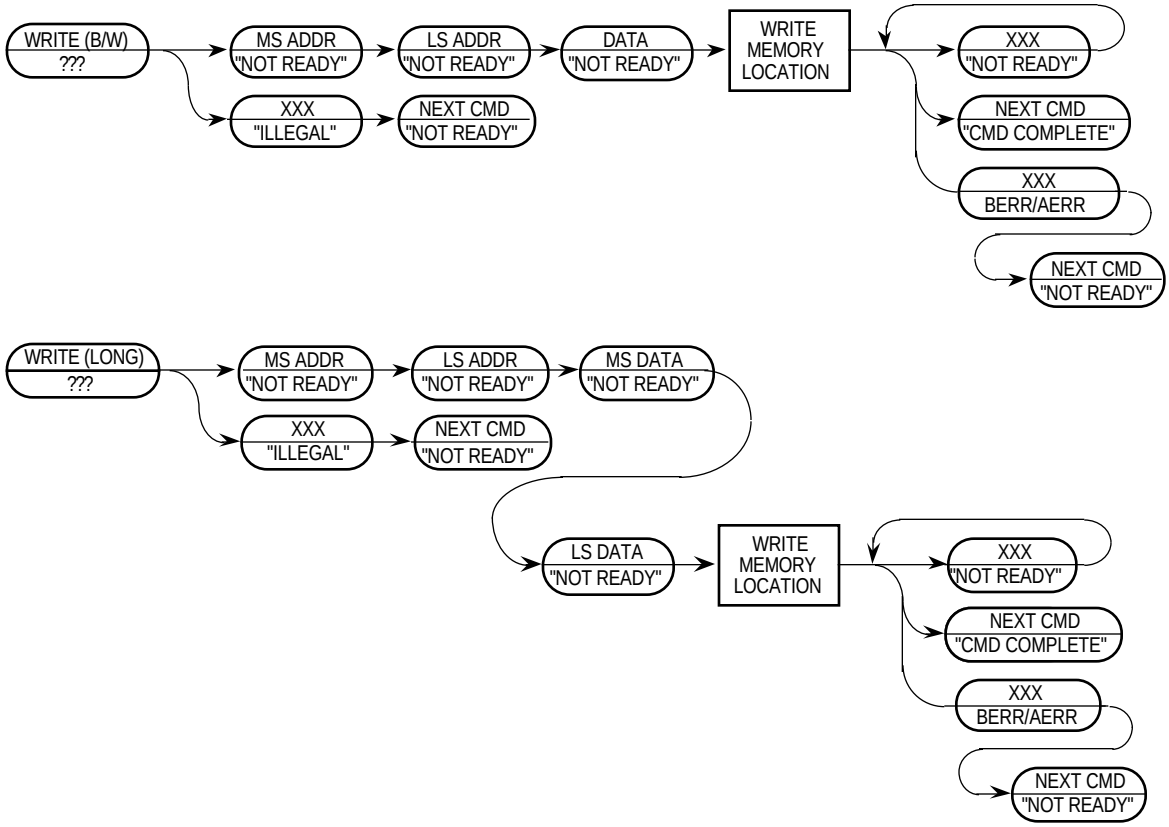
5.6.2.8.9 Write Memory Location (WRITE). Write the operand data to the memory location specified by the long-word address. The DFC register determines the address space accessed. Only absolute addressing is supported. Valid data sizes include byte, word, and long word.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	0	0	0	OP SIZE		0	0	0	0	0	0

Command Sequence:



Operand Data:

Two operands are required for this instruction. The first operand is a long-word absolute address that specifies a location to which the operand data is to be written. The second operand is the data. Byte data is transmitted as a 16-bit word, justified in the least significant byte; 16- and 32-bit operands are transmitted as 16 and 32 bits, respectively.

Result Data:

Successful write operations return a status of $0FFFF. Bus or address errors on the write cycle are indicated by the assertion of bit 16 in the status message and by a data pattern of $0001.

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5.6.2.8.10 Dump Memory Block (DUMP). DUMP is used in conjunction with the READ command to dump large blocks of memory. An initial READ is executed to set up the starting address of the block and to retrieve the first result. Subsequent operands are retrieved with the DUMP command. The initial address is incremented by the operand size (1, 2, or 4) and saved in a temporary register. Subsequent DUMP commands use this address, increment it by the current operand size, and store the updated address back in the temporary register.

NOTE

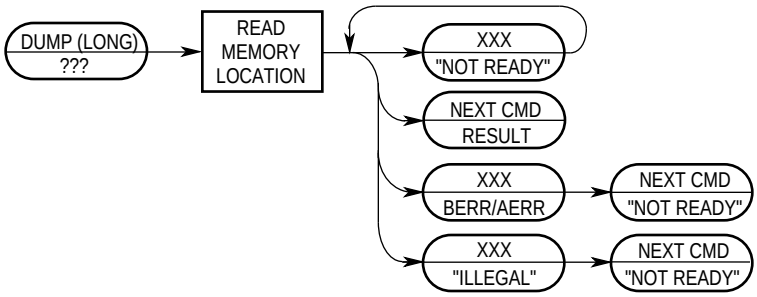
The DUMP command does not check for a valid address in the temporary register—DUMP is a valid command only when preceded by another DUMP or by a READ command. Otherwise, the results are undefined. The NOP command can be used for intercommand padding without corrupting the address pointer.

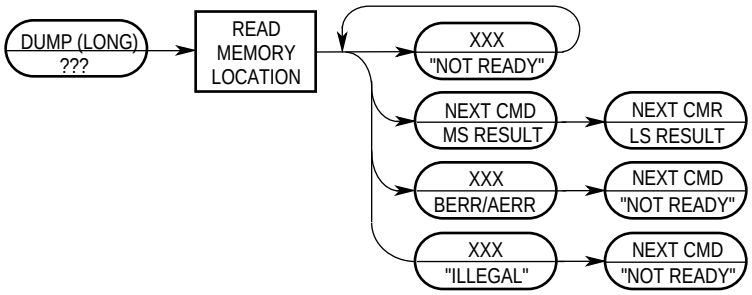
The size field is examined each time a DUMP command is given, allowing the operand size to be altered dynamically.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	1	OP SIZE		0	0	0	0	0	0

Command Sequence:





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Operand Data:

None

Result Data:

Requested data is returned as either a word or long word. Byte data is returned in the least significant byte of a word result. Word results return 16 bits of significant data; long-word results return 32 bits. Status of the read operation is returned as in the READ command: $0xxxx for success, $10001 for bus or address errors.

5.6.2.8.11 Fill Memory Block (FILL). FILL is used in conjunction with the WRITE command to fill large blocks of memory. An initial WRITE is executed to set up the starting address of the block and to supply the first operand. Subsequent operands are written with the FILL command. The initial address is incremented by the operand size (1, 2, or 4) and is saved in a temporary register. Subsequent FILL commands use this address, increment it by the current operand size, and store the updated address back in the temporary register.

NOTE

The FILL command does not check for a valid address in the temporary register—FILL is a valid command only when preceded by another FILL or by a WRITE command. Otherwise, the results are undefined. The NOP command can be used for intercommand padding without corrupting the address pointer.

The size field is examined each time a FILL command is given, allowing the operand size to be altered dynamically.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	1	1	0	0	OP SIZE		0	0	0	0	0	0

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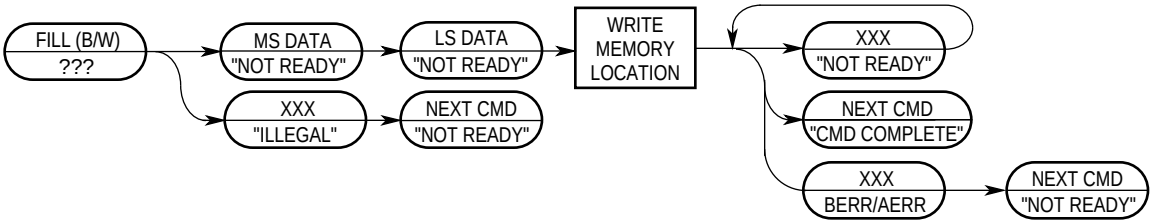
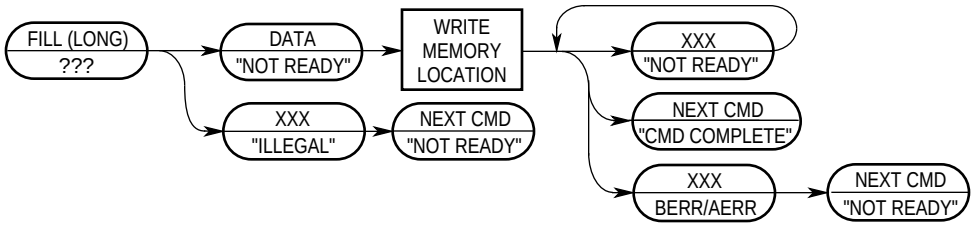
Command Sequence:





Operand Data:

A single operand is data to be written to the memory location. Byte data is transmitted as a 16-bit word, justified in the least significant byte; 16- and 32-bit operands are transmitted as 16 and 32 bits, respectively.

Result Data:

Status is returned as in the WRITE command: $0FFFF for a successful operation and $10001 for a bus or address error during write.

5.6.2.8.12 Resume Execution (GO). The pipeline is flushed and refilled before normal instruction execution is resumed. Prefetching begins at the return PC and current privilege level. If either the PC or SR is altered during BDM, the updated value of these registers is used when prefetching commences.

NOTE

The processor exits BDM when a bus error or address error occurs on the first instruction prefetch from the new PC—the error is trapped as a normal mode exception. The stacked value of the current PC may not be valid in this case, depending on the state of the machine prior to entering BDM. For address error, the PC does not reflect the true return PC. Instead, the stacked fault address is the (odd) return PC.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

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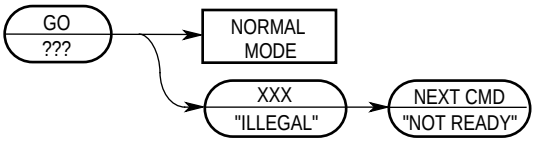
Command Sequence:



Operand Data:

None

Result Data:

None

5.6.2.8.13 Call User Code (CALL). This instruction provides a convenient way to patch user code. The return PC is stacked at the location pointed to by the current SP. The stacked PC serves as a return address to be restored by the RTS command that terminates the patch routine. After stacking is complete, the 32-bit operand data is loaded into the PC. The pipeline is flushed and refilled from the location pointed to by the new PC, BDM is exited, and normal mode instruction execution begins.

NOTE

If a bus error or address error occurs during return address stacking, the CPU returns an error status via the serial interface and remains in BDM.

If a bus error or address error occurs on the first instruction prefetch from the new PC, the processor exits BDM and the error is trapped as a normal mode exception. The stacked value of the current PC may not be valid in this case, depending on the state of the machine prior to entering BDM. For address error, the PC does not reflect the true return PC. Instead, the stacked fault address is the (odd) return PC.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0

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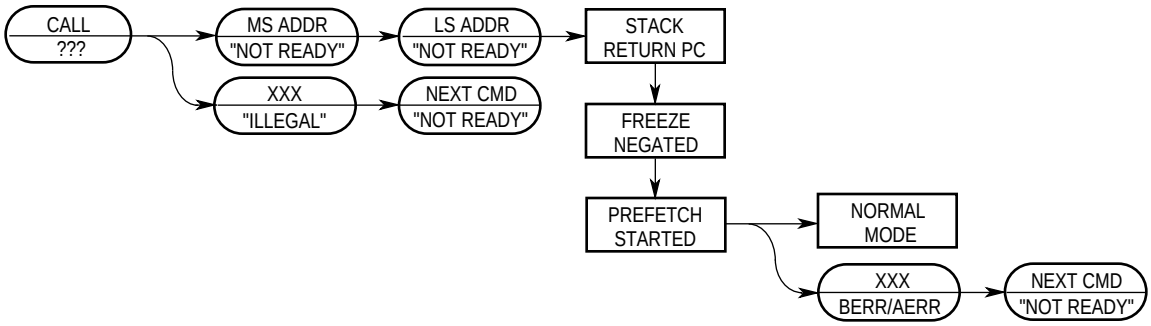
Command Sequence:



Operand Data:

The 32-bit operand data is the starting location of the patch routine, which is the initial PC upon exiting BDM.

Result Data:

None

As an example, consider the following code segment. It outputs a character from the MC68341 serial module channel A.

```
CHKSTAT:    MOVE.B    SRA,D0        Move serial status to D0
            BNE.B     CHKSTAT       Loop until condition true
            MOVE.B    TBA,OUTPUT    Transmit character


MISSING:    ANDI.B    #3,D0         Check for TxEMP flag
            RTS
```

BDM and the CALL command can be used to patch the code as follows:

1. Breakpoint user program at CHKSTAT
2. Enter BDM
3. Execute CALL command to MISSING
4. Exit BDM
5. Execute MISSING code
6. Return to user program

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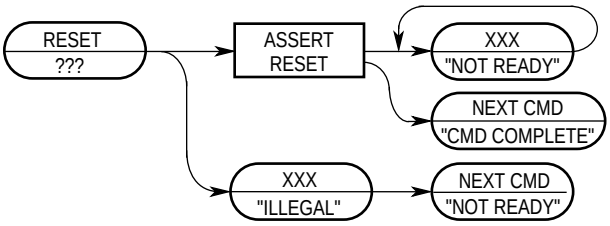
5.6.2.8.14 Reset Peripherals (RST). RST asserts $\overline{\text{RESET}}$ for 512 clock cycles. The CPU is not reset by this command. This command is synonymous with the CPU RESET instruction.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

Command Sequence:



Operand Data:

None

Result Data:

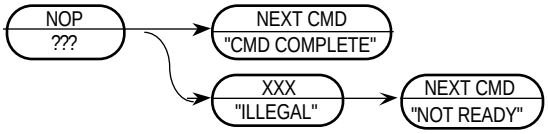
The “command complete” response ($0FFFF) is loaded into the serial shifter after negation of RESET.

5.6.2.8.15 No Operation (NOP). NOP performs no operation and may be used as a null command where required.

Command Format:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Command Sequence:



Operand Data:

None

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Result Data:

The “command complete” response ($0FFFF) is returned during the next shift operation.

5.6.2.8.16 Future Commands. Unassigned command opcodes are reserved by Motorola for future expansion. All unused Comand:formats within any revision level will perform a NOP and return the ILLEGAL command response.

5.6.3 Deterministic Opcode Tracking

The CPU32 utilizes deterministic opcode tracking to trace program execution. Two signals, $\overline{\text{IPIPE}}$ and $\overline{\text{IFETCH}}$, provide all information required to analyze instruction pipeline operation.

5.6.3.1 INSTRUCTION FETCH ($\overline{\text{IFETCH}}$). $\overline{\text{IFETCH}}$ indicates which bus cycles are accessing data to fill the instruction pipeline. $\overline{\text{IFETCH}}$ is pulse-width modulated to multiplex two indications on a single pin. Asserted for a single clock cycle, $\overline{\text{IFETCH}}$ indicates that the data from the current bus cycle is to be routed to the instruction pipeline. $\overline{\text{IFETCH}}$ held low for two clock cycles indicates that the instruction pipeline has been flushed. The data from the bus cycle is used to begin filling the empty pipeline. Both user and supervisor mode fetches are signaled by $\overline{\text{IFETCH}}$.

Proper tracking of bus cycles via $\overline{\text{IFETCH}}$ on a fast bus requires a simple state machine. On a two-clock bus, $\overline{\text{IFETCH}}$ may signal a pipeline flush with associated prefetch followed immediately by a second prefetch. That is, $\overline{\text{IFETCH}}$ remains asserted for three clocks, two clocks indicating the flush/fetch and a third clock signaling the second fetch. These two operations are easily discerned if the tracking logic samples $\overline{\text{IFETCH}}$ on the two rising edges of CLKOUT, which follow the $\overline{\text{AS}}$ ($\overline{\text{DS}}$ during show cycles) falling edge. Three-clock and slower bus cycles allow time for negation of the signal between consecutive indications and do not experience this operation.

5.6.3.2 INSTRUCTION PIPE ($\overline{\text{IPIPE}}$). The internal instruction pipeline can be modeled as a three-stage FIFO (see Figure 5-28). Stage A is an input buffer—data can be used out of stages B and C. $\overline{\text{IPIPE}}$ signals advances of instructions in the pipeline.

Instruction register A (IRA) holds incoming words as they are prefetched. No decoding takes place in the buffer. Instruction register B (IRB) provides initial decoding of the opcode and decoding of extension words; it is a source of immediate data. Instruction register C (IRC) supplies residual opcode decoding during instruction execution.

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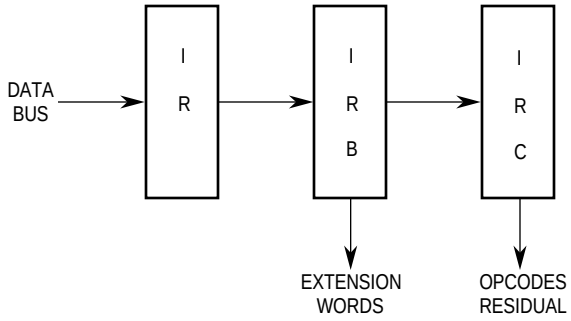

Figure 5-28. Functional Model of Instruction Pipeline

Assertion of $\overline{\text{IPIPE}}$ for a single clock cycle indicates the use of data from IRB. Regardless of the presence of valid data in IRA, the contents of IRB are invalidated when $\overline{\text{IPIPE}}$ is asserted. If IRA contains valid data, the data is copied into IRB (IRA ⇒ IRB), and the IRB stage is revalidated.

Assertion of $\overline{\text{IPIPE}}$ for two clock cycles indicates the start of a new instruction and subsequent replacement of data in IRC. This action causes a full advance of the pipeline (IRB ⇒ IRC and IRA ⇒ IRB). IRA is refilled during the next instruction fetch bus cycle.

Data loaded into IRA propagates automatically through subsequent empty pipeline stages. Signals that show the progress of instructions through IRB and IRC are necessary to accurately monitor pipeline operation. These signals are provided by IRA and IRB validity bits. When a pipeline advance occurs, the validity bit of the stage being loaded is set, and the validity bit of the stage supplying the data is negated.

Because instruction execution is not timed to bus activity, $\overline{\text{IPIPE}}$ is synchronized with the system clock, not the bus. Figure 5-29 illustrates the timing in relation to the system clock.

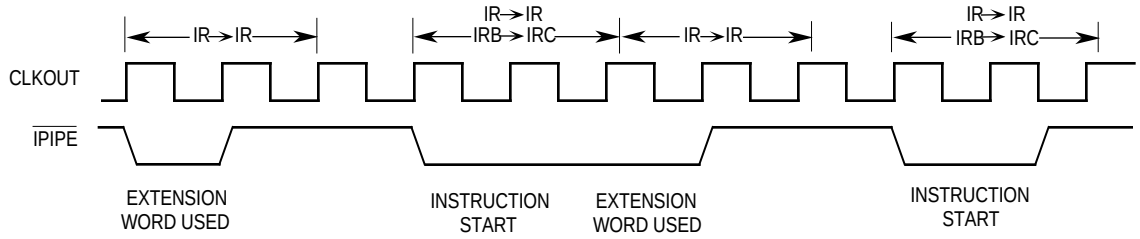

Figure 5-29. Instruction Pipeline Timing Diagram

$\overline{\text{IPIPE}}$ should be sampled on the falling edge of the clock. The assertion of $\overline{\text{IPIPE}}$ for a single cycle after one or more cycles of negation indicates use of the data in IRB (advance of IRA into IRB). Assertion for two clock cycles indicates that a new instruction has started (IRB ⇒ IRC and IRA ⇒ IRB transfers have occurred). Loading IRC always indicates that an instruction is beginning execution—the opcode is loaded into IRC by the transfer.

In some cases, instructions using immediate addressing begin executing and initiate a second pipeline advance simultaneously at the same time. $\overline{\text{IPIPE}}$ will not be negated

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between the two indications, which implies the need for a state machine to track the state of $\overline{\text{IPIPE}}$. The state machine can be resynchronized during periods of inactivity on the signal.

5.6.3.3 OPCODE TRACKING DURING LOOP MODE. $\overline{\text{IPIPE}}$ and $\overline{\text{IFETCH}}$ continue to work normally during loop mode. $\overline{\text{IFETCH}}$ indicates all instruction fetches up through the point that data begins recirculating within the instruction pipeline. $\overline{\text{IPIPE}}$ continues to signal the start of instructions and the use of extension words even though data is being recirculated internally. $\overline{\text{IFETCH}}$ returns to normal operation with the first fetch after exiting loop mode.

5.7 INSTRUCTION EXECUTION TIMING

This section describes the instruction execution timing of the CPU32. External clock cycles are used to provide accurate execution and operation timing guidelines, but not exact timing for every possible circumstance. This approach is used because exact execution time for an instruction or operation depends on concurrence of independently scheduled resources, on memory speeds, and on other variables.

An assembly language programmer or compiler writer can use the information in this section to predict the performance of the CPU32. Additionally, timing for exception processing is included so that designers of multitasking or real-time systems can predict task-switch overhead, maximum interrupt latency, and similar timing parameters. Instruction timing is given in clock cycles to eliminate clock frequency dependency.

5.7.1 Resource Scheduling

The CPU32 contains several independently scheduled resources. The organization of these resources within the CPU32 is shown in Figure 5-30. Some variation in instruction execution timing results from concurrent resource utilization. Because resource scheduling is not directly related to instruction boundaries, it is impossible to make an accurate prediction of the time required to complete an instruction without knowing the entire context within which the instruction is executing.

5.7.1.1 MICROSEQUENCER. The microsequencer either executes microinstructions or awaits completion of accesses necessary to continue microcode execution. The microsequencer supervises the bus controller, instruction execution, and internal processor operations such as calculation of EA and setting of condition codes. It also initiates instruction word prefetches after a change of flow and controls validation of instruction words in the instruction pipeline.

5.7.1.2 INSTRUCTION PIPELINE. The CPU32 contains a two-word instruction pipeline where instruction opcodes are decoded. Each stage of the pipeline is initially filled under microsequencer control and subsequently refilled by the prefetch controller as it empties.

Stage A of the instruction pipeline is a buffer. Prefetches completed on the bus before stage B empties are temporarily stored in this buffer. Instruction words (instruction

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operation words and all extension words) are decoded at stage B. Residual decoding and execution occur in stage C.

Each pipeline stage has an associated status bit that shows whether the word in that stage was loaded with data from a bus cycle that terminated abnormally.

5.7.1.3 BUS CONTROLLER RESOURCES. The bus controller consists of the instruction prefetch controller, the write pending buffer, and the microbus controller. These three resources transact all reads, writes, and instruction prefetches required for instruction execution.

The bus controller and microsequencer operate concurrently. The bus controller can perform a read or write or schedule a prefetch while the microsequencer controls EA calculation or sets condition codes.

The microsequencer can also request a bus cycle that the bus controller cannot perform immediately. When this happens, the bus cycle is queued, and the bus controller runs the cycle when the current cycle has completed.

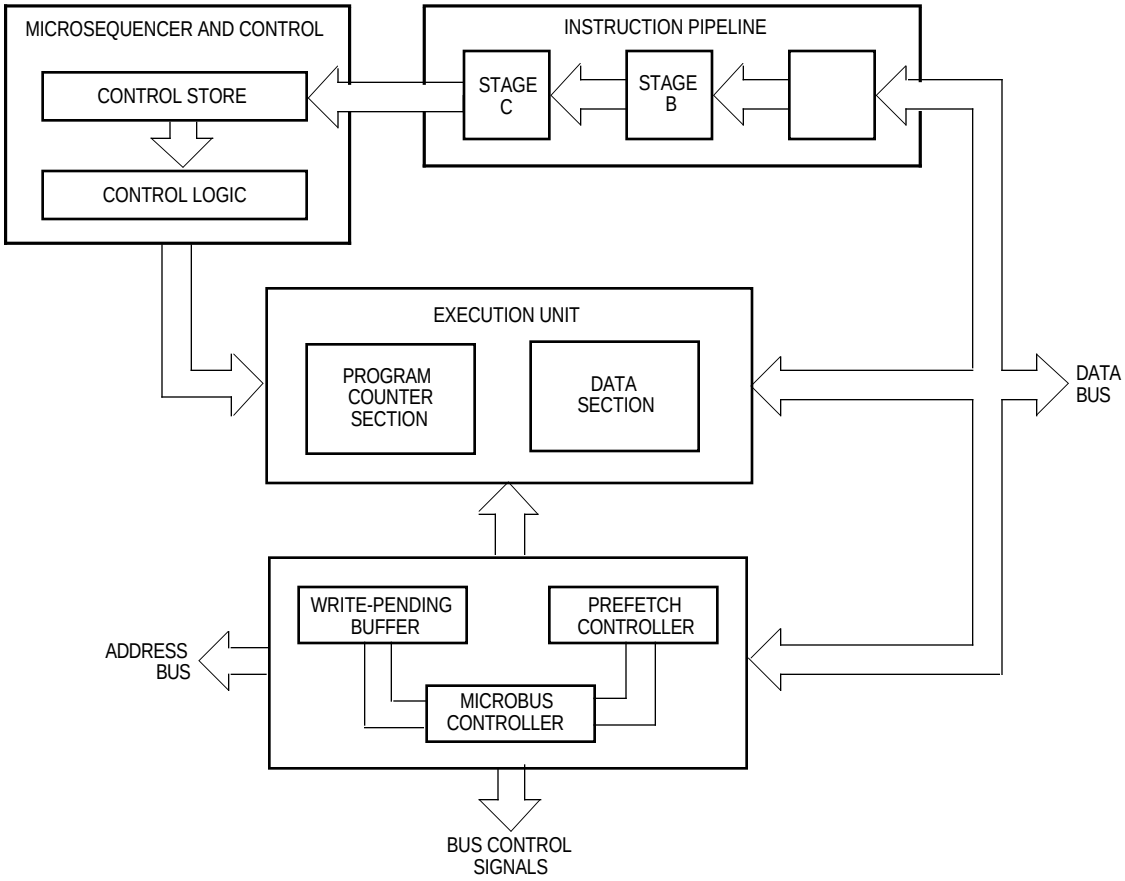

Figure 5-30. Block Diagram of Independent Resources

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5.7.1.3.1 Prefetch Controller. The instruction prefetch controller receives an initial request from the microsequencer to initiate prefetching at a given address. Subsequent prefetches are initiated by the prefetch controller whenever a pipeline stage is invalidated, either through instruction completion or through use of extension words. Prefetch occurs as soon as the bus is free of operand accesses previously requested by the microsequencer. Additional state information permits the controller to inhibit prefetch requests when a change in instruction flow (e.g., a jump or branch instruction) is anticipated.

In a typical program, 10 to 25 percent of the instructions cause a change of flow. Each time a change occurs, the instruction pipeline must be flushed and refilled from the new instruction stream. If instruction prefetches, rather than operand accesses, were given priority, many instruction words would be flushed unused, and necessary operand cycles would be delayed. To maximize available bus bandwidth, the CPU32 will schedule a prefetch only when the next instruction is not a change-of-flow instruction and when there is room in the pipeline for the prefetch.

5.7.1.3.2 Write-Pending Buffer. The CPU32 incorporates a single-operand write-pending buffer. The buffer permits the microsequencer to continue execution after a request for a write cycle is queued in the bus controller. The time needed for a write at the end of an instruction can overlap the head cycle time for the following instruction, thus reducing overall execution time. Interlocks prevent the microsequencer from overwriting the buffer.

5.7.1.3.3 Microbus Controller. The microbus controller performs bus cycles issued by the microsequencer. Operand accesses always have priority over instruction prefetches. Word and byte operands are accessed in a single CPU-initiated bus cycle, although the external bus interface may be required to initiate a second cycle when a word operand is sent to a byte-sized external port. Long operands are accessed in two bus cycles, most significant word first.

The instruction pipeline is capable of recognizing instructions that cause a change of flow. It informs the bus controller when a change of flow is imminent, and the bus controller refrains from starting prefetches that would be discarded due to the change of flow.

5.7.1.4 INSTRUCTION EXECUTION OVERLAP. Overlap is the time, measured in clock cycles, that an instruction executes concurrently with the previous instruction. As shown in Figure 5-31, portions of instructions A and B execute simultaneously, reducing total execution time. Because portions of instructions B and C also overlap, overall execution time for all three instructions is also reduced.

Each instruction contributes to the total overlap time. The portion of execution time at the end of instruction A that can overlap the beginning of instruction B is called the tail of instruction A. The portion of execution time at the beginning of instruction B that can overlap the end of instruction A is called the head of instruction B. The total overlap time between instructions A and B is the smaller tail of A and the head of B.

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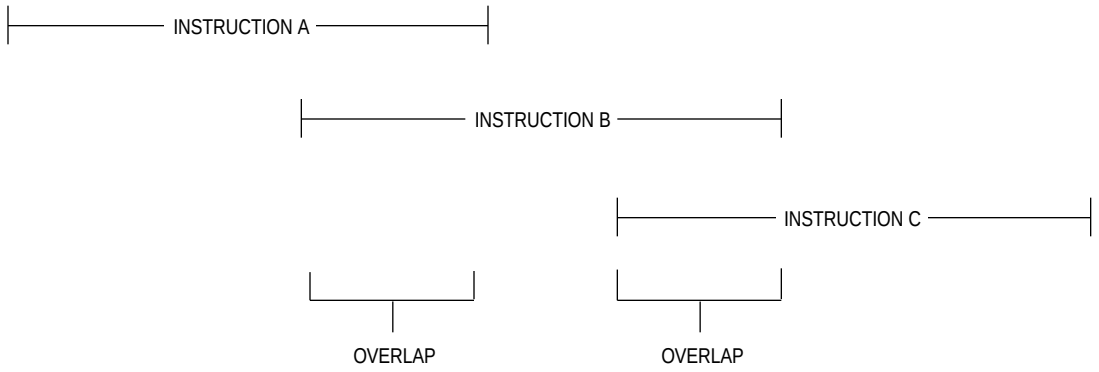

Figure 5-31. Simultaneous Instruction Execution

The execution time attributed to instructions A, B, and C after considering the overlap is illustrated in Figure 5-32. The overlap time is attributed to the execution time of the completing instruction. The following equation shows the method for calculating the overlap time:

$$\text{Overlap} = \min\left(\text{Tail}_N, \text{Head}_{N+1}\right)$$

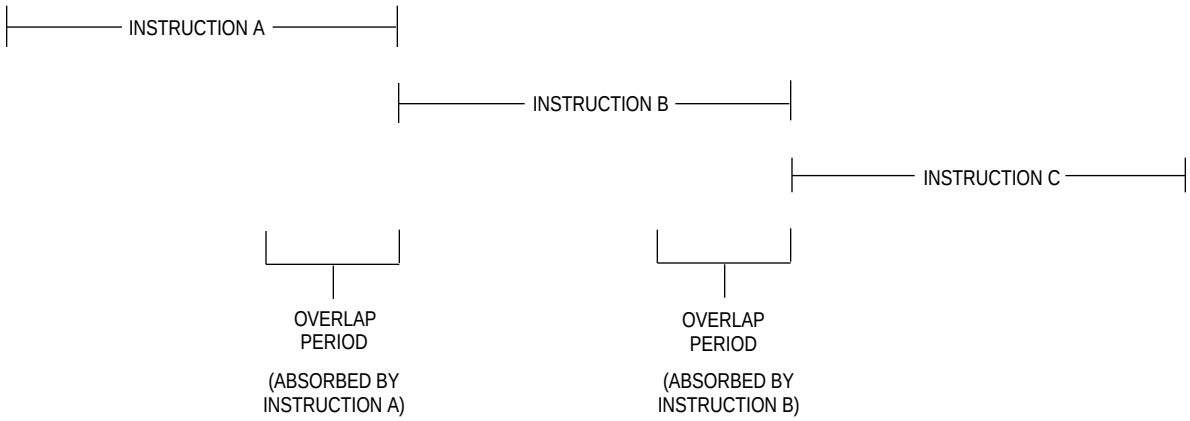

Figure 5-32. Attributed Instruction Times

5.7.1.5 EFFECTS OF WAIT STATES. The CPU32 access time for on-chip peripherals is two clocks. While two-clock external accesses are possible when the bus is operated in a synchronous mode, a typical external memory speed is three or more clocks.

All instruction times listed in this section are for word access only (unless an explicit exception is given), and are based on the assumption that both instruction fetches and operand cycles are to a two-clock memory. Any time a long access is made, time for the additional bus cycle(s) must be added to the overall execution time. Wait states due to slow external memory must be added to the access time for each bus cycle.

A typical application has a mixture of bus speeds—program execution from an off-chip ROM, accesses to on-chip peripherals, storage of variables in slow off-chip RAM, and accesses to external peripherals with speeds ranging from moderate to very slow. To arrive at an accurate instruction time calculation, each bus access must be individually

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considered. Many instructions have a head cycle count, which can overlap the cycles of an operand fetch to slower memory started by a previous instruction. In these cases, an increase in access time has no effect on the total execution time of the pair of instructions.

To trace instruction execution time by monitoring the external bus, note that the order of operand accesses for a particular instruction sequence is always the same provided bus speed is unchanged and the interleaving of instruction prefetches with operands within each sequence is identical.

5.7.1.6 INSTRUCTION EXECUTION TIME CALCULATION. The overall execution time for an instruction depends on the amount of overlap with previous and subsequent instructions. To calculate an instruction time estimate, the entire code sequence must be analyzed. To derive the actual instruction execution times for an instruction sequence, the instruction times listed in the tables must be adjusted to account for overlap.

The formula for this calculation is as follows:

$$C_1 - \min(T_1, H_2) + C_2 - \min(T_2, H_3) + C_3 - \min(T_3, H_4) + \ldots\ldots$$

where:

C_N is the number of cycles listed for instruction N

T_N is the tail time for instruction N

H_N is the head time for instruction N

$\min(T_N, H_M)$ is the minimum of parameters T_N and H_M

The number of cycles for the instruction (C_N) can include one or two EA calculations in addition to the raw number in the cycles column. In these cases, calculate overall instruction time as if it were for multiple instructions, using the following equation:

$$\langle CEA \rangle - \min(T_{EA}, H_{OP}) + C_{OP}$$

where:

$\langle CEA \rangle$ is the instruction's EA time

C_{OP} is the instruction's operation time

T_{EA} is the EA's tail time

H_{OP} is the instruction operation's head time

$\min(T_N, H_M)$ is the minimum of parameters T_N and H_M

The overall head for the instruction is the head for the EA, and the overall tail for the instruction is the tail for the operation. Therefore, the actual equation for execution time becomes:

$$C_{OP1} - \min(T_{OP1}, H_{EA2}) + \langle CEA \rangle_2 - \min(T_{EA2}, H_{OP2}) + C_{OP2} - \min(T_{OP2}, H_{EA3}) + \ldots$$

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Every instruction must prefetch to replace itself in the instruction pipe. Usually, these prefetches occur during or after an instruction. A prefetch is permitted to begin in the first clock of any indexed EA mode operation.

Additionally, a prefetch for an instruction is permitted to begin two clocks before the end of an instruction provided the bus is not being used. If the bus is being used, then the prefetch occurs at the next available time when the bus would otherwise be idle.

5.7.1.7 EFFECTS OF NEGATIVE TAILS. When the CPU32 changes instruction flow, the instruction decode pipeline must begin refilling before instruction execution can resume. Refilling forces a two-clock idle period at the end of the change-of-flow instruction. This idle period can be used to prefetch an additional word on the new instruction path. Because of the stipulation that each instruction must prefetch to replace itself, the concept of negative tails has been introduced to account for these free clocks on the bus.

On a two-clock bus, it is not necessary to adjust instruction timing to account for the potential extra prefetch. The cycle times of the microsequencer and bus are matched, and no additional benefit or penalty is obtained. In the instruction execution time equations, a zero should be used instead of a negative number.

Negative tails are used to adjust for slower fetches on slower buses. Normally, increasing the length of prefetch bus cycles directly affects the cycle count and tail values found in the tables.

In the following equations, negative tail values are used to negate the effects of a slower bus. The equations are generalized, however, so that they may be used on any speed bus with any tail value.

```
NEW_TAIL = OLD_TAIL + (NEW_CLOCK – 2)
IF ((NEW_CLOCK – 4) > 0) THEN
    NEW_CYCLE = OLD_CYCLE + (NEW_CLOCK -2) + (NEW_CLOCK – 4)
ELSE
    NEW_CYCLE = OLD_CYCLE + (NEW _CLOCK – 2)
```

where:

NEW_TAIL/NEW_CYCLE is the adjusted tail/cycle at the slower speed

OLD_TAIL/OLD_CYCLE is the value listed in the instruction timing tables

NEW_CLOCK is the number of clocks per cycle at the slower speed

Note that many instructions listed as having negative tails are change-of-flow instructions and that the bus speed used in the calculation is that of the new instruction stream.

5.7.2 Instruction Stream Timing Examples

The following programming examples provide a detailed examination of timing effects. In all examples, the memory access is from external synchronous memory, the bus is idle, and the instruction pipeline is full at the start.

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5.7.2.1 TIMING EXAMPLE 1—EXECUTION OVERLAP. Figure 5-33 illustrates execution overlap caused by the bus controller's completion of bus cycles while the sequencer is calculating the next EA. One clock is saved between instructions since that is the minimum time of the individual head and tail numbers.

Instructions

```
MOVE.W    A1, (A0) +
ADDQ.W    #1, (A0)
CLR.W     $30 (A1)
```

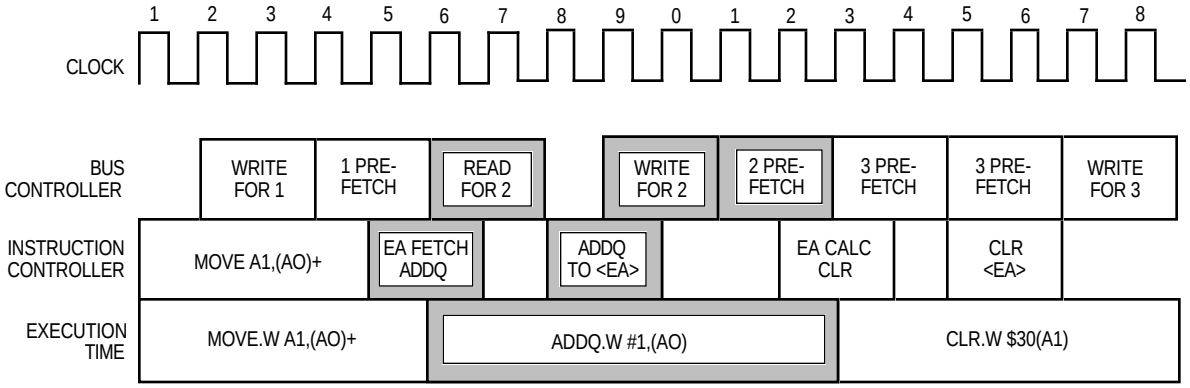

Figure 5-33. Example 1—Instruction Stream

5.7.2.2 TIMING EXAMPLE 2—BRANCH INSTRUCTIONS. Example 2 shows what happens when a branch instruction is executed for both the taken and not-taken cases. (see Figures 5-34 and 5-35). The instruction stream is for a simple limit check with the variable already in a data register.

Instructions

```
MOVEQ     #7, D1
CMP.L     D1, D0
BLE.B     NEXT
MOVE.L    D1, (A0)
```

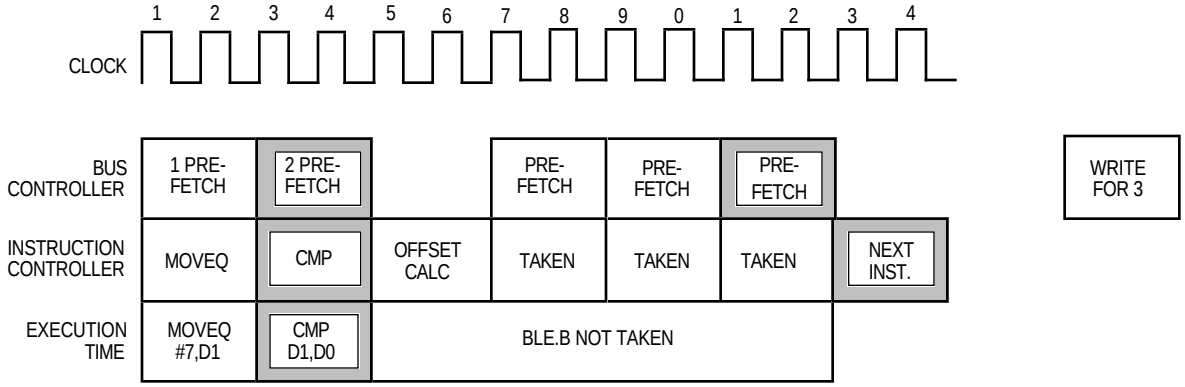

Figure 5-34. Example 2—Branch Taken

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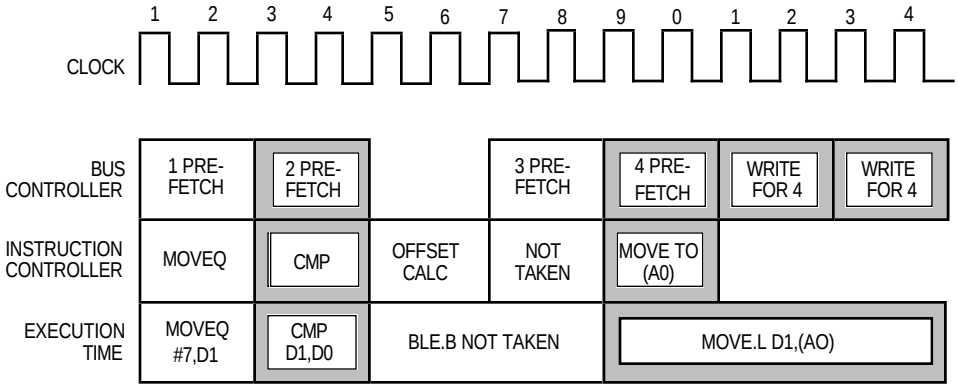

Figure 5-35. Example 2—Branch Not Taken

5.7.2.3 TIMING EXAMPLE 3—NEGATIVE TAILS. This example (see Figure 5-36) shows how to use negative tail figures for branches and other change-of-flow instructions. In this example, bus speed is assumed to be four clocks per access. Instruction three is at the branch destination.

Although the CPU32 has a two-word instruction pipeline, internal delay causes minimum branch instruction time to be three bus cycles. The negative tail is a reminder that an extra two clocks are available for prefetching a third word on a fast bus; on a slower bus, there is no extra time for the third word.

Instructions

MOVEQ	#7, D1
BRA.W	FARAWAY
MOVE.L	D1, D0

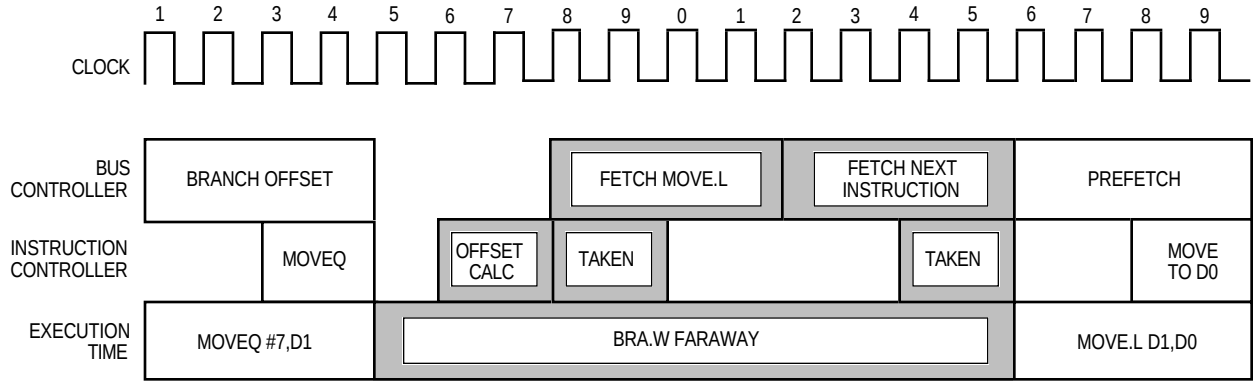

Figure 5-36. Example 3—Branch Negative Tail

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Example 3 illustrates three different aspects of instruction time calculation:

1. The branch instruction does not attempt to prefetch beyond the minimum number of words needed for itself.
2. The negative tail allows execution to begin sooner than a three-word pipeline would allow.
3. There is a one-clock delay due to late arrival of the displacement at the CPU.

Only changes of flow require negative tail calculation, but the concept can be generalized to any instruction—only two words are required to be in the pipeline, but up to three words may be present. When there is an opportunity for an extra prefetch, it is made. A prefetch to replace an instruction can begin ahead of the instruction, resulting in a faster processor.

5.7.3 Instruction Timing Tables

The following assumptions apply to the times shown in the subsequent tables:

1. A 16-bit data bus is used for all memory accesses.
2. Memory access times are based on two clock bus cycles with no wait states.
3. The instruction pipeline is full at the beginning of the instruction and is refilled by the end of the instruction.

Three values are listed for each instruction and addressing mode:

Head: The number of cycles available at the beginning of an instruction to complete a previous instruction write or to perform a prefetch.

Tail: The number of cycles an instruction uses to complete a write.

Cycles: Four numbers per entry, three contained in parentheses. The outer number is the minimum number of cycles required for the instruction to complete. Numbers within the parentheses represent the number of bus accesses performed by the instruction. The first number is the number of operand read accesses performed by the instruction. The second number is the number of instruction fetches performed by the instruction, including all prefetches that keep the instruction and the instruction pipeline filled. The third number is the number of write accesses performed by the instruction.

As an example, consider an ADD.L (12, A3, D7.W ∗ 4), D2 instruction.

Paragraph **5.7.3.5 Arithmetic/Logic Instructions** shows that the instruction has a head = 0, a tail = 0, and cycles = 2 (0/1/0). However, in indexed address register indirect addressing mode, additional time is required to fetch the EA. Paragraph **5.7.3.1 Fetch Effective Address** gives addressing mode data. For (d_8, An, Xn.Sz ∗ Scale), head = 4, tail = 2, cycles = 8 (2/1/0). Because this example is for a long access and the fetch EA table lists data for word accesses, add two clocks to the tail and to the number of cycles (“X” in table notation) to obtain head = 4, tail = 4, cycles = 10 (2/1/0).

Assuming that no trailing write exists from the previous instruction, EA calculation requires six clocks. Replacement fetch for the EA occurs during these six clocks, leaving a head of

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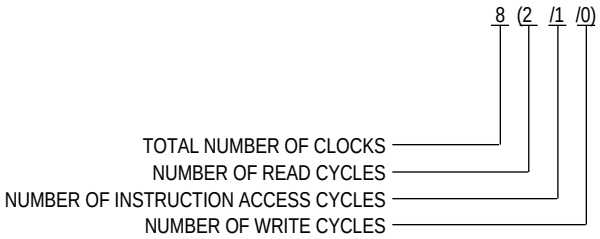
four. If there is no time in the head to perform a prefetch due to a previous trailing write, then additional time to perform the prefetches must be allotted in the middle of the instruction or after the tail.



The total number of clocks for bus activity is as follows:

$$(2 \text{ Reads} \times 2 \text{ Clocks/Read}) + (1 \text{ Instruction Access} \times 2 \text{ Clocks/Access}) + (0 \text{ Writes} \times 2 \text{ Clocks/Write}) = 6 \text{ Clocks of Bus Activity}$$

The number of internal clocks (not overlapped by bus activity) is as follows:

$$10 \text{ Clocks Total} - 6 \text{ Clocks Bus Activity} = 4 \text{ Internal Clocks}$$

Memory read requires two bus cycles at two clocks each. This read time, implied in the tail figure for the EA, cannot be overlapped with the instruction because the instruction has a head of zero. An additional two clocks are required for the ADD instruction itself. The total is $6 + 4 + 2 = 12$ clocks. If bus cycles take more time (i.e., the memory is off-chip), add an appropriate number of clocks to each memory access.

The instruction sequence MOVE.L D0, (A0) followed by LSL.L #7, D2 provides an example of overlapped execution. The MOVE instruction has a head of zero and a tail of four because it is a long write. The LSL instruction has a head of four. The trailing write from the MOVE overlaps the LSL head completely. Thus, the two-instruction sequence has a head of zero and a tail of zero, and a total execution of 8 rather than 12 clocks.

General observations regarding calculation of execution time are as follows:

- Any time the number of bus cycles is listed as "X", substitute a value of one for byte and word cycles and a value of two for long cycles. For long bus cycles, usually add a value of two to the tail.
- The time calculated for an instruction on a three-clock (or longer) bus is usually longer than the actual execution time. All times shown are for two-clock bus cycles.
- If the previous instruction has a negative tail, then a prefetch for the current instruction can begin during the execution of that previous instruction.
- Certain instructions requiring an immediate extension word (immediate word EA, absolute word EA, address register indirect with displacement EA, conditional branches with word offsets, bit operations, LPSTOP, TBL, MOVEM, MOVEC, MOVES, MOVEP, MUL.L, DIV.L, CHK2, CMP2, and DBcc) are not permitted to begin until the extension word has been in the instruction pipeline for at least one cycle. This does not apply to long offsets or displacements.

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5.7.3.1 FETCH EFFECTIVE ADDRESS. The fetch EA table indicates the number of clock periods needed for the processor to calculate and fetch the specified EA. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction	Head	Tail	Cycles	Notes
Dn	–	–	0(0/0/0)	–
An	–	–	0(0/0/0)	–
(An)	1	1	3(X/0/0)	1
(An)+	1	1	3(X/0/0)	1
–(An)	2	2	4(X/0/0)	1
(d_{16},An) or (d_{16},PC)	1	3	5(X/1/0)	1,3
(xxx).W	1	3	5(X/1/0)	1
(xxx).L	1	5	7(X/2/0)	1
#⟨data⟩.B	1	1	3(0/1/0)	1
#⟨data⟩.W	1	1	3(0/1/0)	1
#⟨data⟩.L	1	3	5(0/2/0)	1
(d_8,An,Xn.Sz × Sc) or (d_8,PC,Xn.Sz × Sc)	4	2	8(X/1/0)	1,2,3,4
(0) (All Suppressed)	2	2	6(X/1/0)	1,4
(d_{16})	1	3	7(X/2/0)	1,4
(d_{32})	1	5	9(X/3/0)	1,4
(An)	1	1	5(X/1/0)	1,2,4
(Xm.Sz × Sc)	4	2	8(X/1/0)	1,2,4
(An,Xm.Sz × Sc)	4	2	8(X/1/0)	1,2,3,4
(d_{16},An) or (d_{16},PC)	1	3	7(X/2/0)	1,3,4
(d_{32},An) or (d_{32},PC)	1	5	9(X/3/0)	1,3,4
(d_{16},An,Xm) or (d_{16},PC,Xm)	2	2	8(X/2/0)	1,3,4
(d_{32},An,Xm) or (d_{32},PC,Xm)	1	3	9(X/3/0)	1,3,4
(d_{16},An,Xm.Sz × Sc) or (d_{16},PC,Xm.Sz × Sc)	2	2	8(X/2/0)	1,2,3,4
(d_{32},An,Xm.Sz × Sc) or (d_{32},PC,Xm.Sz × Sc)	1	3	9(X/3/0)	1,2,3,4

X = There is one bus cycle for byte and word operands and two bus cycles for long-word operands. For long-word bus cycles, add two clocks to the tail and to the number of cycles.

NOTES:

1. The read of the EA and replacement fetches overlap the head of the operation by the amount specified in the tail.
2. Size and scale of the index register do not affect execution time.
3. The PC may be substituted for the base address register An.
4. When adjusting the prefetch time for slower buses, extra clocks may be subtracted from the head until the head reaches zero, at which time additional clocks must be added to both the tail and cycle counts.

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5.7.3.2 CALCULATE EFFECTIVE ADDRESS. The calculate EA table indicates the number of clock periods needed for the processor to calculate a specified EA. The timing is equivalent to fetch EA except there is no read cycle. The tail and cycle time are reduced by the amount of time the read would occupy. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction	Head	Tail	Cycles	Notes
Dn	–	–	0(0/0/0)	–
An	–	–	0(0/0/0)	–
(An)	1	0	2(0/0/0)	–
(An)+	1	0	2(0/0/0)	–
–(An)	2	0	2(0/0/0)	–
(d_{16},An) or (d_{16},PC)	1	1	3(0/1/0)	1,3
(xxx).W	1	1	3(0/1/0)	1
(xxx).L	1	3	5(0/2/0)	1
(d_8,An,Xn.Sz × Sc) or (d_8,PC,Xn.Sz × Sc)	4	0	6(0/1/0)	2,3,4
(0) (All Suppressed)	2	0	4(0/1/0)	4
(d_{16})	1	1	5(0/2/0)	1,4
(d_{32})	1	3	7(0/3/0)	1,4
(An)	1	0	4(0/1/0)	4
(Xm.Sz × Sc)	4	0	6(0/1/0)	2,4
(An,Xm.Sz × Sc)	4	0	6(0/1/0)	2,4
(d_{16},An) or (d_{16},PC)	1	1	5(0/2/0)	1,3,4
(d_{32},An) or (d_{32},PC)	1	3	7(0/3/0)	1,3,4
(d_{16},An,Xm) or (d_{16},PC,Xm)	2	0	6(0/2/0)	3,4
(d_{32},An,Xm) or (d_{32},PC,Xm)	1	1	7(0/3/0)	1,3,4
(d_{16},An,Xm.Sz × Sc) or (d_{16},PC,Xm.Sz × Sc)	2	0	6(0/2/0)	2,3,4
(d_{32},An,Xm.Sz × Sc) or (d_{32},PC,Xm.Sz × Sc)	1	1	7(0/3/0)	1,2,3,4

X = There is one bus cycle for byte and word operands and two bus cycles for long operands.
For long bus cycles, add two clocks to the tail and to the number of cycles.

NOTES:

1. Replacement fetches overlap the head of the operation by the amount specified in the tail.
2. Size and scale of the index register do not affect execution time.
3. The PC may be substituted for the base address register An.
4. When adjusting the prefetch time for slower buses, extra clocks may be subtracted from the head until the head reaches zero, at which time additional clocks must be added to both the tail and cycle counts.

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5.7.3.3 MOVE INSTRUCTION. The MOVE instruction table indicates the number of clock periods needed for the processor to calculate the destination EA and to perform a MOVE or MOVEA instruction. For entries with CEA or FEA, refer to the appropriate table to calculate that portion of the instruction time.

Destination EAs are divided by their formats (see **5.3.4.4 Effective Address Encoding Summary**). The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

When using this table, begin at the top and move downward. Use the first entry that matches both source and destination addressing modes.

Instruction	Head	Tail	Cycles
MOVE Rn, Rn	0	0	2(0/1/0)
MOVE ⟨FEA⟩, Rn	0	0	2(0/1/0)
MOVE Rn, (Am)	0	2	4(0/1/x)
MOVE Rn, (Am)+	1	1	5(0/1/x)
MOVE Rn, –(Am)	2	2	6(0/1/x)
MOVE Rn, ⟨CEA⟩	1	3	5(0/1/x)
MOVE ⟨FEA⟩, (An)	2	2	6(0/1/x)
MOVE ⟨FEA⟩, (An)+	2	2	6(0/1/x)
MOVE ⟨FEA⟩, –(An)	2	2	6(0/1/x)
MOVE #, ⟨CEA⟩	2	2	6(0/1/x)*
MOVE ⟨CEA⟩, ⟨FEA⟩	2	2	6(0/1/x)

X = There is one bus cycle for byte and word operands and two bus cycles for long-word operands. For long-word bus cycles, add two clocks to the tail and to the number of cycles.

* = An # fetch EA time must be added for this instruction: ⟨FEA⟩+⟨CEA⟩+⟨OPER⟩

NOTE: For instructions not explicitly listed, use the MOVE ⟨CEA⟩, ⟨FEA⟩ entry. The source EA is calculated by the calculate EA table, and the destination EA is calculated by the fetch EA table, even though the bus cycle is for the source EA.

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5.7.3.4 SPECIAL-PURPOSE MOVE INSTRUCTION. The special-purpose MOVE instruction table indicates the number of clock periods needed for the processor to fetch, calculate, and perform the special-purpose MOVE operation on control registers or a specified EA. Footnotes indicate when to account for the appropriate EA times. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction		Head	Tail	Cycles
EXG	Rn, Rm	2	0	4(0/1/0)
MOVEC	Cr, Rn	10	0	14(0/2/0)
MOVEC	Rn, Cr	12	0	14-16(0/1/0)
MOVE	CCR, Dn	2	0	4(0/1/0)
MOVE	CCR, ⟨CEA⟩	0	2	4(0/1/1)
MOVE	Dn, CCR	2	0	4(0/1/0)
MOVE	⟨FEA⟩, CCR	0	0	4(0/1/0)
MOVE	SR, Dn	2	0	4(0/1/0)
MOVE	SR, ⟨CEA⟩	0	2	4(0/1/1)
MOVE	Dn, SR	4	–2	10(0/3/0)
MOVE	⟨FEA⟩, SR	0	–2	10(0/3/0)
MOVEM.W	⟨CEA⟩, RL	1	0	$8 + n \times 4$ (n + 1, 2, 0) *
MOVEM.W	RL, ⟨CEA⟩	1	0	$8 + n \times 4$ (0, 2, n) *
MOVEM.L	⟨CEA⟩, RL	1	0	$12 + n \times 4$(2n + 2, 2, 0)
MOVEM.L	RL, ⟨CEA⟩	1	2	$10 + n \times 4$ (0, 2, 2n)
MOVEP.W	Dn, (d_{16}, An)	2	0	10(0/2/2)
MOVEP.W	(d_{16}, An), Dn	1	2	11(2/2/0)
MOVEP.L	Dn, (d_{16}, An)	2	0	14(0/2/4)
MOVEP.L	(d_{16}, An), Dn	1	2	19(4/2/0)
MOVES (Save)	⟨CEA⟩, Rn	1	1	3(0/1/0)
MOVES (Op)	⟨CEA⟩, Rn	7	1	11(X/1/0)
MOVES (Save)	Rn, ⟨CEA⟩	1	1	3(0/1/0)
MOVES (Op)	Rn, ⟨CEA⟩	9	2	12(0/1/X)
MOVE	USP, An	0	0	2(0/1/0)
MOVE	An, USP	0	0	2(0/1/0)
SWAP	Dn	4	0	6(0/1/0)

X = There is one bus cycle for byte and word operands and two bus cycles for long operands. For long bus cycles, add two clocks to the tail and to the number of cycles.

* = Each bus cycle may take up to four clocks without increasing total execution time.

Cr = Control registers USP, VBR, SFC, and DFC

n = Number of registers to transfer

RL = Register List

< = Maximum time (certain data or mode combinations may execute faster).

NOTE: The MOVES instruction has an additional save step that other instructions do not have. To calculate the total instruction time, calculate the save, the EA, and the operation execution times, and combine in the order listed, using the equations given in **5.7.1.6 Instruction Execution Time Calculation**.

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5.7.3.5 ARITHMETIC/LOGIC INSTRUCTIONS. The arithmetic/logic instruction table indicates the number of clock periods needed to perform the specified arithmetic/logical instruction using the specified addressing mode. Footnotes indicate when to account for the appropriate EA times. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction		Head	Tail	Cycles
ADD(A)	Rn, Rm	0	0	2(0/1/0)
ADD(A)	⟨FEA⟩, Rn	0	0	2(0/1/0)
ADD	Dn, ⟨FEA⟩	0	3	5(0/1/x)
AND	Dn, Dm	0	0	2(0/1/0)
AND	⟨FEA⟩, Dn	0	0	2(0/1/0)
AND	Dn, ⟨FEA⟩	0	3	5(0/1/x)
EOR	Dn, Dm	0	0	2(0/1/0)
EOR	Dn, ⟨FEA⟩	0	3	5(0/1/x)
OR	Dn, Dm	0	0	2(0/1/0)
OR	⟨FEA⟩, Dn	0	0	2(0/1/0)
OR	Dn, ⟨FEA⟩	0	3	5(0/1/x)
SUB(A)	Rn, Rm	0	0	2(0/1/0)
SUB(A)	⟨FEA⟩, Rn	0	0	2(0/1/0)
SUB	Dn, ⟨FEA⟩	0	3	5(0/1/x)
CMP(A)	Rn, Rm	0	0	2(0/1/0)
CMP(A)	⟨FEA⟩, Rn	0	0	2(0/1/0)
CMP2 (Save) *	⟨FEA⟩, Rn	1	1	3(0/1/0)
CMP2 (Op)	⟨FEA⟩, Rn	2	0	16-18(X/1/0)
MUL(su).W	⟨FEA⟩, Dn	0	0	26(0/1/0)
MUL(su).L (Save) *	⟨FEA⟩, Dn	1	1	3(0/1/0)
MUL(su).L (Op)	⟨FEA⟩, Dl	2	0	46-52(0/1/0)
MUL(su).L (Op)	⟨FEA⟩, Dn:Dl	2	0	46(0/1/0)
DIVU.W	⟨FEA⟩, Dn	0	0	32(0/1/0)
DIVS.W	⟨FEA⟩, Dn	0	0	42(0/1/0)
DIVU.L (Save)*	⟨FEA⟩, Dn	1	1	3(0/1/0)
DIVU.L (Op)	⟨FEA⟩, Dn	2	0	<46(0/1/0)
DIVS.L (Save) *	⟨FEA⟩, Dn	1	1	3(0/1/0)
DIVS.L (Op)	⟨FEA⟩, Dn	2	0	<62(0/1/0)
TBL(su)	Dn:Dm, Dp	26	0	28-30(0/2/0)
TBL(su) (Save) *	⟨CEA⟩, Dn	1	1	3(0/1/0)
TBL(su) (Op)	⟨CEA⟩, Dn	6	0	33-35(2X/1/0)
TBLSN	Dn:Dm, Dp	30	0	30-34(0/2/0)
TBLSN (Save)*	⟨CEA⟩, Dn	1	1	3(0/1/0)
TBLSN (Op)	⟨CEA⟩, Dn	6	0	35-39(2X/1/0)

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Instruction		Head	Tail	Cycles
TBLUN	Dn:Dm, Dp	30	0	34-40(0/2/0)
TBLUN (Save)*	⟨CEA⟩, Dn	1	1	3(0/1/0)
TBLUN (Op)	⟨CEA⟩, Dn	6	0	39-45(2X/1/0)

X = There is one bus cycle for byte and word operands and two bus cycles for long operands. For long bus cycles, add two clocks to the tail and to the number of cycles.

< = Maximum time (certain data or mode combinations may execute faster).

su = The execution time is identical for signed or unsigned operands.

*These instructions have an additional save operation that other instructions do not have. To calculate total instruction time, calculate save, ⟨ea⟩, and operation execution times, then combine in the order listed, using equations in **5.7.1.6 Instruction Execution Time Calculations**. A save operation is not run for long-word divide and multiply instructions when ⟨FEA⟩ = Dn,

5.7.3.6 IMMEDIATE ARITHMETIC/LOGIC INSTRUCTIONS. The immediate arithmetic/logic instruction table indicates the number of clock periods needed for the processor to fetch the source immediate data value and to perform the specified arithmetic/logic instruction using the specified addressing mode. Footnotes indicate when to account for the appropriate fetch effective or fetch immediate EA times. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction		Head	Tail	Cycles
MOVEQ	#, Dn	0	0	2(0/1/0)
ADDQ	#, Rn	0	0	2(0/1/0)
ADDQ	#, ⟨FEA⟩	0	3	5(0/1/x)
SUBQ	#, Rn	0	0	2(0/1/0)
SUBQ	#, ⟨FEA⟩	0	3	5(0/1/x)
ADDI	#, Rn	0	0	2(0/1/0)∗
ADDI	#, ⟨FEA⟩	0	3	5(0/1/x)∗
ANDI	#, Rn	0	0	2(0/1/0)∗
ANDI	#, ⟨FEA⟩	0	3	5(0/1/x)∗
EORI	#, Rn	0	0	2(0/1/0)∗
EORI	#, ⟨FEA⟩	0	3	5(0/1/x)∗
ORI	#, Rn	0	0	2(0/1/0)∗
ORI	#, ⟨FEA⟩	0	3	5(0/1/x)∗
SUBI	#, Rn	0	0	2(0/1/0)∗
SUBI	#, ⟨FEA⟩	0	3	5(0/1/x)∗
CMPI	#, Rn	0	0	2(0/1/0)∗
CMPI	#, ⟨FEA⟩	0	3	5(0/1/x)∗

X = There is one bus cycle for byte and word operands and two bus cycles for long-word operands. For long-word bus cycles, add two clocks to the tail and to the number of cycles.

∗ = An # fetch EA time must be added for this instruction: ⟨FEA⟩ +⟨FEA⟩ + ⟨OPER⟩

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5.7.3.7 BINARY-CODED DECIMAL AND EXTENDED INSTRUCTIONS. The BCD and extended instruction table indicates the number of clock periods needed for the processor to perform the specified operation using the specified addressing mode. No additional tables are needed to calculate total effective execution time for these instructions. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction		Head	Tail	Cycles
ABCD	Dn, Dm	2	0	4(0/1/0)
ABCD	–(An), –(Am)	2	2	12(2/1/1)
SBCD	Dn, Dm	2	0	4(0/1/0)
SBCD	–(An), –(Am)	2	2	12(2/1/1)
ADDX	Dn, Dm	0	0	2(0/1/0)
ADDX	–(An), –(Am)	2	2	10(2/1/1)
SUBX	Dn, Dm	0	0	2(0/1/0)
SUBX	–(An), –(Am)	2	2	10(2/1/1)
CMPM	(An)+, (Am)+	1	0	8(2/1/0)

5.7.3.8 SINGLE OPERAND INSTRUCTIONS. The single operand instruction table indicates the number of clock periods needed for the processor to perform the specified operation using the specified addressing mode. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction		Head	Tail	Cycles
CLR	Dn	0	0	2(0/1/0)
CLR	⟨CEA⟩	0	2	4(0/1/x)
NEG	Dn	0	0	2(0/1/0)
NEG	⟨FEA⟩	0	3	5(0/1/x)
NEGX	Dn	0	0	2(0/1/0)
NEGX	⟨FEA⟩	0	3	5(0/1/x)
NOT	Dn	0	0	2(0/1/0)
NOT	⟨FEA⟩	0	3	5(0/1/x)
EXT	Dn	0	0	2(0/1/0)
NBCD	Dn	2	0	4(0/1/0)
NBCD	⟨FEA⟩	0	2	6(0/1/1)
Scc	Dn	2	0	4(0/1/0)
Scc	⟨CEA⟩	2	2	6(0/1/1)
TAS	Dn	4	0	6(0/1/0)
TAS	⟨CEA⟩	1	0	10(0/1/1)
TST	⟨FEA⟩	0	0	2(0/1/0)

X = There is one bus cycle for byte and word operands and two bus cycles for long-word operands. For long-word bus cycles, add two clocks to the tail and to the number of cycles.

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5.7.3.9 SHIFT/ROTATE INSTRUCTIONS. The shift/rotate instruction table indicates the number of clock periods needed for the processor to perform the specified operation on the given addressing mode. Footnotes indicate when to account for the appropriate EA times. The number of bits shifted does not affect the execution time, unless noted. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction		Head	Tail	Cycles	Note
LSd	Dn, Dm	–2	0	(0/1/0)	1
LSd	#, Dm	4	0	6(0/1/0)	—
LSd	⟨FEA⟩	0	2	6(0/1/1)	—
ASd	Dn, Dm	–2	0	(0/1/0)	1
ASd	#, Dm	4	0	6(0/1/0)	—
ASd	⟨FEA⟩	0	2	6(0/1/1)	—
ROd	Dn, Dm	–2	0	(0/1/0)	1
ROd	#, Dm	4	0	6(0/1/0)	—
ROd	⟨FEA⟩	0	2	6(0/1/1)	—
ROXd	Dn, Dm	–2	0	(0/1/0)	2
ROXd	#, Dm	–2	0	(0/1/0)	3
ROXd	⟨FEA⟩	0	2	6(0/1/1)	—

d = Direction (left or right)

NOTES:

1. Head and cycle times can be derived from the following table or calculated as follows:
   Max (3 + (n/4) + mod(n,4) + mod (((n/4) + mod (n,4) + 1,2), 6)
2. Head and cycle times are calculated as follows: (count ≤ 63): max (3 + n + mod (n + 1,2), 6).
3. Head and cycle times are calculated as follows: (count ≤ 8): max (2 + n + mod (n,2), 6).

Clocks	Shift Counts									
6	0	1	2	3	4	5	6	8	9	12
8	7	10	11	13	14	16	17	20		
10	15	18	19	21	22	24	25	28		
12	23	26	27	29	30	32	33	36		
14	31	34	35	37	38	40	41	44		
16	39	42	43	45	46	48	49	52		
18	47	50	51	53	54	56	57	60		
20	55	58	59	61	62					
22	63									

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5.7.3.10 BIT MANIPULATION INSTRUCTIONS. The bit manipulation instruction table indicates the number of clock periods needed for the processor to perform the specified operation on the given addressing mode. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction	Head	Tail	Cycles
BCHG #, Dn	2	0	6(0/2/0)∗
BCHG Dn, Dm	4	0	6(0/1/0)
BCHG #, ⟨FEA⟩	1	2	8(0/2/1)∗
BCHG Dn, ⟨FEA⟩	2	2	8(0/1/1)
BCLR #, Dn	2	0	6(0/2/0)∗
BCLR Dn, Dm	4	0	6(0/1/0)
BCLR #, ⟨FEA⟩	1	2	8(0/2/1)∗
BCLR Dn, ⟨FEA⟩	2	2	8(0/1/1)
BSET #, Dn	2	0	6(0/2/0)∗
BSET Dn, Dm	4	0	6(0/1/0)
BSET #, ⟨FEA⟩	1	2	8(0/2/1)∗
BSET Dn, ⟨FEA⟩	2	2	8(0/1/1)
BTST #, Dn	2	0	4(0/2/0)∗
BTST Dn, Dm	2	0	4(0/1/0)
BTST #, ⟨FEA⟩	1	0	4(0/2/0)∗
BTST Dn, ⟨FEA⟩	2	0	8(0/1/0)

∗ = An # fetch EA time must be added for this instruction: ⟨FEA⟩ + ⟨FEA⟩ + ⟨OPER⟩

5.7.3.11 CONDITIONAL BRANCH INSTRUCTIONS. The conditional branch instruction table indicates the number of clock periods needed for the processor to perform the specified branch on the given branch size, with complete execution times given. No additional tables are needed to calculate total effective execution time for these instructions. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction	Head	Tail	Cycles
Bcc (taken)	2	–2	8(0/2/0)
Bcc.B (not taken)	2	0	4(0/1/0)
Bcc.W (not taken)	0	0	4(0/2/0)
Bcc.L (not taken)	0	0	6(0/3/1)
DBcc (T, not taken)	1	1	4(0/2/0)
DBcc (F, –1, not taken)	2	0	6(0/2/0)
DBcc (F, not –1, taken)	6	–2	10(0/2/0)
DBcc (T, not taken)	4	0	6(0/1/0)∗
DBcc (F, –1, not taken)	6	0	8(0/1/0)∗
DBcc (F, not –1, taken)	6	0	10(0/0/0)∗

∗ = In loop mode

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5.7.3.12 CONTROL INSTRUCTIONS. The control instruction table indicates the number of clock periods needed for the processor to perform the specified operation on the given addressing mode. Footnotes indicate when to account for the appropriate EA times. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction		Head	Tail	Cycles
ANDI	#, SR	0	–2	12(0/2/0)
EORI	#, SR	0	–2	12(0/2/0)
ORI	#, SR	0	–2	12(0/2/0)
ANDI	#, CCR	2	0	6(0/2/0)
EORI	#, CCR	2	0	6(0/2/0)
ORI	#, CCR	2	0	6(0/2/0)
BSR.B		3	–2	13(0/2/2)
BSR.W		3	–2	13(0/2/2)
BSR.L		1	–2	13(0/2/2)
CHK	⟨FEA⟩, Dn (no ex)	2	0	8(0/1/0)
CHK	⟨FEA⟩, Dn (ex)	2	–2	42(2/2/6)
CHK2 (Save)	⟨FEA⟩, Dn (no ex)	1	1	3(0/1/0)
CHK2 (Op)	⟨FEA⟩, Dn (no ex)	2	0	18(X/0/0)
CHK2 (Save)	⟨FEA⟩, Dn (ex)	1	1	3(0/1/0)
CHK2 (Op)	⟨FEA⟩, Dn (ex)	2	–2	52(X + 2/1/6)
JMP	⟨CEA⟩	0	–2	6(0/2/0)
JSR	⟨CEA⟩	3	–2	13(0/2/2)
LEA	⟨CEA⟩, An	0	0	2(0/1/0)
LINK.W	An, #	2	0	10(0/2/2)
LINK.L	An, #	0	0	10(0/3/2)
NOP		0	0	2(0/1/0)
PEA	⟨CEA⟩	0	0	8(0/1/2)
RTD	#	1	–2	12(2/2/0)
RTR		1	–2	14(3/2/0)
RTS		1	–2	12(2/2/0)
UNLK	An	1	0	9(2/1/0)

X = There is one bus cycle for byte and word operands and two bus cycles for long-word operands. For long-word bus cycles, add two clocks to the tail and to the number of cycles.

NOTE: The CHK2 instruction involves a save step that other instructions do not have. To calculate the total instruction time, calculate the save, the EA, and the operation execution times, and combine in the order listed using the equations given in **5.7.1.6 Instruction Execution Time Calculation**.

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5.7.3.13 EXCEPTION-RELATED INSTRUCTIONS AND OPERATIONS. The exception-related instructions and operations table indicates the number of clock periods needed for the processor to perform the specified exception-related actions. No additional tables are needed to calculate total effective execution time for these instructions. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction	Head	Tail	Cycles
BKPT (Acknowledged)	0	0	14(1/0/0)
BKPT (Bus Error)	0	–2	35(3/2/4)
Breakpoint (Acknowledged)	0	0	10(1/0/0)
Breakpoint (Bus Error)	0	–2	42(3/2/6)
Interrupt	0	–2	30(3/2/4)∗
RESET	0	0	518(0/1/0)
STOP	2	0	12(0/1/0)
LPSTOP	3	–2	25(0/3/1)
Divide-by-Zero	0	–2	36(2/2/6)
Trace	0	–2	36(2/2/6)
TRAP #	4	–2	29(2/2/4)
ILLEGAL	0	–2	25(2/2/4)
A-line	0	–2	25(2/2/4)
F-line (First word illegal)	0	–2	25(2/2/4)
F-line (Second word illegal) ea = Rn	1	–2	31(2/3/4)
F-line (Second word illegal) ea ≠ Rn (Save)	1	1	3(0/1/0)
F-line (Second word illegal) ea ≠ Rn (Op)	4	–2	29(2/2/4)
Privileged	0	–2	25(2/2/4)
TRAPcc (trap)	2	–2	38(2/2/6)
TRAPcc (no trap)	2	0	4(0/1/0)
TRAPcc.W (trap)	2	–2	38(2/2/6)
TRAPcc.W (no trap)	0	0	4(0/2/0)
TRAPcc.L (trap)	0	–2	38(2/2/6)
TRAPcc.L (no trap)	0	0	6(0/3/0)
TRAPV (trap)	2	–2	38(2/2/6)
TRAPV (no trap)	2	0	4(0/1/0)

∗ = Minimum interrupt acknowledge cycle time is assumed to be three clocks.

NOTE: The F-line (second word illegal) operation involves a save step which other operations do not have. To calculate the total operation time, calculate the save, the calculate EA, and the operation execution times, and combine in the order listed, using the equations given in **5.7.1.6 Instruction Execution Time Calculation**.

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5.7.3.14 SAVE AND RESTORE OPERATIONS. The save and restore operations table indicates the number of clock periods needed for the processor to perform the specified state save or return from exception. Complete execution times and stack length are given. No additional tables are needed to calculate total effective execution time for these instructions. The total number of clock cycles is outside the parentheses. The numbers inside parentheses (r/p/w) are included in the total clock cycle number. All timing data assumes two-clock reads and writes.

Instruction	Head	Tail	Cycles
BERR on instruction	0	–2	<58(2/2/12)
BERR on exception	0	–2	48(2/2/12)
RTE (four-word frame)	1	–2	24(4/2/0)
RTE (six-word frame)	1	–2	26(4/2/0)
RTE (BERR on instruction)	1	–2	50(12/12/Y)
RTE (BERR on four-word frame)	1	–2	66(10/2/4)
RTE (BERR on six-word frame)	1	–2	70(12/2/6)

< = Maximum time is indicated (certain data or mode combinations execute faster).

Y = If a bus error occurred during a write cycle, the cycle is rerun by the RTE.

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SECTION 6
DMA CONTROLLER MODULE

The direct memory access (DMA) controller module provides for high-speed transfer capability to/from an external peripheral or for memory-to-memory data transfer. The DMA module, shown in Figure 6-1, provides two channels that allow byte, word, or long-word operand transfers. These transfers can be either single or dual address and to either on- or off-chip devices. The DMA contains the following features:

- Two Independent, Fully Programmable DMA Channels
- Single-Address Transfers and Dual-Address Transfers
- 32-Bit Address and 32-Bit Data Capability
- Two 32-Bit Transfer Counters
- Four 32-Bit Address Pointers That Can Increment or Remain Constant
- Operand Packing and Unpacking for Dual-Address Transfers
- Supports All Bus-Termination Modes
- Provides Two-Clock-Cycle Internal Module Access
- Provides Two-Clock-Cycle External Access Using MC68341 Chip Selects
- Provides Full DMA Handshake for Burst Transfers and Cycle Steal
- Programmable Interrupt Level Allows Central Processing Unit (CPU) to Preempt DMA Activity

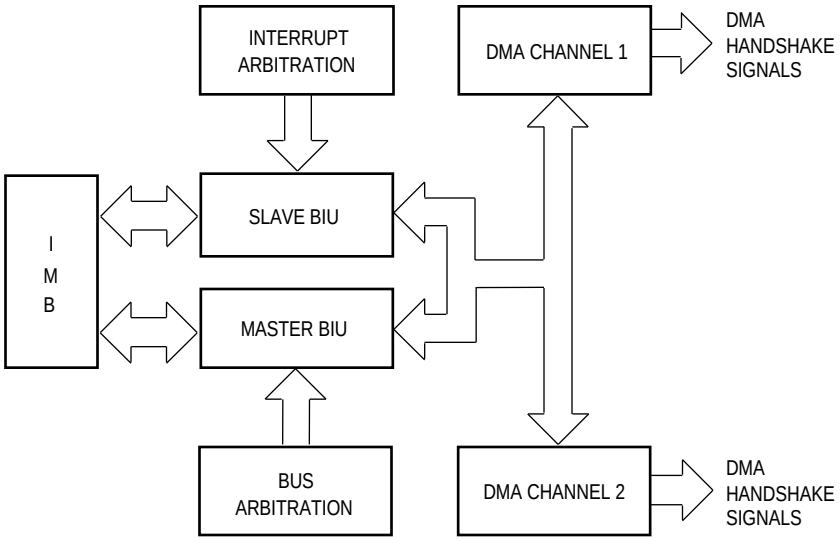

Figure 6-1. DMA Block Diagram

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6.1 DMA MODULE OVERVIEW

The DMA module is the same as the DMA implemented in the MC68340, with three extra signals added to provide additional handshaking flexibility. Paragraphs 6.1 through 6.9 describe the standard DMA module. The MC68341 additions are described in paragraph **6.10 MC68341 Enhancements**.

The main purpose of the DMA controller module is to transfer data at very high rates, usually much faster than the CPU32 under software control can handle. The term DMA is used to refer to the ability of a peripheral device to access memory in a system in the same manner as a microprocessor does. DMA operations can greatly increase overall system performance.

The DMA module consists of two independent, programmable channels. The term DMA is used throughout this section to reference either channel 1 or channel 2 since the two are functionally equivalent. Each channel has independent request, acknowledge, and done signals. However, both channels cannot own the bus at the same time. Therefore, it is impossible to implicitly address both DMA channels at the same time. The MC68341 on-chip peripherals do not support the single-address transfer mode.

DMA requests may be internally generated by the channel or externally generated by a device. For an internal request, the amount of bus bandwidth allocated for the DMA can be programmed. The DMA channels support two external request modes: burst mode and cycle steal mode.

Each DMA channel has a configurable interrupt service mask (ISM) level which causes the channel to temporarily suspend DMA activity when the CPU interrupt service level exceeds the ISM value. This feature can be used to minimize the effects of DMA activity or time-critical interrupt sources.

The DMA controller supports single- and dual-address transfers. In single-address mode, a channel supports 32 bits of address and 32 bits of data. Only an external request can be used to start a transfer in the single-address mode. The DMA provides address and control signals during a single-address transfer. The requesting device either sends or receives data to or from the specified address (see Figure 6-2). In dual-address mode, a channel supports 32 bits of address and 32 bits of data. The dual-address transfers can be started by either the internal request mode or by an external device using the request signal. In this mode, two bus transfers occur, one from a source device and the other to a destination device (see Figure 6-3). In dual-address mode, operands are packed or unpacked according to port sizes and addresses.

Any operation involving the DMA will follow the same basic steps: channel initialization, data transfer, and channel termination. In the channel initialization step, the DMA channel registers are loaded with control information, address pointers, and a byte transfer count. The channel is then started. During the data transfer step, the DMA accepts requests for operand transfers and provides addressing and bus control for the transfers. The channel termination step occurs after operation is complete. The channel indicates the status of the operation in the channel status register.

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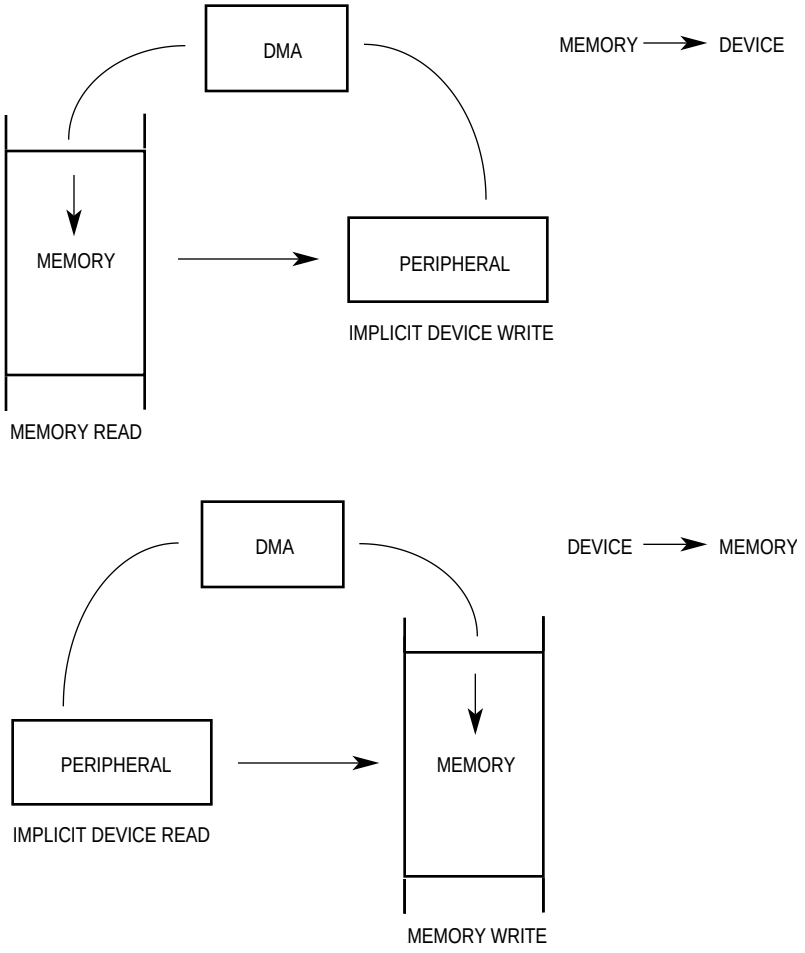

Figure 6-2. Single-Address Transfers

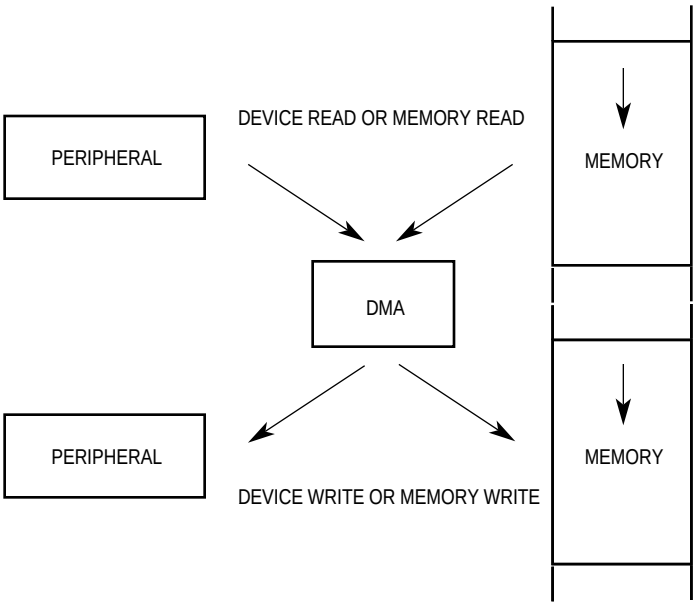

Figure 6-3. Dual-Address Transfer

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6.2 DMA MODULE SIGNAL DEFINITIONS

This section contains a brief description of the DMA module signals used to provide handshake control for either a source or destination external device.

NOTE

The terms *assertion* and *negation* are used throughout this section to avoid confusion when dealing with a mixture of active-low and active-high signals. The term *assert* or *assertion* indicates that a signal is active or true, independent of the level represented by a high or low voltage. The term *negate* or *negation* indicates that a signal is inactive or false.

6.2.1 DMA Request ($\overline{\text{DREQ1}}$, $\overline{\text{DREQ2}}$)

This active-low input is asserted by a peripheral device to request an operand transfer between that peripheral and memory. The assertion of $\overline{\text{DREQx}}$ starts the DMA process. The assertion level in external burst mode is level sensitive; in external cycle steal mode, it is falling-edge sensitive.

6.2.2 DMA Acknowledge ($\overline{\text{DACK1}}$, $\overline{\text{DACK2}}$)

This active-low output is asserted by the DMA to signal to a peripheral that an operand is being transferred in response to a previous transfer request.

6.2.3 Ready ($\overline{\text{RDY1}}$, $\overline{\text{RDY2}}$)

This active-low input is asserted by a peripheral device when it is ready to complete the DMA transfer. A slow device can delay assertion of $\overline{\text{RDYx}}$ to delay termination of a single-address DMA transfer between the device and faster memory. $\overline{\text{RDY1}}$ and $\overline{\text{RDY2}}$ are multiplexed with timer signals $\overline{\text{TGATE}}$ and TIN.

6.2.4 DMA Done ($\overline{\text{DONE1}}$, $\overline{\text{DONE2}}$)

This active-low bidirectional signal is asserted by the DMA or a peripheral device during any DMA bus cycle to indicate that the last data transfer is being performed. $\overline{\text{DONEx}}$ is an active input in any mode. As an output, $\overline{\text{DONEx}}$ is only active in external request mode. An external pullup resistor is required even if operating only in the internal request mode.

6.2.5 Data Transfer Complete ($\overline{\text{DTC}}$)

This active-low output is asserted for one clock at the end of all MC68341 bus cycles (CPU or DMA) to indicate completion of the cycle. $\overline{\text{DTC}}$ is multiplexed with FC3.

6.3 TRANSFER REQUEST GENERATION

The DMA channel supports two types of request generation methods: internal and external. Internally generated requests can be programmed to limit the amount of bus utilization.

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Externally generated requests can be either burst mode or cycle steal mode. The request generation method used for the channel is programmed by the REQ field in the channel control register (CCR).

6.3.1 Internal Request Generation

The channel is started as soon as the STR bit in the CCR is set. The channel immediately requests the bus and begins transferring data. Only internal requests can limit the amount of bus utilization. The percentage of the bus bandwidth that the DMA channel uses during a transfer is selected by the CCR bus bandwidth (BB) field.

6.3.1.1 INTERNAL REQUEST, MAXIMUM RATE. Internal generation using 100% of the internal bus always has a transfer request pending for the channel until the block transfer is complete. As soon as the channel is started, the DMA will arbitrate for the internal bus and begin to transfer data when it becomes bus master. If no exceptions occur, all operands in the data block will be transferred in one burst so that the DMA will use 100% of the available bus bandwidth.

6.3.1.2 INTERNAL REQUEST, LIMITED RATE. To guarantee that the DMA does not use all of the available bus bandwidth during a transfer, the bus bandwidth allocated to the DMA can be limited. There are three programmed constants in the CCR used to monitor the bus activity and allow the DMA to use a percentage of the bus bandwidth. Options are 25%, 50%, and 75% of 1024 clock periods. See Table 6-5 for more information.

6.3.2 External Request Generation

To control the transfer of operands to or from memory in an orderly manner, a peripheral device uses the $\overline{\text{DREQx}}$ input signal to request service. If the channel is programmed for external request and the CCR STR bit is set, an external request ($\overline{\text{DREQx}}$) signal must be asserted before the channel requests the bus and begins a transfer. The DMA supports external burst mode and external cycle steal mode.

The generation of the request from the source or destination is specified by the ECO bit of the CCR. The external requests can be for either single- or dual-address transfers.

6.3.2.1 EXTERNAL BURST MODE. For external devices that require very high data transfer rates, the burst request mode allows the DMA channel to use all of the bus bandwidth under control of the external device. In burst mode, the $\overline{\text{DREQx}}$ input to the DMA is level sensitive and is sampled at certain points to determine when a valid request is asserted by the device. The device requests service by asserting $\overline{\text{DREQx}}$ and leaving it asserted. In response, the DMA arbitrates for the bus and performs an operand transfer. During each operand transfer, the DMA asserts DMA acknowledge ($\overline{\text{DACKx}}$) to indicate to the device that a request is being serviced. $\overline{\text{DACKx}}$ is asserted on the cycle of either the source or destination device, depending on which one generated the request as programmed by the CCR ECO bit.

To allow more than one transfer to be recognized, $\overline{\text{DREQx}}$ must meet the asynchronous setup and hold times while $\overline{\text{DACKx}}$ is asserted in the DMA bus cycle. Upon completion of a

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request, $\overline{\text{DREQx}}$ should be held asserted (bursting) into the following DMA bus cycle to allow another transfer to occur. The recognized request will immediately be serviced. If $\overline{\text{DREQx}}$ is negated before $\overline{\text{DACKx}}$ is asserted, a new request is not recognized, and the DMA channel releases ownership of the bus.

6.3.2.2 EXTERNAL CYCLE STEAL MODE. For external devices that generate a pulsed signal for each operand to be transferred, the cycle steal request mode uses the $\overline{\text{DREQx}}$ signal as a falling-edge-sensitive input. The $\overline{\text{DREQx}}$ pulse generated by the device must be asserted during two consecutive falling edges of the clock to be recognized as valid. Therefore, if a peripheral generates it asynchronously, it must be at least two clock periods long.

The DMA channel responds to cycle steal requests the same as all other requests. However, if subsequent $\overline{\text{DREQx}}$ pulses are generated before $\overline{\text{DACKx}}$ is asserted in response to each request, they are ignored. If $\overline{\text{DREQx}}$ is asserted after the DMA channel asserts $\overline{\text{DACKx}}$ for the previous request but before $\overline{\text{DACKx}}$ is negated, then the new request is serviced before bus ownership is released. If a new request is not generated by the time $\overline{\text{DACKx}}$ is negated, the bus is released.

6.3.2.3 EXTERNAL REQUEST WITH OTHER MODULES. The DMA controller can be externally connected to the serial module and used in conjunction with the serial module to send or receive data. The DMA takes the place of a separate service routine for accessing or storing data that is sent or received by the serial module. Using the DMA also lowers the CPU32 overhead required to handle the data transferred by the serial module. Figure 6-4 shows the external connections required for using the DMA with the serial module.

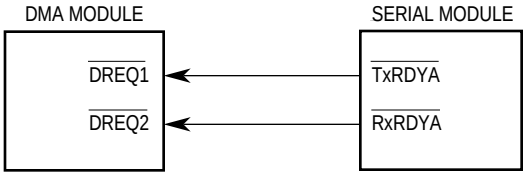

Figure 6-4. DMA External Connections to Serial Module

For serial receive, the DMA reads data from the serial receive buffer register (when the serial module has filled the buffer on input) and writes data to memory. For serial transmit, the DMA reads data from memory and writes data to the serial transmit buffer register. Only dual-address mode can be used with the serial module. The MC68341 on-chip peripherals do not support single-address transfers.

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6.4 DATA TRANSFER MODES

The DMA channel supports single- and dual-address transfers. The single-address transfer mode consists of one DMA bus cycle, which allows either a read or a write cycle to occur. The dual-address transfer mode consists of a source operand read and a destination operand write. Two DMA bus cycles are executed for the dual-address mode: a DMA read cycle and a DMA write cycle.

6.4.1 Single-Address Mode

The single-address DMA bus cycle allows data to be transferred directly between a device and memory without going through the DMA. In this mode, the operand transfer takes place in one bus cycle, where only the memory is explicitly addressed. The DMA bus cycle may be either a read or a write cycle. The DMA provides the address and control signals required for the operation. The requesting device either sends or receives data to or from the specified address. Only external requests can be used to start a transfer when the single-address mode is selected. An external device uses $\overline{\text{DREQx}}$ to request a transfer.

Each DMA channel can be independently programmed to provide single-address transfers. The CCR ECO bit controls whether a source read or a destination write cycle occurs on the data bus. If the ECO bit is set, the external handshake signals are used with the source operand and a single-address source read occurs. If the ECO bit is cleared, the external handshake signals are used with the destination operand, and a single-address destination write occurs. The channel can be programmed to operate in either burst transfer mode or cycle steal mode. See **6.7 Register Description** for more information.

6.4.1.1 SINGLE-ADDRESS READ. During the single-address source (read) cycle, the DMA controls the transfer of data from memory to a device. The memory selected by the address specified in the source address register (SAR), the source function codes in the function code register (FCR), and the source size in the CCR provides the data and control signals on the data bus. This bus cycle operates like a normal read bus cycle. The DMA control signals ($\overline{\text{DACKx}}$ and $\overline{\text{DONEx}}$) are asserted in the source (read) cycle. See Figures 6-5 and 6-6 for timing diagrams single-address read for external burst and cycle steal modes.

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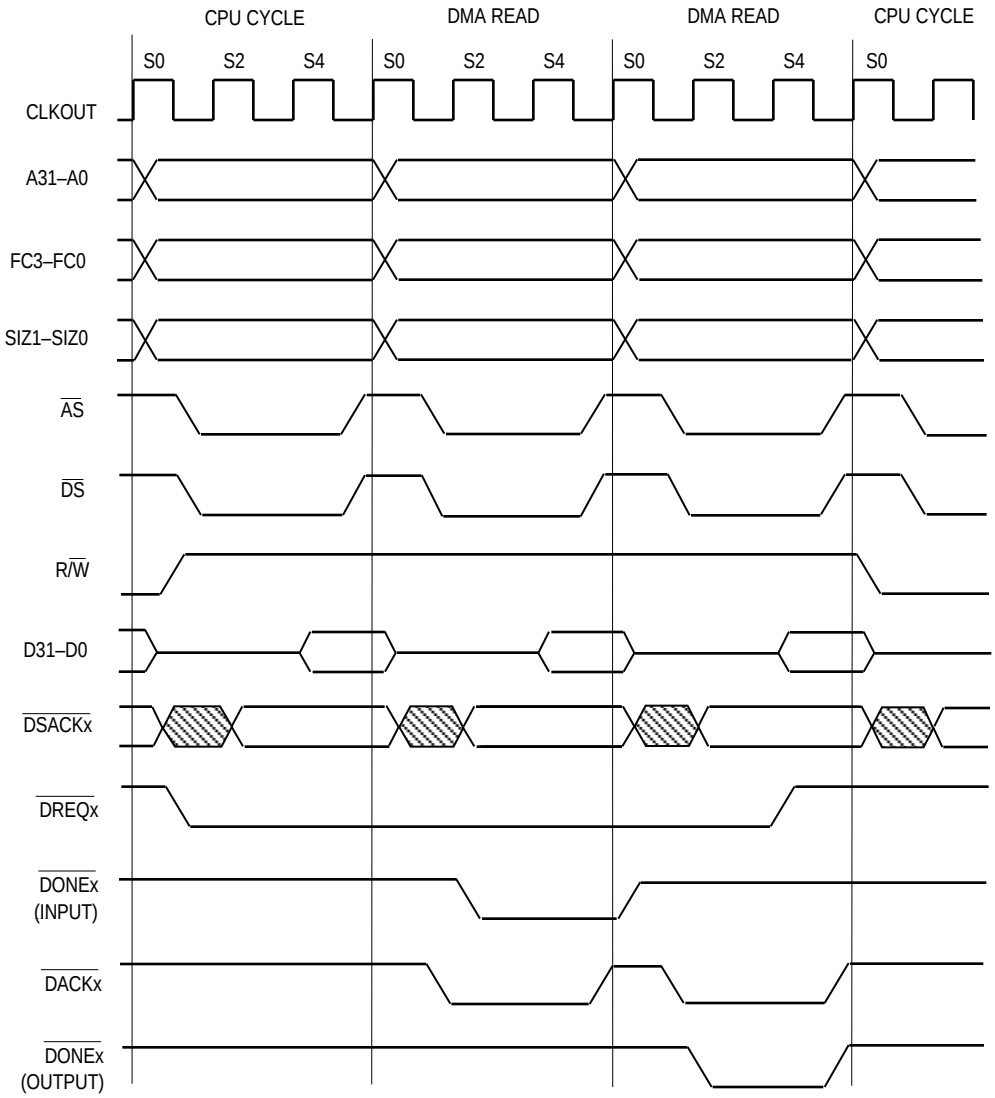

NOTES:
1. Timing to generate more than one DMA request.
2. DACKx and DONEx (DMA control signals) are asserted in the source (read) DMA cycle.
3. DREQx must be asserted while DACKx is asserted and meet the setup and hold times for more than one DMA transfer to be recognized.

Figure 6-5. Single-Address Read Timing (External Burst)

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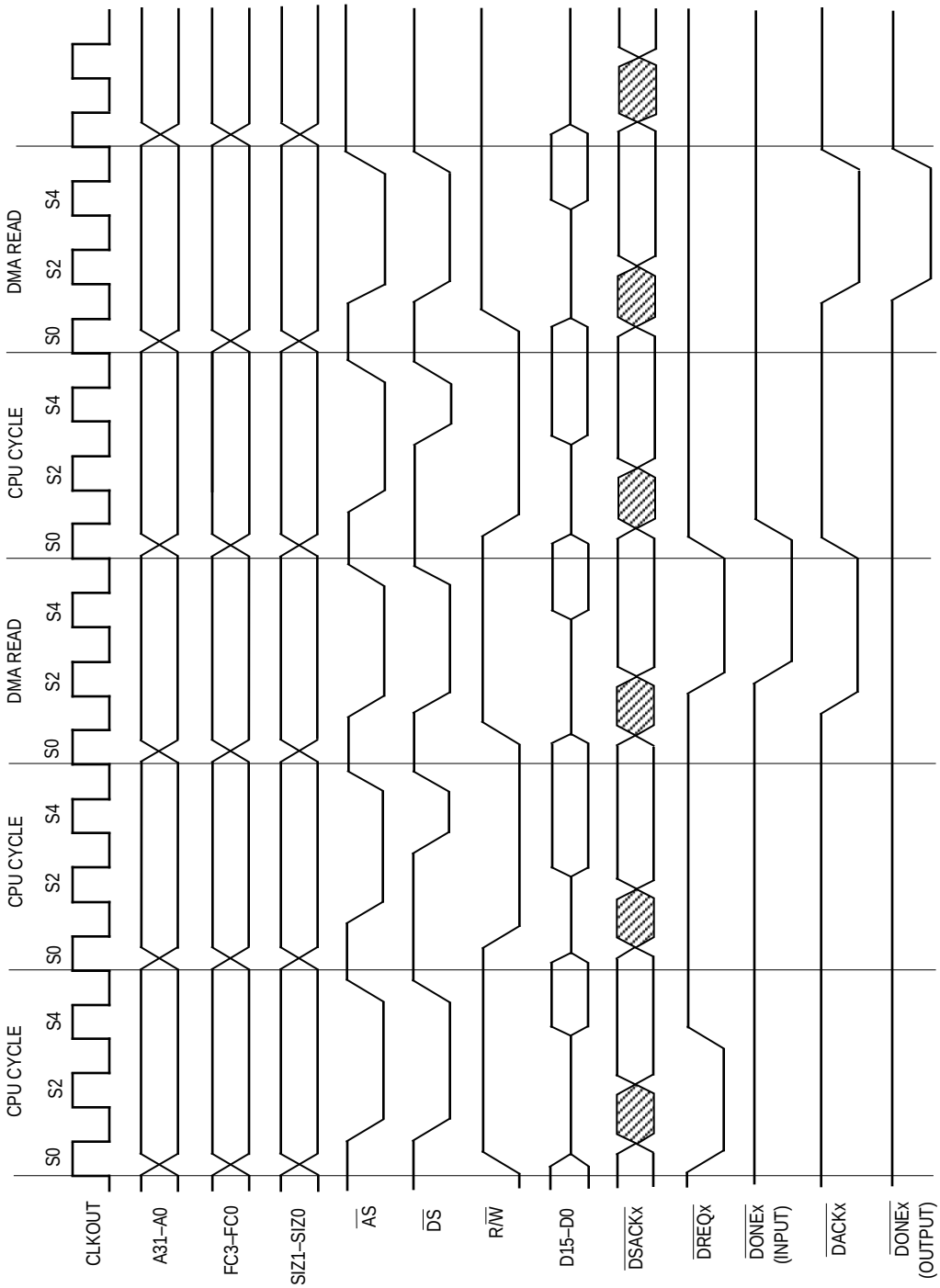

NOTE:
1. DREQx must be active for two consecutive clocks for a DMA request to be recognized.
2. To cause another DMA transfer, DREQx is asserted after DACKx is asserted and before DACKx is negated.
3. DACKx and DONEx (DMA control signals) are asserted in the source (read) DMA cycle.

Figure 6-6. Single-Address Read Timing (Cycle Steal)

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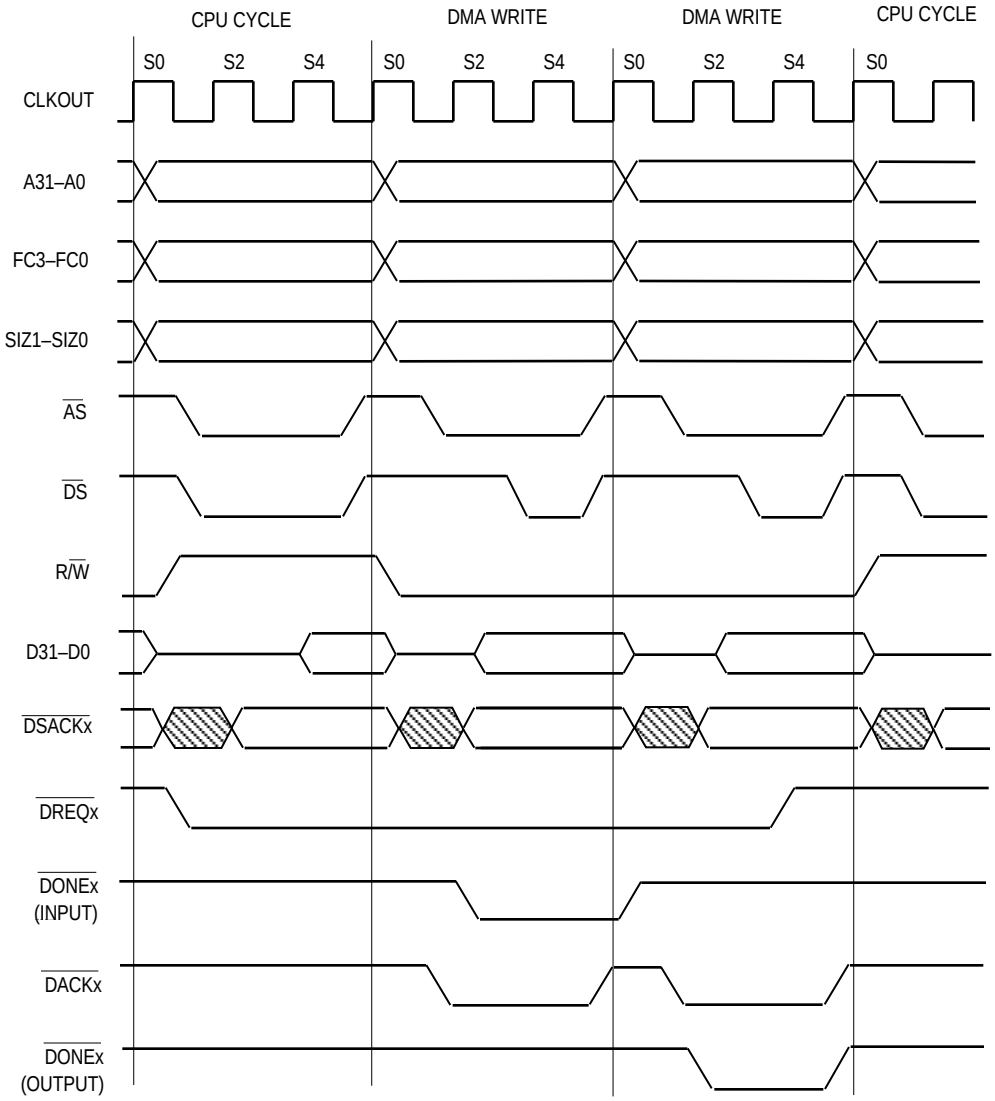
6.4.1.2 SINGLE-ADDRESS WRITE. During the single-address destination (write) cycle, the DMA controls the transfer of data from a device to memory. The data is written to memory selected by the address specified in the destination address register (DAR), the destination function codes in the FCR, and the size in the CCR. The destination (write) DMA bus cycle has timing identical to a write bus cycle. The DMA control signals ($\overline{\text{DACKx}}$ and $\overline{\text{DONEx}}$) are asserted in the destination (write) cycle. See Figures 6-7 and 6-8 for timing diagrams of single-address write for external burst and cycle steal modes.



NOTES:
1. Timing to generate more than one DMA request.
2. $\overline{\text{DACKx}}$ and $\overline{\text{DONEx}}$ (DMA control signals) are asserted in the source (read) DMA cycle.
3. $\overline{\text{DREQx}}$ must be asserted while $\overline{\text{DACKx}}$ is asserted, and meet the setup and hold times for more than one DMA transfer to be recognized.

Figure 6-7. Single-Address Write Timing (External Burst)

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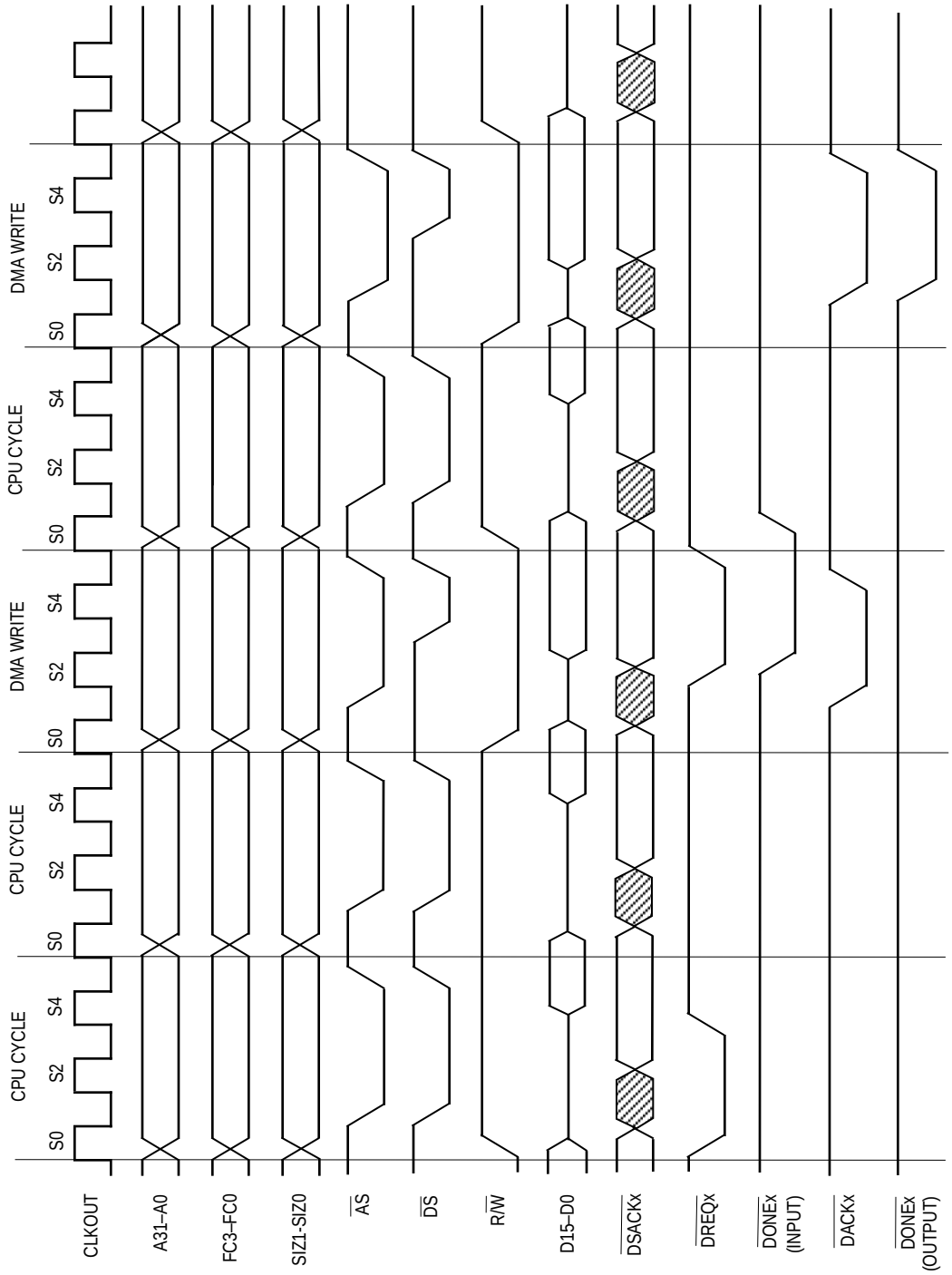

NOTE:
1. DREQx must be active for two consecutive clocks for a DMA request to be recognized.
2. To cause another DMA transfer, DREQx is asserted after DACKx is asserted and before DACKx is negated.
3. DACKx and DONEx (DMA control signals) are asserted in the destination (write) DMA cycle.

Figure 6-8. Single-Address Write Timing (Cycle Steal)

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6.4.2 Dual-Address Mode

The dual-address DMA bus cycle transfers data between a device or memory and the DMA internal data holding register (DHR). In this mode, any operand transfer takes place in two DMA bus cycles, one where a device is addressed and one where memory is addressed. The data transferred during a dual-address operation is either read from the data bus into the DHR or written from the DHR to the data bus.

Each DMA channel can be programmed to operate in the dual-address transfer mode. In this mode, the operand is read from the source address specified in the SAR and placed in the DHR. The operand read may take up to four bus cycles to complete because of differences in operand sizes of the source and destination. The operand is then written to the address specified in the DAR. This transfer may also be up to four bus cycles long. In this manner, various combinations of peripheral, memory, and operand sizes may be used. See **6.7 Register Description** for more information.

The dual-address transfers can be started by either the internal request mode or by an external device using the $\overline{\text{DREQx}}$ input signal. When the external device uses $\overline{\text{DREQx}}$, the channel can be programmed to operate in either burst transfer mode or cycle steal mode.

6.4.2.1 DUAL-ADDRESS READ. During the dual-address read cycle, the DMA reads data from a device or memory into the internal DHR. The device or memory is selected by the address specified in the SAR, the source function codes in the FCR, and the source size in the CCR. Data is read from the memory or peripheral and placed in the DHR when the bus cycle is terminated. When the complete operand has been read, the SAR is incremented by 0, 1, 2, or 4, according to the size and increment information specified by the SSIZE and SAPI bits of the CCR. The DMA control signals ($\overline{\text{DACKx}}$ and $\overline{\text{DONEx}}$) are asserted in the source (read) cycle when the source device makes a request. See Figures 6-9 and 6-10 for timing diagrams of dual-address reads for external burst and cycle steal modes.

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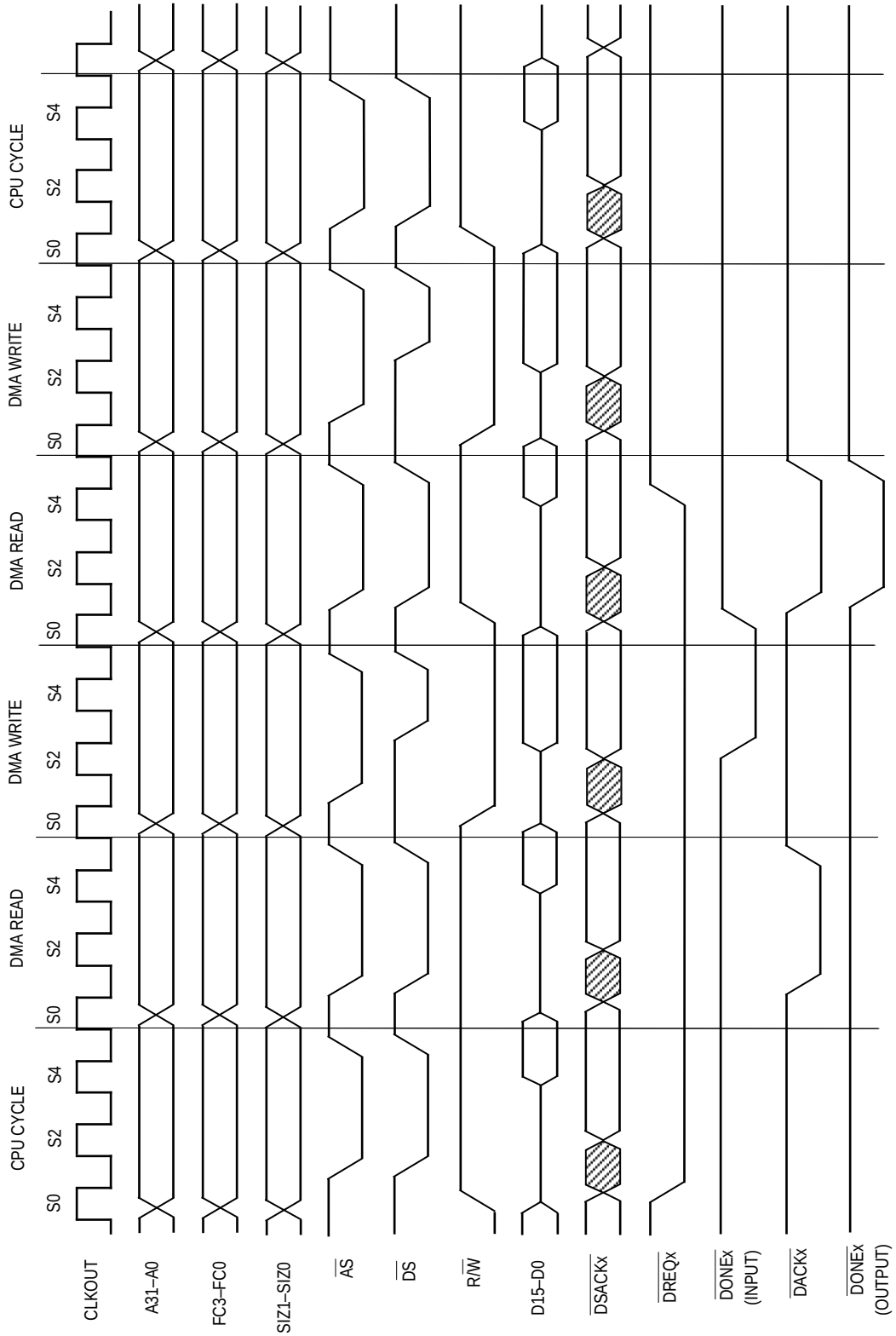

NOTE:
1. Timing to generate more than one DMA transfer.
2. DACKx and DONEx (DMA control signals) are asserted in the source (read) DMA cycle.
3. DREQx must be asserted while DACKx is asserted and meet the setup and hold times for more than one DMA transfer to be recognized.
4. DONEx (input) can be asserted in either the read or write DMA bus cycle to indicate that the next DMA transfer will be the last one.

Figure 6-9. Dual-Address Read Timing (External Burst-Source Requesting)

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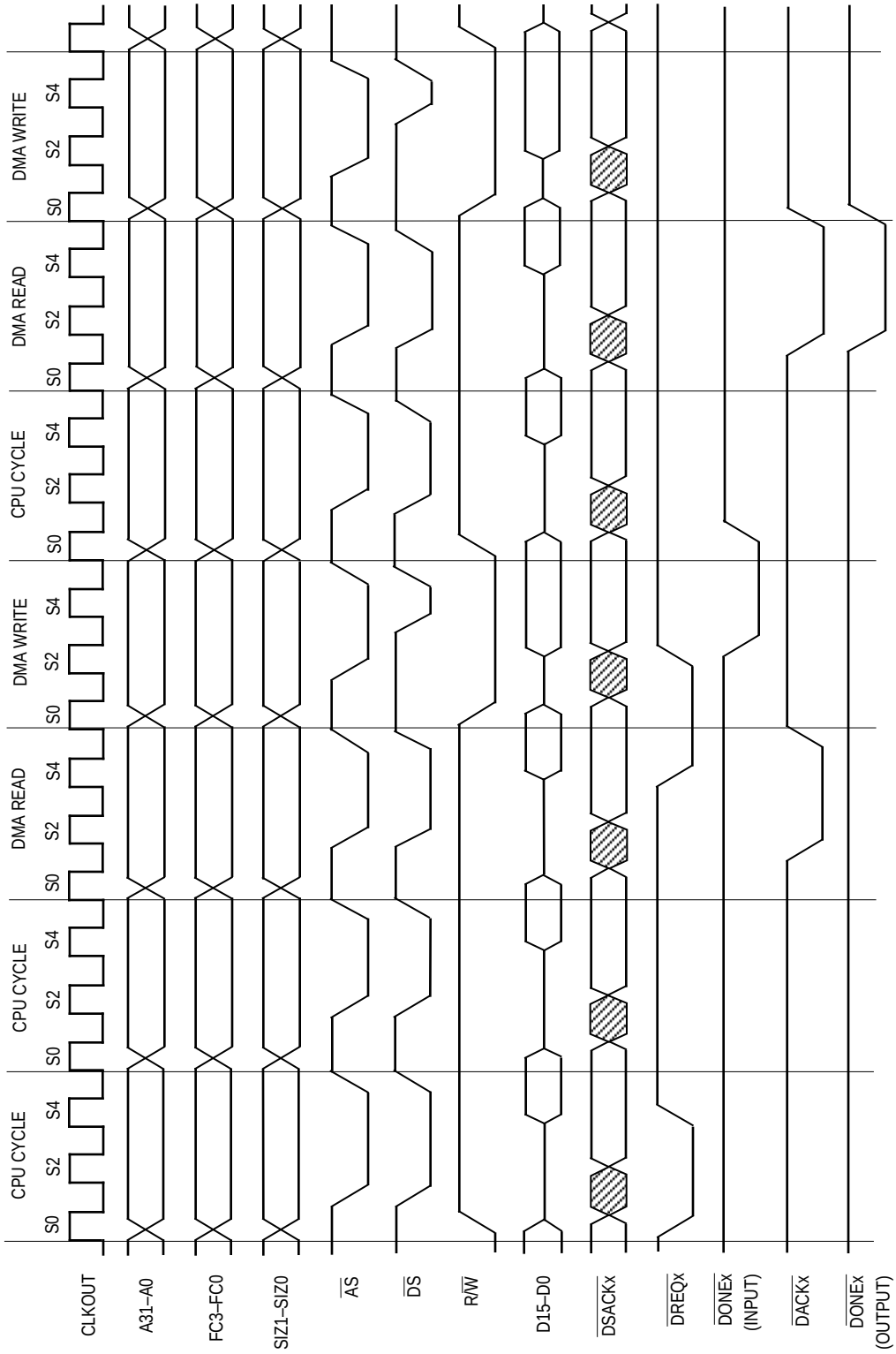

NOTE
1. DREQx must be active for two consecutive clocks for a DMA request to be recognized.
2. To cause another DMA transfer, the DREQx is asserted after DACKx is asserted and before DACKx is negated.
3. DACKx and DONEx (DMA control signals) are asserted in the source (read) DMA cycle.
4. DONEx (input) can be asserted in either the read or write DMA bus cycle to indicate that the next DMA transfer will be the last one.

Figure 6-10. Dual-Address Read Timing (Cycle Steal-Source Requesting)

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6.4.2.2 DUAL-ADDRESS WRITE. During the dual-address write cycle, the DMA writes data to a device or memory from the internal DHR. The data in the DHR is written to the device or memory selected by the address in the DAR, the destination function codes in the FCR, and the size in the CCR. When the complete operand is written, the DAR is incremented by 0, 1, 2, or 4, according to the increment and size information specified by the DAPI and DSIZE bits of the CCR, and the byte transfer count register (BTC) is decremented by the number of bytes transferred. If the BTC is equal to zero and there were no errors, the channel status register (CSR) DONE bit is set, and the $\overline{\text{DONEx}}$ signal for the DMA handshake is asserted. The DMA control signals ($\overline{\text{DACKx}}$ and $\overline{\text{DONEx}}$) are asserted in the destination (write) cycle when the destination device makes a request. See Figures 6-11 and 6-12 for timing diagrams of dual-address writes for external burst and cycle steal modes.

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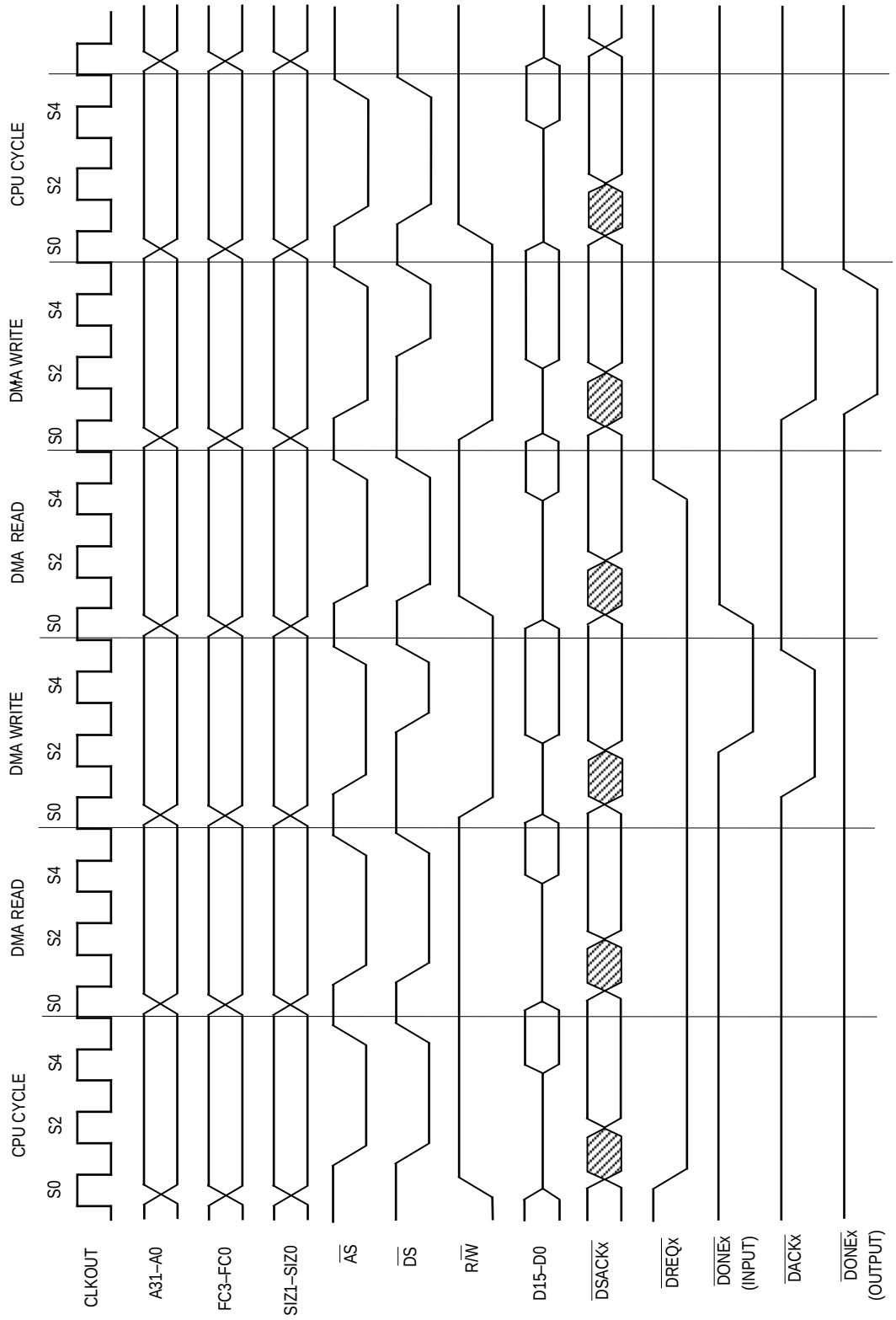

NOTE:
1. Timing to generate more than one DMA transfer.
2. DACKx and DONEx (DMA control signals) are asserted in the destination (write) DMA cycle.
3. DREQx must be asserted while DACKx is asserted and meet the setup and hold times for more than one DMA transfer to be recognized.
4. DONEx (input) can be asserted in either the read or write DMA bus cycle to indicate that the next DMA transfer will be the last one.

Figure 6-11. Dual-Address Write Timing (External Burst-Destination Requesting)

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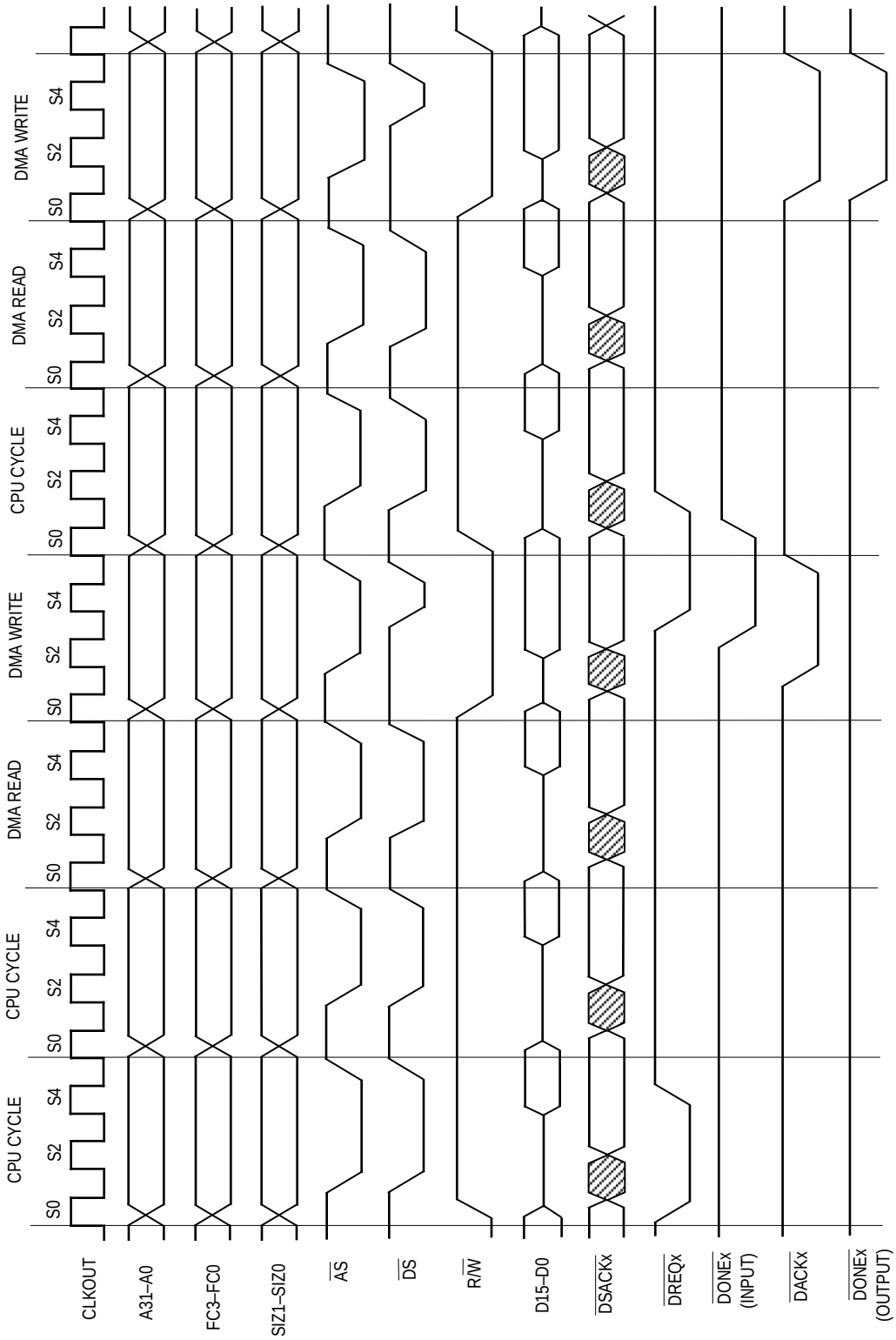

NOTE:
1. DREQx must be active for two consecutive clocks for a DMA request to be recognized.
2. To cause another DMA transfer, DREQx is asserted after DACKx is asserted and before DACKx is negated.
3. DACKx and DONEx (DMA control signals) are asserted in the destination (write) DMA cycle.
4. DONEx (Input) can be asserted in either the read or write DMA bus cycle to indicate that the next DMA transfer will be the last one.

Figure 6-12. Dual-Address Write Timing (Cycle Steal-Destination Requesting)

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6.5 BUS ARBITRATION

The DMA controller module uses the 68000 bus arbitration protocol to request bus mastership for DMA transfers. Each channel arbitrates for the bus independently. The source (read) DMA bus cycle has timing identical to a read bus cycle. The destination (write) DMA bus cycle has timing identical to a write bus cycle. However, the DMA channel transfers are unique in that the FC3 signal can be asserted during the source operand bus cycle and remain asserted until the end of the destination operand bus cycle.

For internal request generation, as soon as the CCR STR bit is set, the DMA channel arbitrates for the bus and begins to transfer data when it becomes bus master. For external request generation, the STR bit must be set and a $\overline{\text{DREQx}}$ signal must be asserted before the channel arbitrates for the bus and begins a transfer.

6.6 DMA CHANNEL OPERATION

The following paragraphs describe the programmable channel functions available for the DMA channel, the data transfer operations, and behavior during cycle termination. This description applies to both channels.

Any DMA channel operation adheres to the following basic sequence:

1. Channel Initialization and Startup—The channel registers are initialized. The channel is then started by setting the CCR STR bit. The first operand transfer request (either internally or externally generated) is recognized.
2. Data Transfer—After a channel is started, it transfers one operand in response to each request until an entire data block is transferred.
3. Channel Termination—The channel can terminate by normal completion or from an error. The CSR indicates the status of the operation.

6.6.1 Channel Initialization and Startup

Before starting a block transfer operation, the channel registers must be initialized with information describing the channel configuration, request generation method, and data block. This initialization is accomplished by programming the appropriate information into the channel registers.

The SAR is loaded with the source (read) address. If the transfer is from a peripheral device to memory, the source address is the location of the peripheral data register. If the transfer is from memory to a peripheral device or memory to memory, the source address is the starting address of the data block. This address may be any byte address. In the single-address mode with the destination (write) device requesting mode of operation, this register is not used.

The DAR should contain the destination (write) address. If the transfer is from a peripheral device to memory or memory to memory, the DAR is loaded with the starting address of the data block to be written. If the transfer is from memory to a peripheral device, the DAR is

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loaded with the address of the peripheral data register. This address may be any byte address. In the single-address mode with the source (read) device requesting mode of operation, this register is not used.

The manner in which the SAR and DAR change after each cycle depends upon the values in the CCR SSIZE and DSIZE fields and SAPI and DAPI bits, and the starting address in the SAR and DAR. If programmed to increment, the increment value is 1, 2, or 4 for byte, word, or long-word operands, respectively. If the address register is programmed to remain unchanged (no count), the register is not incremented after the operand transfer. The SAR and DAR are incremented if a bus error terminates the transfer. Therefore, either the SAR or the DAR contain the next address after the one that caused the bus error.

The BTC must be loaded with the number of byte transfers that are to occur. This register is decremented by 1, 2, or 4 at the end of each transfer. The FCR must be loaded with the source and destination function codes. Although these function codes may not be used in the address decode for the memory or peripheral, they are provided if needed. The CSR must be cleared for channel startup.

Once the channel has been initialized, it is started by writing a one to the STR bit in the CCR. Programming the channel for internal request causes the channel to request the bus and start transferring data immediately. If the channel is programmed for external request, $\overline{\text{DREQx}}$ must be asserted before the channel requests the bus. The $\overline{\text{DREQx}}$ input is ignored until the channel is started, since the channel does not recognize transfer requests until it is active.

If any fields in the CCR are modified while the channel is active, that change is effective immediately. To avoid any problems with changing the setup for the DMA channel, a zero should be written to the STR bit in the CCR to halt the DMA channel at the end of the current bus cycle.

6.6.2 Data Transfers

Each operand transfer requires from one to five bus cycles to complete. Once a bus request is recognized and the operand transfer begins, both the source (read) cycle and/or the destination (write) cycle occur before a new bus request may be honored, even if the new bus request is of higher priority.

6.6.2.1 INTERNAL REQUEST TRANSFERS. The percentage of bus bandwidth utilization can be limited for internal request transfers.

6.6.2.2 EXTERNAL REQUEST TRANSFERS. In single-address mode, only one bus cycle is run for each request. Since the operand size must be equal to the device port size in single-address mode, the number of normally terminated bus cycles executed during a transfer operation is always equal to the value programmed into the corresponding size field of the CCR. The sequencing of the address bus follows the programming of the CCR and address register (SAR or DAR) for the channel.

Each operand transfer in dual-address mode requires from two to five bus cycles in response to each operand transfer request. If the source and destination operands are the

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same size, two cycles will transfer the complete operand. If the source and destination operands are different sizes, the number of cycles will vary. If the source is a long-word and the destination is a byte, there would be one bus cycle for the read and four bus cycles for the write. Once the DMA channel has started a dual-address operand transfer, it must complete that transfer before releasing ownership of the bus or servicing a request for another channel of equal or higher priority, unless one of the bus cycles is terminated with a bus error during the transfer.

6.6.3 Channel Termination

The channel can terminate by normal completion or as the result of an error. The status of a DMA operation can be determined by reading the CSR. The DMA channel can also interrupt the processor to inform it of errors, normal transfer completion, or breakpoints. The fast termination option can also be used to provide a two-clock access for external requests.

6.6.3.1 CHANNEL TERMINATION. The channel operation can be terminated for several reasons: the BTC is decremented to zero, a peripheral device asserts $\overline{\text{DONEx}}$ during an operand transfer, the STR bit is cleared in the CCR, a bus cycle is terminated with a bus error, or a reset occurs.

6.6.3.2 INTERRUPT OPERATION. Interrupts can be generated by error termination of a bus cycle or by normal channel completion. Specifically, if the CCR interrupt error (INTE) bit is set and a bus error on source (CCR BES) bit, bus error on destination (CCR BED) bit, or configuration error (CCR CONF) bit is set, the CCR IRQ bit is set. In this case, clearing the INTE, BES, BED, or CONF bits causes the IRQ bit to be cleared. If the interrupt normal (CCR INTN) bit is set and the CCR DONE bit is set, the IRQ bit is set. In this case, clearing the INTN or the DONE bit causes the IRQ bit to be cleared. If the interrupt breakpoint (CCR INTB) and the CSR BRKP bits are set, the IRQ bit is set. Clearing INTB or BRKP clears IRQ.

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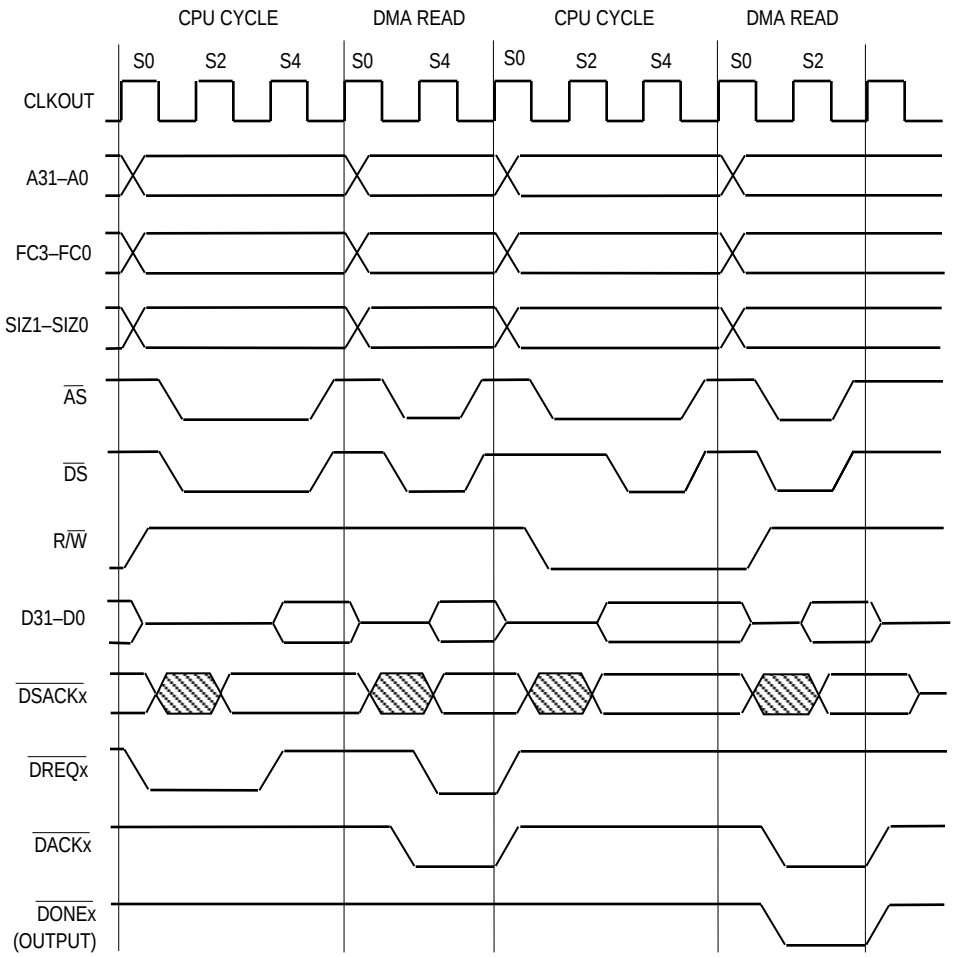
6.6.3.3 FAST TERMINATION OPTION. Using the system integration module (SIM41) chip select logic, the fast termination option (Figure 6-13) can be employed to give a fast bus access of two clock cycles rather than the standard three-cycle access time for external requests. The fast termination option is described in **Section 3 Bus Operation** and **Section 4 System Integration Module**.



NOTES:
1. To cause another DMA transfer, DREQx is asserted after DACKx is asserted and before DACKx is negated.
2. DACKx and DONEx (DMA control signals) are asserted in the source (read) DMA cycle.

Figure 6-13. Fast Termination Option Timing (Cycle Steal)

If the fast termination option is used with external burst request mode (Figure 6-14), an extra DMA cycle may result on every burst transfer. Normally, DREQx is negated when DACKx is returned. In the burst mode with fast termination selected, a new cycle starts even if DREQx is negated simultaneously with DACKx assertion.

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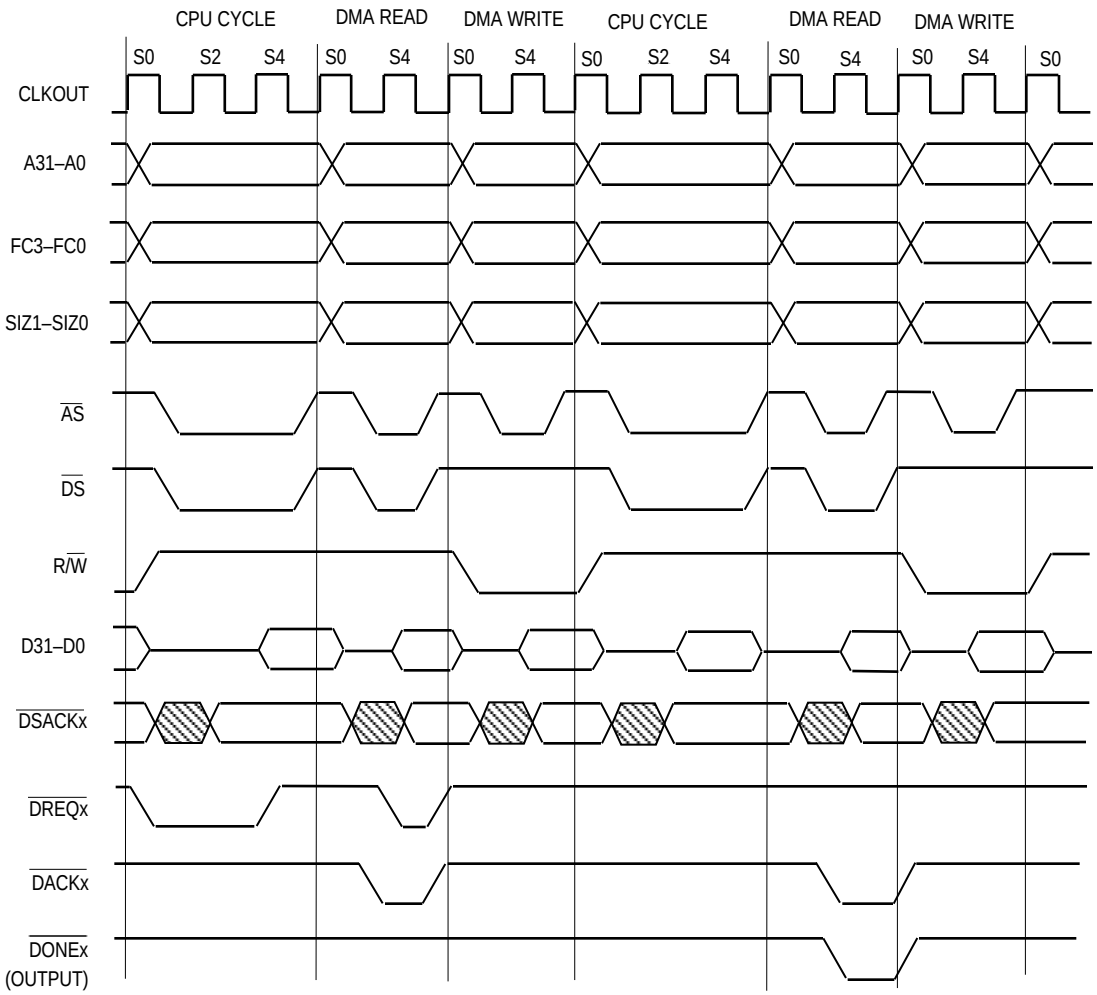

NOTES:
1. To cause another DMA transfer, the DREQx is asserted after DACKx is asserted and before DACKx is negated.
2. DACKx and DONEx (DMA control signals) are asserted in the source (read) DMA cycle.

Figure 6-14. Fast Termination Option Timing (External Burst–Source Requesting)

6.7 REGISTER DESCRIPTION

The following paragraphs contain a detailed description of each register and its specific function. Figure 6-15 is a programmer's model (register map) of all registers in the DMA module. Each channel has an independent set of registers. For more information about a particular register, refer to the individual register description. The ADDRESS column indicates the offset of the register from the base address of the DMA channel. The FC column designation of S indicates that register access is restricted to supervisor only. A designation of S/U indicates that access is governed by the SUPV bit in the module configuration register (MCR).

Unimplemented memory locations return logic zero when accessed. All registers support byte, word, and long-word transfers. The register interface from the IMB is 16 bits, which forces long-word accesses to complete as two successive word accesses.

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ADDRESS CH1	ADDRESS CH2	FC	15 … 8	7 … 0
780	7A0	S	MODULE CONFIGURATION REGISTER	
782	7A2	S	RESERVED	
784	7A4	S	INTERRUPT REGISTER	
786	7A6	S/U	RESERVED	
788	7A8	S/U	CHANNEL CONTROL REGISTER	
78A	7AA	S/U	CHANNEL STATUS REGISTER	FUNCTION CODE REGISTER
78C	7AC	S/U	SOURCE ADDRESS REGISTER MSBs	
78E	7AE	S/U	SOURCE ADDRESS REGISTER LSBs	
790	7B0	S/U	DESTINATION ADDRESS REGISTER MSBs	
792	7B2	S/U	DESTINATION ADDRESS REGISTER LSBs	
794	7B4	S/U	BYTE TRANSFER COUNTER MSBs	
796	7B6	S/U	BYTE TRANSFER COUNTER LSBs	
798	7B8	S/U	RESERVED	
79A	7BA	S/U	RESERVED	
79C	7BC	S/U	RESERVED	
79E	7BE	S/U	RESERVED	

Figure 6-15. DMA Module Programming Model

The registers are discussed in the following paragraphs in alphabetical order. The numbers in the upper right-hand corner of the register diagrams indicate the offset of the register from the base address specified by the module base address register (MBAR) in the SIM41. The first number is the offset for channel 1; the second number is the offset for channel 2. The numbers above the register represent the bit position in the register. The register contains the mnemonic for the bit. The value of these bits after a hardware reset is shown below the register. The access privilege is shown in the lower right-hand corner.

NOTE

A CPU32 RESET instruction will not affect the MCR but will reset all other registers in the DMA module as though a hardware reset occurred. The term DMA is used to reference either channel 1 or channel 2, since the two are functionally equivalent.

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6.7.1 Byte Transfer Counter Register (BTC)

The BTC is a 32-bit register that contains the number of bytes left to transfer in a given block. This register is accessible in either supervisor or user space. The BTC can always be read or written to when the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

BTC1, BTC2 $794, $7B4

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

U = Unaffected by reset Supervisor/User

This register is decremented by 1, 2, or 4 for each successful operand transfer from source to destination locations. When the BTC decrements to zero and no error has occurred, the CSR DONE bit is set. In the external request mode, the $\overline{\text{DONEx}}$ handshake line is also asserted when the BTC is decremented to zero.

If the operand size is byte, then the register is always decremented by 1. If the operand size is word and the starting count is even word, the register is decremented by 2. If the operand size is word and the byte count is not a multiple of 2, the CSR CONF bit is set, and a transfer does not occur. If the operand size is long word and the count is a multiple of four, then the register is decremented by 4. If the operand size is long word and the byte count is not a multiple of 4, the CSR CONF bit is set, and a transfer does not occur. If the STR bit is set with a zero count in the BTC, the CONF bit is set, and the STR bit is cleared.

When read, this register always contains the count for the next access. If a bus error terminates the transfer, this register contains the count for the next access that would have been run had the error not occurred.

6.7.2 Channel Control Register (CCR)

The CCR controls the configuration of the DMA channel. This register is accessible in either supervisor or user space. The CCR can always be read or written to when the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

CCR1, CCR2 $788, $7A8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTB	INTN	INTE	ECO	SAPI	DAPI	SSIZE		DSIZE		REQ		BB		S/D	STR
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	0

U = Unaffected by reset Supervisor/User

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INTB—Interrupt Breakpoint

Setting the interrupt breakpoint bit sets the BRKP bit in the CSR. The logic AND of INTB and BRKP generates an interrupt request.

1 = Enables an $\overline{\text{IRQx}}$ when a breakpoint is recognized and the channel is the bus master.

0 = Does not enable an $\overline{\text{IRQx}}$ when a breakpoint is recognized and the channel is the bus master.

INTN—Interrupt Normal

1 = Enables $\overline{\text{IRQx}}$ when the channel finishes a transfer without an error condition (CSR DONE bit is set).

0 = Does not enable $\overline{\text{IRQx}}$ when the channel finishes a transfer without an error condition.

INTE—Interrupt Error

1 = Enables $\overline{\text{IRQx}}$ when the channel encounters an error on source read (CSR BES bit is set), destination write (CSR BED bit is set), or configuration for channel setup (CSR CONF bit is set).

0 = Does not enable $\overline{\text{IRQx}}$ when the channel encounters an error on source read, destination write, or configuration for channel setup.

ECO—External Control Option

If request generation is programmed to be internal (REQ bits = 00), this bit has no effect.

Single-Address Mode—This bit defines the direction of transfer.

1 = If request generation is programmed to be external (REQ = 1x), the requesting device receives the data (read from memory), and the control signals ($\overline{\text{DREQx}}$, $\overline{\text{DACKx}}$, and $\overline{\text{DONEx}}$) are used by the requesting device to write data during the source (read) portion of the transfer.

0 = If request generation is programmed to be external (REQ = 1x), the requesting device provides the data (write to memory), and the control signals ($\overline{\text{DREQx}}$, $\overline{\text{DACKx}}$, and $\overline{\text{DONEx}}$) are used by the requesting device to provide data during the destination (write) portion of the transfer.

Dual-Address Mode—This bit defines which device generates requests.

1 = If request generation is programmed to be external (REQ = 1x), the source device generates the request, and the control signals ($\overline{\text{DREQx}}$, $\overline{\text{DACKx}}$, and $\overline{\text{DONEx}}$) are part of the source (read) portion of the transfer.

0 = If request generation is programmed to be external (REQ = 1x), the destination device generates the request, and the control signals ($\overline{\text{DREQx}}$, $\overline{\text{DACKx}}$, and $\overline{\text{DONEx}}$) are part of the destination (write) portion of the transfer.

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SAPI—Source Address Pointer Increment

1 = The SAR is incremented by 1, 2, or 4 after each transfer, according to the source size. The address that is written into the SAR points to a memory block and is incremented to complete the data transfer.

0 = The SAR is not incremented during operand transfer. The address that is written into the SAR points to a peripheral device and is used for the complete data transfer.

DAPI—Destination Address Pointer Increment

1 = The DAR is incremented by 1, 2, or 4 after each transfer, according to the source size. The address that is written into the DAR points to a memory block and is incremented to complete the data transfer.

0 = The DAR is not incremented during operand transfer. The address that is written into the DAR points to a peripheral device and is used for the complete data transfer.

SSIZE—Source Size Control Field

This field controls the size of the source (read) bus cycle that the DMA channel is running. Table 6-1 defines these bits.

Table 6-1. SSIZEx Encoding

Bit 9	Bit 8	Definition
0	0	Long Word
0	1	Byte
1	0	Word
1	1	Not Used

DSIZE—Destination Size Control Field

This field controls the size of the destination (write) bus cycle that the DMA channel is running. Table 6-2 defines these bits.

Table 6-2. DSIZEx Encoding

Bit 7	Bit 6	Definition
0	0	Long Word
0	1	Byte
1	0	Word
1	1	Not Used

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REQ—Request Generation Field

This field controls the mode of operation the DMA channel uses to make an operand transfer request. Table 6-3 defines these bits.

Table 6-3. REQx Encoding

Bit 5	Bit 4	Definition
0	0	Internal Request at Programmable Rate
0	1	Reserved
1	0	External Request Burst Transfer Mode
1	1	External Request Cycle Steal

BB—Bus Bandwidth Field

This field controls the percentage of 1024 clock periods of the IMB that the DMA channel can use during internal requests only (REQx = 00). Table 6-4 defines these bits.

Table 6-4. BBx Encoding and Bus Bandwidth

BB Field		Definition	Bus Bandwidth (Clock Periods)
Bit 3	Bit 2		
0	0	25%	256
0	1	50%	512
1	0	75%	768
1	1	100%	1024

S/D—Single-/Dual-Address Transfer

1 = The DMA channel runs single-address transfers from a peripheral to memory or from memory to a peripheral. The destination holding register is not used for these transfers because the data is transferred directly into the destination location. The MC68341 on-chip peripherals do not support single-address transfers.

0 = The DMA channel runs dual-address transfers.

STR—Start

This bit is cleared by a hardware/software reset, writing a logic zero, or setting one of the following CSR bits: DONE, BES, BED, CONF, or BRKP. The STR bit cannot be set when the CSR IRQ bit is set. The DMA channel cannot be started until the CSR DONE, BES, BED, CONF, and BRKP bits are cleared.

Internal Request Mode:

1 = The DMA transfer starts as soon as this bit is set.

0 = The DMA transfer can be stopped by clearing this bit.

External Request Mode:

1 = Setting this bit allows the DMA to start the transfer when a $\overline{\text{DREQx}}$ input is received from an external device.

0 = The DMA transfer can be stopped by clearing this bit.

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NOTE

If any fields in the CCR are modified while the channel is active, that change is effective immediately. To avoid any problems with changing the setup for the DMA channel, a zero should be written to the STR bit in the CCR to halt the DMA channel at the end of the current bus cycle.

6.7.3 Channel Status Register (CSR)

The CSR contains the channel status information. This register is accessible in either supervisor or user space. The CSR can always be read or written to when the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

CSR1, CSR2 $78A, $7AA

7	6	5	4	3	2	1	0
IRQ	DONE	BES	BED	CONF	BRKP	0	0
RESET 0	0	0	0	0	0	0	0

Supervisor/User

IRQ—Interrupt Request

This bit is the logical OR of the DONE, BES, BED, CONF, and BRKP bits and is cleared when they are all cleared. IRQ is positioned to allow conditional testing as a signed binary integer. The state of this bit is not affected by the interrupt enable bits in the CCR. The STR bit in the CCR cannot be set when this bit is set; all error status bits, except the BRKP bit, must be cleared before the STR bit can be set.

1 = An interrupt condition has occurred.
0 = An interrupt condition has not occurred.

DONE—DMA Done

1 = The DMA channel has terminated normally.
0 = The DMA channel has not terminated normally. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

BES—Bus Error on Source

1 = The DMA channel has terminated with a bus error during the read bus cycle.
0 = The DMA channel has not terminated with a bus error during the read bus cycle. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

BED—Bus Error on Destination

1 = The DMA channel has terminated with a bus error during the write bus cycle.
0 = The DMA channel has not terminated with a bus error during the write bus cycle. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

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CONF—Configuration Error

A configuration error results when either the SAR or the DAR contains an address that does not match the port size specified in the CCR and the BTC register does not match the larger port size or is zero.

1 = The CCR STR bit is set, and a configuration error is present.
0 = The CCR STR bit is set, and no configuration error exists. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

BRKP—Breakpoint

1 = The breakpoint signal was set during a DMA transfer.
0 = The breakpoint signal was not set during a DMA transfer. This bit is cleared by writing a logic one or by a hardware reset. Writing a zero has no effect.

Bits 1, 0—Reserved by Motorola

NOTE

The CSR is cleared by writing $7C to its location. The DMA channel cannot be started until the CSR DONE, BES, BED, CONF and BRKP bits are cleared.

6.7.4 Destination Address Register (DAR)

The DAR is a 32-bit register that contains the address of the destination operand used by the DMA to write to memory or peripheral registers. This register is accessible in either supervisor or user space. The DAR can always be read or written to when the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

DAR1, DAR2 $790, $7B0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

U = Unaffected by reset Supervisor/User

During the DMA write cycle, this register drives the address on the address bus. This register can be programmed to increment (CCR DAPI bit set) or remain constant (CCR DAPI bit cleared) after each operand transfer.

The register is incremented using unsigned arithmetic and will roll over if overflow occurs. For example, if a register contains $FFFFFFFF and is incremented by 1, it will roll over to $00000000. This register can be incremented by 1, 2, or 4, depending on the size of the operand and the starting address. If the operand size is byte, the register is always incremented by 1. If the operand size is word and the starting address is word aligned, the

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register is incremented by 2. If the operand size is long word and the address is word aligned, the register is incremented by 4. The DAR value must be aligned to an word boundary if the transfer size is word or long word; otherwise, the CSR CONF bit is set, and the transfer does not occur.

When read, this register always contains the next destination address. If a bus error terminates the transfer, this register contains the next destination address that would have been run had the error not occurred.

6.7.5 Function Code Register (FCR)

The FCR contains the source and destination function codes for the channel. This register is accessible in either supervisor or user space. The FCR can always be read or written to when the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

FCR1, FCR2 $78B, $7AB

7	6	5	4	3	2	1	0
SFC				DFC			
RESET:							
U	U	U	U	U	U	U	U

U = Unaffected by reset Supervisor/User

SFC—Source Function Code Field

This field specifies the source access to a certain address space type. The source function code bits 3–0 are defined in Table 6-5.

DFC—Destination Function Code Field

This field specifies the destination access to a certain address space type. The destination function code bits 3–0 are defined in Table 6-5.

Table 6-5. Address Space Encoding

Source/Destination Function Code Bits				
3	**2**	**1**	**0**	**Address Spaces**
0	0	0	0	Reserved (Motorola)
0	0	0	1	User Data Space
0	0	1	0	User Program Space
0	0	1	1	Reserved (User)
0	1	0	0	Reserved (Motorola)
0	1	0	1	Supervisor Data Space
0	1	1	0	Supervisor Program Space
0	1	1	1	CPU Space
1	x	x	x	DMA Space

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NOTE

Although SFC3/DFC3 can be set for DMA transfers to distinguish the source or destination space from other data or program spaces, it is not required to be set. Since the CPU32 currently has only 3-bit SFC and DFC capability, it cannot emulate SFC3 = 1 or DFC3 = 1 at this time. However, it is recommended that SFC3/DFC3 be set to one to distinguish DMA and CPU accesses during debug.

6.7.6 Interrupt Register (INTR)

The INTR contains the priority level for the channel interrupt request and the 8-bit vector number of the interrupt. The register can be read or written to at any time while in supervisor mode and while the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

INTR1, INTR2 $784, $7A4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	INTL			INTV							
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Supervisor Only

Bits 15–11—Reserved by Motorola

INTL—Interrupt Level Bits

Each module that can generate interrupts has an interrupt level field. The interrupt level field contains the priority level of the interrupt for its associated channel. The priority level encoded in these bits is sent to the CPU32 on the appropriate $\overline{\text{IRQx}}$ signal. The CPU32 uses this value to determine servicing priority. See **Section 5 CPU030** for more information.

INTV—Interrupt Vector Bits

Each module that can generate interrupts has an interrupt vector field. The interrupt vector field contains the vector number of the interrupt for its associated channel. This 8-bit field indicates the offset from the base of the vector table where the address of the exception handler for the specified interrupt is located. The INTV field is reset to $0F, which indicates an uninitialized interrupt condition. See **Section 5 CPU030** for more information.

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6.7.7 Module Configuration Register (MCR)

The MCR controls the DMA channel configuration. Each DMA channel has an MCR. This register can be either read or written when the channel is enabled and is in the supervisor state. The MCR is not affected by a CPU32 RESET instruction.

MCR1, MCR2 $780, $7A0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STP	FRZ1	FRZ0	SE	0	ISM			SUPV	MAID			IARB			
RESET:															
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Supervisor Only

STP—Stop Bit

1 = Setting the STP bit stops all clocks within the DMA module except for the clock from the IMB. The clock from the IMB remains active to allow the CPU32 access to the MCR. The clock stops on the low phase of the clock and remains stopped until the STP bit is cleared by the CPU32 or a hardware reset. Accesses to DMA module registers while in stop mode produce a bus error. The DMA module should be disabled in a known state before setting the STP bit. The STP bit should be set prior to executing the LPSTOP instruction to reduce overall power consumption.

0 = The channel operates in normal mode.

NOTE

The DMA module uses only one STP bit for both channels. A read or write to either MCR accesses the same STP control bit.

FRZ1, FRZ0—Freeze

These bits determine the action taken when the FREEZE signal is asserted on the IMB when the CPU32 has entered background debug mode. The DMA module negates $\overline{BR}$ and keeps it negated until FREEZE is negated or reset. Table 6-6 lists the action taken for each bit combination.

Table 6-6. FRZx Control Bits

FRZ1	FRZ0	Action
0	0	Ignore FREEZE
0	1	Reserved
1	0	Freeze on Boundary*
1	1	Reserved

*The boundary is defined as any bus cycle by the DMA module.

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NOTE

The DMA module uses only one set of FRZx bits for both channels. A read or write to either MCR accesses the same FRZx control bits.

SE—Single-Address Enable

This bit is implemented for future M68300 family compatibility.

1 = In single-address mode, the external data bus is driven during a DMA transfer.
0 = In single-address mode, the external data bus remains in a high-impedance state during a DMA transfer (used for intermodule DMA).

In dual-address mode, the SE bit has no effect.

Bit 11—Reserved by Motorola

ISM2–ISM0—Interrupt Service Mask

These bits contain the interrupt service mask level for the channel. When the interrupt service level on the IMB is greater than the interrupt service mask level, the DMA vacates the bus and negates $\overline{BR}$ until the interrupt service level is less than or equal to the interrupt service mask level.

NOTE

When the CPU32 status register (SR) interrupt priority mask bits I2–I0 are at a higher level than the DMA ISM bits, the DMA channel will not start. The channel will begin operation when the level of the SR I2–I0 bits is less than or equal to the level of the DMA ISM bits.

SUPV—Supervisor/User

The value of this bit has no effect on registers permanently defined as supervisor-only access.

1 = The DMA channel registers defined as supervisor/user reside in supervisor data space and are only accessible from supervisor programs.
0 = The DMA channel registers defined as supervisor/user reside in user data space and are accessible from either supervisor or user programs.

MAID—Master Arbitration ID

These bits establish bus arbitration priority level among modules that have the capability of becoming bus master. For the MC68341, the MAID bits are used to arbitrate between DMA channel 1 and channel 2. If both channels are programmed with the same MAID level, channel 1 will have priority. These bits are implemented for future M68300 family compatibility. In the MC68341, only the SIM and the DMA can be bus masters. However, future versions of the M68300 family may incorporate other modules that may also be bus masters. For these devices, the MAID bits will be required. For the MAID bits, zero is the lowest priority and seven is the highest priority.

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IARB — Interrupt Arbitration ID

Each module that generates interrupts has an IARB field. These bits are used to arbitrate for the bus in the case that two or more modules simultaneously generate an interrupt at the same priority level. No two modules can share the same IARB value. The reset value of the IARB field is $0, which prevents the DMA module from arbitrating during the interrupt acknowledge cycle. The system software should initialize the IARB field to a value from $F (highest priority) to $1 (lowest priority).

NOTE

The DMA module uses only one set of IARB bits for both channels. A read or write to either MCR accesses the same IARB control bits.

6.7.8 Source Address Register (SAR)

The SAR is a 32-bit register that contains the address of the source operand used by the DMA to access memory or peripheral registers. This register is accessible in either supervisor or user space. The SAR can always be read or written to when the DMA module is enabled (i.e., the STP bit in the MCR is cleared).

SAR1, SAR2 $78C, $7AC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
RESET: U	U	U	U	U	U	U	U	U	U	U	U	U	U	U	U

U = Unaffected by reset Supervisor/User

During the DMA read cycle, the SAR drives the address on the address bus. This register can be programmed to increment (CCR SAPI bit set) or remain constant (CCR SAPI bit cleared) after each operand transfer.

The register is incremented using unsigned arithmetic and will roll over if overflow occurs. For example, if the register contains $FFFFFFFF and is incremented by 1, it will roll over to $00000000. This register is incremented by 1, 2, or 4, depending on the size of the operand and the memory starting address. If the operand size is byte, then the register is always incremented by 1. If the operand size is word and the starting address is word aligned, then the register is incremented by 2. If the operand size is long word and the address is word aligned, then the register is incremented by 4. The SAR value must be aligned to an word boundary if the transfer size is word or long word; otherwise, the CSR CONF bit is set, and the transfer does not occur.

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When read, this register always contains the next source address. If a bus error terminates the transfer, this register contains the next source address that would have been run had the error not occurred.

6.8 DATA PACKING

The internal DHR is a 32-bit register that can serve as a buffer register for the data being transferred during dual-address DMA cycles. No address is specified since this register can not be addressed by the programmer. The DHR allows the data to be packed and unpacked by the DMA during the dual-address transfer. For example, if the source operand size is byte and the destination operand size is word, then for each DMA request two byte read cycles occur, followed by one word write cycle (see Figure 6-16). The two bytes of data are buffered in the DHR until the destination (write) word cycle occurs. The DHR allows for packing and unpacking of operands for the following sizes: bytes to words, bytes to long words, words to long words, words to bytes, long words to bytes, and long words to words.

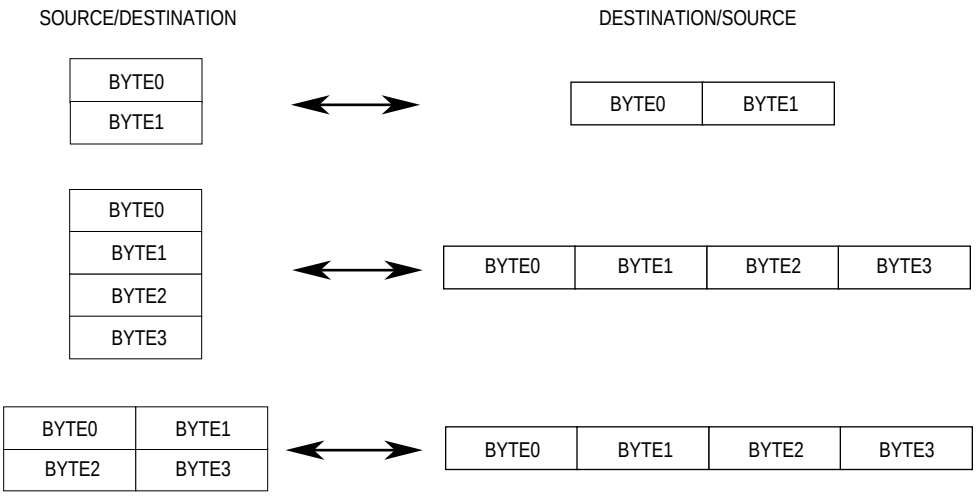

Figure 6-16. Packing and Unpacking of Operands

For normal transfers aligned with the size and address, only two bus cycles are required for each transfer: a read from the source and a write to the destination.

6.9 DMA CHANNEL INITIALIZATION SEQUENCE

The following paragraphs describe DMA channel initialization and operation. If the DMA capability of the MC68341 is being used, the initialization steps should be performed during the part initialization sequence. The mode operation steps should be performed to start a DMA transfer. The $\overline{\text{DONEx}}$ pin requires an external pullup resistor even if operating only in the internal request mode.

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6.9.1 DMA Channel Configuration

The following steps can be accomplished in any order when initializing the DMA channel. These steps need to be performed for each channel used.

Module Configuration Register (MCR)

- Clear the stop bit (STP) for normal operation. (Only one STP bit exists for both channels.)
- Select whether to respond to or ignore FREEZE (FRZx bits). (Only one set of FRZx bits exists for both channels.)
- If desired, enable the external data bus operation in single-address mode (SE bit).
- Program the interrupt service mask to set the level below which interrupts are ignored during a DMA transfer (ISM bits). The channel will begin operation when the level of the CPU32 SR I2-I0 bits is less than or equal to the level of the DMA ISM bits.
- Select the access privilege for the supervisor/user registers (SUPV bit).
- Program the master arbitration ID (MAID) to establish priority on the IMB between both DMA channels. Note that the two DMA channels should have distinct MAIDs if both channels are being used. (If they are programmed the same, channel 1 has priority.)
- Select the interrupt arbitration level for the DMA channel (IARB bits). (Only one set of IARB bits exists for both channels.)

Interrupt Register (INTR)

- Program the interrupt priority level for the channel interrupt (INTL bits).
- Program the vector number for the channel interrupt (INTV bits).

Channel Control Register (CCR)

- If desired, enable the interrupt when breakpoint is recognized and the channel is the bus master (INTB bit).
- If desired, enable the interrupt when done without an error condition (INTN bit).
- If desired, enable the interrupt when the channel encounters an error (INTE bit).
- Select the direction of transfer if in single-address mode (ECO bit), or select which device generates requests if in dual-address mode.

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6.9.1.1 DMA CHANNEL OPERATION IN SINGLE-ADDRESS MODE. The following steps are required to begin a DMA transfer in single-address mode.

Channel Control Register (CCR)

- Write a zero to the start bit (STR) to prevent the channel from starting the transfer prematurely.
- Select the amount by which to increment the source address for a read cycle (SAPI bit) or the destination address for a write cycle (DAPI bit).
- Define the transfer size by selecting the source size for a read cycle (SSIZE field) or by selecting the destination size for a write cycle (DSIZE field).
- Select external burst request mode or external cycle steal request mode (REQ field).
- Set the S/D bit for signal-address transfer.

Channel Status Register (CSR)

- Clear the CSR by writing $7C into it. The DMA cannot be started until the DONE, BES, BED, CONF, and BRKP bits are cleared.

Function Code Register (FCR)

- Encode the source function code for a read cycle or the destination function code for a write cycle.

Address Register (SAR or DAR)

- Write the source address for a read cycle or the destination address for a write cycle.

Byte Transfer Counter (BTC)

- Encode the number of bytes to be transferred.

Channel Control Register (CCR)

- Write a one to the start bit (STR) to allow the transfer to begin.

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6.9.1.2 DMA CHANNEL OPERATION IN DUAL-ADDRESS MODE. The following steps are required to begin a DMA transfer in dual-address mode.

Channel Control Register (CCR)

- Write a zero to the start bit (STR) to prevent the channel from starting the transfer prematurely.
- Select the amount by which to increment the source and destination addresses (SAPI and DAPI bits).
- Select the source and destination sizes (SSIZE and DSIZE fields).
- Select internal request, external burst request mode, or external cycle steal request mode (REQ field).
- If using internal request, select the amount of bus bandwidth to be used by the DMA (BB field).
- Clear the S/D bit for dual-address transfer.

Channel Status Register (CSR)

- Clear the CSR by writing $7C into it. The DMA cannot be started until the DONE, BES, BED, CONF, and BRKP bits are cleared.

Function Code Register (FCR)

- Encode the source and destination function codes.

Address Registers (SAR and DAR)

- Write the source and destination addresses.

Byte Transfer Counter (BTC)

- Encode the number of bytes to be transferred.

Channel Control Register (CCR)

- Write a one to the start bit (STR) to allow the transfer to begin.

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6.9.2 DMA Channel Example Configuration Code

The following are examples of configuration sequences for a DMA channel in single- and dual-addressing modes.

This common set of equates is used by all of the following examples:

```
*****************************************************************************
* SIM41 equates
*****************************************************************************
MBAR        EQU         $0003FF00               Address of SIM41 Module Base Address Reg.
MODBASE                 EQU         $FFFFF000               SIM41 MBAR address value
PPARC       EQU         $29                     Port C pin assignment register
*****************************************************************************
* DMA Channel 1 equates
DMACH1      EQU         $780                    Offset from MBAR for channel 1 regs
DMAMCR1                 EQU         $0                      MCR for channel 1
* Channel 1 register offsets from channel 1 base address
DMAINT1     EQU         $4                      interrupt register channel 1
DMACCR1     EQU         $8                      control register channel 1
DMACSR1     EQU         $A                      status register channel 1
DMAFCR1     EQU         $B                      function code register channel 1
DMASAR1     EQU         $C                      source address register channel 1
DMADAR1     EQU         $10                     destination address register channel 1
DMABTC1     EQU         $14                     byte transfer count register channel 1
*****************************************************************************
```

In addition to the initialization shown in each example, the Port C Pin Assignment Register should also be configured if DTC, RDYx, or delayed DACKx signals are used:

```
*****************************************************************************
* PPARC initialization for DMA signal functionality
* The following example selects RDY1 and delayed DACKx functionality for
* DMA channel 1 - other pins unchanged:
            OR.B        #$50,MODBASE+PPARC          Select RDY1 & delayed DACK1 funct
*****************************************************************************
```

Example 1: External Burst Request Generation, Single-Address Transfers.

```
*****************************************************************************
* MC68341 basic DMA channel register initialization example code.
* This code is used to initialize the 68341's internal DMA channel
* registers, providing basic functions for operation.
* The code sets up channel 1 for external burst request generation,
* single-address mode, long word size transfers.
* Control signals are asserted on the DMA read cycle.
*****************************************************************************
* Equates
*****************************************************************************
SARADD      EQU         $10000      source address
```


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```
NUMBYTE  EQU        $C                      number of bytes to transfer

*****************************************************************************
* Initialize DMA Channel 1
*****************************************************************************
            LEA         MODBASE+DMACH1,A0           Pointer to channel 1

* Initialize DMA channel 1 MCR
* Normal Operation, ignore FREEZE, single-address mode. ISM field at 2. Make
* sure SR I2-I0 bits are less than or equal to ISM bits for channel startup.
* Supervisor/user reg. unrestricted, MAID field at 7. IARB priority at 1.
            MOVE.W    #$1271,(A0)

* Clear channel control reg.
* Clear STR (start) bit to prevent the channel from starting a transfer early.
            CLR.W     DMACCR1(A0)

* Initialize interrupt reg.
* Interrupt priority at 7, interrupt vector at $42.
            MOVE.W    #$0742,DMAINT1(A0)

* Initialize channel status reg.
* Clear the DONE, BES, BED, CONF and BRKP bits to allow channel to startup.
            MOVE.B    #$7C,DMACSR1(A0)

* Initialize function code reg.
* DMA space, user data space for source.
            MOVE.B    #$99,DMAFCR1(A0)

* Initialize source operand address
* Source address is equal to $10000.
            MOVE.L    SARADD,DMASAR1(A0)

* Initialize the byte transfer count reg.
* The number of bytes to be transferred is $C or 3 long words
            MOVE.L    NUMBYTE,DMABTC1(A0)

* Channel control reg. init. and Start DMA transfers
* No interrupts are enabled, source (read) cycle. Increment source
* address, source size is long word, REQ is external burst request.
* Single-address mode, start the DMA transfers.
            MOVE.W    #$1823,DMACCR1(A0)

            END
*****************************************************************************
```


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Example 2: Internal Request Generation, Memory to Memory Transfers.

```
*****************************************************************************
* MC68341 basic DMA channel register initialization example code.
* This code is used to initialize the 68341's internal DMA channel
* registers, providing basic functions for operation.
* The code sets up channel 1 for internal request generation
* memory to memory transfers.
*****************************************************************************
* Equates
*****************************************************************************
SARADD   EQU     $6000          source address
DARADD   EQU     $8000          destination address
NUMBYTE  EQU     $E             number of bytes to transfer

*****************************************************************************
* Initialize DMA Channel 1
*****************************************************************************
         LEA     MODBASE+DMACH1,A0          Pointer to channel 1

* Initialize DMA channel 1 MCR
* Normal Operation, ignore FREEZE, dual-address mode. ISM field at 3. CPU32
* SR I2-I0 bits must be less than or equal to ISM bits for channel startup.
* Supervisor/user reg. unrestricted, MAID field at 3. IARB priority at 4.
         MOVE.W  #$0334,(A0)

* Clear channel control reg.
* Clear STR (start) bit to prevent the channel from starting a transfer early.
         CLR.W   DMACCR1(A0)

* Initialize interrupt reg.
* Interrupt priority at 7, interrupt vector at $42.
         MOVE.W  #$0742,DMAINT1(A0)

* Initialize channel status reg.
* Clear the DONE, BES, BED, CONF and BRKP bits to allow channel to startup.
         MOVE.B  #$7C,DMACSR1(A0)

* Initialize function code reg.
* DMA space, supervisor data space for source and destination.
         MOVE.B  #$DD,DMAFCR1(A0)

* Initialize source operand address
* Source address is equal to $6000.
         MOVE.L  SARADD,DMASAR1(A0)

* Initialize destination operand address
* Destination address is equal to $8000.
```


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```
            MOVE.L      DARADD,DMADAR1(A0)

* Initialize the byte transfer count reg.
* The number of bytes to be transferred is $E or 7 words
            MOVE.L      NUMBYTE,DMABTC1(A0)

* Channel control reg. init. and Start DMA transfers
* No interrupts are enabled, destination (write) cycle. Increment source and
* destination addresses,source size is word, destination size is word.
* REQ is internal. 100% of bus bandwidth, dual-address transfers,
* start the DMA transfers.
            MOVE.W      #$0E8D,DMACCR1(A0)

            END
*****************************************************************************
```

Example 3: Internal Request Generation, Memory Block Initialization.

```
*****************************************************************************
* MC68341 basic DMA channel register initialization example code.
* This code is used to initialize the 68341's internal DMA channel
* registers, providing basic functions for operation.
* The code sets up channel 1 for internal request generation
* to perform a memory block initialization for 100 bytes.
*****************************************************************************
* Equates
*****************************************************************************
SARADD    EQU       $6000       source address
DARADD    EQU       $8000       destination address
NUMBYTE   EQU       $64         number of bytes to transfer

*****************************************************************************
* Initialize DMA Channel 1
*****************************************************************************
            LEA         MODBASE+DMACH1,A0                 Pointer to channel 1

* Initialize DMA channel 1 MCR
* Normal Operation, ignore FREEZE, dual-address mode. ISM field at 3. CPU32
* SR I2-I0 bits must be less than or equal to ISM bits for channel startup.
* Supervisor/user reg. unrestricted, MAID field at 3.
* IARB priority at 4.
            MOVE.W      #$0334,(A0)

* Clear channel control reg.
* Clear STR (start) bit to prevent the channel from starting a transfer early.
            CLR.W       DMACCR1(A0)

* Initialize interrupt reg.
```


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```
* Interrupt priority at 7, interrupt vector at $42.
            MOVE.W    #$0742,DMAINT1(A0)

* Initialize channel status reg.
* Clear the DONE, BES, BED, CONF and BRKP bits to allow channel to startup.
            MOVE.B    #$7C,DMACSR1(A0)

* Initialize function code reg.
* DMA space, supervisor data space for source and destination.
            MOVE.B    #$DD,DMAFCR1(A0)

* Initialize source operand address
* Source address is equal to $6000.
            MOVE.L    SARADD,DMASAR1(A0)

* Initialize destination operand address
* Destination address is equal to $8000.
            MOVE.L    DARADD,DMADAR1(A0)

* Initialize the byte transfer count register
* The number of bytes to be transferred is $64 or 50 words
            MOVE.L    NUMBYTE,DMABTC1(A0)

* Channel control reg. init. and Start DMA transfers
* No interrupts are enabled, destination (write) cycle.
* Source address is not incremented. Increment the destination address.
* Source size is word, destination size is word. REQ is internal.
* 100% of bus bandwidth, dual-address transfers, start the DMA transfers.
            MOVE.W    #$068D,DMACCR1(A0)

            END
*******************************************************************************
```

Example 4: Cycle Steal Request Generation, Dual-Address Transfers.

```
*******************************************************************************
* MC68341 basic DMA channel register initialization example code.
* This code is used to initialize the 68341's internal DMA channel
* registers, providing basic functions for operation.
* The code sets up channel 1 for external cycle steal request generation,
* dual-address transfers. DMA 16-bit wide data from an odd address to an
* even address. Control signals are asserted on the DMA read cycle.
*******************************************************************************
* Equates
*******************************************************************************
SARADD    EQU       $6001      source address is an ODD address
DARADD    EQU       $10000     destination address is and EVEN address
NUMBYTE   EQU       $14        number of bytes to transfer
```


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```
*****************************************************************************
* Initialize DMA Channel 1
*****************************************************************************
            LEA         MODBASE+DMACH1,A0               Pointer to channel 1

* Initialize DMA channel 1 MCR
* Normal Operation, ignore FREEZE, dual-address mode. ISM field at 0. CPU32
* SR I2-I0 bits must be less than or equal to ISM bits for channel startup.
* Supervisor/user reg. unrestricted, MAID field at 4. IARB priority at 8.
            MOVE.W    #$00C8,(A0)

* Clear channel control reg.
* Clear STR (start) bit to prevent the channel from starting a transfer early.
            CLR.W     DMACCR1(A0)

* Initialize interrupt reg.
* Interrupt priority at 7, interrupt vector at $42.
            MOVE.W    #$0742,DMAINT1(A0)

* Initialize channel status reg.
* Clear the DONE, BES, BED, CONF and BRKP bits to allow channel to startup.
            MOVE.B    #$7C,DMACSR1(A0)

* Initialize function code reg.
* DMA space, supervisor data space for source and destination.
            MOVE.B    #$DD,DMAFCR1(A0)

* Initialize source operand address
* Source address is equal to $6001, and odd address.
            MOVE.L    SARADD,DMASAR1(A0)

* Initialize destination operand address
* Destination address is equal to $10000, and even address.
            MOVE.L    DARADD,DMADAR1(A0)

* Initialize the byte transfer count register
* The number of bytes to be transferred is $14 or 20 bytes
            MOVE.L    NUMBYTE,DMABTC1(A0)

* Channel control reg. init. and Start DMA transfers
* No interrupts are enabled, source (read) cycle.
* Increment the source and destination addresses.
* Source size is byte, destination size is word. REQ is external cycle steal.
* dual-address transfers, start the DMA transfers.
            MOVE.W    #$1DB1,DMACCR1(A0)

            END
*****************************************************************************
```


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6.10 MC68341 DMA ENHANCEMENTS

The MC68341 DMA module implementation adds three new signals - $\overline{RDY1}$, $\overline{RDY2}$, and $\overline{DTC}$ - and a new delayed $\overline{DACKx}$ operating mode to the original MC68340 DMA. These changes provide additional handshaking flexibility and minimize additional glue logic for single address transfers. $\overline{RDY1}$ and $\overline{RDY2}$ are multiplexed with timer signals $\overline{TGATE}$ and TIN, and $\overline{DTC}$ is multiplexed with FC3. Selection of these multiplexed pin functions, and normal versus delayed $\overline{DACKx}$ assertion, is controlled by programming the Port C Pin Assignment Register in the SIM41. Refer to the PPARC register description in **Section 4 SIM** for initialization information.

6.10.1 $\overline{RDYx}$

Configuring $\overline{TGATE}$/$\overline{RDY1}$ or TIN/$\overline{RDY2}$ as a $\overline{RDYx}$ input for single address transfers automatically enables the ready handshake function for that channel. In this mode, termination of the DMA transfer requires the assertion of both $\overline{DSACKx}$ and $\overline{RDYx}$, instead of just $\overline{DSACKx}$. This feature allows a slow external peripheral device to delay termination of the DMA transfer until it has supplied data or is ready to receive data from memory.

Like $\overline{DSACKx}$, $\overline{RDYx}$ is an asynchronous input which is sampled on the falling edge of CLKOUT, but must be recognized one clock cycle sooner than $\overline{DSACKx}$ to provide the same termination timing. If $\overline{RDYx}$ is asserted for the same clock falling edge or a later edge than $\overline{DSACKx}$, termination of the bus cycle is controlled by $\overline{RDYx}$ and will occur two clocks after $\overline{RDYx}$ is recognized. An early internal $\overline{DSACKx}$ termination (M68300 fast termination or 68000 3-clock termination) is delayed to the earliest external $\overline{DSACKx}$ recognition point, forcing a minimum three clock bus cycle for M68300 transfers, and four clock for 68000 transfers.

$\overline{RDYx}$ can be held asserted between DMA cycles to allow $\overline{DSACKx}$ to control termination of the cycle. Note that fast termination M68300 and 3-clock 68000 cycles are still forced to 3 clocks and 4 clocks, respectively. Note that $\overline{RDYx}$ should not be enabled during dual address mode transfers.

6.10.2 Delayed $\overline{DACKx}$

Delayed $\overline{DACKx}$ operation can be selected during single address transfers to delay assertion of $\overline{DACKx}$ to the peripheral device on reads until memory has provided valid data on the data bus. For transfers from memory to device, $\overline{DACKx}$ is asserted after $\overline{DSACKx}$ is recognized. On device to memory transfers, $\overline{DACKx}$ is asserted with $\overline{AS}$. Delayed $\overline{DACKx}$ programmed without $\overline{RDYx}$ generates a one clock assertion of the $\overline{DACKx}$ pin (except on fast termination cycles). Typically, delayed $\overline{DACKx}$ is programmed with $\overline{RDYx}$ to allow the peripheral to delay termination of the cycle and negation of $\overline{DACKx}$.

6.10.3 $\overline{DTC}$

$\overline{DTC}$ is asserted for one clock at the end of all MC68341 bus cycles when selected (CPU or DMA) to indicate the bus transfer is complete. $\overline{DTC}$ does not assert for bus cycles terminated with a normal bus error or retry, but does assert for cycles terminated with late bus error or late retry.

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$\overline{DTC}$ can be used by device or memory control logic during DMA transfers with $\overline{RDYx}$ to detect the last clock of a bus cycle, before the address or data strobes negate. Since termination of the bus cycle is dependent on two different termination sources ($\overline{DSACKx}$ and $\overline{RDYx}$), neither the device nor the memory can deterministically predict the end of the bus cycle unless the alternate termination is also taken into account. $\overline{DTC}$ provides a direct end-of-transfer indication.

6.10.4 Timing Examples

Figures 6-17—6-20 show timing examples of the the DMA handshake signals used with M68300 bus cycles. $\overline{DREQx}$ timing is not shown in these examples.

Figure 6-17 shows single-address burst reads from two-clock memory with $\overline{RDYx}$ enabled. Although the memory interface in this example is configured for internal fast termination, enabling $\overline{RDYx}$ delays termination until two clocks after $\overline{RDYx}$ is recognized. The first bus cycle shows $\overline{RDYx}$ asserted for the S2 falling edge - this causes the bus cycle to terminate two clocks later for a four clock bus cycle. If $\overline{RDYx}$ remains asserted into the next DMA transfer, it is recognized asserted on the falling edge of S0 and the bus cycle ends two clocks later for a three clock bus cycle.

A single address write with $\overline{RDYx}$ enabled is shown in Figure 6-18. The memory interface in this example again uses fast termination, but end of the bus cycle is delayed by $\overline{RDYx}$. The assertion of $\overline{DS}$ and $\overline{UWE}$/$\overline{LWE}$ is delayed until one clock after $\overline{RDYx}$ is recognized to allow write data from the device to become valid before data strobes are asserted to memory.

Figure 6-19 shows a single address read with both delayed $\overline{DACKx}$ and $\overline{RDYx}$ enabled. $\overline{DACKx}$ remains negated until after $\overline{DSACKx}$ from memory is recognized, allowing memory to place valid data on the bus before $\overline{DACKx}$ is asserted to the peripheral device. The device asserts $\overline{RDYx}$ to signal readiness to complete the transfer.

In Figure 6-20, a single address write with delayed $\overline{DACKx}$ and $\overline{RDYx}$ is shown. $\overline{DACKx}$ asserts immediately with $\overline{AS}$ in this example to select the device and gate its data onto the bus for the memory write. $\overline{RDYx}$ asserts before $\overline{DSACKx}$, delaying the bus cycle until $\overline{DSACKx}$ asserts.

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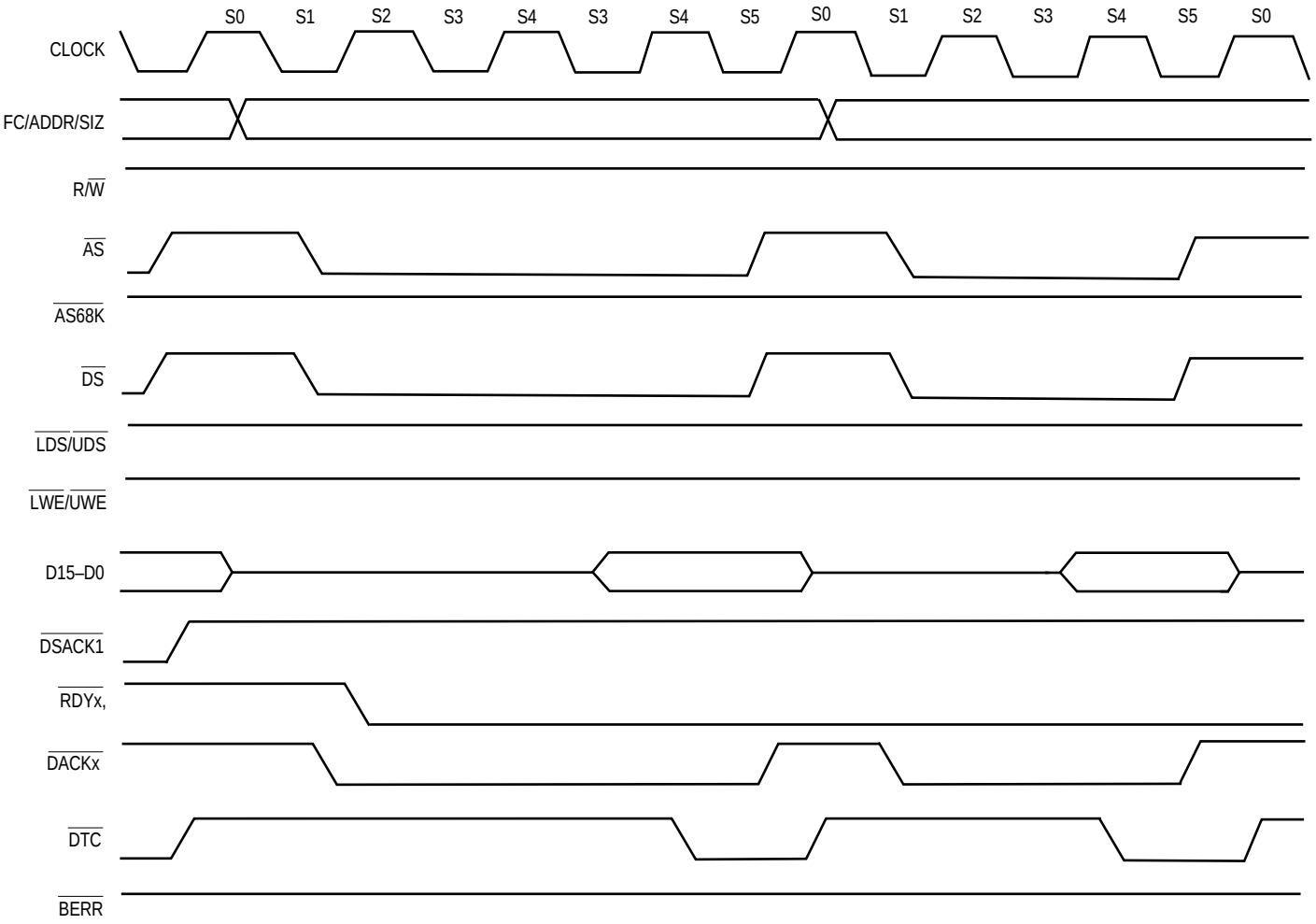

Figure 6-17. M68300 Single Address Read with RDYÅ

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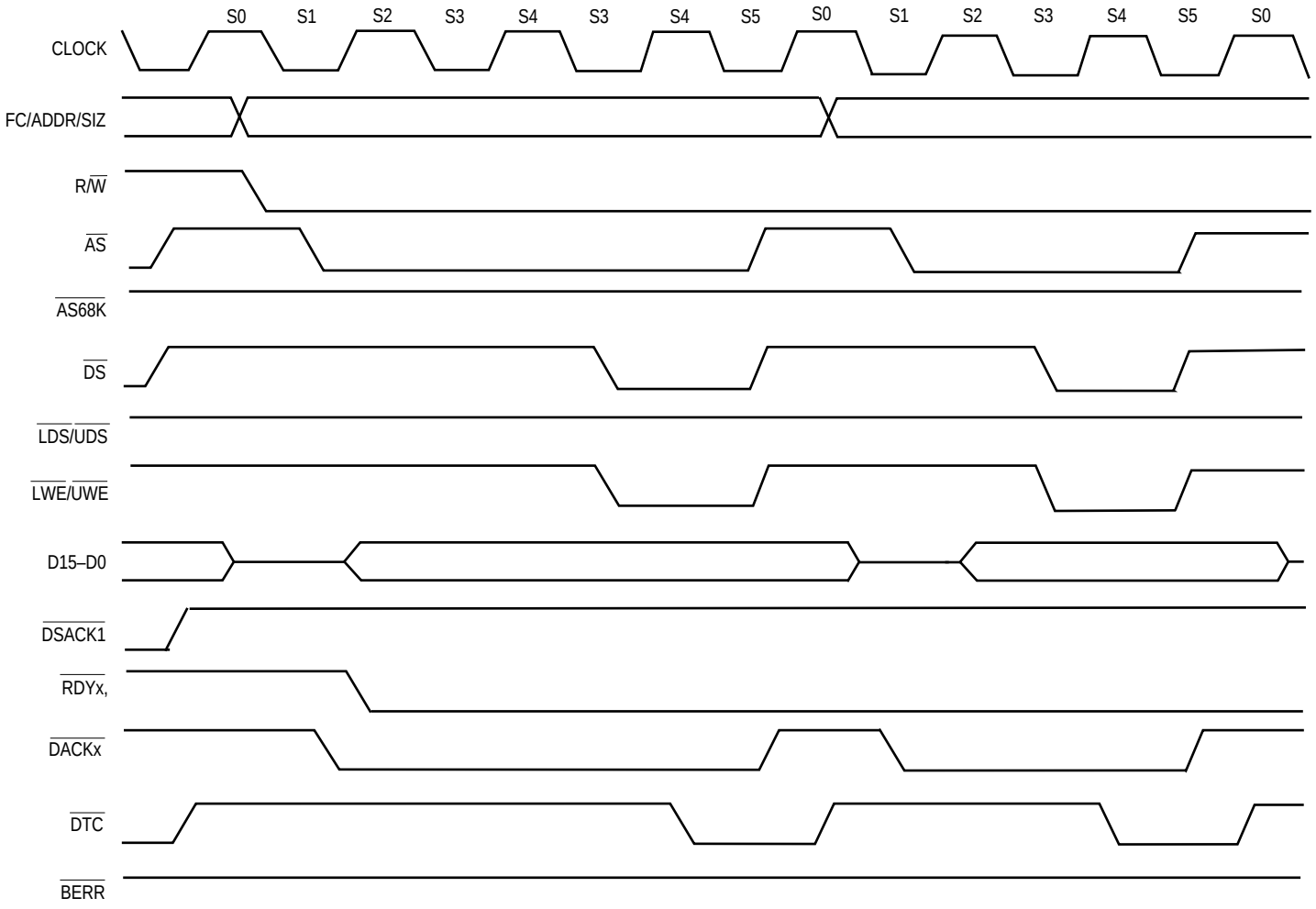

Figure 6-18. M68300 Single Address Write with RDYÅ

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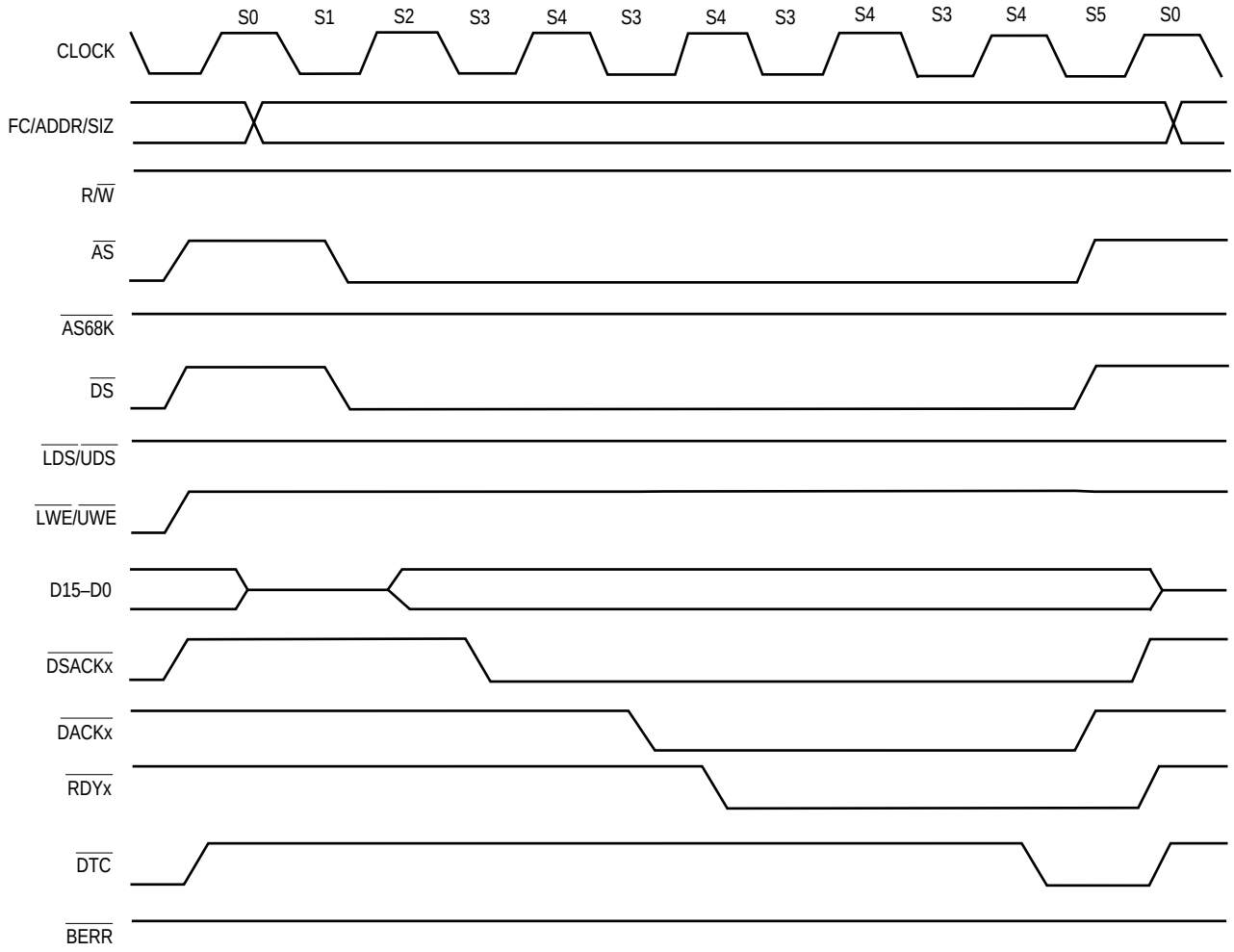

Figure 6-19. M68300 Single Address Read with Delayed DACKÅ and RDYÅ

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SECTION 7
SERIAL MODULE

The MC68341 serial module is a dual universal asynchronous/synchronous receiver/transmitter that interfaces directly to the CPU32 processor via the intermodule bus (IMB). The serial module, shown in Figure 7-1, consists of the following major functional areas:

- Two Independent Serial Communication Channels (A and B)
- Baud Rate Generator Logic
- Internal Channel Control Logic
- Interrupt Control Logic

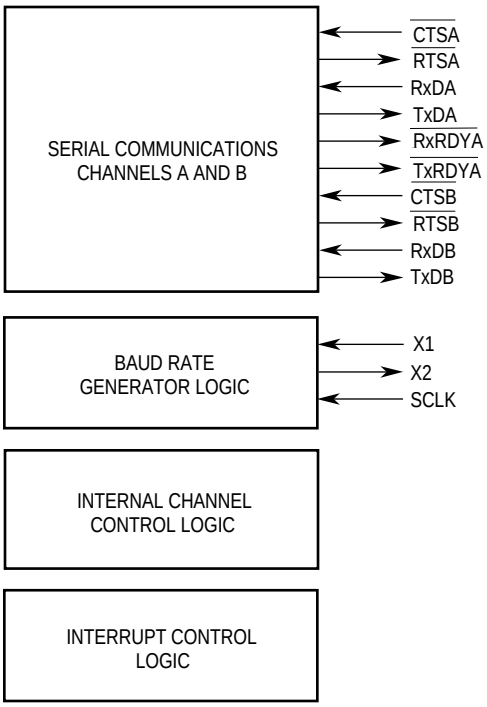

Figure 7-1. Simplified Block Diagram

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7.1 MODULE OVERVIEW

Features of the serial module are as follows:

- Two, Independent, Full-Duplex Asynchronous/Synchronous Receiver/Transmitter Channels
- Quadruple-Buffered Receiver
- Double-Buffered Transmitter
- Independently Programmable Baud Rate for Each Receiver and Transmitter Selectable from:
  - —19 Fixed Rates: 50 to 76.8k Baud
  - —External 1× Clock or 16× Clock
- Programmable Data Format:
  - —Five to Eight Data Bits Plus Parity
  - —Odd, Even, No Parity, or Force Parity
  - —Nine-Sixteenths to Two Stop Bits Programmable in One-Sixteenth Bit Increments
- Programmable Channel Modes:
  - —Normal (Full Duplex)
  - —Automatic Echo
  - —Local Loopback
  - —Remote Loopback
- Automatic Wakeup Mode for Multidrop Applications
- Seven Maskable Interrupt Conditions
- Parity, Framing, and Overrun Error Detection
- False Start-Bit Detection
- Line-Break Detection and Generation
- Detection of Breaks Originating in the Middle of a Character
- Start/End Break Interrupt/Status
- On-Chip Crystal Oscillator

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7.1.1 Serial Communication Channels A and B

Each communication channel provides a full-duplex asynchronous/synchronous receiver and transmitter using an operating frequency independently selected from a baud rate generator or an external clock input.

The transmitter accepts parallel data from the IMB, converts it to a serial bit stream, inserts the appropriate start, stop, and optional parity bits, then outputs a composite serial data stream on the channel transmitter serial data output (TxDx). Refer to **7.3.2.1 Transmitter** for additional information.

The receiver accepts serial data on the channel receiver serial data input (RxDx), converts it to parallel format, checks for a start bit, stop bit, parity (if any), or break condition, and transfers the assembled character onto the IMB during read operations. Refer to **7.3.2.2 Receiver** for additional information.

7.1.2 Baud Rate Generator Logic

The crystal oscillator operates directly from a 3.6864-MHz crystal connected across the X1 input and the X2 output or from an external clock of the same frequency connected to X1. The clock serves as the basic timing reference for the baud rate generator and other internal circuits.

The baud rate generator operates from the oscillator or external TTL clock input and is capable of generating 19 commonly used data communication baud rates ranging from 50 to 76.8k by producing internal clock outputs at 16 times the actual baud rate. Refer to **7.2 Serial Module Signal Definitions** and **7.3.1 Baud Rate Generator** for additional information.

The external clock input (SCLK), which bypasses the baud rate generator, provides a synchronous clock mode of operation when used as a divide-by-1 clock and an asynchronous clock mode when used as a divide-by-16 clock. The external clock input allows the user to use SCLK as the only clock source for the serial module if multiple baud rates are not required.

7.1.3 Internal Channel Control Logic

The serial module receives operation commands from the CPU32 and, in turn, issues appropriate operation signals to the internal serial module control logic. This mechanism allows the registers within the module to be accessed and various commands to be performed. Refer to **7.4 Register Description and Programming** for additional information.

7.1.4 Interrupt Control Logic

Seven interrupt request ($\overline{IRQ7}$–$\overline{IRQ1}$) signals are provided to notify the CPU32 that an interrupt has occurred. These interrupts are described in **7.4 Register Description and Programming**. The interrupt status register (ISR) is read by the CPU32 to determine all

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currently active interrupt conditions. The interrupt enable register (IER) is programmable to mask any events that can cause an interrupt.

7.1.5 Comparison of the Serial Module to the MC68681

The serial module is code compatible with the MC68681 with some modifications. The following paragraphs describe the differences.

The programming model is slightly altered. The supervisor/user block in the MC68341 closely follows the MC68681. The supervisor-only block has the following changes:

- The interrupt vector register is moved from supervisor/user to supervisor only at a new address.
- MR2A and MR2B are moved from a hidden address location to a location at the bottom of the programming model.

The timer/counter is eliminated as well as all associated command and status registers.

Only certain output port pins are available.

There are no IP pins on the MC68341.

RxRTS is more automated on the MC68341.

The XTAL_RDY bit in the ISR should be polled until it is cleared to prevent an unstable frequency from being applied to the baud rate generator. The following pseudocode is an example:

```
if (XTAL_RDY==0)
   begin
     write CSR
   end
else
   begin
      wait
      jump loop
   end
```

7.2 SERIAL MODULE SIGNAL DEFINITIONS

The following paragraphs contain a brief description of the serial module signals. Figure 7-2 shows both the external and internal signal groups.

NOTE

The terms *assertion* and *negation* are used throughout this section to avoid confusion when dealing with a mixture of active-low and active-high signals. The term *assert* or *assertion* indicates that a signal is active or true, independent of the level represented by a high or low voltage. The term *negate* or *negation* indicates that a signal is inactive or false.

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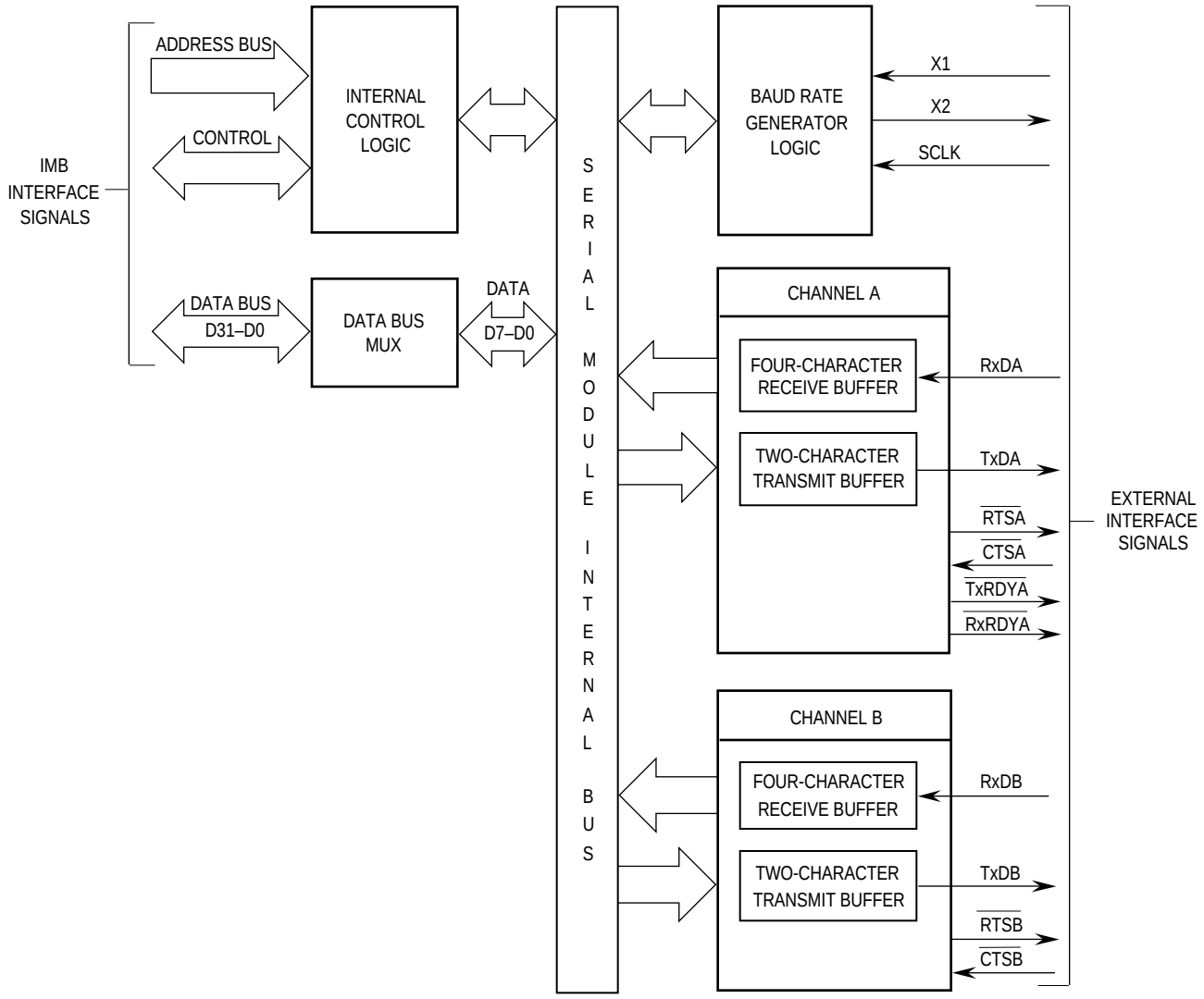

Figure 7-2. External and Internal Interface Signals

7.2.1 Crystal Input or External Clock (X1)

This input is one of two connections to a crystal or a single connection to an external clock. A crystal or an external clock signal, at 3.6864 MHz, must be supplied when using the baud rate generator. If a crystal is used, a capacitor of approximately 10 pF should be connected from this signal to ground. If this input is not used, it must be connected to V_{CC} or GND. Refer to **Section 11 Applications** for an example of a clock driver circuit.

7.2.2 Crystal Output (X2)

This output is the additional connection to a crystal. If a crystal is used, a capacitor of approximately 5 pF should be connected from this signal to ground. If an external TTL-level clock is used on X1, the X2 output must be left open. Refer to **Section 11 Applications** for an example of a clock driver circuit.

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7.2.3 External Input (SCLK)

This input can be used as the clock input for channel A and/or channel B and is programmable in the clock-select registers (CSR). When used as the receiver clock, received data is sampled on the rising edge of the clock. When used as the transmitter clock, data is output on the falling edge of the clock. If this input is not used, it must be connected to V_{CC} or GND.

7.2.4 Channel A Transmitter Serial Data Output (TxDA)

This signal is the transmitter serial data output for channel A. The output is held high ('mark' condition) when the transmitter is disabled, idle, or operating in the local loopback mode. Data is shifted out on this signal on the falling edge of the clock source, with the least significant bit transmitted first.

7.2.5 Channel A Receiver Serial Data Input (RxDA)

This signal is the receiver serial data input for channel A. Data received on this signal is sampled on the rising edge of the clock source, with the least significant bit received first.

7.2.6 Channel B Transmitter Serial Data Output (TxDB)

This signal is the transmitter serial data output for channel B. The output is held high ('mark' condition) when the transmitter is disabled, idle, or operating in the local loopback mode. Data is shifted out on this signal at the falling edge of the clock source, with the least significant bit transmitted first.

7.2.7 Channel B Receiver Serial Data Input (RxDB)

This signal is the receiver serial data input for channel B. Data on this signal is sampled on the rising edge of the clock source, with the least significant bit received first.

7.2.8 Channel A Request-To-Send ($\overline{RTSA}$)

This active-low output signal is programmable as the channel A request-to-send or as a dedicated parallel output.

$\overline{RTSA}$

When used for this function, this signal can be programmed to be automatically negated and asserted by either the receiver or transmitter. When connected to the clear-to-send ($\overline{CTSx}$) input of a transmitter, this signal can be used to control serial data flow.

OP0

When used for this function, this output is controlled by bit 0 in the output port data register (OP).

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7.2.9 Channel B Request-To-Send ($\overline{\text{RTSB}}$)

This active-low output signal is programmable as the channel B request-to-send or as a dedicated parallel output.

$\overline{\text{RTSB}}$

When used for this function, this signal can be programmed to be automatically negated and asserted by either the receiver or transmitter. When connected to the $\overline{\text{CTSx}}$ input of a transmitter, this signal can be used to control serial data flow.

OP1

When used for this function, this output is controlled by bit 1 in the OP.

7.2.10 Channel A Clear-To-Send ($\overline{\text{CTSA}}$)

This active-low input is the channel A clear-to-send.

7.2.11 Channel B Clear-To-Send ($\overline{\text{CTSB}}$)

This active-low input is the channel B clear-to-send.

7.2.12 Channel A Transmitter Ready ($\overline{\text{TxRDYA}}$)

This active-low output signal is programmable as the channel A transmitter ready or as a dedicated parallel output and cannot be masked by the IER.

$\overline{\text{TxRDYA}}$

When used for this function, this signal reflects the complement of the status of bit 2 of the channel A status register (SRA). This signal can be used to control parallel data flow by acting as an interrupt to indicate when the transmitter contains a character.

OP6

When used for this function, this output is controlled by bit 6 in the OP.

7.2.13 Channel A Receiver Ready ($\overline{\text{RxRDYA}}$)

This active-low output signal is programmable as the channel A receiver ready, channel A first-in-first-out (FIFO) full indicator, or a dedicated parallel output and cannot be masked by the IER.

$\overline{\text{RxRDYA}}$

When used for this function, this signal reflects the complement of the status of bit 1 of the ISR. This signal can be used to control parallel data flow by acting as an interrupt to indicate when the receiver contains a character.

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$\overline{\text{FFULLA}}$

When used for this function, this signal reflects the complement of the status of bit 1 of the ISR. This signal can be used to control parallel data flow by acting as an interrupt to indicate when the receiver FIFO is full.

OP4

When used for this function, this output is controlled by bit 4 in the OP.

7.3 OPERATION

The following paragraphs describe the operation of the baud rate generator, transmitter and receiver, and other functional operating modes of the serial module.

7.3.1 Baud Rate Generator

The baud rate generator consists of a crystal oscillator, baud rate generator, and clock selectors (see Figure 7-3). The crystal oscillator operates directly from a 3.6864-MHz crystal or from an external clock of the same frequency. The SCLK input bypasses the baud rate generator and provides a synchronous clock mode of operation when used as a divide-by-1 clock and an asynchronous clock mode when used as a divide-by-16 clock. The clock is selected by programming the CSR for each channel.

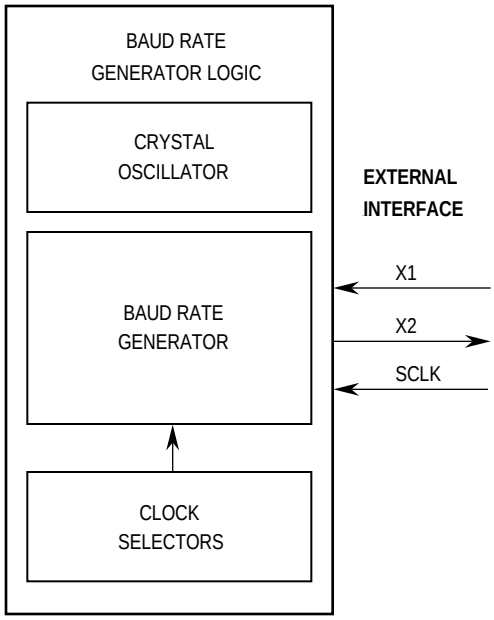

Figure 7-3. Baud Rate Generator Block Diagram

7.3.2 Transmitter and Receiver Operating Modes

The functional block diagram of the transmitter and receiver, including command and operating registers, is shown in Figure 7-4. The paragraphs that follow contain descriptions for both these functions in reference to this diagram. For detailed register information, refer to **7.4 Register Description and Programming**.

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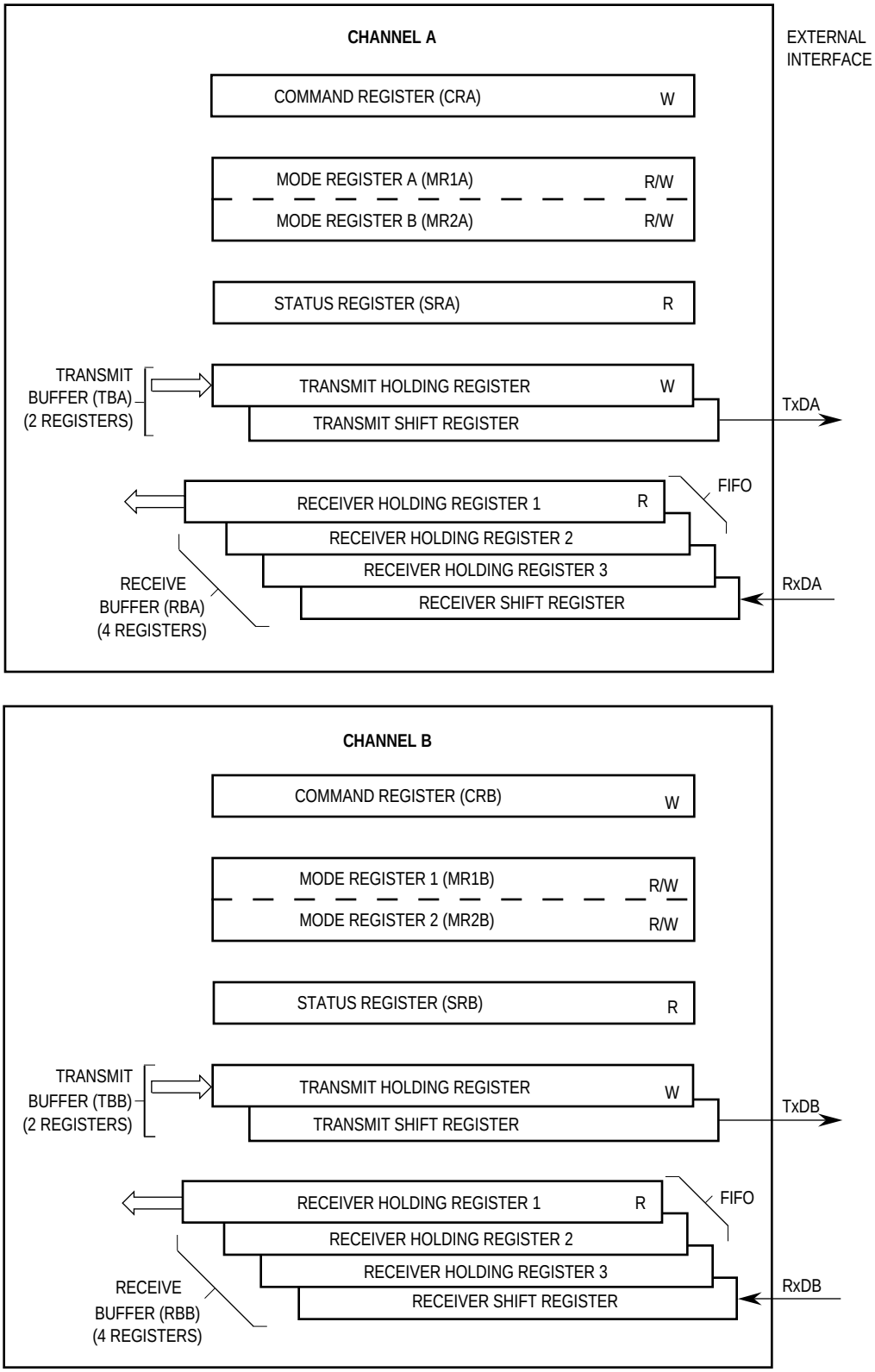

NOTE:
R/W = READ/WRITE
R = READ
W = WRITE

Figure 7-4. Transmitter and Receiver Functional Diagram

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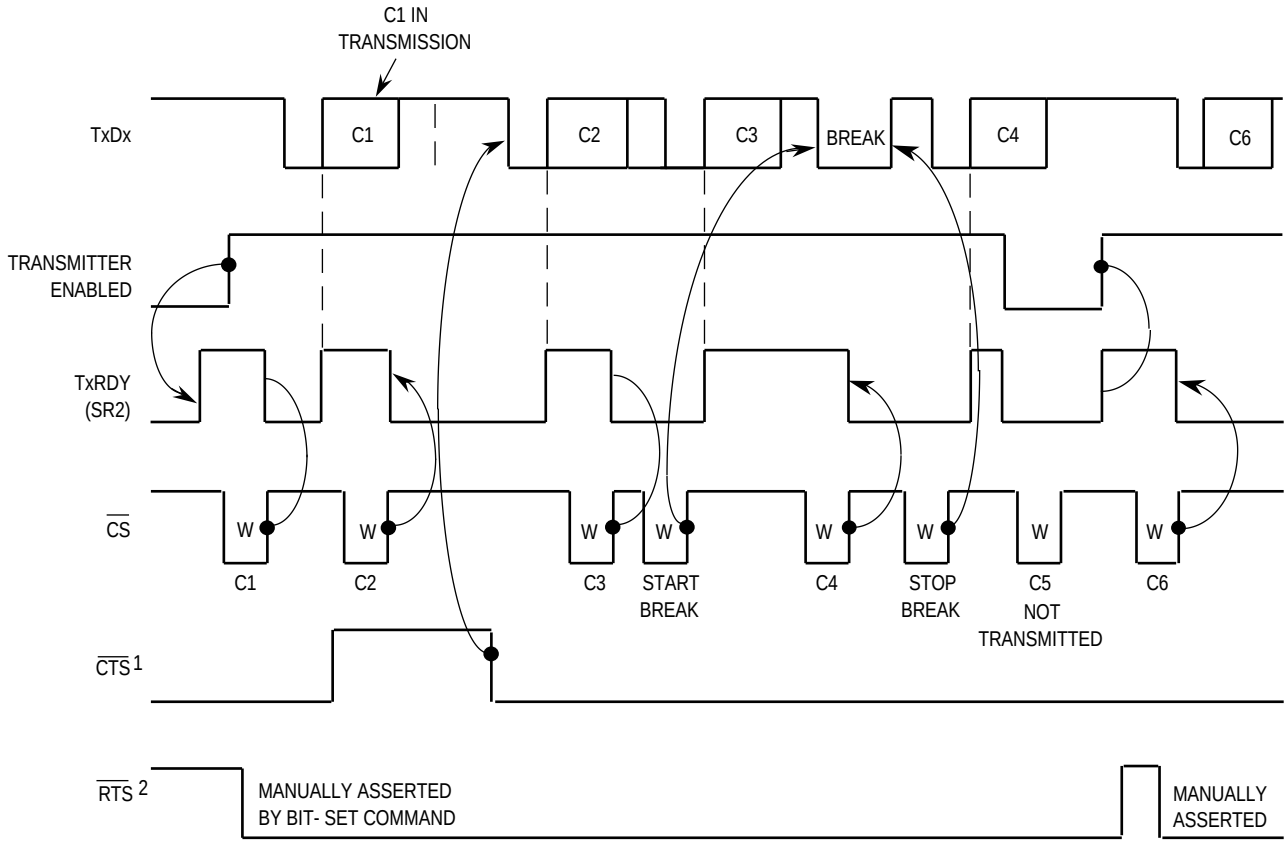
7.3.2.1 TRANSMITTER. The transmitters are enabled through their respective command registers (CR) located within the serial module. The serial module signals the CPU32 when it is ready to accept a character by setting the transmitter-ready bit (TxRDY) in the channel's status register (SR). Functional timing information for the transmitter is shown in Figure 7-5.

The transmitter converts parallel data from the CPU32 to a serial bit stream on TxDx. It automatically sends a start bit followed by the programmed number of data bits, an optional parity bit, and the programmed number of stop bits. The least significant bit is sent first. Data is shifted from the transmitter output on the falling edge of the clock source.



NOTES:
1. TIMING SHOWN FOR MR2(4) = 1
2. TIMING SHOWN FOR MR2(5) = 1
3. C_N = TRANSMIT CHARACTER
4. W = WRITE

Figure 7-5. Transmitter Timing Diagram

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Following transmission of the stop bits, if a new character is not available in the transmitter holding register, the TxDx output remains high ('mark' condition), and the transmitter empty bit (TxEMP) in the SR is set. Transmission resumes and the TxEMP bit is cleared when the CPU32 loads a new character into the transmitter buffer (TB). If a disable command is sent to the transmitter, it continues operating until the character in the transmit shift register, if any, is completely sent out. If the transmitter is reset through a software command, operation ceases immediately (refer to **7.4.1.3 Command Register (CR)**). The transmitter is re-enabled through the CR to resume operation after a disable or software reset.

If clear-to-send operation is enabled, $\overline{\text{CTSx}}$ must be asserted for the character to be transmitted. If $\overline{\text{CTSx}}$ is negated in the middle of a transmission, the character in the shift register is transmitted, and TxDx remains in the 'mark' state until $\overline{\text{CTSx}}$ is asserted again. If the transmitter is forced to send a continuous low condition by issuing a send break command, the state of $\overline{\text{CTSx}}$ is ignored by the transmitter.

The transmitter can be programmed to automatically negate request-to-send ($\overline{\text{RTSx}}$) outputs upon completion of a message transmission. If the transmitter is programmed to operate in this mode, $\overline{\text{RTSx}}$ must be manually asserted before a message is transmitted. In applications in which the transmitter is disabled after transmission is complete and $\overline{\text{RTSx}}$ is appropriately programmed, $\overline{\text{RTSx}}$ is negated one bit time after the character in the shift register is completely transmitted. The transmitter must be manually re-enabled by reasserting $\overline{\text{RTSx}}$ before the next message is to be sent.

7.3.2.2 RECEIVER. The receivers are enabled through their respective CRs located within the serial module. Functional timing information for the receiver is shown in Figure 7-6. The receiver looks for a high-to-low (mark-to-space) transition of the start bit on RxDx. When a transition is detected, the state of RxDx is sampled each 16× clock for eight clocks, starting one-half clock after the transition (asynchronous operation) or at the next rising edge of the bit time clock (synchronous operation). If RxDx is sampled high, the start bit is invalid, and the search for the valid start bit begins again. If RxDx is still low, a valid start bit is assumed, and the receiver continues to sample the input at one-bit time intervals, at the theoretical center of the bit, until the proper number of data bits and parity, if any, is assembled and one stop bit is detected. Data on the RxDx input is sampled on the rising edge of the programmed clock source. The least significant bit is received first. The data is then transferred to a receiver holding register, and the RxRDY bit in the appropriate SR is set. If the character length is less than eight bits, the most significant unused bits in the receiver holding register are cleared.

After the stop bit is detected, the receiver immediately looks for the next start bit. However, if a nonzero character is received without a stop bit (framing error) and RxDx remains low for one-half of the bit period after the stop bit is sampled, the receiver operates as if a new start bit is detected. The parity error (PE), framing error (FE), overrun error (OE), and received break (RB) conditions (if any) set error and break flags in the appropriate SR at the received character boundary and are valid only when the RxRDY bit in the SR is set.

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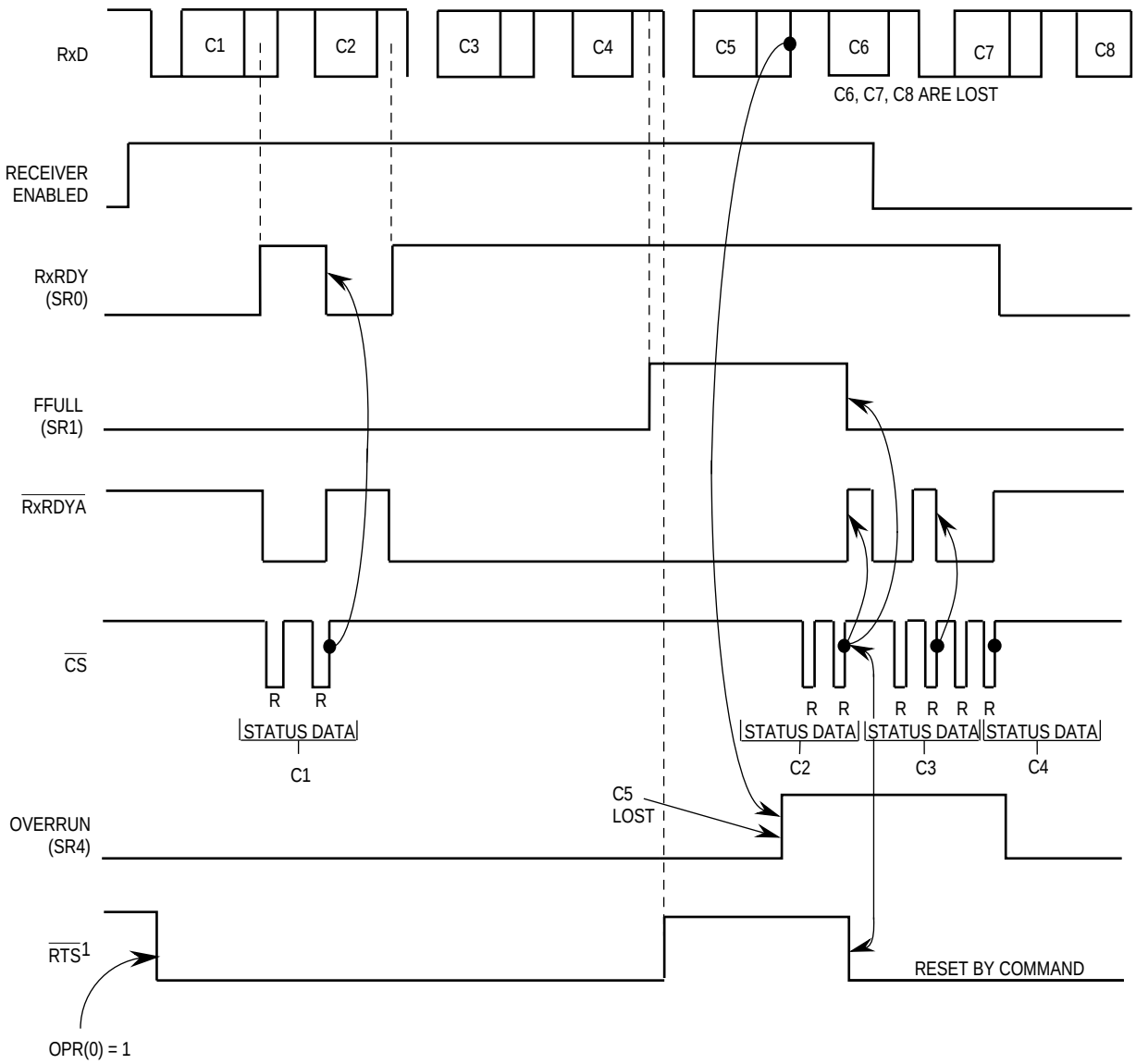

NOTES:
1. Timing shown for MR1(7) = 1
2. Timing shown for OPCR(4) = 1 and MR1(6) = 0
3. R = Read
4. C_N = Received Character

Figure 7-6. Receiver Timing Diagram

If a break condition is detected (RxDx is low for the entire character including the stop bit), a character of all zeros is loaded into the receiver holding register, and the receive buffer (RB) and RxRDY bits in the SR are set. The RxDx signal must return to a high condition for at least one-half bit time before a search for the next start bit begins.

The receiver detects the beginning of a break in the middle of a character if the break persists through the next character time. When the break begins in the middle of a character, the receiver places the damaged character in the receiver FIFO stack and sets the corresponding error conditions and RxRDY bit in the SR. Then, if the break persists

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until the next character time, the receiver places an all-zero character into the receiver FIFO and sets the corresponding RB and RxRDY bits in the SR.

7.3.2.3 FIFO STACK. The FIFO stack is used in each channel's receiver buffer logic. The stack consists of three receiver holding registers. The receive buffer consists of the FIFO and a receiver shift register connected to the RxDx (refer to Figure 7-4). Data is assembled in the receiver shift register and loaded into the top empty receiver holding register position of the FIFO. Thus, data flowing from the receiver to the CPU32 is quadruple buffered.

In addition to the data byte, three status bits, PE, FE, and RB, are appended to each data character in the FIFO; OE is not appended. By programming the ERR bit in the channel's mode register (MR1), status is provided in character or block modes.

The RxRDY bit in the SR is set whenever one or more characters are available to be read by the CPU32. A read of the receiver buffer produces an output of data from the top of the FIFO stack. After the read cycle, the data at the top of the FIFO stack and its associated status bits are 'popped', and new data can be added at the bottom of the stack by the receiver shift register. The FIFO-full status bit (FFULL) is set if all three stack positions are filled with data. Either the RxRDY or FFULL bit can be selected to cause an interrupt.

In the character mode, status provided in the SR is given on a character-by-character basis and thus applies only to the character at the top of the FIFO. In the block mode, the status provided in the SR is the logical OR of all characters coming to the top of the FIFO stack since the last reset error command. A continuous logical OR function of the corresponding status bits is produced in the SR as each character reaches the top of the FIFO stack. The block mode is useful in applications where the software overhead of checking each character's error cannot be tolerated. In this mode, entire messages are received, and only one data integrity check is performed at the end of the message. This mode allows a data-reception speed advantage, but does have a disadvantage since each character is not individually checked for error conditions by software. If an error occurs within the message, the error is not recognized until the final check is performed, and no indication exists as to which character in the message is at fault.

In either mode, reading the SR does not affect the FIFO. The FIFO is 'popped' only when the receive buffer is read. The SR should be read prior to reading the receive buffer. If all three of the FIFO's receiver holding registers are full when a new character is received, the new character is held in the receiver shift register until a FIFO position is available. If an additional character is received during this state, the contents of the FIFO are not affected. However, the character previously in the receiver shift register is lost, and the OE bit in the SR is set when the receiver detects the start bit of the new overrunning character.

To support control flow capability, the receiver can be programmed to automatically negate and assert $\overline{\text{RTSx}}$. When in this mode, $\overline{\text{RTSx}}$ is automatically negated by the receiver when a valid start bit is detected and the FIFO stack is full. When a FIFO position

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becomes available, $\overline{RTSx}$ is asserted by the receiver. Using this mode of operation, overrun errors are prevented by connecting the $\overline{RTSx}$ to the $\overline{CTSx}$ input of the transmitting device.

If the FIFO stack contains characters and the receiver is disabled, the characters in the FIFO can still be read by the CPU32. If the receiver is reset, the FIFO stack and all receiver status bits, corresponding output ports, and interrupt request are reset. No additional characters are received until the receiver is re-enabled.

7.3.3 Looping Modes

Each serial module channel can be configured to operate in various looping modes as shown in Figure 7-7. These modes are useful for local and remote system diagnostic functions. The modes are described in the following paragraphs with further information available in **7.4 Register Description and Programming**.

The channel's transmitter and receiver should both be disabled when switching between modes. The selected mode is activated immediately upon mode selection, regardless of whether a character is being received or transmitted.

7.3.3.1 AUTOMATIC ECHO MODE. In this mode, the channel automatically retransmits the received data on a bit-by-bit basis. The local CPU32-to-receiver communication continues normally, but the CPU32-to-transmitter link is disabled. While in this mode, received data is clocked on the receiver clock and retransmitted on TxDx. The receiver must be enabled, but the transmitter need not be enabled.

Since the transmitter is not active, the SR TxEMP and TxRDY bits are inactive, and data is transmitted as it is received. Received parity is checked, but not recalculated for transmission. Character framing is also checked, but stop bits are transmitted as received. A received break is echoed as received until the next valid start bit is detected.

7.3.3.2 LOCAL LOOPBACK MODE. In this mode, TxDx is internally connected to RxDx. This mode is useful for testing the operation of a local serial module channel by sending data to the transmitter and checking data assembled by the receiver. In this manner, correct channel operations can be assured. Also, both transmitter and CPU32-to-receiver communications continue normally in this mode. While in this mode, the RxDx input data is ignored, the TxDx is held marking, and the receiver is clocked by the transmitter clock. The transmitter must be enabled, but the receiver need not be enabled.

7.3.3.3 REMOTE LOOPBACK MODE. In this mode, the channel automatically transmits received data on the TxDx output on a bit-by-bit basis. The local CPU32-to-transmitter link is disabled. This mode is useful in testing receiver and transmitter operation of a remote channel. While in this mode, the receiver clock is used for the transmitter.

Since the receiver is not active, received data cannot be read by the CPU32, and the error status conditions are inactive. Received parity is not checked and is not recalculated for transmission. Stop bits are transmitted as received. A received break is echoed as received until the next valid start bit is detected.

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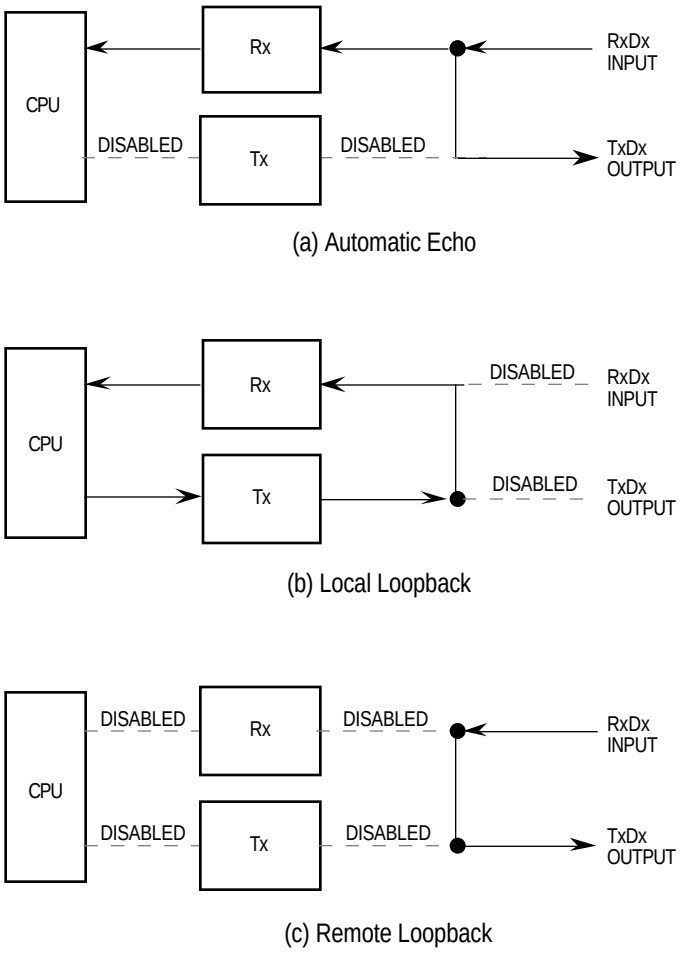

Figure 7-7. Looping Modes Functional Diagram

7.3.4 Multidrop Mode

A channel can be programmed to operate in a wakeup mode for multidrop or multiprocessor applications. Functional timing information for the multidrop mode is shown in Figure 7-8. The mode is selected by setting bits 3 and 4 in mode register 1 (MR1). This mode of operation allows the master station to be connected to several slave stations (maximum of 256). In this mode, the master transmits an address character followed by a block of data characters targeted for one of the slave stations. The slave stations have their channel receivers disabled. However, they continuously monitor the data stream sent out by the master station. When an address character is sent by the master, the slave receiver channel notifies its respective CPU by setting the RxRDY bit in the SR and generating an interrupt (if programmed to do so). Each slave station CPU then compares the received address to its station address and enables its receiver if it wishes to receive the subsequent data characters or block of data from the master station. Slave stations not addressed continue to monitor the data stream for the next address character. Data fields in the data stream are separated by an address character. After a slave receives a block of data, the slave station's CPU disables the receiver and initiates the process again.

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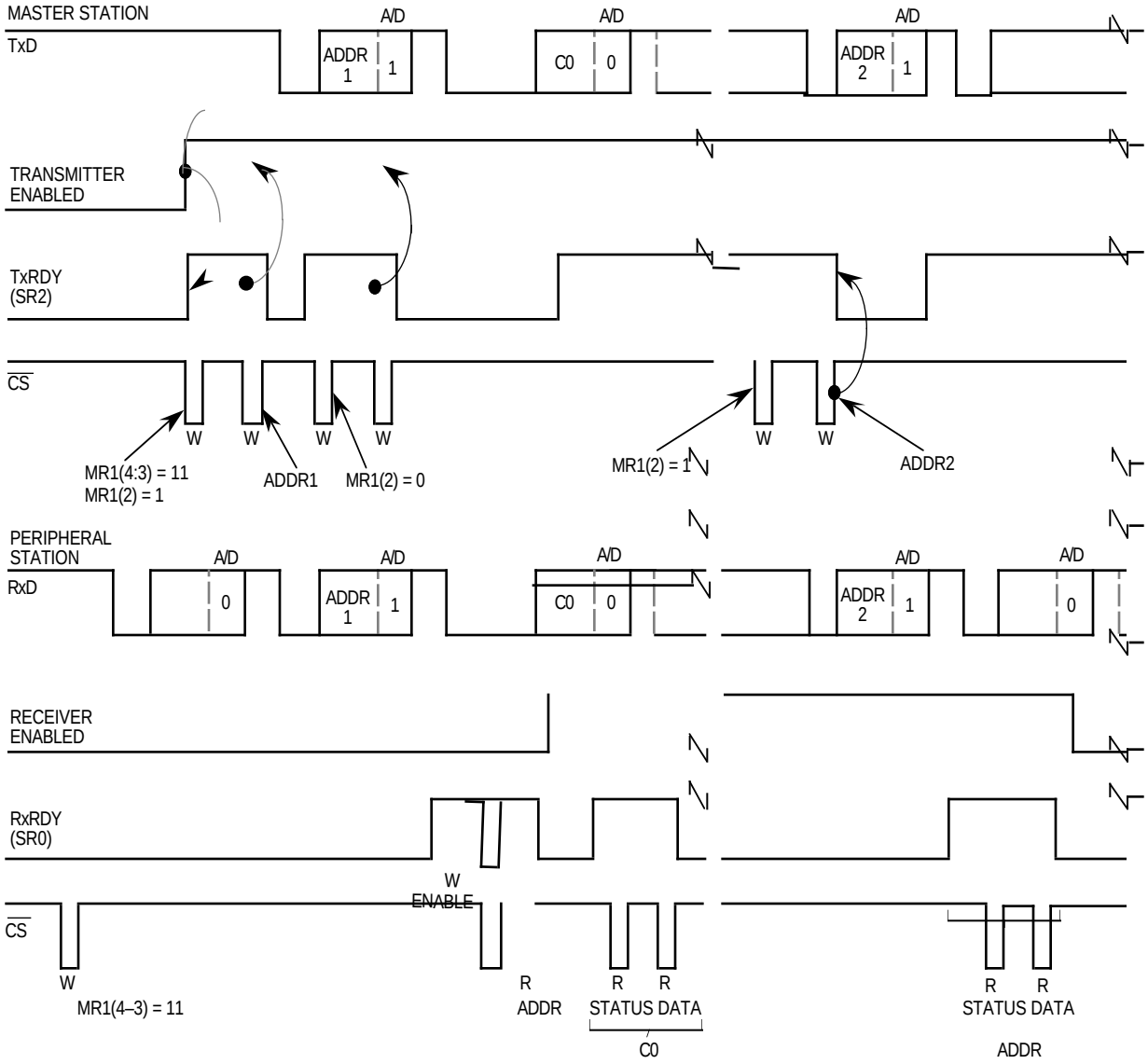

Figure 7-8. Multidrop Mode Timing Diagram

A transmitted character from the master station consists of a start bit, a programmed number of data bits, an address/data (A/D) bit flag, and a programmed number of stop bits. The A/D bit identifies the type of character being transmitted to the slave station. The character is interpreted as an address character if the A/D bit is set or as a data character if the A/D bit is cleared. The polarity of the A/D bit is selected by programming bit 2 of the MR1. The MR1 should be programmed before enabling the transmitter and loading the corresponding data bits into the transmit buffer.

In multidrop mode, the receiver continuously monitors the received data stream, regardless of whether it is enabled or disabled. If the receiver is disabled, it sets the RxRDY bit and loads the character into the receiver holding register FIFO stack provided the received A/D bit is a one (address tag). The character is discarded if the received A/D bit is a zero (data tag). If the receiver is enabled, all received characters are transferred to the CPU32 via the receiver holding register stack during read operations.

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In either case, the data bits are loaded into the data portion of the stack while the A/D bit is loaded into the status portion of the stack normally used for a parity error (SR bit 5). Framing error, overrun error, and break detection operate normally. The A/D bit takes the place of the parity bit; therefore, parity is neither calculated nor checked. Messages in this mode may still contain error detection and correction information. One way to provide error detection, if 7-bit characters are not required, is to use software to calculate parity and append it to the 5-, 6-, or 7-bit character.

7.3.5 Bus Operation

This section describes the operation of the IMB during read, write, and interrupt acknowledge cycles to the serial module. All serial module registers must be accessed as bytes.

7.3.5.1 READ CYCLES. The serial module is accessed by the CPU32 with no wait states. The serial module responds to byte reads. Reserved registers return logic zero during reads.

7.3.5.2 WRITE CYCLES. The serial module is accessed by the CPU32 with no wait states. The serial module responds to byte writes. Write cycles to read-only registers and reserved registers complete in a normal manner without exception processing; however, the data is ignored.

7.3.5.3 INTERRUPT ACKNOWLEDGE CYCLES. The serial module is capable of arbitrating for interrupt servicing and supplying the interrupt vector when it has successfully won arbitration. The vector number must be provided if interrupt servicing is necessary; thus, the interrupt vector register (IVR) must be initialized. If the IVR is not initialized, a spurious interrupt exception will be taken if interrupts are generated.

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7.4 REGISTER DESCRIPTION AND PROGRAMMING

This section contains a detailed description of each register and its specific function as well as flowcharts of basic serial module programming.

7.4.1 Register Description

The operation of the serial module is controlled by writing control bytes into the appropriate registers. A list of serial module registers and their associated addresses are shown in Figure 7-9. The mode, status, command, and clock-select registers are duplicated for each channel to provide independent operation and control.

NOTE

All serial module registers are only accessible as bytes. The contents of the mode registers (MR1 and MR2), CSR, and the auxiliary control register (ACR) bit 7 should only be changed after the receiver/transmitter is issued a software RESET command—i.e., channel operation must be disabled. Care should also be taken if the register contents are changed during receiver/transmitter operations, as undesirable results may be produced.

The registers of the serial module are discussed in the following paragraphs in alphabetical order. The numbers in the upper right-hand corner indicate the offset of the register from the base address specified in the module base address register (MBAR) in the SIM41. The numbers above the register description represent the bit position in the register. The register description contains the mnemonic for the bit. The values shown below the register description are the values of those register bits after a hardware reset. A value of U indicates that the bit value is unaffected by reset. The read/write status and the access privilege are shown in the last line.

NOTE

A CPU32 RESET instruction will not affect the MCR, but will reset all the other serial module registers as though a hardware reset had occurred. The module is enabled when the STP bit in the MCR is cleared. The module is disabled when the STP bit in the MCR is set.

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Address	FC	Register Read (R/W = 1)	Register Write (R/W = 0)
700	S[1]	MCR (HIGH BYTE)	MCR (HIGH BYTE)
701	S	MCR (LOW BYTE)	MCR (LOW BYTE)
702	S	DO NOT ACCESS[3]	DO NOT ACCESS[3]
703	S	DO NOT ACCESS[3]	DO NOT ACCESS[3]
704	S	INTERRUPT LEVEL (ILR)	INTERRUPT LEVEL (ILR)
705	S	INTERRUPT VECTOR (IVR)	INTERRUPT VECTOR (IVR)
710	S/U[2]	MODE REGISTER 1A (MR1A)	MODE REGISTER 1A (MR1A)
711	S/U	STATUS REGISTER A (SRA)	CLOCK-SELECT REGISTER A (CSRA)
712	S/U	DO NOT ACCESS[3]	COMMAND REGISTER A (CRA)
713	S/U	RECEIVER BUFFER A (RBA)	TRANSMITTER BUFFER A (TBA)
714	S/U	INPUT PORT CHANGE REGISTER (IPCR)	AUXILIARY CONTROL REGISTER (ACR)
715	S/U	INTERRUPT STATUS REGISTER (ISR)	INTERRUPT ENABLE REGISTER (IER)
716	S/U	DO NOT ACCESS[3]	DO NOT ACCESS[3]
717	S/U	DO NOT ACCESS[3]	DO NOT ACCESS[3]
718	S/U	MODE REGISTER 1B (MR1B)	MODE REGISTER 1B (MR1B)
719	S/U	STATUS REGISTER B (SRB)	CLOCK-SELECT REGISTER B (CSRB)
71A	S/U	DO NOT ACCESS[3]	COMMAND REGISTER B (CRB)
71B	S/U	RECEIVER BUFFER B (RBB)	TRANSMITTER BUFFER B (TBB)
71C	S/U	DO NOT ACCESS[3]	DO NOT ACCESS[3]
71D	S/U	INPUT PORT REGISTER (IP)	OUTPUT PORT CONTROL REGISTER (OPCR)
71E	S/U	DO NOT ACCESS[3]	OUTPUT PORT (OP)[4] BIT SET
71F	S/U	DO NOT ACCESS[3]	OUTPUT PORT (OP)[4] BIT RESET
720	S/U	MODE REGISTER 2A (MR2A)	MODE REGISTER 2A (MR2A)
721	S/U	MODE REGISTER 2B (MR2B)	MODE REGISTER 2B (MR2B)

NOTES:
1. S = Register permanently defined as supervisor-only access
2. S/U = Register programmable as either supervisor or user access
3. A read or write to these locations currently has no effect.
4. Address-triggered commands

Figure 7-9. Serial Module Programming Model

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7.4.1.1 AUXILIARY CONTROL REGISTER (ACR). The ACR selects which baud rate is used and controls the handshake of the transmitter/receiver. This register can only be written when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

ACR $714

7	6	5	4	3	2	1	0
BRG	0	0	0	0	0	IECB	IECA
RESET: 0	0	0	0	0	0	0	0

Write Only Supervisor/User

BRG—Baud Rate Generator Set Select

1 = Set 2 of the available baud rates is selected.
0 = Set 1 of the available baud rates is selected. Refer to **7.4.1.2 Clock-Select Register (CSR)** for more information on the baud rates.

IECB, IECA—Input Enable Control

1 = ISR bit 7 will be set and an interrupt will be generated when the corresponding bit in the IPCR (COSB or COSA) is set by an external transition on the channel's $\overline{\text{CTSx}}$ input (if bit 7 of the IER) is set to enable interrupts).
0 = Setting the corresponding bit in the IPCR has no effect on ISR bit 7.

7.4.1.2 CLOCK-SELECT REGISTER (CSR). The CSR selects the baud rate clock for the channel receiver and transmitter. This register can only be written when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

NOTE

This register should only be written after the external crystal is stable (XTAL_RDY bit of the ISR is zero).

CSRA, CSRB $711, $719

7	6	5	4	3	2	1	0
RCS3	RCS2	RCS1	RCS0	TCS3	TCS2	TCS1	TCS0
RESET: 0	0	0	0	0	0	0	0

Write Only Supervisor/User

RCS3–RCS0—Receiver Clock Select

These bits select the baud rate clock for the channel receiver from a set of baud rates listed in Table 7-1. The baud rate set selected depends upon the ACR bit 7. Set 1 is selected if ACR bit 7 = 0, and set 2 is selected if ACR bit 7 = 1. The receiver clock is always 16 times the baud rate shown in this list, except when SCLK is used.

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Table 7-1. RCSx Control Bits

RCS3	RCS2	RCS1	RCS0	Set 1	Set 2
0	0	0	0	50	75
0	0	0	1	110	110
0	0	1	0	134.5	134.5
0	0	1	1	200	150
0	1	0	0	300	300
0	1	0	1	600	600
0	1	1	0	1200	1200
0	1	1	1	1050	2000
1	0	0	0	2400	2400
1	0	0	1	4800	4800
1	0	1	0	7200	1800
1	0	1	1	9600	9600
1	1	0	0	38.4k	19.2k
1	1	0	1	76.8k	38.4k
1	1	1	0	SCLK/16	SCLK/16
1	1	1	1	SCLK/1	SCLK/1

TCS3–TCS0—Transmitter Clock Select

These bits select the baud rate clock for the channel transmitter from a set of baud rates listed in Table 7-2. The baud rate set selected depends upon ACR bit 7. Set 1 is selected if ACR bit 7 = 0, and set 2 is selected if ACR bit 7 = 1. The transmitter clock is always 16 times the baud rate shown in this list, except when SCLK is used.

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Table 7-2 . TCSx Control Bits

TCS3	TCS2	TCS1	TCS0	Set 1	Set 2
0	0	0	0	50	75
0	0	0	1	110	110
0	0	1	0	134.5	134.5
0	0	1	1	200	150
0	1	0	0	300	300
0	1	0	1	600	600
0	1	1	0	1200	1200
0	1	1	1	1050	2000
1	0	0	0	2400	2400
1	0	0	1	4800	4800
1	0	1	0	7200	1800
1	0	1	1	9600	9600
1	1	0	0	38.4k	19.2k
1	1	0	1	76.8k	38.4k
1	1	1	0	SCLK/16	SCLK/16
1	1	1	1	SCLK/1	SCLK/1

7.4.1.3 COMMAND REGISTER (CR). The CR is used to supply commands to the channel. Multiple commands can be specified in a single write to the CR if the commands are not conflicting—e.g., reset transmitter and enable transmitter commands cannot be specified in a single command. This register can only be written when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

CRA, CRB $712, $71A

7	6	5	4	3	2	1	0
MISC3	MISC2	MISC1	MISC0	TC1	TC0	RC1	RC0
RESET:							
0	0	0	0	0	0	0	0

Write Only Supervisor/User

MISC3–MISC0—Miscellaneous Commands

These bits select a single command as listed in Table 7-3.

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Table 7-3. MISCx Control Bits

MISC3	MISC2	MISC1	MISC0	Command
0	0	0	0	No Command
0	0	0	1	No Command
0	0	1	0	Reset Receiver
0	0	1	1	Reset Transmitter
0	1	0	0	Reset Error Status
0	1	0	1	Reset Break-Change Interrupt
0	1	1	0	Start Break
0	1	1	1	Stop Break
1	0	0	0	Assert $\overline{RTS}$
1	0	0	1	Negate $\overline{RTS}$
1	0	1	0	No Command
1	0	1	1	No Command
1	1	0	0	No Command
1	1	0	1	No Command
1	1	1	0	No Command
1	1	1	1	No Command

Reset Receiver—The reset receiver command resets the channel receiver. The receiver is immediately disabled, the FFULL and RxRDY bits in the SR are cleared, and the receiver FIFO pointer is reinitialized. All other registers are unaltered. This command should be used in lieu of the receiver disable command whenever the receiver configuration is changed because it places the receiver in a known state.

Reset Transmitter—The reset transmitter command resets the channel transmitter. The transmitter is immediately disabled, and the TxEMP and TxRDY bits in the SR are cleared. All other registers are unaltered. This command should be used in lieu of the transmitter disable command whenever the transmitter configuration is changed because it places the transmitter in a known state.

Reset Error Status—The reset error status command clears the channel's RB, FE, PE, and OE bits (in the SR). This command is also used in the block mode to clear all error bits after a data block is received.

Reset Break-Change Interrupt—The reset break-change interrupt command clears the delta break (DBx) bits in the ISR.

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Start Break—The start break command forces the channel's TxDx low. If the transmitter is empty, the start of the break conditions can be delayed up to one bit time. If the transmitter is active, the break begins when transmission of the character is complete. If a character is in the transmitter shift register, the start of the break is delayed until the character is transmitted. If the transmitter holding register has a character, that character is transmitted after the break. The transmitter must be enabled for this command to be accepted. The state of the $\overline{\text{CTSx}}$ input is ignored for this command.

Stop Break—The stop break command causes the channel's TxDx to go high (mark) within two bit times. Characters stored in the transmitter buffer, if any, are transmitted.

Assert $\overline{\text{RTS}}$—The assert $\overline{\text{RTS}}$ command forces the channel's $\overline{\text{RTSx}}$ output low.

Negate $\overline{\text{RTS}}$—The negate $\overline{\text{RTS}}$ command forces the channel's $\overline{\text{RTSx}}$ output high.

TC1–TC0—Transmitter Commands

These bits select a single command as listed in Table 7-4.

Table 7-4. TCx Control Bits

TC1	TC0	Command
0	0	No Action Taken
0	1	Enable Transmitter
1	0	Disable Transmitter
1	1	Do Not Use

No Action Taken—The no action taken command causes the transmitter to stay in its current mode. If the transmitter is enabled, it remains enabled; if disabled, it remains disabled.

Transmitter Enable—The transmitter enable command enables operation of the channel's transmitter. The TxEMP and TxRDY bits in the SR are also set. If the transmitter is already enabled, this command has no effect.

Transmitter Disable—The transmitter disable command terminates transmitter operation and clears the TxEMP and TxRDY bits in the SR. However, if a character is being transmitted when the transmitter is disabled, the transmission of the character is completed before the transmitter becomes inactive. If the transmitter is already disabled, this command has no effect.

Do Not Use—Do not use this bit combination because the result is indeterminate.

RC1–RC0—Receiver Commands

These bits select a single command as listed in Table 7-5.

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Table 7-5. RCx Control Bits

RC1	RC0	Command
0	0	No Action Taken
0	1	Enable Receiver
1	0	Disable Receiver
1	1	Do Not Use

No Action Taken—The no action taken command causes the receiver to stay in its current mode. If the receiver is enabled, it remains enabled; if disabled, it remains disabled.

Receiver Enable—The receiver enable command enables operation of the channel's receiver. If the serial module is not in multidrop mode, this command also forces the receiver into the search-for-start-bit state. If the receiver is already enabled, this command has no effect.

Receiver Disable—The receiver disable command disables the receiver immediately. Any character being received is lost. The command has no effect on the receiver status bits or any other control register. If the serial module is programmed to operate in the local loopback mode or multidrop mode, the receiver operates even though this command is selected. If the receiver is already disabled, this command has no effect.

Do Not Use—Do not use this bit combination because the result is indeterminate.

7.4.1.4 INPUT PORT CHANGE REGISTER (IPCR). The IPCR shows the current state and the change-of-state for the $\overline{\text{CTSA}}$ and $\overline{\text{CTSB}}$ pins. This register can only be read when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

IPCR $714

7	6	5	4	3	2	1	0
0	0	COSB	COSA	0	0	CTSB	CTSA
RESET: 0	0	0	0	0	0	U	U

Read Only Supervisor/User

Bits 7, 6, 3, 2—Reserved by Motorola

COSB, COSA—Change-of-State

1 = A change-of-state (high-to-low or low-to-high transition), lasting longer than 25–50 µs when using a crystal as the sampling clock or longer than one or two periods when using SCLK, has occurred at the corresponding $\overline{\text{CTSx}}$ input (MCR ICCS bit controls selection of the sampling clock for clear-to-send operation). When these bits are set, the ACR can be programmed to generate an interrupt to the CPU32.

0 = The CPU32 has read the IPCR. No change-of-state has occurred. A read of the IPCR also clears the ISR COS bit.

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CTSB, CTSA—Current State

Starting two serial clock periods after reset, the $\overline{\text{CTSx}}$ bits reflect the state of the $\overline{\text{CTSx}}$ pins. If a $\overline{\text{CTSx}}$ pin is detected as asserted at that time, the associated COSx bit will be set, which will initiate an interrupt if the corresponding IECx bit of the ACR register is enabled.

1 = The current state of the respective $\overline{\text{CTSx}}$ input is negated.
0 = The current state of the respective $\overline{\text{CTSx}}$ input is asserted.

7.4.1.5 INPUT PORT REGISTER (IP). The IP shows the current state of the $\overline{\text{CTSx}}$ inputs. This register can only be read when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

IP $71D

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CTSB	CTSA
RESET:							
0	0	0	0	0	0	U	U

Read Only Supervisor/User

CTSB, CTSA—Current State

1 = The current state of the respective $\overline{\text{CTSx}}$ input is negated.
0 = The current state of the respective $\overline{\text{CTSx}}$ input is asserted.

The information contained in these bits is latched and reflects the state of the input pins at the time that the IP is read.

NOTE

These bits have the same function and value of the IPCR bits 1 and 0.

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7.4.1.6 INTERRUPT ENABLE REGISTER (IER). The IER selects the corresponding bits in the ISR that cause an interrupt output ($\overline{IRQx}$). If one of the bits in the ISR is set and the corresponding bit in the IER is also set, the $\overline{IRQx}$ output is asserted. If the corresponding bit in the IER is zero, the state of the bit in the ISR has no effect on the $\overline{IRQx}$ output. The IER does not mask the reading of the ISR. The ISR XTAL_RDY bit cannot be enabled to generate an interrupt. This register can only be written when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

IER $715

7	6	5	4	3	2	1	0
COS	DBB	RxRDYB	TxRDYB	0	DBA	RxRDYA	TxRDYA
RESET:							
0	0	0	0	0	0	0	0

Write Only Supervisor/User

COS—Change-of-State

1 = Enable interrupt
0 = Disable interrupt

DBB—Delta Break B

1 = Enable interrupt
0 = Disable interrupt

RxRDYB—Channel B Receiver Ready or FIFO full

1 = Enable interrupt
0 = Disable interrupt

TxRDYB—Channel B Transmitter Ready

1 = Enable interrupt
0 = Disable interrupt

Bit 3—Reserved by Motorola

DBA—Delta Break A

1 = Enable interrupt
0 = Disable interrupt

RxRDYA—Channel A Receiver Ready or FIFO full

1 = Enable interrupt
0 = Disable interrupt

TxRDYA—Channel A Transmitter Ready

1 = Enable interrupt
0 = Disable interrupt

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7.4.1.7 INTERRUPT LEVEL REGISTER (ILR). The ILR contains the priority level for the serial module interrupt request. When the serial module is enabled (i.e., the STP bit in the MCR is cleared), this register can be read or written to at any time while in supervisor mode.

ILR $704

7	6	5	4	3	2	1	0
0	0	0	0	0	IL2	IL1	IL0
RESET: 0	0	0	0	0	0	0	0

Read/Write Supervisor Only

Bits 7–3—Reserved by Motorola

IL2–IL0—Interrupt Level Bits

Each module that can generate interrupts has an interrupt level field. The priority level encoded in these bits is sent to the CPU32 on the appropriate $\overline{\text{IRQx}}$ signal. The CPU32 uses this value to determine servicing priority. The hardware reset value of $00 will not generate any interrupts. See **Section 5 CPU030** for more information.

7.4.1.8 INTERRUPT STATUS REGISTER (ISR). The ISR provides status for all potential interrupt sources. The contents of this register are masked by the IER. If a flag in the ISR is set and the corresponding bit in IER is also set, the $\overline{\text{IRQx}}$ output is asserted. If the corresponding bit in the IER is cleared, the state of the bit in the ISR has no effect on the output. This register can only be read when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

NOTE

The IER does not mask reading of the ISR. True status is provided regardless of the contents of IER. The contents of ISR are cleared when the serial module is reset.

ISR $715

7	6	5	4	3	2	1	0
COS	DBB	RxRDYB	TxRDYB	XTAL_ RDY	DBA	RxRDYA	TxRDYA
RESET: 0	0	0	0	1	0	0	0

Read Only Supervisor/User

COS—Change-of-State

1 = A change-of-state has occurred at one of the $\overline{\text{CTSx}}$ inputs and has been selected to cause an interrupt by programming bit 1 and/or bit 0 of the ACR.

0 = The CPU32 has read the IPCR.

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DBB—Delta Break B

1 = The channel B receiver has detected the beginning or end of a received break.
0 = The CPU32 has issued a channel B reset break-change interrupt command. Refer to **7.4.1.3 Command Register (CR)** for more information on the reset break-change interrupt command.

RxRDYB—Channel B Receiver Ready or FIFO Full

The function of this bit is programmed by MR1B bit 6.

1 = If programmed as receiver ready, a character has been received in channel B and is waiting in the receiver buffer FIFO. If programmed as FIFO full, a character has been transferred from the receiver shift register to the FIFO, and the transfer has caused the channel B FIFO to become full (all three positions are occupied).
0 = If programmed as receiver ready, the CPU32 has read the RB. After this read, if more characters are still in the FIFO, the bit is set again after the FIFO is 'popped'. If programmed as FIFO full, the CPU32 has read the RB. If a character is waiting in the receiver shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

TxRDYB—Channel B Transmitter Ready

This bit is the duplication of the TxRDY bit in SRB.

1 = The transmitter holding register is empty and ready to be loaded with a character. This bit is set when the character is transferred to the transmitter shift register. This bit is also set when the transmitter is first enabled. Characters loaded into the transmitter holding register while the transmitter is disabled are not transmitted.
0 = The transmitter holding register was loaded by the CPU32, or the transmitter is disabled.

XTAL_RDY—Serial Clock Running

This bit is always read as a zero when the X1 clock is running. This bit cannot be enabled to generate an interrupt.

1 = This bit is set at reset.
0 = This bit is cleared after the baud rate generator is stable. The CSR should not be accessed until this bit is zero.

DBA—Delta Break A

1 = The channel A receiver has detected the beginning or end of a received break.
0 = The CPU32 has issued a channel A reset break-change interrupt command. Refer to **7.4.1.3 Command Register (CR)** for more information on the reset break-change interrupt command.

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RxRDYA—Channel A Receiver Ready or FIFO Full

The function of this bit is programmed by MR1A bit 6.

1 = If programmed as receiver ready, a character has been received in channel A and is waiting in the receiver buffer FIFO. If programmed as FIFO full, a character has been transferred from the receiver shift register to the FIFO, and the transfer has caused the channel A FIFO to become full (all three positions are occupied).

0 = If programmed as receiver ready, the CPU32 has read the receiver buffer. After this read, if more characters are still in the FIFO, the bit is set again after the FIFO is 'popped'. If programmed as FIFO full, the CPU32 has read the receiver buffer. If a character is waiting in the receiver shift register because the FIFO is full, the bit will be set again when the waiting character is loaded into the FIFO.

TxRDYA—Channel A Transmitter Ready

This bit is the duplication of the TxRDY bit in SRA.

1 = The transmitter holding register is empty and ready to be loaded with a character. This bit is set when the character is transferred to the transmitter shift register. This bit is also set when the transmitter is first enabled. Characters loaded into the transmitter holding register while the transmitter is disabled are not transmitted.

0 = The transmitter holding register was loaded by the CPU32, or the transmitter is disabled.

7.4.1.9 INTERRUPT VECTOR REGISTER (IVR). The IVR contains the 7-bit vector number of the interrupt. When the serial module is enabled (i.e., the STP bit in the MCR is cleared), this register can be read or written to at any time while in supervisor mode.

IVR $705

7	6	5	4	3	2	1	0
IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
RESET:							
0	0	0	0	1	1	1	1

Read /Write Supervisor Only

IVR7–IVR0—Interrupt Vector Bits

Each module that generates interrupts has an interrupt vector field. This 7-bit number indicates the offset from the base of the vector table where the address of the exception handler for the specified interrupt is located. The IVR is reset to $0F, which indicates an uninitialized interrupt condition. See **Section 5 CPU32** for more information.

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7.4.1.10 MODULE CONFIGURATION REGISTER (MCR). The MCR controls the serial module configuration. This register can be either read or written when the module is enabled and is in the supervisor state. The MCR is not affected by a CPU32 RESET instruction. Only the MCR can be accessed when the module is disabled (i.e., the STP bit in the MCR is set).

MCR $700

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STP	FRZ1	FRZ0	ICCS	0	0	0	0	SUPV	0	0	0	IARB			
RESET:															
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Read/Write Supervisor Only

STP—Stop Mode Bit

1 = The serial module will be disabled. Setting the STP bit stops all clocks within the serial module (including the crystal or external clock and SCLK), except for the clock from the IMB. The clock from the IMB remains active to allow CPU32 access to the MCR. The clock stops on the low phase of the clock and remains stopped until the STP bit is cleared by the CPU32 or a hardware reset. Accesses to serial module registers while in stop mode produce a bus error. The serial module should be disabled in a known state prior to setting the STP bit; otherwise, unpredictable results may occur. The STP bit should be set prior to executing the LPSTOP instruction to reduce overall power consumption.

0 = The serial module is enabled and will operate in normal mode. When STP = 0, make sure the external crystal is stable (XTAL_RDY bit (bit 3) of the ISR is zero) before continuing.

NOTE

The serial module should be disabled (i.e., the STP bit in the MCR is set) before executing the LPSTOP instruction to obtain the lowest power consumption. The X1/X2 oscillator will continue to run during LPSTOP if STP = 0.

FRZ1–FRZ0—Freeze

These bits determine the action taken when the FREEZE signal is asserted on the IMB when the CPU32 has entered background debug mode. Table 7-6 lists the action taken for each combination of bits.

Table 7-6. FRZx Control Bits

FRZ1	FRZ0	Action
0	0	Ignore FREEZE
0	1	Reserved (FREEZE Ignored)
1	0	Freeze on Character Boundary
1	1	Freeze on Character Boundary

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If FREEZE is asserted, channel A and channel B freeze independently of each other. The transmitter and receiver freeze at character boundaries. The transmitter does not freeze in the send break mode. Communications can be lost if the channel is not programmed to support flow control. See **Section 5 CPU32** for more information on FREEZE.

ICCS—Input Capture Clock Select

1 = Selects SCLK as the clear-to-send input capture clock for both channels. Clear-to-send operation is enabled by setting bit 4 in MR2. The data is captured on the $\overline{\text{CTSx}}$ pins on the rising edge of the clock.

0 = The crystal clock is the clear-to-send input capture clock for both channels.

Bits 11–8, 6–4—Reserved by Motorola

SUPV—Supervisor/User

The value of this bit has no affect on registers permanently defined as supervisor only.

1 = The serial module registers, which are defined as supervisor or user, reside in supervisor data space and are only accessible from supervisor programs.

0 = The serial module registers, which are defined as supervisor or user, reside in user data space and are accessible from either supervisor or user programs.

IARB3–IARB0—Interrupt Arbitration Bits

Each module that generates interrupts has an IARB field. These bits are used to arbitrate for the bus in the case that two or more modules simultaneously generate an interrupt at the same priority level. No two modules can share the same IARB value. The reset value of the IARB field is $0, which prevents this module from arbitrating during the interrupt acknowledge cycle. The system software should initialize the IARB field to a value from $F (highest priority) to $1 (lowest priority).

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7.4.1.11 MODE REGISTER 1 (MR1). MR1 controls some of the serial module configuration. This register can be read or written at any time when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

MR1A, MR1B $710, $718

7	6	5	4	3	2	1	0
RxRTS	R/F	ERR	PM1	PM0	PT	B/C1	B/C0
RESET:							
0	0	0	0	0	0	0	0

Read/Write Supervisor/User

RxRTS—Receiver Request-to-Send Control

1 = Upon receipt of a valid start bit, $\overline{\text{RTSx}}$ is negated if the channel's FIFO is full. $\overline{\text{RTSx}}$ is reasserted when the FIFO has an empty position available.

0 = $\overline{\text{RTSx}}$ is asserted by setting bit 1 or 0 in the OP and negated by clearing bit 1 or 0 in the OP.

This feature can be used for flow control to prevent overrun in the receiver by using the $\overline{\text{RTSx}}$ output to control the $\overline{\text{CTSx}}$ input of the transmitting device. If both the receiver and transmitter are programmed for $\overline{\text{RTS}}$ control, $\overline{\text{RTS}}$ control will be disabled for both since this configuration is incorrect. See **7.4.1.12 Mode Register 2** for information on programming the transmitter $\overline{\text{RTSx}}$ control.

R/F—Receiver-Ready Select

1 = Bit 5 for channel B and bit 1 for channel A in the ISR reflect the channel FIFO full status. These ISR bits are set when the receiver FIFO is full and are cleared when a position is available in the FIFO.

0 = Bit 5 for channel B and bit 1 for channel A in the ISR reflect the channel receiver-ready status. These ISR bits are set when a character has been received and are cleared when the CPU32 reads the receive buffer.

ERR—Error Mode

This bit controls the meaning of the three FIFO status bits (RB, FE, and PE) in the SR for the channel.

1 = Block mode—The values in the channel SR are the accumulation (i.e., the logical OR) of the status for all characters coming to the top of the FIFO since the last reset error status command for the channel was issued. Refer to **7.4.1.3 Command Register (CR)** for more information on serial module commands.

0 = Character mode—The values in the channel SR reflect the status of the character at the top of the FIFO.

NOTE

ERR = 0 must be used to get the correct A/D flag information when in multidrop mode.

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PM1–PM0—Parity Mode

These bits encode the type of parity used for the channel (see Table 7-2). The parity bit is added to the transmitted character, and the receiver performs a parity check on incoming data. These bits can alternatively select multidrop mode for the channel.

PT—Parity Type

This bit selects the parity type if parity is programmed by the parity mode bits, and if multidrop mode is selected, it configures the transmitter for data character transmission or address character transmission. Table 7-7 lists the parity mode and type or the multidrop mode for each combination of the parity mode and the parity type bits.

Table 7-7. PMx and PT Control Bits

PM1	PM0	Parity Mode	PT	Parity Type
0	0	With Parity	0	Even Parity
0	0	With Parity	1	Odd Parity
0	1	Force Parity	0	Low Parity
0	1	Force Parity	1	High Parity
1	0	No Parity	X	No Parity
1	1	Multidrop Mode	0	Data Character
1	1	Multidrop Mode	1	Address Character

B/C1–B/C0—Bits per Character

These bits select the number of data bits per character to be transmitted. The character length listed in Table 7-8 does not include start, parity, or stop bits.

Table 7-8. B/Cx Control Bits

B/C1	B/C0	Bits/Character
0	0	Five Bits
0	1	Six Bits
1	0	Seven Bits
1	1	Eight Bits

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7.4.1.12 MODE REGISTER 2 (MR2). MR2 controls some of the serial module configuration. This register can be read or written at any time the serial module is enabled (i.e., the STP bit in the MCR is cleared).

MR2A, MR2B $720, $721

7	6	5	4	3	2	1	0
CM1	CM0	TxRTS	TxCTS	SB3	SB2	SB1	SB0
RESET:							
0	0	0	0	0	0	0	0

Read/Write Supervisor/User

CM1, CM0—Channel Mode

These bits select a channel mode as listed in Table 7-9. See **7.3.3 Looping Modes** for more information on the individual modes.

Table 7-9. CMx Control Bits

CM1	CM0	Mode
0	0	Normal
0	1	Automatic Echo
1	0	Local Loopback
1	1	Remote Loopback

TxRTS—Transmitter Ready-to-Send

This bit controls the negation of the $\overline{\text{RTSA}}$ or $\overline{\text{RTSB}}$ signals. The output is normally asserted by setting OP0 or OP1 in the OPCR and negated by clearing OP0 or OP1 in the OPCR (see **7.4.1.14 Output Port Control Register (OPCR)**).

1 = In applications where the transmitter is disabled after transmission is complete, setting this bit causes the particular OP bit to be cleared automatically one bit time after the characters, if any, in the channel transmit shift register and the transmitter holding register are completely transmitted, including the programmed number of stop bits. This feature is used to automatically terminate transmission of a message. If both the receiver and the transmitter in the same channel are programmed for $\overline{\text{RTSx}}$ control, $\overline{\text{RTSx}}$ control is disabled for both since this is an incorrect configuration.

0 = Clearing this bit has no effect on the transmitter $\overline{\text{RTSx}}$.

TxCTS—Transmitter Clear-to-Send

1 = Enables clear-to-send operation. The transmitter checks the state of the $\overline{\text{CTSx}}$ input each time it is ready to send a character. If $\overline{\text{CTSx}}$ is asserted, the character is transmitted. If $\overline{\text{CTSx}}$ is negated, the channel TxDx remains in the high state, and the transmission is delayed until $\overline{\text{CTSx}}$ is asserted. Changes in $\overline{\text{CTSx}}$ while a character is being transmitted do not affect transmission of that character. If both TxCTS and TxRTS are enabled, TxCTS controls the operation of the transmitter.

0 = The $\overline{\text{CTSx}}$ has no effect on the transmitter.

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SB3–SB0—Stop-Bit Length Control

These bits select the length of the stop bit appended to the transmitted character as listed in Table 7-10. Stop-bit lengths of nine-sixteenth to two bits, in increments of one-sixteenth bit, are programmable for character lengths of six, seven, and eight bits. For a character length of five bits, one and one-sixteenth to two bits are programmable in increments of one-sixteenth bit. In all cases, the receiver only checks for a high condition at the center of the first stop-bit position—i.e., one bit time after the last data bit or after the parity bit, if parity is enabled.

If an external 1× clock is used for the transmitter, MR2 bit 3 = 0 selects one stop bit, and MR2 bit 3 = 1 selects two stop bits for transmission.

Table 7-10. SBx Control Bits

SB3	SB2	SB1	SB0	Length 6-8 Bits	Length 5 Bits
0	0	0	0	0.563	1.063
0	0	0	1	0.625	1.125
0	0	1	0	0.688	1.188
0	0	1	1	0.750	1.250
0	1	0	0	0.813	1.313
0	1	0	1	0.875	1.375
0	1	1	0	0.938	1.438
0	1	1	1	1.000	1.500
1	0	0	0	1.563	1.563
1	0	0	1	1.625	1.625
1	0	1	0	1.688	1.688
1	0	1	1	1.750	1.750
1	1	0	0	1.813	1.813
1	1	0	1	1.875	1.875
1	1	1	0	1.938	1.938
1	1	1	1	2.000	2.000

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7.4.1.13 OUTPUT PORT DATA REGISTER (OP). The bits in the OP register are set by performing a bit set command (writing to offset $71E) and are cleared by performing a bit reset command (writing to offset $71F). This register can only be written when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

Bit Set

OP $71E

7	6	5	4	3	2	1	0
$\overline{OP7}$	$\overline{OP6}$	$\overline{OP5}$	$\overline{OP4}$	$\overline{OP3}$	$\overline{OP2}$	$\overline{OP1}$	$\overline{OP0}$
RESET:							
0	0	0	0	0	0	0	0

Write Only Supervisor/User

NOTE

OP bits 7, 5, 3, and 2 are not pinned out on the MC68341; thus, changing these bits has no effect.

$\overline{OP6}$, $\overline{OP4}$, $\overline{OP1}$, $\overline{OP0}$ —Output Port Parallel Outputs

The state of these register bits is the complement of the output signal level (e.g., a reset clears these bits (logic 0), while the output signals are asserted (logic 1))

1 = These bits can be set by writing a one to the bit position(s) at this address.
0 = These bits are not affected by writing a zero to this address.

Bit Reset

OP $71F

7	6	5	4	3	2	1	0
$\overline{OP7}$	$\overline{OP6}$	$\overline{OP5}$	$\overline{OP4}$	$\overline{OP3}$	$\overline{OP2}$	$\overline{OP1}$	$\overline{OP0}$
RESET:							
0	0	0	0	0	0	0	0

Write Only Supervisor/User

NOTE

OP bits 7, 5, 3, and 2 are not pinned out on the MC68341; thus, changing these bits has no effect.

$\overline{OP6}$, $\overline{OP4}$, $\overline{OP1}$, $\overline{OP0}$ —Output Port Parallel Outputs

The state of these register bits is the complement of the output signal level (e.g., a reset clears these bits (logic 0), while the output signals are asserted (logic 1))

1 = These bits can be cleared by writing a one to the bit position(s) at this address.
0 = These bits are not affected by writing a zero to this address.

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7.4.1.14 OUTPUT PORT CONTROL REGISTER (OPCR). The OPCR individually configures four bits of the 7-bit parallel OP for general-purpose use or as an auxiliary function serving the communication channels. This register can only be written when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

OPCR $71D

7	6	5	4	3	2	1	0
OP7 $\overline{\text{TxRDYB}}$	OP6 $\overline{\text{TxRDYA}}$	OP5 $\overline{\text{RxRDYB}}$	OP4 $\overline{\text{RxRDYA}}$	OP3	OP2	OP1 $\overline{\text{RTSB}}$	OP0 $\overline{\text{RTSA}}$
RESET:							
0	0	0	0	0	0	0	0

Write Only Supervisor/User

NOTE

OP bits 7, 5, 3, and 2 are not pinned out on the MC68341; thus, changing these bits has no effect.

OP6—Output Port 6/$\overline{\text{TxRDYA}}$

1 = The OP6/$\overline{\text{TxRDYA}}$ pin functions as the transmitter-ready signal for channel A. The signal reflects the complement of the value of bit 2 of the SRA; thus, $\overline{\text{TxRDYA}}$ is a logic zero when the transmitter is ready.

0 = The OP6/$\overline{\text{TxRDYA}}$ pin functions as a dedicated output. The signal reflects the complement of the value of bit 6 of the OP.

OP4—Output Port 4/$\overline{\text{RxRDYA}}$

1 = The OP4/$\overline{\text{RxRDYA}}$ pin functions as the FIFO-full or receiver-ready signal for channel A (depending on the value of bit 6 of MR1A). The signal reflects the complement of the value of ISR bit 1; thus, $\overline{\text{RxRDYA}}$ is a logic zero when the receiver is ready.

0 = The OP4/$\overline{\text{RxRDYA}}$ pin functions as a dedicated output. The signal reflects the complement of the value of bit 4 of the OP.

OP1—Output Port 1/$\overline{\text{RTSB}}$

1 = The OP1/$\overline{\text{RTSB}}$ pin functions as the ready-to-send signal for channel B. The signal is asserted and negated according to the configuration programmed by RxRTS bit 7 in the MR1B for the receiver and TxRTS bit 5 in the MR2B for the transmitter.

0 = The OP1/$\overline{\text{RTSB}}$ pin functions as a dedicated output. The signal reflects the complement of the value of bit 1 of the OP.

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OP0—Output Port 0/$\overline{\text{RTSA}}$

1 = The OP0/$\overline{\text{RTSA}}$ pin functions as the ready-to-send signal for channel A. The signal is asserted and negated according to the configuration programmed by RxRTS bit 7 in the MR1A for the receiver and TxRTS bit 5 in the MR2A for the transmitter.

0 = The OP0/$\overline{\text{RTSA}}$ pin functions as a dedicated output. The signal reflects the complement of the value of bit 0 of the OP.

7.4.1.15 RECEIVER BUFFER (RB). The RB contains three receiver holding registers and a serial shift register. The channel's RxDx pin is connected to the serial shift register. The holding registers act as a FIFO. The CPU32 reads from the top of the stack while the receiver shifts and updates from the bottom of the stack when the shift register has been filled (see Figure 7-4). This register can only be read when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

RBA, RBB $713, $71B

7	6	5	4	3	2	1	0
RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
RESET:							
0	0	0	0	0	0	0	0

Read Only Supervisor/User

RB7–RB0—These bits contain the character in the RB.

7.4.1.16 STATUS REGISTER (SR). The SR indicates the status of the characters in the FIFO and the status of the channel transmitter and receiver. This register can only be read when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

SRA, SRB $711, $719

7	6	5	4	3	2	1	0
RB	FE	PE	OE	TxEMP	TxRDY	FFULL	RxRDY
RESET:							
0	0	0	0	0	0	0	0

Read Only Supervisor/User

RB—Received Break

1 = An all-zero character of the programmed length has been received without a stop bit. The RB bit is only valid when the RxRDY bit is set. Only a single FIFO position is occupied when a break is received. Further entries to the FIFO are inhibited until the channel RxDx returns to the high state for at least one-half bit time, which is equal to two successive edges of the internal or external 1× clock or 16 successive edges of the external 16× clock.
The received break circuit detects breaks that originate in the middle of a received character. However, if a break begins in the middle of a character, it must persist until the end of the next detected character time.

0 = No break has been received.

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FE—Framing Error

1 = A stop bit was not detected when the corresponding data character in the FIFO was received. The stop-bit check is made in the middle of the first stop-bit position. The bit is valid only when the RxRDY bit is set.

0 = No framing error has occurred.

PE—Parity Error

1 = When the with parity or force parity mode is programmed in the MR1, the corresponding character in the FIFO was received with incorrect parity. When the multidrop mode is programmed, this bit stores the received A/D bit. This bit is valid only when the RxRDY bit is set.

0 = No parity error has occurred.

OE—Overrun Error

1 = One or more characters in the received data stream have been lost. This bit is set upon receipt of a new character when the FIFO is full and a character is already in the shift register waiting for an empty FIFO position. When this occurs, the character in the receiver shift register and its break detect, framing error status, and parity error, if any, are lost. This bit is cleared by the reset error status command in the CR.

0 = No overrun has occurred.

TxEMP—Transmitter Empty

1 = The channel transmitter has underrun (both the transmitter holding register and transmitter shift registers are empty). This bit is set after transmission of the last stop bit of a character if there are no characters in the transmitter holding register awaiting transmission.

0 = The transmitter buffer is not empty. The transmitter holding register is loaded by the CPU32, or the transmitter is disabled. The transmitter is enabled/disabled by programming the TCx bits in the CR.

TxRDY—Transmitter Ready

This bit is duplicated in the ISR; bit 0 for channel A and bit 4 for channel B.

1 = The transmitter holding register is empty and ready to be loaded with a character. This bit is set when the character is transferred to the transmitter shift register. This bit is also set when the transmitter is first enabled. Characters loaded into the transmitter holding register while the transmitter is disabled are not transmitted and are lost.

0 = The transmitter holding register was loaded by the CPU32, or the transmitter is disabled.

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FFULL—FIFO Full

1 = A character was transferred from the receiver shift register to the receiver FIFO and the transfer caused the FIFO to become full (all three FIFO holding register positions are occupied).

0 = The CPU32 has read the receiver buffer and one or more FIFO positions are available. Note that if there is a character in the receiver shift register because the FIFO is full, this character will be moved into the FIFO when a position is available, and the FIFO will remain full.

RxRDY—Receiver Ready

1 = A character has been received and is waiting in the FIFO to be read by the CPU32. This bit is set when a character is transferred from the receiver shift register to the FIFO.

0 = The CPU32 has read the receiver buffer, and no characters remain in the FIFO after this read.

7.4.1.17 TRANSMITTER BUFFER (TB). The TB consists of two registers, the transmitter holding register and the transmitter shift register (see Figure 7-4). The holding register accepts characters from the bus master if the TxRDY bit in the channel's SR is set. A write to the TB clears the TxRDY bit, inhibiting any more characters until the shift register is ready to accept more data. When the shift register is empty, it checks to see if the holding register has a valid character to be sent (TxRDY bit cleared). If there is a valid character, the shift register loads the character and reasserts the TxRDY bit in the channel's SR. Writes to the TB when the channel's SR TxRDY bit is clear and when the transmitter is disabled have no effect on the TB. This register can only be written when the serial module is enabled (i.e., the STP bit in the MCR is cleared).

TBA, TBB $713, $71B

7	6	5	4	3	2	1	0
TB7	TB6	TB5	TB4	TB3	TB2	TB1	TB0
RESET:							
0	0	0	0	0	0	0	0

Write Only Supervisor/User

TB7–TB0—These bits contain the character in the TB.

7.4.2 Programming

The basic interface software flowchart required for operation of the serial module is shown in Figure 7-10. The routines are divided into three categories:

- Serial Module Initialization
- I/O Driver
- Interrupt Handling

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7.4.2.1 SERIAL MODULE INITIALIZATION. The serial module initialization routines consist of SINIT and CHCHK. SINIT is called at system initialization time to check channel A and channel B operation. Before SINIT is called, the calling routine allocates two words on the system stack. Upon return to the calling routine, SINIT passes information on the system stack to reflect the status of the channels. If SINIT finds no errors in either channel A or channel B, the respective receivers and transmitters are enabled. The CHCHK routine performs the actual channel checks as called from the SINIT routine. When called, SINIT places the specified channel in the local loopback mode and checks for the following errors:

- Transmitter Never Ready
- Receiver Never Ready
- Parity Error
- Incorrect Character Received

7.4.2.2 I/O DRIVER EXAMPLE. The I/O driver routines consist of INCH, OUTCH, and POUTCH. INCH is the terminal input character routine and gets a character from the channel A receiver and places it in the lower byte of register D0. OUTCH is used to send the character in the lower byte of register D0 to the channel A transmitter. POUTCH sends the character in the lower byte of D0 to the channel B transmitter.

7.4.2.3 INTERRUPT HANDLING. The interrupt handling routine consists of SIRQ, which is executed after the serial module generates an interrupt caused by a channel A change-in-break (beginning of a break). SIRQ then clears the interrupt source, waits for the next change-in-break interrupt (end of break), clears the interrupt source again, then returns from exception processing to the system monitor.

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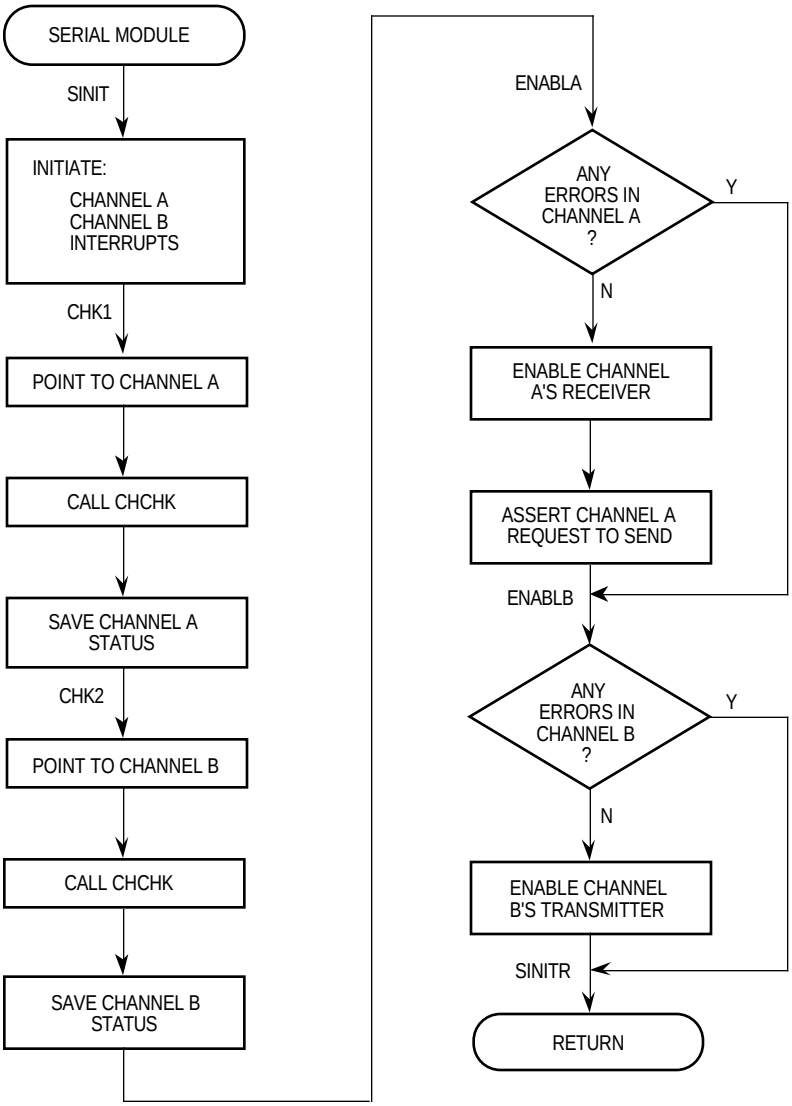

Figure 7-10. Serial Module Programming Flowchart (1 of 5)

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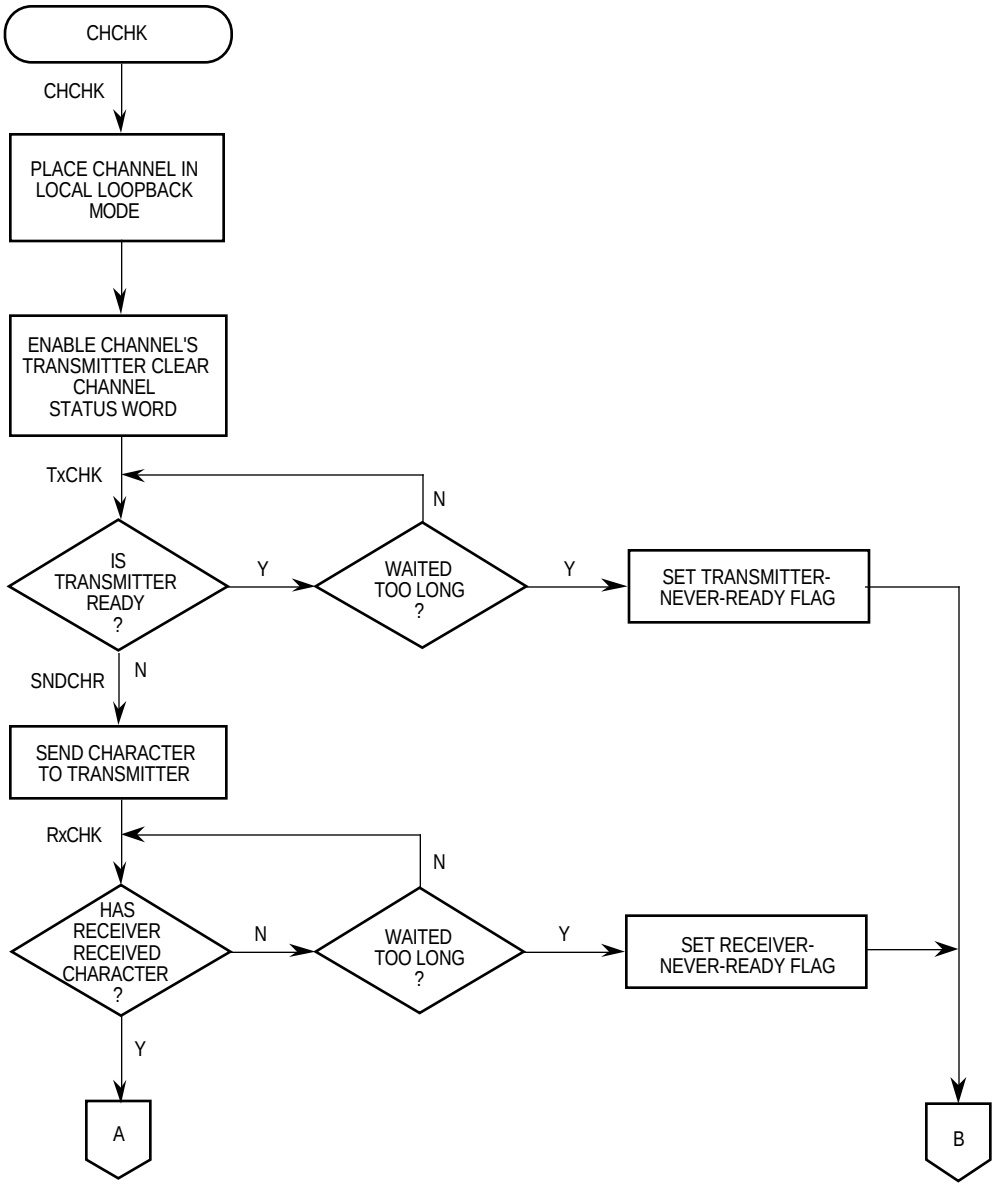

Figure 7-10. Serial Module Programming Flowchart (2 of 5)

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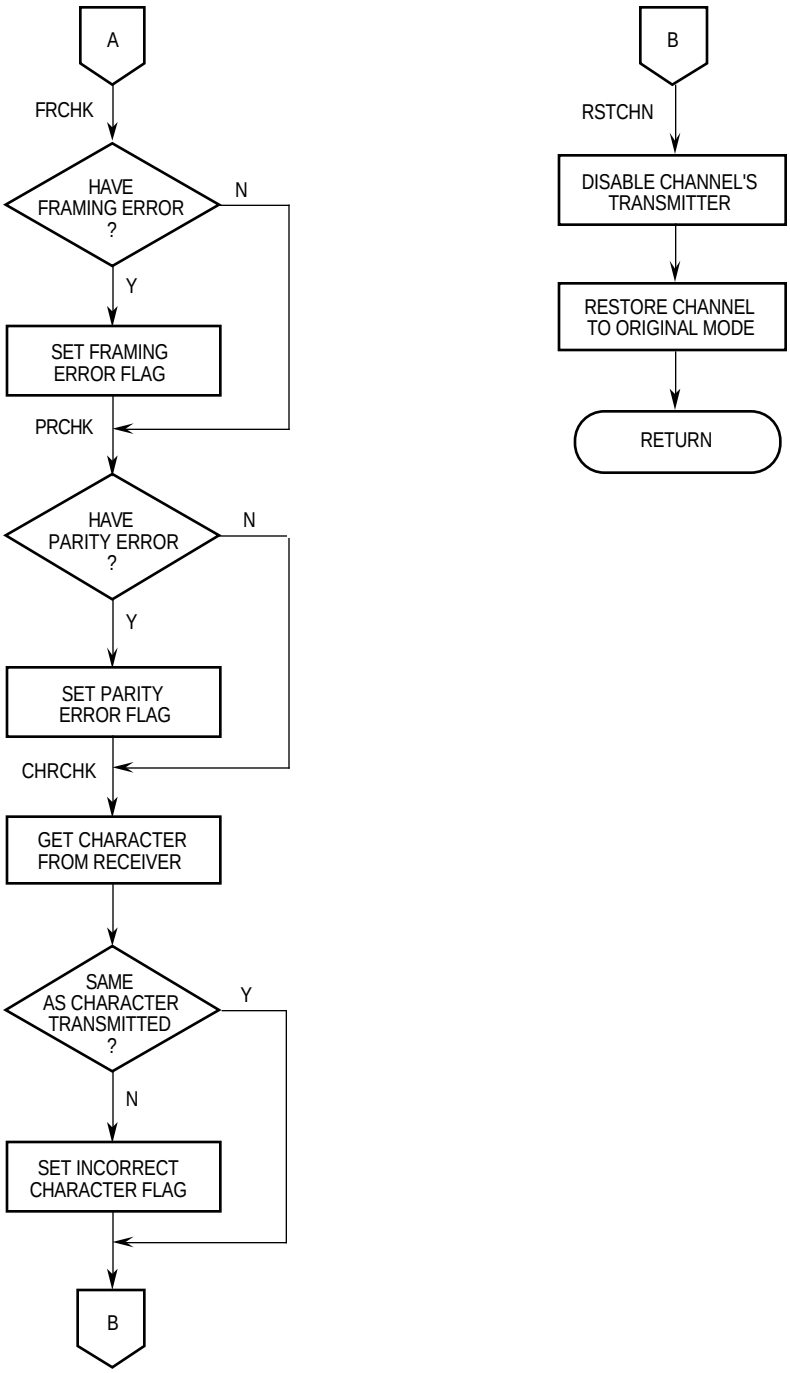

Figure 7-10. Serial Module Programming Flowchart (3 of 5)

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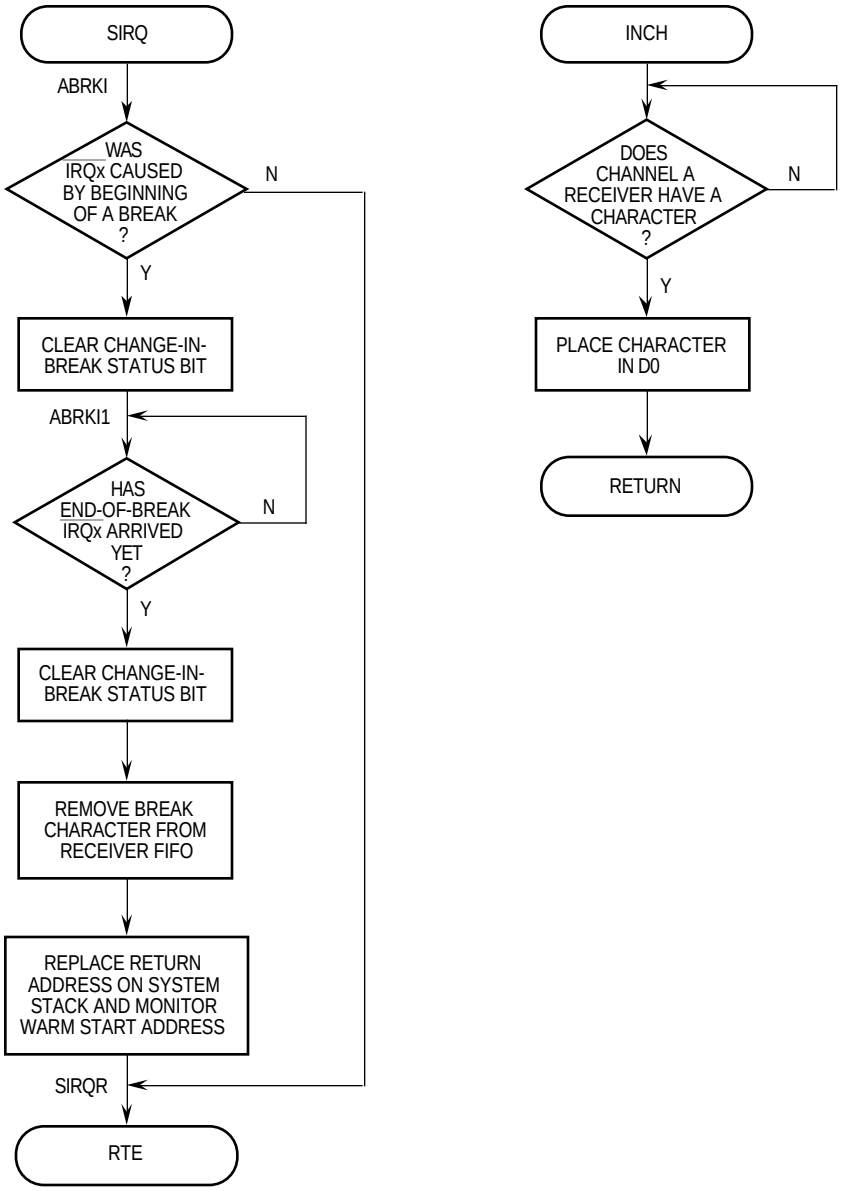

Figure 7-10. Serial Module Programming Flowchart (4 of 5)

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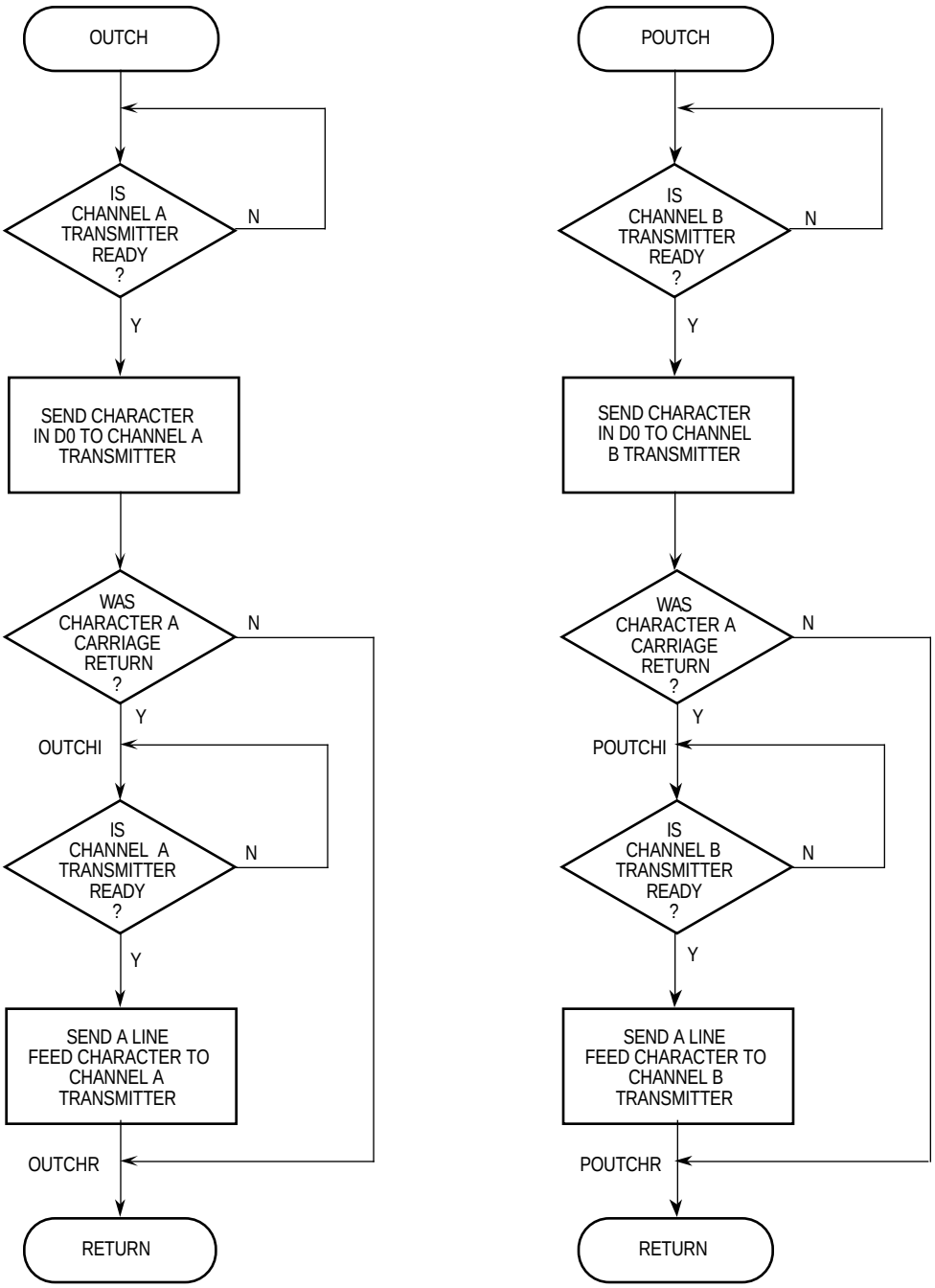

Figure 7-10. Serial Module Programming Flowchart (5 of 5)

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7.5 SERIAL MODULE INITIALIZATION SEQUENCE

The following paragraphs discuss a suggested method for initializing the serial module.

7.5.1 Serial Module Configuration

If the serial capability of the MC68341 is being used, the following steps are required to properly initialize the serial module.

NOTE

The serial module registers can only be accessed by byte operations.

Command Register (CR)

- Reset the receiver and transmitter for each channel.

The following steps program both channels:

Module Configuration Register (MCR)

- Initialize the stop bit (STP) for normal operation.
- Select whether to respond to or ignore FREEZE (FRZx bits).
- Select the input capture clock (ICCS bit).
- Select the access privilege for the supervisor/user registers (SUPV bit).
- Select the interrupt arbitration level for the serial module (IARBx bits).

Interrupt Vector Register (IVR)

- Program the vector number for a serial module interrupt.

Interrupt Level Register (ILR)

- Program the interrupt priority level for a serial module interrupt.

Interrupt Enable Register (IER)

- Enable the desired interrupt sources.

Auxiliary Control Register (ACR)

- Select baud rate set (BRG bit).
- Initialize the input enable control (IEC bits).

Output Port Control Register (OPCR)

- Select the function of the output port pins.

Interrupt Status Register (ISR)

- The XTAL_RDY bit should be polled until it is cleared to ensure that an unstable crystal input is not applied to the baud rate generator.

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The following steps are channel specific:

Clock Select Register (CSR)

- Select the receiver and transmitter clock.

Mode Register 1 (MR1)

- If desired, program operation of receiver ready-to-send (RxRTS bit).
- Select receiver-ready or FIFO-full notification (R/F bit).
- Select character or block error mode (ERR bit).
- Select parity mode and type (PM and PT bits).
- Select number of bits per character (B/Cx bits).

Mode Register 2 (MR2)

- Select the mode of channel operation (CMx bits).
- If desired, program operation of transmitter ready-to-send (TxRTS bit).
- If desired, program operation of clear-to-send (TxCTS bit).
- Select stop-bit length (SBx bits).

Command Register (CR)

- Enable the receiver and transmitter.

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7.5.2 Serial Module Example Configuration Code

The following code is an example of a configuration sequence for the serial module.

```
*****************************************************************************
* MC68341 basic serial module register initialization example code.
* This code is used to initialize the 68341's internal serial module registers,
* providing basic functions for operation.
* It sets up serial channel A for communication with a 9600 baud terminal.
* Note: All serial module registers must be accessed as bytes.
*****************************************************************************
*****************************************************************************
* equates
*****************************************************************************
MBAR  EQU   $0003FF00   Address of SIM41 Module Base Address Reg.
MODBASE     EQU   $FFFFF000   SIM41 MBAR address value

*****************************************************************
* Serial module equates
SERIAL      EQU   $700              Offset from MBAR for serial module regs
MCRH  EQU   $0                 serial MCR high byte
MCRL  EQU   $1                 serial MCR low byte

* Serial register offsets from serial base address
MR1A      EQU     $10         Mode register 1 A
MR2A      EQU     $20         Mode register 2 A
SRA       EQU     $11         Status register A
CSRA      EQU     $11         Clock select reg A
CRA       EQU     $12         Command reg A

ACR       EQU     $14         Auxiliary control reg
OPCR      EQU     $1D         Output port control reg
OP_BS     EQU     $1E         Output port bit set (write 1 to set)
OP_BR     EQU     $1F         Output port bit reset (write 1 to clear)


*****************************************************************************
*****************************************************************************
* Initialize Serial channel A
*****************************************************************************
      LEA   MODBASE+SERIAL,A0 Pointer to serial channel A

* Module configuration register:
* Enable serial module for normal operation, ignore FREEZE, select the
* crystal clock. Supervisor/user serial registers unrestricted.
* Interrupt arbitration at priority $02.
      MOVE.B      #$00,MCRH(A0)
      MOVE.B      #$02,MCRL(A0)

* WAIT FOR TRANSMITTER EMPTY (OR TIMEOUT)
      MOVE.W      #$2000,D0               init loop counter
XBMTWAIT EQU      *
      BTST        #3,SRA(A0)              TX empty in status reg?
      NOP
      DBNE  D0,XBMTWAIT       loop until set or timeout
```


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```
* NEGATE RTSA SIGNAL OUTPUT
      MOVE.B      #0,OPCR(A0)       make OP0-7 general purpose
      MOVE.B      #$01,OP_BR(A0)          clear RTSA/OP0 output

* RESET RECEIVER/TRANSMITTER
      MOVE.B      #$20,CRA(A0)            Issue reset receiver command
      MOVE.B      #$30,CRA(A0)            Issue reset transmitter command

* SET BAUD RATE SET 2
      MOVE.B      #$80,ACR(A0)

* MODE REGISTER 1
      MOVE.B      #$93,MR1A(A0)           8 bits, no parity, auto RTS control

* MODE REGISTER 2
      MOVE.B      #$07,MR2A(A0)           Normal, 1 stop bit

* SET UP BAUD RATE FOR PORT IN CLOCK SELECT REGISTER
      MOVE.B      #$BB,CSRA(A0)           Set 9600 baud for RX and TX

* SET RTSA ACTIVE
      MOVE.B      #$01,OP_BS(A0)          set RTSA/OP0 output

* ENABLE PORT
      MOVE.B      #$45,CRA(A0)            Reset error status, enable RX & TX

*****************************************************************************
      END
*****************************************************************************
```

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SECTION 8
TIMER MODULE

The MC68341 timer module contains a counter/timer as shown in Figure 8-1. The timer interfaces directly to the CPU32 via the intermodule bus (IMB). The timer consists of the following major areas:

- A General-Purpose Counter/Timer
- Internal Control Logic
- Interrupt Control Logic

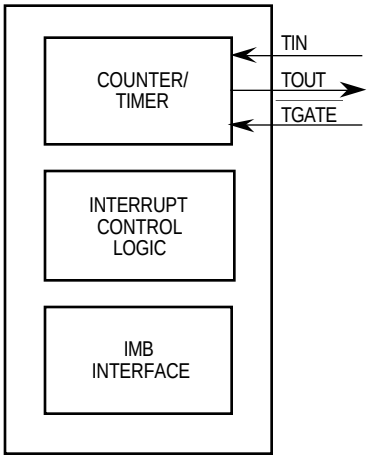

Figure 8-1. Simplified Block Diagram

8.1 MODULE OVERVIEW

The timer module consists of the following functional features:

- Versatile General-Purpose Timer
- 8-Bit Prescaler/16-Bit Counter
- Programmable Timer Modes:

— Input Capture/Output Compare

— Square-Wave Generation

— Variable Duty-Cycle Square-Wave Generation

— Variable-Width Single-Shot Pulse Generation

— Pulse-Width Measurement

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— Period Measurement

— Event Counting

• Seven Maskable Interrupt Conditions Based on Programmable Events

8.1.1 Timer and Counter Functions

The timer can perform virtually any application traditionally assigned to timers and counters. The timer can be used to generate timed events that are independent of the timing errors to which real-time programmed microprocessors are susceptible—for example, those of dynamic memory refreshing, DMA cycle steals, and interrupt servicing.

The timer has several functional areas: an 8-bit countdown prescaler, a 16-bit down counter, time-out logic, compare logic, and clock selection logic. Figure 8-2 shows a functional diagram of the timer module.

8.1.1.1 PRESCALER AND COUNTER. The counter can be driven directly by the selected clock or the prescaler output. Both the counter and prescaler are updated on the falling edge of the clock. During reset, the prescaler is set to $FF, and the counter is set to $0000. The counter is loaded with a programmed value on the first falling edge of the counter clock after the timer is enabled and again when a time-out occurs (counter reaches $0000). The prescaler and counter can be used as one 24-bit counter by enabling the prescaler and selecting the divide-by-256 prescaler output. Refer to **8.4 Register Description** for additional information on how to program the timer.

8.1.1.2 TIME-OUT DETECTION. Time-out is achieved when all 16 stages of the counter transition to zero, a counter value of $0000. Time-out is a defined counter event which triggers specific actions depending upon the programmed mode of operation. Refer to **8.3 Operating Modes** for descriptions of the individual modes.

8.1.1.3 COMPARATOR. The comparator block compares the value in the 16-bit compare register (COM) with the output of the 16-bit counter. When an exact match is detected, bits in the status register (SR) are set to indicate this condition. When in the input capture/output compare mode, a match is a defined counter event that can affect the output of the timer (TOUT). Refer to **8.3.1 Input Capture/Output Compare** for additional information on this mode.

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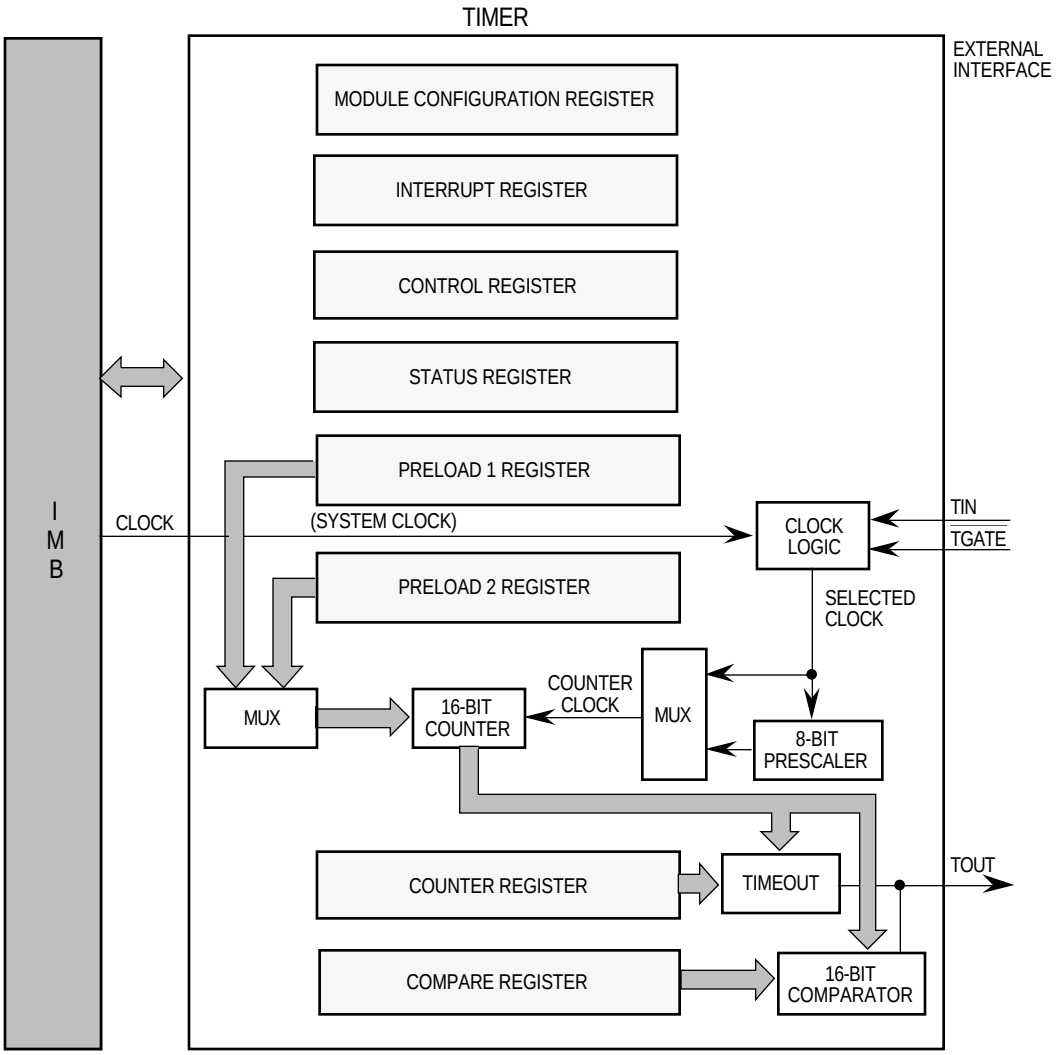

Figure 8-2. Timer Functional Diagram

8.1.1.4 CLOCK SELECTION LOGIC. The clock selection logic consists of two multiplexers that select the clocks applied to the prescaler and counter. The first multiplexer (labeled clock logic in Figure 8-2) selects between the clock input to the timer (TIN) or one-half the frequency of the system clock (CLKOUT). This output of the first multiplexer (called selected clock) is applied to both the 8-bit prescaler and the second multiplexer. The second multiplexer selects the clock for the 16-bit counter, which is either the selected clock or the 8-bit prescaler output.

8.1.2 Internal Control Logic

The timer receives operation commands on the IMB and, in turn, issues appropriate operation signals to the internal timer control logic. This mechanism allows the timer registers to be accessed and programmed. Refer to **8.4 Register Description** for additional information.

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8.1.3 Interrupt Control Logic

The timer provides seven interrupt request outputs ($\overline{IRQ7}$–$\overline{IRQ1}$) to notify the CPU32 that an interrupt has occurred. The interrupts are described in **8.4 Register Description**. Bits in the SR indicate all currently active interrupt conditions. The interrupt enable (IE) bits in the control register (CR) are programmable to mask any events that may cause an interrupt.

8.2 TIMER MODULES SIGNAL DEFINITIONS

This section contains a brief description of the timer module signals (see Figure 8-3).

NOTE

The terms *assertion* and *negation* are used throughout this section to avoid confusion when dealing with a mixture of active-low and active-high signals. The term *assert* or *assertion* indicates that a signal is active or true independent of the level represented by a high or low voltage. The term *negate* or *negation* indicates that a signal is inactive or false.

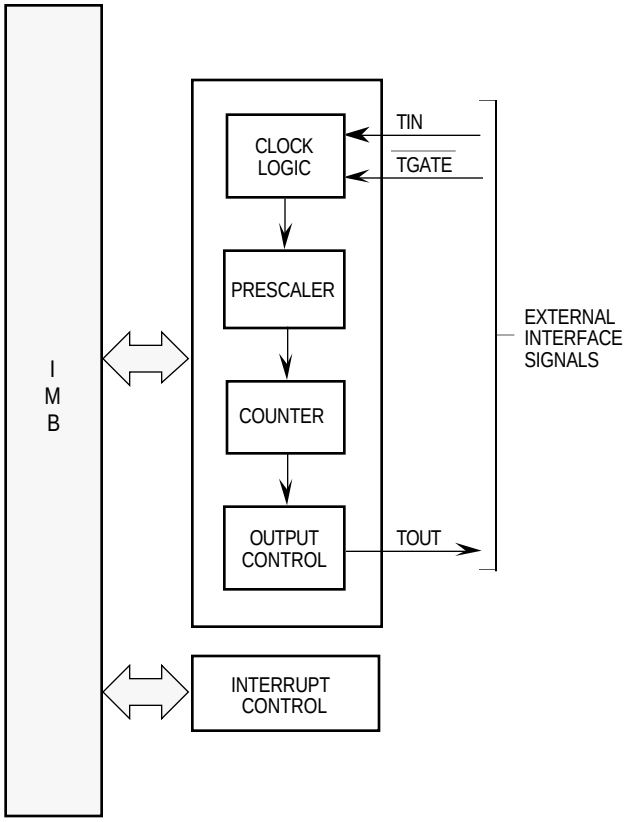

Figure 8-3. External and Internal Interface Signals

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8.2.1 Timer Input (TIN)

This input can be programmed to be the clock that causes events to occur in the counter and prescaler. TIN is internally synchronized to the system clock to guarantee that a valid TIN level is recognized. Additionally, the high and low levels of TIN must each be stable for at least one system clock period plus the sum of the setup and hold times for TIN. Refer to **Section 12 Electrical Characteristics**, for additional information.

8.2.2 Timer Gate ($\overline{\text{TGATE}}$)

This active-low input can be programmed to enable and disable the counter and prescaler. $\overline{\text{TGATE}}$ may also be programmed to be a simple input. For more information on the modes of operation, refer to **8.3 OPERATING MODES**. To guarantee that the timer recognizes a valid level on $\overline{\text{TGATE}}$, the signal is synchronized with the system clock. Additionally, the high and low levels of this input must each be stable for at least one system clock period plus the sum of the setup and hold times for $\overline{\text{TGATE}}$. Refer to **Section 12 Electrical Characteristics**, for additional information.

8.2.3 Timer Output (TOUT)

This output drives the various output waveforms generated by the timer. The initial level and transitions can be programmed by the output control (OC) bits in the CR.

8.3 OPERATING MODES

The following paragraphs contain a detailed description of each timer operation mode and of the IMB operation during accesses to the timer. Changing the contents of the CR should only be attempted when the timer is disabled (the software reset (SWR) bit in the CR is cleared). Changing the CR while the timer is running may produce unpredictable results.

8.3.1 Input Capture/Output Compare

This mode has the capability of capturing a counter value by holding the value in the counter register (CNTR). Additionally, this mode can provide compare information via TOUT to indicate when the counter has reached the compare value. This mode can be used for square-wave generation, pulse-width modulation, or periodic interrupt generation. This mode can be selected by programming the operation mode bits (MODEx) in the CR to 000.

The timer is enabled when the counter prescaler enable (CPE) and SWRx bits in the CR are set. Once enabled, the counter enable (ON) bit in the SR is set, and the next falling edge of the counter clock causes the counter to be loaded with the value in the preload 1 register (PREL1).

The $\overline{\text{TGATE}}$ signal functions differently in this mode than it does in the other modes. $\overline{\text{TGATE}}$ does not enable or disable the counter/prescaler input clock; instead, it is used to disable shadowing. Normally, the counter is decremented on the falling edge of the counter clock, and the CNTR is updated on the next rising edge of the system clock; thus,

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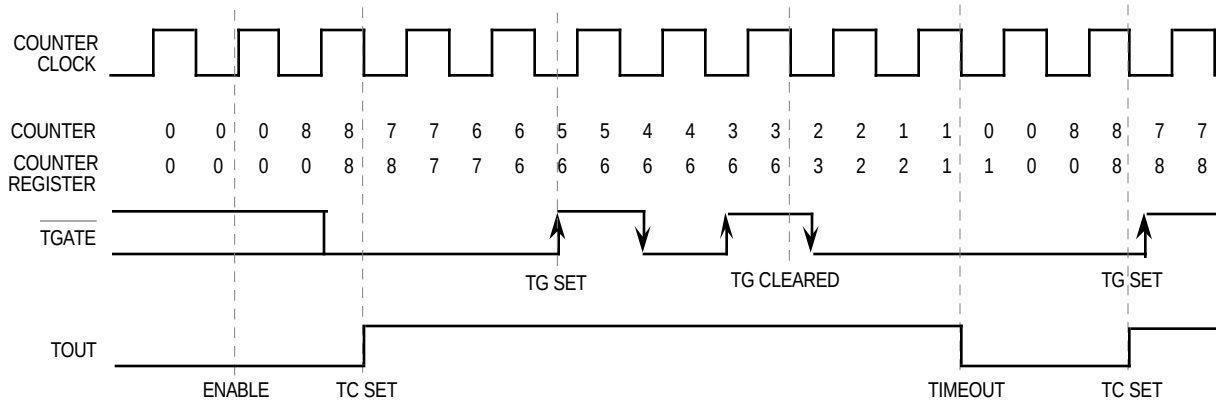
the CNTR shadows the actual value of the counter. The timer gate interrupt (TG) bit in the SR must be cleared for shadowing to occur. $\overline{\text{TGATE}}$ is used to set the TG bit and disable shadowing. If the timing gate is enabled (TGE bit of the CR is set), the TG bit is set by the rising edge of $\overline{\text{TGATE}}$. Shadowing is disabled until the TG bit is cleared by writing a one to its location in the SR. See Figure 8-4 for a depiction of this mode. If the timing gate is disabled (CR TGE bit is cleared), $\overline{\text{TGATE}}$ has no effect on the operation of the timer; thus the input capture function is inoperative. At all times, the $\overline{\text{TGATE}}$ level bit (TGL) in the SR reflects the level of the $\overline{\text{TGATE}}$ signal.



Modex Bits in Control Register = 000
Preload 1 Register = 8
Compare Register = 7
TGE Bit of Status Register = 1
TG Bit in Status Register Initially = 0
OCx Bits in Control Register = 10

Figure 8-4. Input Capture/Output Compare Mode

Since the counter is not affected by $\overline{\text{TGATE}}$, it continues to decrement on the falling edge of the counter clock and load from the PREL1 at time-out, regardless of the value of $\overline{\text{TGATE}}$.

When the counter counts down to the value contained in the COM, this condition is reflected by setting the timer compare (TC) and compare (COM) bits in the SR. TOUT responds as selected by the OCx bits in the CR. The output level (OUT) bit in the SR reflects the value on TOUT. Shadowing does not affect this operation.

If the counter counts down to $0000, a time-out is detected, causing the SR time-out interrupt (TO) bit to be set and the SR COM bit to be cleared. On the next falling edge of the counter clock after the time-out is detected, the value in PREL1 is again loaded into the counter. TOUT responds as selected by the CR OCx bits.

A square-wave generator can be implemented by programming the CR OCx bits to toggle mode. The value in the COM should be one-half the value in PREL1 to cause an event to happen twice in the countdown.

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This mode can be used as a pulse-width modulator by programming the CR OCx bits to zero mode or one mode. The value in the PREL1 specifies the frequency, and the COM determines the pulse width. The pulse widths can be changed by writing a new value to the COM.

Periodic interrupt generation can be accomplished by enabling the TO, TG, and/or TC bits in the SR to generate interrupts by programming the IE bits of the CR. When enabled, the programmed $\overline{\text{IRQx}}$ signal is asserted whenever the specified bits are set.

TOUT signal transitions can be controlled by writing new values into the COM. Caution must be exercised when accessing the COM. If it were to be accessed simultaneously by the compare logic and by a write, the old compare value may actually get compared to the counter value.

8.3.2 Square-Wave Generator

This mode can be used for generating both square-wave output and periodic interrupts. The square wave is generated by counting down from the value in the PREL1 to time-out (counter value of $0000). TOUT changes state on each time-out as programmed. This mode can be selected by programming the CR MODEx bits to 001.

The timer is enabled by setting the SWR and CPE bits in the CR and, if $\overline{\text{TGATE}}$ is programmed to control the enabling and disabling of the counter (TGE bit set in the CR), then asserting $\overline{\text{TGATE}}$. When the timer is enabled, the ON bit in the SR is set. On the next falling edge of the counter clock, the counter is loaded with the value stored in the PREL1 (N). With each successive falling edge of the counter clock, the counter decrements. The time between enabling the timer and the first time-out can range from N to N + 1 periods. When $\overline{\text{TGATE}}$ is used to enable the timer, the enabling of the timer is asynchronous; however, if timing is carefully considered, the time to the first time-out can be known. For additional details on timing, see **Section 12 Electrical Characteristics**.

TOUT behaves as a square wave when the OCx bits of the CR are programmed for toggle mode. A time-out occurs every N + 1 periods (allowing for the zero cycle), resulting in a change of state on TOUT (see Figure 8-5). The SR OUT bit reflects the level of TOUT. If this mode is used to generate periodic interrupts, TOUT may be enabled if a square wave is also desired.

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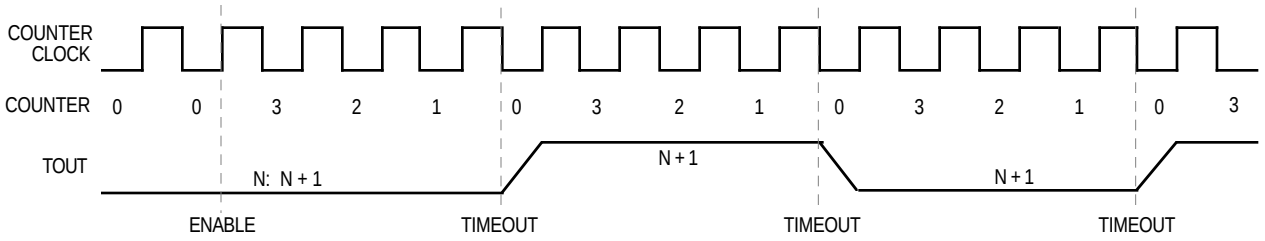

MODEx Bits in Control Register = 001
Preload 1 Register = N = 3
OCx Bits in Control Register = 01

Figure 8-5. Square-Wave Generator Mode

If $\overline{\text{TGATE}}$ is negated when it is enabled to control the timer (TGE = 1), the prescaler and counter are disabled. Additionally, the SR TG bit is set, indicating that $\overline{\text{TGATE}}$ was negated. The SR ON bit is cleared, indicating that the timer is disabled. If $\overline{\text{TGATE}}$ is reasserted, the timer is re-enabled and begins counting from the value attained when $\overline{\text{TGATE}}$ was negated. The SR ON bit is set again.

If $\overline{\text{TGATE}}$ is disabled (TGE = 0), $\overline{\text{TGATE}}$ has no effect on the operation of the timer. In this case, the counter begins counting on the falling edge of the counter clock immediately after the SWR and CPE bits in the CR are set. The TG bit of the SR cannot be set. At all times, TGL in the SR reflects the level of $\overline{\text{TGATE}}$.

If the counter counts down to the value stored in the COM register, then the COM and TC bits in the SR are set. The counter continues counting down to time-out. At this time, the SR TO bit is set, and the SR COM bit is cleared. The next falling edge of the counter clock after time-out causes the value in PREL1 to be loaded back into the counter, and the counter begins counting down from this value.

The period of the square-wave generator can be changed dynamically by writing a new value into the PREL1. Caution must be used because, if PREL1 is accessed simultaneously by the counting logic and a CPU32 write, the old PREL1 value may actually get loaded into the counter at time-out.

Periodic interrupt generation can be accomplished by enabling the TO, TG, and/or TC bits in the SR to generate interrupts by programming the CR IE bits. When enabled, the programmed $\overline{\text{IRQx}}$ signal is asserted whenever the specified bits are set.

8.3.3 Variable Duty-Cycle Square-Wave Generator

In this mode, both the PREL1 and PREL2 registers are used to generate a square wave with virtually any duty cycle. The square wave is generated by counting down from the value in the PREL1 to time-out (count value $0000), then loading that value from PREL2 and again counting down to time-out. When this second time-out occurs, the value from PREL1 is loaded into the counter, and the cycle repeats. TOUT can be programmed to change state with every time-out, thus generating a variable duty-cycle square wave. This mode can be selected by programming the MODE bits in the CR to 010.

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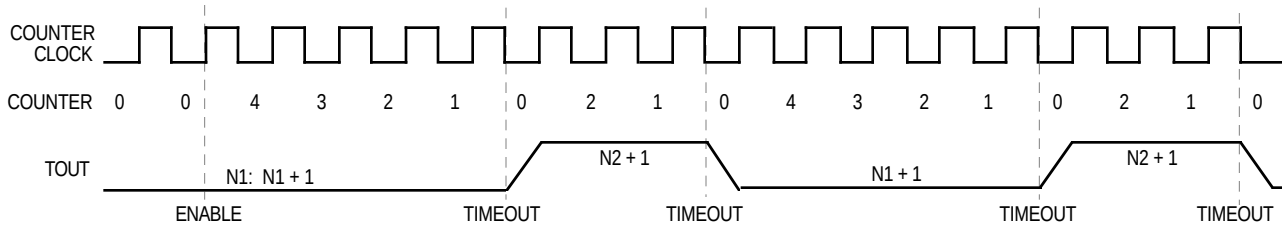
The timer is enabled by setting both the SWR and CPE bits in the CR and, if $\overline{\text{TGATE}}$ is enabled (CR TGE bit is set), then asserting $\overline{\text{TGATE}}$. When the timer is enabled, the ON bit in the SR is set. On the next falling edge of the counter clock, the counter is loaded with the value stored in the PREL1 register (N1). With each successive falling edge of the counter clock, the counter decrements. The time between enabling the timer and the first time-out can range from N1 to N1+1 periods. When $\overline{\text{TGATE}}$ is used to enable the timer, the enabling of the timer is asynchronous; however, if timing is carefully considered, the time to the first time-out can be known. For additional details on timing, see the **Section 12 Electrical Characteristics**.

If the counter counts down to the value stored in the COM register, the COM and timer compare interrupt (TC) bits in the SR are set. The counter continues counting down to time-out. At this time, the TO bit in the SR is set, and the COM bit is cleared. The next falling edge of the counter clock after time-out causes the value in PREL2 (N2) to be loaded into the counter, and the counter begins counting down from this value. Each successive time-out causes the counter to be loaded alternately with the values from PREL1 and PREL2.

TOUT behaves as a variable duty-cycle square wave when the CR OC bits are programmed for toggle mode. The second time-out occurs after N2 + 1 periods (allowing for the zero cycle), resulting in a change of state on TOUT. The third time-out occurs after N1 + 1 periods, resulting in a change of state on TOUT, and so on (see Figure 8-6). The OUT bit in the SR reflects the level of TOUT.



MODEx Bits in Control Register = 010
Preload 1 Register = N1 = 4
Preload 2 Register = N2 = 2
OCx Bits in Control Register = 01

Figure 8-6. Variable Duty-Cycle Square-Wave Generator Mode

If $\overline{\text{TGATE}}$ is negated when it is enabled (TGE = 1), the prescaler and counter are disabled. Additionally, the TG bit of the SR is set, indicating that $\overline{\text{TGATE}}$ was negated. The ON bit of the SR is cleared, indicating that the timer is disabled. If $\overline{\text{TGATE}}$ is reasserted, the timer is re-enabled and begins counting from the value attained when $\overline{\text{TGATE}}$ was negated. The ON bit is set again.

If $\overline{\text{TGATE}}$ is not enabled (TGE = 0), $\overline{\text{TGATE}}$ has no effect on the operation of the timer. In this case, the counter would begin counting on the falling edge of the counter clock immediately after the SWR and CPE bits in the CR are set. The SR TG bit cannot be set. At all times, the TGL bit in the SR reflects the level of $\overline{\text{TGATE}}$.

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The duty cycle of the waveform generated on TOUT can be dynamically changed by writing new values into PREL1 and/or PREL2. If PREL1 or PREL2 is being accessed simultaneously by the counter logic and a CPU32 write, the old preload value may actually get loaded into the counter at time-out. If at time-out, the counting logic was accessing PREL2 and the CPU32 was writing to PREL1 (or vice versa), there would be no unexpected results.

8.3.4 Variable-Width Single-Shot Pulse Generator

This mode is used to produce a one-time pulse that has a delay controlled by the value stored in PREL1 and a duration controlled by the value stored in PREL2. With TOUT programmed to change state, this sequence creates a single pulse of variable width. This mode can be selected by programming the CR MODE bits to 011.

The timer is enabled by setting both the SWR and CPE bits in the CR and, if $\overline{\text{TGATE}}$ is enabled (TGE bit in the CR is set), then asserting $\overline{\text{TGATE}}$. When the timer is enabled, the ON bit in the SR is set. On the next falling edge of the counter clock, the counter is loaded with the value stored in the PREL1 register (N1). With each successive falling edge of the counter clock, the counter decrements. The time between enabling the timer and the first time-out can range from N1 to N1 + 1 periods. When $\overline{\text{TGATE}}$ is used to enable the counter, the enabling of the timer is asynchronous; however, if timing is carefully considered, the time to the first time-out can be known. For additional details on timing, see **Section 12 Electrical Characteristics**.

If the counter counts down to the value stored in the COM, the COM and TC bits in the SR are set. The counter continues counting down to time-out. At this time, the SR TO bit is set and the SR COM bit is cleared. The next falling edge of the counter clock after time-out causes the value in PREL2 (N2) to be loaded into the counter, and the counter begins counting down from this value. After the second time-out, the selected clock is held high, disabling the prescaler and counter. Additionally, the SR ON and COM bits are cleared.

TOUT behaves as a variable-width pulse when the OCx bits of the CR are programmed for toggle mode. TOUT is a logic zero between the time that the timer is enabled and the first time-out. When this event occurs, TOUT transitions to a logic one. The second time-out occurs after N2 + 1 periods (allowing for the zero cycle), resulting in TOUT returning to a logic zero (see Figure 8-7). The OUT bit in the SR reflects the level of TOUT.

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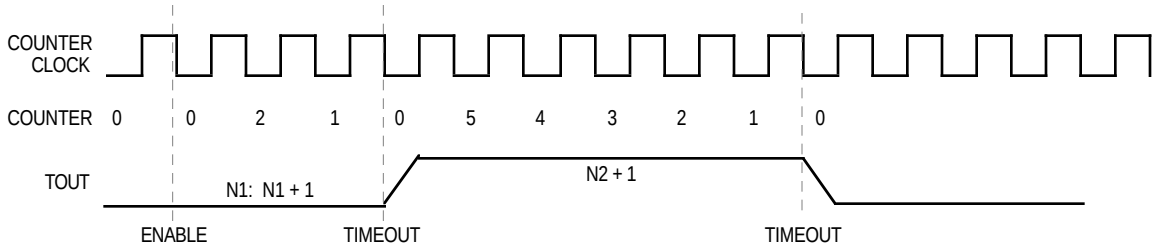

MODEx Bits in Control Register = 011
Preload 1 Register = N1 = 2
Preload 2 Register = N2 = 5
OCx bits in Control Register = 01

Figure 8-7. Variable-Width Single-Shot Pulse Generator Mode

If $\overline{\text{TGATE}}$ is negated when it is enabled (TGE = 1), the prescaler and counter are disabled. Additionally, the SR TG bit is set, indicating that $\overline{\text{TGATE}}$ was negated. The SR ON bit is cleared, indicating that the timer is disabled. If $\overline{\text{TGATE}}$ is reasserted, the timer is re-enabled and begins counting from the value attained when $\overline{\text{TGATE}}$ was negated. The ON bit is set again.

If $\overline{\text{TGATE}}$ is not enabled (TGE = 0), $\overline{\text{TGATE}}$ has no effect on the operation of the timer. In this case, the counter would begin counting on the falling edge of the counter clock immediately after the SWR and CPE bits in the CR are set. The SR TG bit cannot be set. At all times, the TGL bit in the SR reflects the level of $\overline{\text{TGATE}}$.

The width of the pulse generated on TOUT (the value in PREL2) can be changed while the counter is counting down from the value in PREL1. Caution must be used because, if PREL2 is accessed simultaneously by the counting logic and a CPU32 write, the old PREL2 value may actually get loaded into the counter at time-out.

8.3.5 Pulse-Width Measurement

This mode is used to count the clock cycles during a particular event (see Figure 8-8). The event is defined by the assertion and negation of $\overline{\text{TGATE}}$. When $\overline{\text{TGATE}}$ is asserted, the counter begins counting down from $FFFF. When $\overline{\text{TGATE}}$ is negated, the counter stops counting and holds the value at which it stopped. Further assertions and negations of $\overline{\text{TGATE}}$ have no effect on the counter. This mode can be selected by programming the CR MODEx bits to 100.

The timer is enabled by setting the SWR, CPE, and TGE bits in the CR. Asserting $\overline{\text{TGATE}}$ starts the counter. When the timer is enabled, the SR ON bit is set. On the next falling edge of the counter clock, the counter is loaded with the value $FFFF. With each successive falling edge of the counter clock, the counter decrements. The PREL1 and PREL2 registers are not used in this mode.

When $\overline{\text{TGATE}}$ is negated, the SR TG bit is set, the ON bit is negated, and the prescaler and counter are disabled. Subsequent transitions on $\overline{\text{TGATE}}$ do not re-enable the counter. The TGL bit in the SR reflects the level of $\overline{\text{TGATE}}$ at all times.

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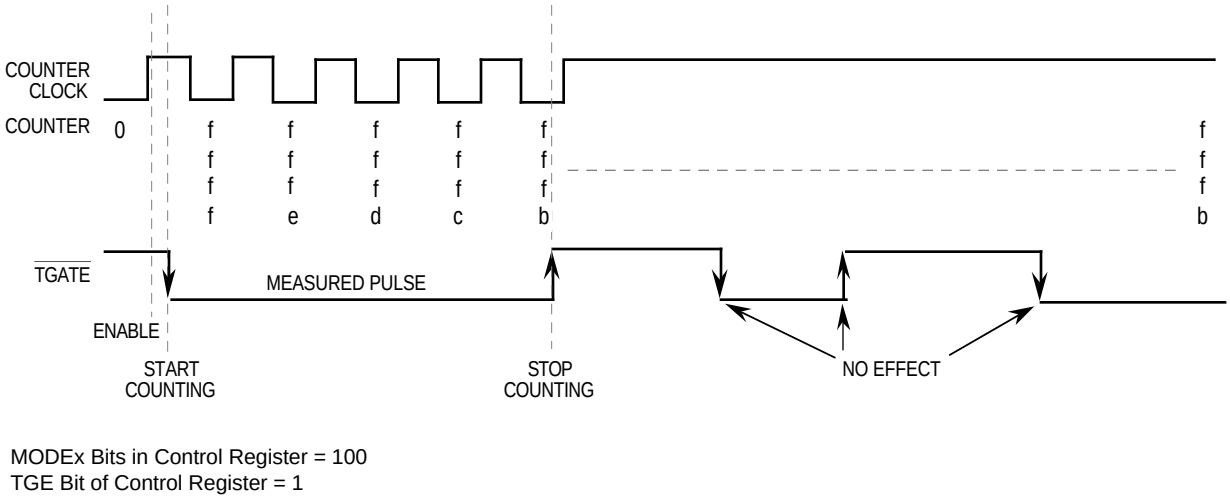

Figure 8-8. Pulse-Width Measurement Mode

If the counter counts down to the value stored in the COM register, the COM and TC bits in the SR are set. If the counter counts down to $0000, a time-out is detected. This sets the SR TO, and the clears the COM bit. At time-out, the next falling edge of the counter clock causes the counter to reload with $FFFF. TOUT transitions at time-out or is disabled as programmed by the CR OCx bits. The SR OUT bit reflects the level on TOUT.

To determine the number of cycles counted, the value in the CNTR must be read, inverted, and incremented by 1 (the first count is $FFFF which, in effect, includes a count of zero). The counter counts in a true 2^{16} fashion. For measuring pulses of even greater duration, the value in the POx bits in the SR is readable and can be thought of as an extension of the least significant bits in the CNTR.

NOTE

Once the timer has been enabled, do not clear the SR TG bit until the pulse has been measured and $\overline{\text{TGATE}}$ has been negated.

8.3.6 Period Measurement

This mode is used to count the period of a particular event. The event is defined by the assertion, negation, and subsequent reassertion of $\overline{\text{TGATE}}$. When $\overline{\text{TGATE}}$ is asserted, the counter begins counting down from $FFFF. The negation of $\overline{\text{TGATE}}$ has no effect on the counter. When $\overline{\text{TGATE}}$ is reasserted, the counter stops counting and holds the value at which it stopped. Further assertions and negations of $\overline{\text{TGATE}}$ have no effect on the counter. This mode can be selected by programming the CR MODEx bits to 101.

The timer is enabled by setting the SWR, CPE, and the TGE bits in the CR. The assertion of $\overline{\text{TGATE}}$ starts the counter. When the timer is enabled, the SR ON bit is set. On the next falling edge of the counter clock, the counter is loaded with the value of $FFFF. With each successive falling edge of the counter clock, the counter decrements. The PREL1 and PREL2 registers are not used in this mode.

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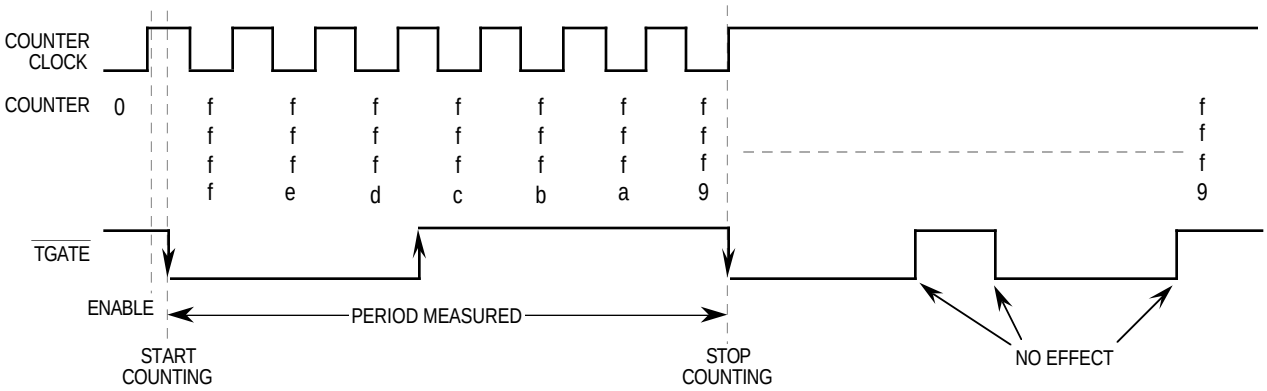
The first negation of $\overline{\text{TGATE}}$ is ignored, but on the second assertion of $\overline{\text{TGATE}}$, the SR TG bit is set, the SR ON bit is negated, and the prescaler and counter are disabled. Subsequent transitions on $\overline{\text{TGATE}}$ do not re-enable the counter. See Figure 8-9 for a depiction of this mode. The SR TGL bit reflects the level of $\overline{\text{TGATE}}$ at all times.



MODEx Bits in Control Register = 101
TGE Bit of Control Register = 1

Figure 8-9. Period Measurement Mode

If the counter counts down to the value stored in the COM register, the COM and TC bits in the SR are set. If the counter counts down to $0000, a time-out is detected. This sets the SR TO bit, and clears the SR COM bit. At time-out, the next falling edge of the counter clock reloads the counter with $FFFF. TOUT transitions at time-out or is disabled as programmed by the OCx bits of the CR, and the OUT bit in the SR reflects the level on TOUT.

To determine the number of cycles counted, the value in the CNTR must be read, inverted, and incremented by 1 (the first count is $FFFF which, in effect, includes a count of zero). The counter counts in a true 2^{16} fashion. For measuring pulses of even greater duration, the value in the POx bits in the SR are readable and can be thought of as an extension of the least significant bits in the CNTR.

NOTE

Once the timer has been enabled, do not clear the SR TG bit until the pulse has been measured and $\overline{\text{TGATE}}$ has been negated.

8.3.7 Event Count

This mode is used to count events by interpreting the falling edges of the counter clock as events (see Figure 8-10). These events may be external or internal to the chip—for example, counting the number of system clock cycles required to execute a sequence of instructions. As another example, by connecting $\overline{\text{AS}}$ to TIN, the number of bus cycles to complete a sequence of instructions could be counted. This mode can be selected by programming the CR MODEx bits to 110.

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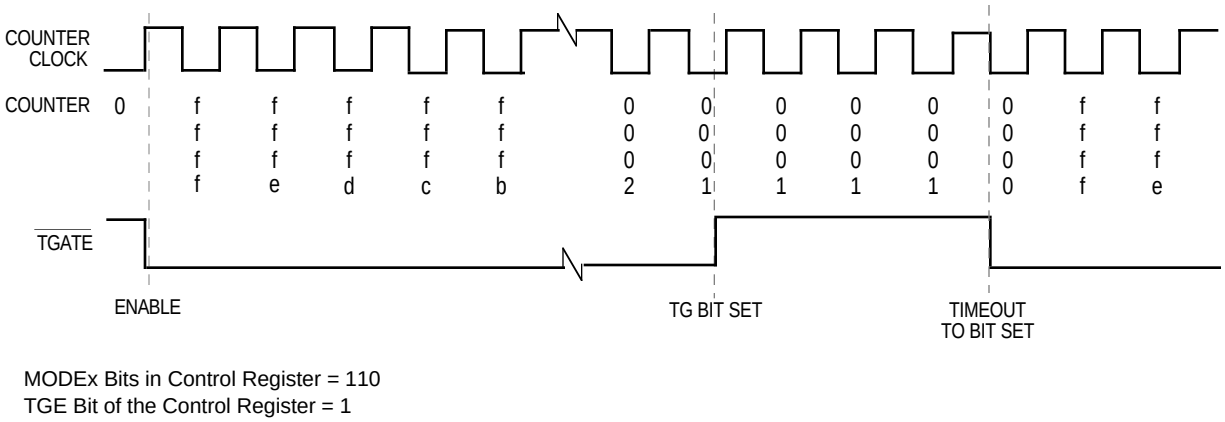

MODEx Bits in Control Register = 110
TGE Bit of the Control Register = 1

Figure 8-10. Event Count Mode

The timer is enabled by setting the SWR and CPE bits in the CR and, if $\overline{\text{TGATE}}$ is enabled (TGE bit of the CR is set), then asserting $\overline{\text{TGATE}}$. When the timer is enabled, the SR ON bit is set. On the next falling edge of the counter clock, the counter is loaded with the value of $FFFF. With each successive falling edge of the counter clock, the counter decrements. The PREL1 and PREL2 registers are not used in this mode.

If $\overline{\text{TGATE}}$ is not enabled (CR TGE bit is cleared), then $\overline{\text{TGATE}}$ does not start or stop the timer or affect the TG bit of the SR. In this case, the counter would begin counting on the falling edge of the counter clock immediately after the SWR and CPE bits in the CR are set.

If $\overline{\text{TGATE}}$ is enabled (CR TGE bit is set), then the assertion of $\overline{\text{TGATE}}$ starts the counter. The negation of $\overline{\text{TGATE}}$ disables the counter, sets the SR TG bit, and clears the ON bit in the SR. If $\overline{\text{TGATE}}$ is reasserted, the timer resumes counting from where it was stopped, and the ON bit is set again. Further assertions and negations of $\overline{\text{TGATE}}$ have the same effect. The TGL bit in the SR reflects the level of $\overline{\text{TGATE}}$ at all times.

If the counter counts down to the value stored in the COM register, the COM and TC bits in the SR are set. If the counter counts down to $0000, a time-out is detected. This event sets the TO in the SR and clears the COM bit. At time-out, the next falling edge of the counter clock reloads the counter with $FFFF. TOUT transitions at time-out or is disabled as programmed by the CR OC bits. The SR OUT bit reflects the level on TOUT.

To determine the number of cycles counted, the value in the CNTR must be read, inverted, and incremented by 1 (the first count is $FFFF which, in effect, includes a count of zero). The counter counts in a true 2^{16} fashion. For measuring pulses of even greater duration, the value in the POx bits in the SR are readable and can be thought of as an extension of the least significant bits in the CNTR.

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8.3.8 Timer Bypass

In this mode, the counter and prescaler cannot be enabled. However $\overline{\text{TGATE}}$ and TOUT can be used for I/O. This mode can be selected by programming the CR MODE bits to 111.

$\overline{\text{TGATE}}$ can be used as a simple input port when the CR is configured as follows:

CR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWR	IE2	IE1	IE0	TGE	PCLK	CPE	CLK	POT2	POT1	POT0	MODE2	MODE1	MODE0	OC1	OC0
$\overline{\text{TGATE}}$ AS A SIMPLE INPUT															
X	X	0	X	X	X	1	X	X	X	X	1	1	1	X	X

X-Don't care

When $\overline{\text{TGATE}}$ is asserted, the SR ON bit is set. When $\overline{\text{TGATE}}$ is negated, the ON bit is cleared. The value of the TGL bit in the SR reflects the level of $\overline{\text{TGATE}}$. $\overline{\text{TGATE}}$ can also be used as an input port that generates interrupts on a low-to-high transition of $\overline{\text{TGATE}}$ when the CR is configured as follows:

CR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWR	IE2	IE1	IE0	TGE	PCLK	CPE	CLK	POT2	POT1	POT0	MODE2	MODE1	MODE0	OC1	OC0
$\overline{\text{TGATE}}$ AS AN INPUT/INTERRUPT															
X	X	1	X	1	X	1	X	X	X	X	1	1	1	X	X

When $\overline{\text{TGATE}}$ is negated, the SR TG bit is set, and the programmed $\overline{\text{IRQ}}$x signal is asserted to the CPU32. The TG bit can only be cleared by writing a one to this bit position. The value of the SR TGL bit reflects the level of $\overline{\text{TGATE}}$.

Additionally, TOUT can be used as a simple output port when the CR is configured as follows:

CR

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWR	IE2	IE1	IE0	TGE	PCLK	CPE	CLK	POT2	POT1	POT0	MODE2	MODE1	MODE0	OC1	OC0
$\overline{\text{TGATE}}$ AS A SIMPLE OUTPUT															
0	X	X	X	X	X	1	X	X	X	X	1	1	1	OC1	OC0

SWR must be a zero to change the value of TOUT. Changing the value of the CR OCx bits determines the level of TOUT as shown in Table 8-1.

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Table 8-1. OCx Encoding

OC1	OC0	TOUT
0	0	Hi-Z
0	1	0
1	0	0
1	1	1

A read of the SR while in this mode always shows the TO, TC, and COM bits cleared, and the PO bits as $FF. The SR OUT bit always indicates the level on the TOUT pin.

8.3.9 Bus Operation

The following paragraphs describe the operation of the IMB during read, write, and interrupt acknowledge cycles to the timer.

8.3.9.1 READ CYCLES. The timer is accessed with no wait states. The timer responds to byte, word, and long-word reads, and 16 bits of valid data are returned. Read cycles from reserved registers return logic zero.

8.3.9.2 WRITE CYCLES. The timer is accessed with no wait states. The timer responds to byte, word, and long-word writes. Write cycles to read-only registers and bits as well as reserved registers complete in a normal manner without exception processing; however, the data is ignored.

8.3.9.3 INTERRUPT ACKNOWLEDGE CYCLES. The timer is capable of arbitrating for interrupt servicing and supplying the interrupt vector when it has successfully won arbitration. The vector number must be provided if interrupt servicing is necessary; thus, the interrupt register (IR) must be initialized. If the IR is not initialized, a spurious interrupt exception will be taken if interrupt servicing is necessary.

8.4 REGISTER DESCRIPTION

The following paragraphs contain a detailed description of each register and its specific function. The operation of the timer is controlled by writing control words into the appropriate registers. Timer registers and their associated addresses are listed in Figure 8-11. For more information about a particular register, refer to the individual register description. The ADDR column indicates the offset of the register from the base address of the timer. An FC column designation of S indicates that register access is restricted to supervisor only. A designation of S/U indicates that access is governed by the SUPV bit in the module configuration register (MCR).

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ADDR	FC	15 0
$600	S	MODULE CONFIGURATION REGISTER (MCR)
$602	S	RESERVED
$604	S	INTERRUPT REGISTER (IR)
$606	S/U	CONTROL REGISTER (CR)
$608	S/U	STATUS/PRESCALER REGISTER (SR)
$60A	S/U	COUNTER REGISTER (CNTR)
$60C	S/U	PRELOAD 1 REGISTER (PREL1)
$60E	S/U	PRELOAD 2 REGISTER (PREL2)
$610	S/U	COMPARE REGISTER (COM)
$612-$63F	S/U	RESERVED

Figure 8-11. Timer Module Programming Model

In the registers discussed in the following paragraphs, the numbers in the upper right-hand corner indicate the offset of the register from the base address specified by the module base address register (MBAR) in the SIM40. The numbers on the top line of the register represent the bit position in the register. The register contains the mnemonic for the bit. The value of these bits after a hardware reset is shown below the register. The access privilege is shown in the lower right-hand corner.

NOTE

A CPU32 RESET instruction will not affect the MCR, but will reset all other registers in the timer modules as though a hardware reset occurred.

8.4.1 Module Configuration Register (MCR)

The MCR controls the timer module configuration. This register can be either read or written when the module is enabled and is in the supervisor state. The MCR is not affected by a CPU32 RESET instruction.

MCR $600

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STP	FRZ1	FRZ0	0	0	0	0	0	SUPV	0	0	0	IARB3	IARB2	IARB1	IARB0
RESET:															
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

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STP—Stop bit

1 = Setting the STP bit stops all clocks within the timer module except for the clock from the IMB. The clock from the IMB remains active to allow the CPU32 access to the MCR. The clock stops on the low phase of the clock and remains stopped until the STP bit is cleared by the CPU32 or a hardware reset. Accesses to timer module registers while in stop mode produce a bus error. The timer module should be disabled in a known state prior to setting the STP bit; otherwise, unpredictable results may occur. The STP bit should be set prior to executing the LPSTOP instruction to reduce overall power consumption.

0 = The timer operates in normal mode.

FRZ1, FRZ0—Freeze

These bits determine the action taken when the FREEZE signal is asserted on the IMB, when the CPU32 has entered background debug mode. Table 8-2 lists the action taken for each bit combination.

Table 8-2. FRZx Control Bits

FRZ1	FRZ0	ACTION
0	0	Ignore FREEZE
0	1	Reserved (FREEZE ignored)
1	0	Execution Freeze
1	1	Execution Freeze

Bits 12–8, 6–4—Reserved

SUPV—Supervisor/User

The value of this bit has no effect on registers permanently defined as supervisor-only access.

1 = The timer registers defined as supervisor/user reside in supervisor data space and are only accessible from supervisor programs.

0 = The timer registers defined as supervisor/user reside in user data space and are accessible from either supervisor or user programs.

IARB3–IARB0—Interrupt Arbitration Bits

Each module that generates interrupts has an IARB field. These bits are used to arbitrate for the bus in the case that two or more modules simultaneously generate an interrupt at the same priority level. No two modules can share the same IARB value. The reset value of the IARB field is $0, which prevents this module from arbitrating during the interrupt acknowledge cycle. The system software should initialize the IARB field to a value from $F (highest priority) to $1 (lowest priority).

8.4.2 Interrupt Register (IR)

The IR contains the priority level for the timer interrupt request and the 8-bit vector number of the interrupt. The register can be read or written to at any time while in supervisor mode and while the timer module is enabled (i.e., the STP bit in the MCR is cleared).

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IR $604

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	IL2	IL1	IL0	IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

Supervisor Only

Bits 15–11—Reserved

IL2–IL0—Interrupt Level Bits

Each module that can generate interrupts has an interrupt level field. The priority level encoded in these bits is sent to the CPU32 on the appropriate $\overline{\text{IRQx}}$ signal. The CPU32 uses this value to determine servicing priority. See **Section 5 CPU32** for more information.

IV7–IV0—Interrupt Vector Bits

Each module that can generate interrupts has an interrupt vector (IV) field. This 8-bit number indicates the offset from the base of the vector table where the address of the exception handler for the specified interrupt is located. The IV field is reset to $0F, which indicates an uninitialized interrupt condition. See **Section 5 CPU32** for more information.

8.4.3 Control Register (CR)

The CR controls the operation of the timer. The register can always be read or written when the timer module is enabled (i.e., the STP bit in the MCR is cleared). Changing the contents of the CR should only be attempted when the timer is disabled (the SWR bit in the CR is cleared). Changing the CR while the timer is running may produce unpredictable results.

CR $606

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SWR	IE2	IE1	IE0	TGE	PCLK	CPE	CLK	POT2	POT1	POT0	MODE2	MODE1	MODE0	OC1	OC0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Supervisor/User

SWR—Software Reset

1 = Removes the software reset.

0 = A software reset is performed by first clearing this bit and then clearing the TO, TG, and TC bits in the SR. The prescaler is loaded with $FF, the counter is set to $0000, and the SR COM bit is cleared. When this bit is zero, the timer is disabled.

IE2–IE0—Interrupt Enable

These bits determine which sources of interrupts, TO, TG, and TC, are enabled to generate an interrupt request to the CPU32. Table 8-3 lists which interrupts are enabled for all bit combinations.

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Table 8-3. IEx Encoding

IE2	IE1	IE0	Enabled Interrupts
0	0	0	Polling Mode (No Interrupts Enabled)
0	0	1	TC Enabled
0	1	0	TG Enabled
0	1	1	TG and TC Enabled
1	0	0	TO Enabled
1	0	1	TO and TC Enabled
1	1	0	TO and TG Enabled
1	1	1	TO, TG, and TC Enabled

TGE—Timing Gate Enable

1 = The $\overline{\text{TGATE}}$ signal is enabled to control the enabling and disabling of the prescaler and counter, except in the input capture/output compare mode (see **8.3.1 Input Capture/Output Compare**).

0 = The $\overline{\text{TGATE}}$ signal has no effect on the timer operation.

PCLK—Prescaler Clock Select

This bit selects which clock is used for the counter clock.

1 = The counter is decremented by the prescaler output tap as selected by the POT field in the CR.

0 = The counter is decremented by the selected clock.

The prescaler continues to decrement regardless of how PCLK is set.

CPE—Counter Prescaler Enable

1 = The selected clock is enabled. If the TGE bit is set, then $\overline{\text{TGATE}}$ must also be asserted (except in the input capture/output compare mode).

0 = The selected clock is held high, halting the prescaler and counter.

CLK—Clock

1 = The selected clock is taken from the TIN input.

0 = The selected clock is one-half the system clock's frequency.

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POT2–POT0—Prescaler Output Tap

If PCLK is set, these bits encode which of the prescaler's output taps act as the counter clock. A division of the selected clock is applied to the counter as listed in Table 8-4.

Table 8-4. POT Encoding

POT2	POT1	POT0	Division of Selected Clock
0	0	1	Divide by 2
0	1	0	Divide by 4
0	1	1	Divide by 8
1	0	0	Divide by 16
1	0	1	Divide by 32
1	1	0	Divide by 64
1	1	1	Divide by 128
0	0	0	Divide by 256

MODE2–MODE0—Operation Mode

These bits select one of the eight modes of operation for the timer as listed in Table 8-5. Refer to **8.3 Operating Modes** for more information on the individual modes.

Table 8-5. MODEx Encoding

MODE2	MODE1	MODE0	OPERATION MODE
0	0	0	Input Capture/Output Compare
0	0	1	Square-Wave Generator
0	1	0	Variable Duty-Cycle Square-Wave Generator
0	1	1	Variable-Width Single-Shot Pulse Generator
1	0	0	Pulse-Width Measurement
1	0	1	Period Measurement
1	1	0	Event Count
1	1	1	Timer Bypass (Simple Test Mode)

OC1–OC0—Output Control

These bits select the conditions under which TOUT changes (see Table 8-6). These bits may have a different effect when in the input capture/output compare mode. Caution should be used when modifying the OC bits near timer events.

Table 8-6. OCx Encoding

OC1	OC0	TOUT MODE
0	0	Disabled
0	1	Toggle Mode
1	0	Zero Mode
1	1	One Mode

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Disabled—TOUT is disabled and three-stated.

Toggle Mode—If the timer is disabled (SWR = 0) when this encoding is programmed, TOUT is immediately set to zero. If the timer is enabled (SWR = 1), time-out events (counter reaches $0000) toggle TOUT. In the input capture/output compare mode, TOUT is immediately set to zero if the timer is disabled (SWR = 0). If the timer is enabled (SWR = 1), timer compare events toggle TOUT. (Timer compare events occur when the counter reaches the value stored in the COM.)

Zero Mode—If the timer is disabled (SWR = 0) when this encoding is programmed, TOUT is immediately set to zero. If the timer is enabled (SWR = 1), TOUT will be set to zero at the next time-out. In the input capture/output compare mode, TOUT is immediately set to zero if the timer is disabled (SWR = 0). If the timer is enabled (SWR = 1), TOUT will be set to zero at time-outs and set to one at timer compare events. If the COM is $0000, TOUT will be set to zero at the time-out/timer compare event.

One Mode—If the timer is disabled (SWR = 0) when this encoding is programmed, TOUT is immediately set to one. If the timer is enabled (SWR = 1), TOUT will be set to one at the next time-out. In the input capture/output compare mode, TOUT is immediately set to one if the timer is disabled (SWR = 0). If the timer is enabled (SWR = 1), TOUT will be set to one at timeouts and set to zero at timer compare events. If the COM is $0000, TOUT will be set to one at the time-out/timer compare event.

8.4.4 Status Register (SR)

The SR contains timer status information as well as the state of the prescaler. This register is updated on the rising edge of the system clock when a read of its location is not in progress, allowing the most current information to be contained in this register. The register can be read, and the TO, TG, and TC bits can be written when the timer module is enabled (i.e., the STP bit in the MCR is cleared).

SR $608

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQ	TO	TG	TC	TGL	ON	OUT	COM	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0
RESET ($\overline{\text{TGATE}}$ NEGATED):															
0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1
RESET ($\overline{\text{TGATE}}$ ASSERTED):															
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Supervisor/User

IRQ—Interrupt Request bit

The positioning of this bit in the most significant location in this register allows it be conditionally tested as if it were a signed binary integer.

1 = An interrupt condition has occurred. This bit is the logical OR of the enabled TO, TG, and TC interrupt bits.

0 = The bit(s) that caused the interrupt condition has been cleared. If an $\overline{\text{IRQx}}$ signal has been asserted, it is negated when this bit is cleared.

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TO—Time-out Interrupt

1 = The counter has transitioned from $0001 to $0000, and the counter has rolled over. This bit does not affect the programmed $\overline{\text{IRQx}}$ signal if the IE2 bit in the CR is cleared.

0 = This bit is cleared by the timer whenever the $\overline{\text{RESET}}$ signal is asserted on the IMB, regardless of the mode of operation. This bit may also be cleared by writing a one to it. Writing a zero to this bit does not alter its contents. This bit is not affected by disabling the timer (SWR = 0).

TG—Timer Gate Interrupt

1 = This bit is set whenever the CR TGE bit is set and the $\overline{\text{TGATE}}$ signal transitions in the manner to which the particular mode of operation responds. Refer to **8.3 Operating Modes** for more details. This bit does not affect the programmed $\overline{\text{IRQx}}$ signal if the IE1 bit in the CR is cleared.

0 = This bit is cleared by the timer whenever the $\overline{\text{RESET}}$ signal is asserted on the IMB, regardless of the mode of operation. This bit may also be cleared by writing a one to it. Writing a zero to this bit does not alter its contents. This bit is not affected by disabling the timer (SWR = 0).

TC—Timer Compare Interrupt

1 = This bit is set when the counter transitions (off a clock/event falling edge) to the value in the COM. This bit does not affect the programmed $\overline{\text{IRQx}}$ signal if the IE0 bit in the CR is cleared.

0 = This bit is cleared by the timer whenever the $\overline{\text{RESET}}$ signal is asserted on the IMB, regardless of the mode of operation. This bit may also be cleared by writing a one to it. Writing a zero to this bit does not alter its contents. This bit is not affected by disabling the timer (SWR = 0).

TGL—$\overline{\text{TGATE}}$ Level

1 = The $\overline{\text{TGATE}}$ signal is negated.

0 = The $\overline{\text{TGATE}}$ signal is asserted.

ON—Counter Enabled

1 = This bit is set whenever the SWR and CPE bits are set in the CR. If the CR TGE bit is set, $\overline{\text{TGATE}}$ must also be asserted (except in the input capture/output compare mode) since this signal then controls the enabling and disabling of the counter. If all these conditions are met, the counter is enabled and begins counting down.

0 = The counter is not enabled and does not begin counting down.

OUT—Output Level

1 = TOUT is a logic one.

0 = TOUT is a logic zero, or the pin is three-stated.

COM—Compare Bit

This bit is used to indicate when the counter output value is at or between the value in the COM and $0000 (time-out).

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1 = This bit is set when the counter output equals the value in the COM.

0 = This bit is cleared when a time-out occurs, the COM register is accessed (read or write), the timer is reset with the SWR bit, or the $\overline{\text{RESET}}$ signal is asserted on the IMB. This bit is cleared regardless of the state of the TC bit.

This bit can be used to indicate when a write to the PREL1 or PREL2 registers will not cause a problem during a counter reload at time-out. To ensure that the write to the PREL register is recognized at time-out, the latency between the read of the COM bit and the write to the PREL register must be considered.

PO7–PO0—Prescaler Output

These bits show the levels on each of the eight output taps of the prescaler. These values are updated every time that the system clock goes high and a read cycle of this byte in the SR is not in progress.

8.4.5 Counter Register (CNTR)

The CNTR reflects the value of the counter. This value can be reliably read at any time since it is updated on every rising edge of the system clock (except in the input capture/output compare mode) when a read of the register is not in progress. This read-only register can be read when the timer module is enabled (i.e., the STP bit in the MCR is cleared).

CNTR $60A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Supervisor/User

All 24 bits of the prescaler and the counter may be obtained by one long-word read at the address of the SR, since the CNTR is contiguous to it. Any changes in the prescaler value due to the two cycles necessary to perform a long-word read should be considered. If this latency presents a problem, the $\overline{\text{TGATE}}$ signal may be used to disable the decrement function while the reads are occurring.

8.4.6 Preload 1 Register (PREL1)

The PREL1 stores a value that is loaded into the counter in some modes of operation. This value is loaded into the counter on the first falling edge of the counter clock after the counter is enabled. This register can be read and written when the timer module is enabled (i.e., the STP bit in the MCR is cleared). However, a write to this register must be completed before time-out for the new value to be reliably loaded into the counter.

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PREL1 $60C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PR1-15	PR1-14	PR1-13	PR1-12	PR1-11	PR1-10	PR1-9	PR1-8	PR1-7	PR1-6	PR1-5	PR1-4	PR1-3	PR1-2	PR1-1	PR1-0
RESET:															
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Supervisor/User

For some modes of operation, this register is also used to reload the counter one falling clock edge after a time-out occurs. Refer to **8.3 Operating Modes** for more information on the individual modes.

8.4.7 Preload 2 Register (PREL2)

PREL2 is used in addition to PREL1 in the variable duty-cycle square-wave generator and variable-width single-shot pulse generator modes. When in either of these modes, the value in PREL1 is loaded into the counter on the first falling edge of the counter clock after the counter is enabled. After time-out, the value in PREL2 is loaded into the counter. This register can be read and written when the timer module is enabled (i.e., the STP bit in the MCR is cleared). However, a write to this register must be completed before time-out for the new value to be reliably loaded into the counter.

PREL2 $60E

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PR2-15	PR2-14	PR2-13	PR2-12	PR2-11	PR2-10	PR2-9	PR2-8	PR2-7	PR2-6	PR2-5	PR2-4	PR2-3	PR2-2	PR2-1	PR2-0
RESET:															
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Supervisor/User

8.4.8 Compare Register (COM)

The COM can be used in any mode. When the 16-bit counter reaches the value in the COM, the TC and COM bits in the SR are set. In the input capture/output compare mode, a compare event can be programmed to set, clear, or toggle TOUT. The register can be read and written when the timer module is enabled (i.e., the STP bit in the MCR is cleared).

COM $610

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COM15	COM14	COM13	COM12	COM11	COM10	COM9	COM8	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Supervisor/User

The COM can be used to produce an interrupt when the SR TC bit has been enabled to produce an interrupt and the counter counts down to a preselected value. The COM can also be used to indicate that the timer is approaching time-out.

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Caution must be exercised when accessing the COM. If it were to be accessed simultaneously by the compare logic and by a write, the old compare value may get compared to the counter value.

8.5 TIMER MODULE INITIALIZATION SEQUENCE

The following paragraphs discuss a suggested method for initializing the timer module.

8.5.1 Timer Module Configuration

If the timer capability of the MC68341 is being used, the following steps should be followed to initialize a timer module properly.

Control Register (CR)

- Clear the SWR bit to disable the timer.

Status Register (SR)

- Clear the TO, TG, and TG bits to reset the interrupts.

Module Configuration Register (MCR)

- Initialize the STP for normal operation.
- Select whether to respond to or ignore FREEZE (FRZx bits).
- Select the access privilege for the supervisor/user registers (SUPV bit).
- Select the interrupt arbitration level for the timer module (IARBx bits).

Interrupt Register (IR)

- Program the interrupt priority level for the timer interrupts (ILx bits).
- Program the interrupt vector number for the timer interrupts (IVx bits).

Preload Registers (PREL1 and PREL2)

- If required, initialize the preload registers for mode of operation.

Compare Register (COM)

- If desired, initialize the compare register.

The following steps begin operation:

Control Register (CR)

- Set the SWR bit to enable the timer.
- Enable the desired interrupts (IEx bits).
- Enable $\overline{\text{TGATE}}$ if required for mode of operation (TGE bit).
- Select the prescaler clock (PCLK bit).
- Enable the counter prescaler (CPE bit).
- Select the selected clock (CLK bit).

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- If the PCLK bit is set, select the POTx bits.
- Select the mode of operation (MODEx bits).
- Select the operation of TOUT (OCx bits).

8.5.2 Timer Module Example Configuration Code

The following code is an example of a configuration sequence for the timer module.

```
*****************************************************************************
* MC68341 basic timer module register initialization example code.
* This code is used to initialize the 68341's internal timer module
* registers, providing basic functions for operation.
* It sets up timer for square wave generation.
*****************************************************************************
*****************************************************************************
* equates
*****************************************************************************
MBAR        EQU   $0003FF00   Address of SIM40 Module Base Address Reg.
MODBASE     EQU   $FFFFF000   SIM40 MBAR address value
*****************************************************************************
* Timer module equates
TIMER       EQU   $600        Offset from MBAR for timer module regs
MCR         EQU   $0          MCR for timer

* Timer register offsets from timer base address
IR          EQU   $604        interrupt register timer
CR          EQU   $606        control register timer
SR          EQU   $608        status register timer
CNTR        EQU   $60A        counter register timer
PRLD1       EQU   $60C        preload register 1 timer
COM         EQU   $610        compare register timer


*****************************************************************************
*****************************************************************************
* Initialize Timer
*****************************************************************************
        LEA         MODBASE+TIMER,A0      Pointer to timer module

* Disable timer
        CLR.W       CR(A0)

* Clear the TO, TG, and TC bits
        CLR.W       SR(A0)

* Module configuration register:
* Timer module is set for normal operation, ignore FREEZE.
```


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```
* Supervisor/user timer registers unrestricted.
* Interrupt arbitration at priority $03.
        MOVE.W      #$0003,MCR(A0)

* Initialize timer interrupt level to 2 and vector to $0F
        MOVE.W      #$020F,IR(A0)

* Initialize preload 1 to 3
        MOVE.W      #$0003,PRLD1(A0)


* Initialize the compare register to 0
        CLR.W       COM(A0)

* Control register:
* Enable timer, no interrupts are enabled, TGATE signal has no effect.
* Use the selected clock for the counter clock, and enable it.
* Selected clock is 1/2 system's freq. Square-wave generation, toggle TOUT.
        MOVE.W      #$8205,CR(A0)
*****************************************************************************
        END
*****************************************************************************


*****************************************************************************
* MC68341 basic timer module register initialization example code.
* This code is used to initialize the 68341's internal timer module
* registers, providing basic functions for operation.
* It sets up timer for pulse-width measurement. In this mode, the number
* of clock cycles during a particular event are counted. The event is
* defined by the assertion and negation of TGATE.
*****************************************************************************
*****************************************************************************
* equates
*****************************************************************************
MBAR        EQU   $0003FF00   Address of SIM40 Module Base Address Reg.
MODBASE     EQU   $FFFFF000   SIM40 MBAR address value

*****************************************************************************
* Timer module equates
TIMER       EQU   $600        Offset from MBAR for timer module regs
MCR         EQU   $0          MCR for timer
```


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```
* Timer register offsets from timer base address
IR          EQU   $604        interrupt register timer
CR          EQU   $606        control register timer
SR          EQU   $608        status register timer
CNTR        EQU   $60A        counter register timer
COM         EQU   $610        compare register timer


*************************************************************************
*************************************************************************
* Initialize Timer
*************************************************************************
        LEA    MODBASE+TIMER,A0      Pointer to timer module

* Disable timer
        CLR.W        CR(A0)

* Allow TGATE to negate and assert so that an accurate count will result.
* If SR TGL bit=1, continue looping. TGATE is negated.
        LOOP1        BTST.B       #$3,SR(A0)
        BNE.B        LOOP1
* If TGL bit=0, continue looping. TGATE is asserted.
        LOOP2        BTST.B       #$3,SR(A0)
        BEQ.B        LOOP2

* Ready to initialize timer, TGATE is negated.

* Module configuration register:
* Timer module is set for normal operation, ignore FREEZE.
* Supervisor/user timer registers unrestricted.
* Interrupt arbitration at priority $03.
        MOVE.W      #$0003,MCR(A0)

* Initialize timer interrupt level to 2 and vector to $0F
        MOVE.W      #$020F,IR(A0)

* Initialize the compare register to 0
        CLR.W        COM(A0)

* Clear the SR TG bit (by writing a 1) to use as a flag
        MOVE.B      #$20,SR(A0)

* Control register:
* Enable timer, no interrupts are enabled, TGATE signal used to control
* the counter. Use the selected clock for the counter clock, and enable it.
* Selected clock is 1/2 system's freq. Pulse-width measurement,
* disable TOUT.
```


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```
        MOVE.W      #$8A10,CR(A0)

* If SR TG bit=0, continue looping TGATE is asserted,
* else TG=1 indicating TGATE was negated. When TG=1, counting is stopped.
 LOOP3              BTST.B      #$5,SR(A0)
        BEQ.B       LOOP3

* Counting is complete. To determine the number of cycles counted, the value
* in CNTR must be read, inverted, and incremented by 1.
        MOVE.W      CNTR(A0),D0
        NOT.W       D0
        ADDQ.W      #$1,DO
* D0 contains the number of cycles counted.
*****************************************************************************
        END
*****************************************************************************
```

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SECTION 9
QUEUED SERIAL PERIPHERAL MODULE

The queued serial peripheral module (QSPM) provides a queued serial peripheral interface (QSPI). The QSPI is a full-duplex, synchronous serial interface for communicating with peripherals or microprocessors. It is enhanced by the addition of a queue for receive and transmit data. This section provides a block diagram, memory map, pin description, and register descriptions of the QSPM, with a breakdown of the QSPI submodule. Operation of the QSPI submodule includes master mode and slave mode. For a detailed description refer to **9.5.5.1 Master Mode** and **9.5.5.2 Slave Mode**. To aid in understanding the numerous bits and fields of the registers that appear throughout the text, a quick reference guide identifies all bit/field acronyms. (Refer to Table 9-3.).

The MC68341 physically integrates the entire MC68332 queued serial module (QSM) on-chip. However, due to the availability of two full-featured serial channels in the serial module, the QSM's serial communications interface (SCI) signals are not brought out. Register bits corresponding to the SCI logic are shown as undefined/reserved for the MC68341 and should not be changed from their default reset state.

9.1 BLOCK DIAGRAM

Figure 9-1 depicts the major components of the QSPM, which consist of the global registers, logic control, and the QSPI submodule. Refer to **9.5 QSPI Submodule** for further definition of these components.

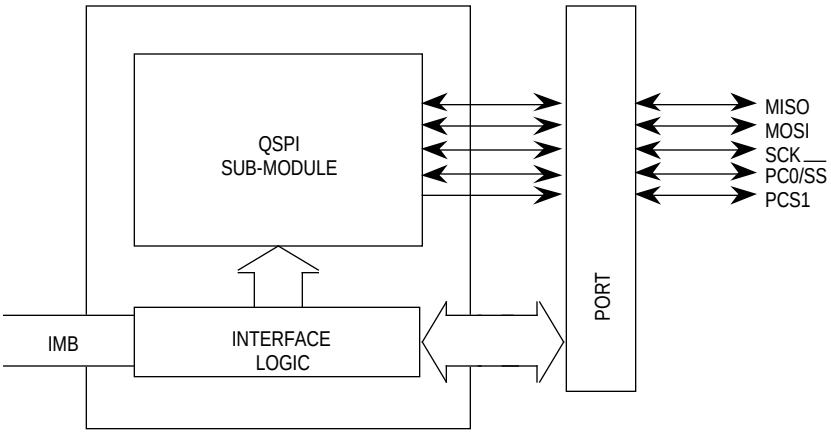

Figure 9-1. QSPM Block Diagram

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9.2 MEMORY MAP

The QSPM memory map is comprised of the global registers, the QSPI control and status registers, and the QSPI RAM as shown in Figure 9-2. For an accurate location of the QSPM in the MC68341 memory map, refer to **Figure 4-1 SIM41 Module Register Block.** The QSPM memory map may be divided into two segments: supervisor-only data space and assignable data space.

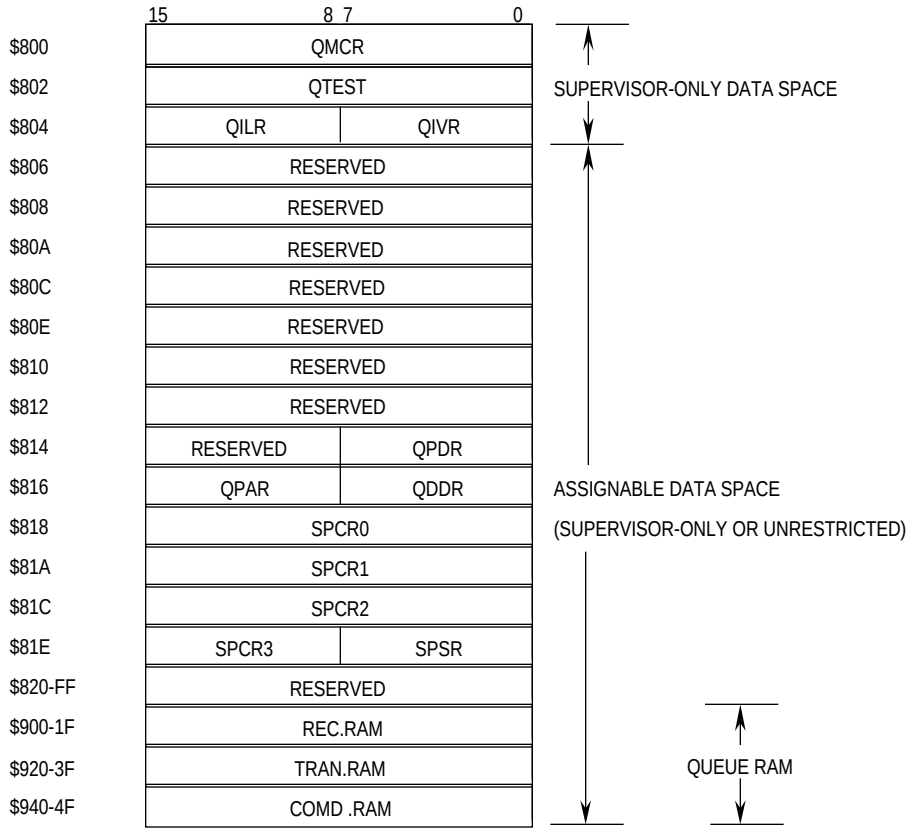

Figure 9-2. QSPM Memory Map

The supervisor-only data space segment contains the QSPM global registers. These registers define parameters needed by the QSPM to integrate with the CPU. Access to these registers is permitted only when the CPU is operating in supervisor mode.

Assignable data space can be either restricted to supervisor-only access or unrestricted to both supervisor and user accesses. The supervisor (SUPV) bit in the QSPM module configuration register (QMCR) designates the assignable data space as either supervisor or unrestricted. If SUPV is set, then the space is designated as supervisor-only space. Access is then permitted only when the CPU is operating in supervisor mode. All attempts to read supervisor data spaces when not in supervisor mode (CPU status register, S bit = 0) return a value of zero, and all attempts to write have no effect. If SUPV is clear, both user and supervisor accesses are permitted. To clear SUPV in the QMCR, the CPU must be in supervisor mode (CPU status register, S-bit = 1).

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The QSPM assignable data space segment contains the QSPI, control/status registers, and the QSPI RAM. All registers and RAM may be accessed on byte, word, and long-word boundaries. The 80 bytes of static RAM are distinct from the QSPM register set. All bytes not used by the QSPI may be used as general-purpose RAM. When operating, the QSPI submodule uses three noncontiguous blocks of the 80-byte RAM for receive, transmit, and control data. More information on the QSPI RAM can be found in **9.5.4.6 QSPI RAM.**

The contents of most locations in the memory map may be rewritten with the identical value to that location, with one exception. (Refer to **9.5.4.3 QSPI Control Register 2 (SPCR2)**.) Writing a different value to certain control registers when a submodule using that register is enabled can cause unpredictable results. For predictable operation, if register bits are to be changed, the CPU should disable the submodule in an orderly fashion before altering the registers.

9.3 QSPM PINS

The QSPM has five external pins as shown in Figure 9-1. These pins, if not in use for their submodule function, can be used as general-purpose I/O port pins.

Table 9-1 summarizes the QSPM pin functions, which are determined by the QSPI mode of operation (master or slave), the pin assignment register (QPAR), and by the appropriate QSPM data direction register (QDDR) bit.

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Table 9-1. QSPM Pin Summary

	Pin	Mode	QDDR Bit	Pin Function
QSPI Pins	MISO	Master	0	Serial Data Input to QSPI
			1	Output Value from QPDR
		Slave	0	Input Value to QPDR
			1	Serial Data Output from QSPI
	MOSI	Master	0	Input Value to QPDR
			1	Serial Data Output from QSPI
		Slave	0	Serial Data Input to QSPI
			1	Output Value from QPDR
	SCK	Master	0	Input Value to QPDR
			1	Clock Output from QSPI
		Slave	0	Clock Input to QSPI
			1	Output Value from QPDR
	PCS0/$\overline{SS}$	Master	0	Input (May Cause Mode Fault)
			1	Output Selects Peripherals
		Slave	0	Input Selects the QSPI
			1	Output Value from QPDR
	PCS1	Master	0	Input Value to QPDR
			1	Output Selects Peripherals
		Slave	0	Input Value to QPDR
			1	Output Value from QPDR

X = QDDR bit ignored.

The QSPM pin control registers—QDDR, QSPM pin assignment register (QPAR), and QSPM port data register (QPDR)—affect pins being used as general-purpose I/O pins. The QSPI control register 0 (SPCR0) has one bit that affects pins employed as general-purpose output pins. Within this register the wired-OR mode (WOMQ) control bit determines whether MISO, MOSI, SCK, PCS1, and PCS0 function as open-drain output pins or as normal output pins, regardless of their use as general-purpose I/O pins or as QSPI output pins.

9.4 REGISTERS

Registers of the QSPM are divided into three categories: QSPM global registers, QSPM pin control registers, and QSPI submodule registers. The QSPI registers are defined in **9.5 QSPI Submodule**. Writes to unimplemented bits have no meaning or effect, and reads from unimplemented bits always return a logic zero value.

In the registers discussed in the following pages, the numbers in the upper right-hand corner indicate the offset of the register from the base address specified in the module base address register (MBAR) in the SIM41. The numbers above the register description

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represent the bit position in the register. The register description contains the mnemonic for the bit. The values shown below the register description are the values of those register bits after a hardware reset. A value of U indicates that the bit value is unaffected by reset.

Table 9-2 is a summary of the registers, bits, and reset states for the full QSPM module.

As previously mentioned, Table 9-3 is a quick reference guide to all the bits/fields of the QSPM module. Along with the function, the register and register location of each bit/field are identified.

Table 9-2. QSPM Register Summary

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
QMCR $800	STOP	FRZ1	FRZ0	0	0	0	0	0	SUPV	0	0	0	IARB			
RESET:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
QTEST $802	0	0	0	0	0	0	0	0	0	0	0	0	TSBD	RSVD	TQSM	RSVD
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
QILR-QIVR $804	0	0	ILQSPI			RESERVED			INTV							
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
$806 – $812	Reserved															
QPDR $814	0	0	0	0	0	0	0	0	RSVD			D4 (PCS1)	D3 (PCS0*)	D2 (SCK)	D1 (MOSI)	D0 (MISO)
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
QPAR-QDDR $816	0	RSVD	RSVD	PCS1	PCS0*	0	MOSI	MISO	RSVD			PCS1	PCS0*	SCK	MOSI	MISO
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SPCRO $818	MSTR	WOMQ	BITS				CPOL	CPHA	SPBR							
RESET:	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0
SPCR1 $81A	SPE	DSCKL							DTL							
RESET:	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0
SPCR2 $81C	SPIFIE	WREN	WRTO	0	ENDQP				0	0	0	0	NEWQP			
RESET:	0	0	0		0	0	0	0	0	0	0	0	0	0	0	0
SPCR3-SPSR $81E	0	0	0	0	0	LOOPQ	HMIE	HALT	SPIF	MODF	HALTA	0	CPTQP			
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
$820- $8FF	Reserved															
REC.RAM $900- $91F	QSPI Receive Data (16 Words)															
TRAN.RAM $920- $93F	QSPI Transmit Data (16 Words)															
COMD.RAM $940- $94F	CONT	BITSE	DT	DSCK	RSVD	RSVD	PCS1	PCS0*	CONT	BITSE	DT	DSCK	RSVD	RSVD	PCS1	PCS0*

* The PCS0 bit listed above represents the dual-function PCS0/$\overline{SS}$.

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Table 9-3. Bit/Field Quick Reference Guide (Sheet 1 of 2)

Bit/Field Mnemonic	Function	Register	Register Location
SPBR	Serial Clock Baud Rate	SPCR0	QSPI
BITS	Bits Per Transfer	SPCR0	QSPI
BITSE	Bits Per Transfer Enable	QSPI RAM	QSPI
CONT	Continue	QSPI RAM	QSPI
CPHA	Clock Phase	SPCR0	QSPI
CPOL	Clock Polarity	SPCR0	QSPI
CPTQP	Completed Queue Pointer	SPSR	QSPI
DSCK	Peripheral Select Chip (PSC) to Serial Clock (SCK) Delay	QSPI RAM	QSPI
DSCKL	Delay before Serial Clock (SCK)	SPCR1	QSPI
DT	Delay after Transfer	QSPI RAM	QSPI
DTL	Length of Delay after Transfer	SPCR1	QSPI
ENDQP	Ending Queue Pointer	SPCR2	QSPI
FRZ1–FRZ0	Freeze1-0	QMCR	QSPM
HALT	Halt	SPCR3	QSPI
HALTA	Halt Acknowledge Flag	SPSR	QSPI
HMIE	Halt Acknowledge Flag (HALTA) and Mode Fault Flag (MODF) Interrupt Enable	SPCR3	QSPI
IARB	Interrupt Arbitration Identification Number	QMCR	QSPM
ILQSPI	Interrupt Level for QSPI	QILR	QSPM
INTV	Interrupt Vector	QIVR	QSPM
LOOPQ	QSPI Loop Mode	SPCR3	QSPI
MISO	Master in Slave Out	QPAR/QDDR/QPDR	QSPM
MODF	Mode Fault Flag	SPSR	QSPI
MOSI	Master Out Slave In	QPAR/QDDR/QPDR	QSPM
MSTR	Master/Slave Mode Select	SPCR0	QSPI
NEWQP	New Queue Pointer Value	SPCR2	QSPI
PCS0/$\overline{SS}$	Peripheral Chip Select/Slave Select	QPAR/QDDR/QPDR	QSPM
PCS1	Peripheral Chip Select	QPAR/QDDR/QPDR	QSPM
SCK	Serial Clock	QDDR/QPDR	QSPM
SPE	QSPI Enable	SPCR1	QSPI
SPIF	QSPI Finished Flag	SPSR	QSPI
SPIFIE	SPI Finished Interrupt Enable	SPCR2	QSPI
STOP	Stop	QMCR	QSPM

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Table 9-3. Bit/Field Quick Reference Guide (Sheet 2 of 2)

Bit/Field Mnemonic	Function	Register	Register Location
SUPV	Supervisor/Unrestricted	QMCR	QSPM
TQSM	Test QSPM Enable	QTEST	QSPM
TSBD	SPI Test Scan Path Select	QTEST	QSPM
WOMQ	Wired-OR Mode for QSPI Pins	SPCR0	QSPI
WREN	Wrap Enable	SPCR2	QSPI
WRTO	Wrap To Select	SPCR2	QSPI

9.4.1 Overall QSPM Configuration Summary

After reset, the QSPM remains in an idle state, requiring initialization of several registers before any serial operations may begin execution. The following registers, fields, and bits are fully described later in this section. A general sequence guide for initialization follows:

- QMCR (refer to **9.4.2.1 QSPM Configuration Register (QMCR)**)

*********em dash under a bullet????

This register must be initialized to properly configure:

—Interrupt arbitration identification number used by the entire QSPM module

—Supervisor/unrestricted bit (SUPV)

—FREEZE and/or STOP configuration should remain cleared to zero for normal operation.

- QIVR and QILR (refer to **9.4.2.3 QSPM Interrupt Level Register (QILR)** and **9.4.2.4 QSPM Interrupt Vector Register (QIVR)**)

These registers are written to choose the base vector number for the QSPM module and interrupt level for the QSPI submodule.

- QPDR and QDDR (refer **9.4.3.1 QSPM Port Data Register (QPDR)** and **9.4.3.3 QSPM Data Direction Register (QDDR)**)

The pin control registers should be initialized in the order QPDR and then QDDR, thus establishing the default state and direction of the QSPM pins.

For configuration of the QSPI submodule, initialize as follows:

- RAM (refer to **9.5.4.6 QSPI RAM**)
- QPAR (refer **9.4.3.2 QSPM Pin Assignment Register (QPAR)**)

Assignment of appropriate pins to the QSPI must be made with this register.

- SPCR0 (refer **9.5.4.1 QSPI Control Register 0 (SPCR0)**)

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The system designer must choose a transfer rate (baud) for operation in master mode, an appropriate clock phase, clock polarity, and the number of bits to be transferred in a serial operation. Master/slave mode select (MSTR) must be set to configure the QSPI for master mode or cleared to configure operation in slave mode. WOMQ should be set to enable or cleared to disable wired-OR mode operation.

- SPCR1 (refer to **9.5.4.2 QSPI Control Register (SPCR1)**)
  - —SPE must be set to enable the QSPI; this register should be written last.
  - —DTL allows the user to program a delay after any serial transfer, which is invoked by the DT bit for any serial transfer.
  - —DSCKL allows the user to set a delay before SCK (after PCS valid), which is invoked by the DSCK bit for any transfer.
- SPCR2 (refer to **9.5.4.3 QSPI Control Register 2 (SPCR2)**)
  - —NEWQP and ENDQP, respectively, determine the beginning of a queue and the number of serial transfers (up to 16) to be considered a complete queue.
  - —WREN is set to enable queue wraparound, and WRTO helps determine the address used in wraparound mode.
  - —SPIFIE is set to enable interrupts when SPIF is asserted.
- SPCR3 (refer to **9.5.4.4 QSPI Control Register 3 (SPCR3)**)

  HALT may be used for program debug, and HMIE is set to enable CPU interrupts when HALTA or MODF is asserted; LOOPQ is set only to enable a feedback loop that can be used for self-test mode.

9.4.2 QSPM Global Registers

The QSPM global registers contain system parameters used by the QSPM to interface with the CPU and other system modules. The four global registers are listed in Table 9-4.

Table 9-4. QSPM Global Registers

Address	Name	Usage
$800	QMCR	QSPM Configuration Register
$802	QTEST	QSPM Test Register
$804	QILR	QSPM Interrupt Level Register
$805	QIVR	QSPM Interrupt Vector Register

9.4.2.1 QSPM CONFIGURATION REGISTER (QMCR). QMCR contains parameters for interfacing to the CPU and the intermodule bus (IMB). This register can be modified only when the CPU is in supervisor mode.

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QMCR $800

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STOP	FRZ1	FRZ0	0	0	0	0	0	SUPV	0	0	0	IARB			
RESET:															
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

STOP—Stop Enable

1 = QSPM clock operation stopped
0 = Normal QSPM clock operation

STOP places the QSPM into a low power state by disabling the system clock in most parts of the module. QMCR is the only register guaranteed to be readable while STOP is asserted. The QSPI RAM is not readable; however, writes to RAM or any register are guaranteed valid while STOP is asserted. STOP may be negated by the CPU and by reset.

The system software must stop each submodule before asserting STOP to avoid complications at restart and to avoid data corruption. The QSPI submodule should be stopped by asserting the HALT bit in SPCR3 and by asserting STOP after the HALTA flag is set.

FRZ1—Freeze1

1 = Halt the QSPM (on a transfer boundary)
0 = Ignore the FREEZE signal on the IMB

FRZ1 determines what action is taken by the QSPM when the FREEZE signal of the IMB is asserted. FREEZE is asserted whenever the CPU enters the background mode.

NOTE

Ignoring the FREEZE signal can cause unpredictable results in the background mode operation of the QSPM, because the CPU is unable to service interrupt requests in this mode. If FRZ1 equals one when the FREEZE line is asserted, the QSPM comes to an orderly halt on a transfer boundary as if HALT had been asserted. The output pins continue to drive their last state. Once the FREEZE signal is negated, the QSPM module restarts automatically.

FRZ0—Freeze0

Reserved for future enhancement.

Bits 12–8—Not Implemented

SUPV—Supervisor/Unrestricted

1 = Supervisor access

All registers in the QSPM are placed in supervisor-only space. For any access from within user mode, address acknowledge (AACK) is not returned and the bus cycle is transferred externally.

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0 = User access

Because the QSPM contains a mix of supervisor and user registers, AACK returns for accesses with either supervisor or user mode, and the bus cycle remains internal. If a supervisor-only register is accessed in user mode, the module responds as if an access had been made to an unimplemented register location.

SUPV defines the assignable QSPM registers as either supervisor-only data space or unrestricted data space.

Bits 6–4—Not Implemented

IARB—Interrupt Arbitration Identification Number

Each module that generates interrupts, including the QSPM, must have an IARB field. The value in this field is used to arbitrate for the IMB when two or more modules generate simultaneous interrupts of the same priority level. No two modules can share the same IARB value. The reset value of the IARB field is $0, which prevents the QSPM from arbitrating during an interrupt acknowledge cycle (IACK). The IARB field should be initialized by system software to a value between $F (top priority) and $1 (lowest priority). Otherwise, any interrupts generated are identified by the CPU as spurious.

9.4.2.2 QSPM TEST REGISTER (QTEST). QTEST is used in testing the QSPM. Accesses to QTEST must be made while the MC68341 is in test mode.

QTEST $802

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TSBD	RSVD	TQSM	RSVD
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TSBD—SPI Test Scan Path Select

1 = Enable delay to SCK scan path
0 = Enable SPI baud clock scan path

RSVD—Reserved

TQSM—QSPM Test Enable

1 = Enable QSPM to send test scan paths
0 = Disable scan path

9.4.2.3 QSPM INTERRUPT LEVEL REGISTER (QILR). The QILR determines the priority level of interrupts requested by the QSPM and the vector used when acknowledging an interrupt. This register may be accessed only when the CPU is in supervisor mode.

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QILR $804

15	14	13	12	11	10	9	8	0
0	0	ILQSPI			RSVD			XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
RESET:								
0	0	0	0	0	0	0	0	

ILQSPI—Interrupt Level for QSPI

ILQSPI determines the priority level of all QSPI interrupts. This field should be programmed to a value between $0 (interrupts disabled) to $7 (highest priority).

9.4.2.4 QSPM INTERRUPT VECTOR REGISTER (QIVR). At reset, QIVR is initialized to $0F, which corresponds to the uninitialized interrupt vector in the exception table. This vector is selected until QIVR is written. QIVR should be programmed to one of the user-defined vectors ($40-$FF) during initialization of the QSPM.

After initialization, QIVR determines which vector in the exception vector table is to be used for QSPM interrupts. The value of INTV0 used during an IACK cycle is supplied by the bus interface unit (BIU). During an IACK, INTV7–INTV1 are driven on the DATA7–DATA1 IMB lines. The BIU drives DATA0 with a one for a QSPI interrupt. Writes to INTV0 have no meaning or effect. Reads of INTV0 return a value of one.

QIVR $805

15	7	6	5	4	3	2	1	0
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	INTV							
RESET:								
	0	0	0	0	1	1	1	1

9.4.3 QSPM Pin Control Registers

Table 9-5 identifies the three pin control registers of the QSPM. The QSPM determines the use of five pins, which form a parallel port. Although these pins are used by the serial subsystems, any pin may alternately be assigned as general-purpose I/O on a pin-by-pin basis. For use of these pins as general-purpose I/O, they must not be assigned to the QSPI submodule in register QPAR. To avoid briefly driving incorrect data, the first byte to be output should be written before register QDDR is configured for any output pins. QDDR should then be written to determine the direction of data flow on the pins and to output the value contained in register QPDR for all pins defined as outputs. Subsequent data for output is then written to QPDR.

Table 9-5. QSPM Pin Control Registers

Address	Name	Usage
$815	QPDR	QSPM Port Data Register
$816	QPAR	QSPM Pin Assignment Register
$817	QDDR	QSPM Data Direction Register

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9.4.3.1 QSPM PORT DATA REGISTER (QPDR). QPDR determines the actual input or output value of a QSPM port pin, if the pin is defined in QPAR as general-purpose I/O. All QSPM port pins may be used as general-purpose I/O. Writes to this register affect the pins defined as outputs; reads of this register return the actual value of the pins.

QPDR $815

15	7	6	5	4	3	2	1	0
RESERVED	RSVD			D4 (PCS1)	D3 (PCS0/$\overline{SS}$)	D2 (SCK)	D1 (MOSI)	D0 (MISO)
RESET:	0	0	0	0	0	0	0	0

9.4.3.2 QSPM PIN ASSIGNMENT REGISTER (QPAR). QPAR determines which of the QSPI pins, with the exception of the SCK pin, are actually used by the QSPI submodule, and which pins are available for general-purpose I/O. Pins may be assigned to the QSPI or to function as general-purpose I/O on a pin-by-pin basis. QSPI pins designated by QPAR as general-purpose I/O are controlled only by QDDR and QPDR. The QSPI has no effect on these pins.

QPAR $816

15	14	13	12	11	10	9	8	0
0	RSVD	RSVD	PCS1	PCS0/$\overline{SS}$	0	MOSI	MISO	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
RESET:								
0	0	0	0	0	0	0	0	

0 = General-purpose I/O
1 = QSPI module

Bit 15—Not Implemented

Bits 14–13—Reserved

PCS1—Peripheral Chip Select 1

PCS0/$\overline{SS}$—Peripheral Chip Select 0/Slave Select

These bits determine whether the associated QSPM port pins function as general-purpose I/O pins or are assigned to the QSPI submodule.

Bit 10—Not Implemented

(When the QSPI is enabled, the SCK pin is required.)

MOSI—Master Out Slave In

MISO—Master In Slave Out

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These bits determine whether the associated QSPM port pin functions as a general-purpose I/O pin or is assigned to the QSPI submodule.

9.4.3.3 QSPM DATA DIRECTION REGISTER (QDDR). QDDR determines each I/O pin as an input or an output regardless of whether the QSPI submodule is enabled or disabled. All QSPM pins are configured during reset as general-purpose inputs. (The QSPI is disabled.)

QDDR $817

15	7	6	5	4	3	2	1	0
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	RSVD			PCS1	PCS0/$\overline{SS}$	SCK	MOSI	MISO
RESET:								
	0	0	0	0	0	0	0	0

0 = Input
1 = Output

Bits 7—Reserved

PCS1—Peripheral Chip Select 1

PSC0/$\overline{SS}$—Peripheral Chip Select 0/Slave Select

SCK—Serial Clock

MOSI—Master Out Slave In

MISO—Master In Slave Out

All of these bits determine the QSPI port pin operation to be input or output.

1 = Output
0 = Input

9.5 QSPI SUBMODULE

The QSPI submodule communicates with external peripherals via synchronous serial bus. The QSPI is fully compatible with the serial peripheral interface (SPI) systems found on other Motorola devices such as the M68HC11 and M68HC05 Families. It has all of the capabilities of the SPI system as well as several new features. The following paragraphs describe the features, block diagram, pin descriptions, programmer's model (memory map) inclusive of registers, and the master and slave operation of the QSPI.

9.5.1 Features

Standard SPI features are listed below, followed by a list of the additional features offered on the QSPI:

- Full Duplex, Three-Wire Synchronous Transfers

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- Half Duplex, Two-Wire Synchronous Transfers
- Master or Slave Operation
- Programmable Master Bit Rates
- Programmable Clock Polarity and Phase
- End-of-Transmission Interrupt Flag
- Master-Master Mode Fault Flag
- Easily Interfaces to Simple Expansion Parts (A/D converters, EEPROMS, display drivers, etc.)

QSPI-Enhanced features are as follows:

- Programmable Queue—Up to 16 Preprogrammed Transfers
- Programmable Peripheral Chip Selects—Two Pins Select Up to Four SPI Chips
- Wraparound Transfer Mode—For Autoscanning of Serial A/D (or Other) Peripherals, With No CPU Overhead
- Programmable Transfer Length—From 8–16 Bits Inclusive
- Programmable Transfer Delay—From 1 µs to 0.5 ms (at 16.78 MHz)
- Programmable Queue Pointer
- Continuous Transfer Mode—Up to 256 Bits

9.5.1.1 PROGRAMMABLE QUEUE. A programmable queue allows the QSPI to perform up to 16 serial transfers without CPU intervention. Each transfer corresponds to a queue entry containing all the information needed by the QSPI to independently complete one serial transfer. This unique feature greatly reduces CPU/QSPI interaction, resulting in increased CPU and system throughput.

9.5.1.2 PROGRAMMABLE PERIPHERAL CHIP SELECTS. Two peripheral chip-select pins allow the QSPI to access up to four independent peripherals by decoding the two peripheral chip-select signals. Two independent peripherals can be selected by direct connection to a chip-select pin. The peripheral chip selects simplify interfacing to two peripherals by providing dedicated peripheral chip-select signals, alleviating the need for CPU intervention.

9.5.1.3 WRAPAROUND TRANSFER MODE. Wraparound transfer mode allows automatic, continuous re-execution of the preprogrammed queue entries. Newly transferred data replaces previously transferred data. Wraparound simplifies interfacing with A/D converters by automatically providing the CPU with the latest A/D conversions in the QSPI RAM. Consequently, serial peripherals appear as memory-mapped parallel devices to the CPU.

9.5.1.4 PROGRAMMABLE TRANSFER LENGTH. The number of bits in a serial transfer is programmable from 8 to 16 bits, inclusive. For example, 10 bits could be used for communicating with an external 10-bit A/D converter. Likewise, a vacuum fluorescent

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display driver might require a 12-bit serial transfer. The programmable length simplifies interfacing to serial peripherals that require different data lengths.

9.5.1.5 PROGRAMMABLE TRANSFER DELAY. An inter-transfer delay may be programmed from approximately 1 to 500 µs (using a 16.78-MHz system clock). For example, an A/D converter may require time between transfers to complete a new conversion. The default delay is 1 µs. The programmable length of delay simplifies interfacing to serial peripherals that require delay time between data transfers.

9.5.1.6 PROGRAMMABLE QUEUE POINTER. The QSPI has a pointer that identifies the queue location containing the data for the next serial transfer. The CPU can switch from one task to another in the QSPI by writing to the queue pointer, changing the location in the queue that is to be transferred next. Otherwise, the pointer increments after each serial transfer. By segmenting the queue, multiple-task support can be provided by the QSPI.

9.5.1.7 CONTINUOUS TRANSFER MODE. The continuous transfer mode allows the user to send and receive an uninterrupted bit stream with a peripheral. A minimum of 8 bits and a maximum of 256 bits may be transferred in a single burst without CPU intervention. Longer transfers are possible; however, minimal CPU intervention is required to prevent loss of data. A 1-µs pause (using a 16.78-MHz system clock) is inserted between each queue entry transfer.

9.5.2 Block Diagram

Figure 9-3 provides a block diagram of the QSPI submodule components.

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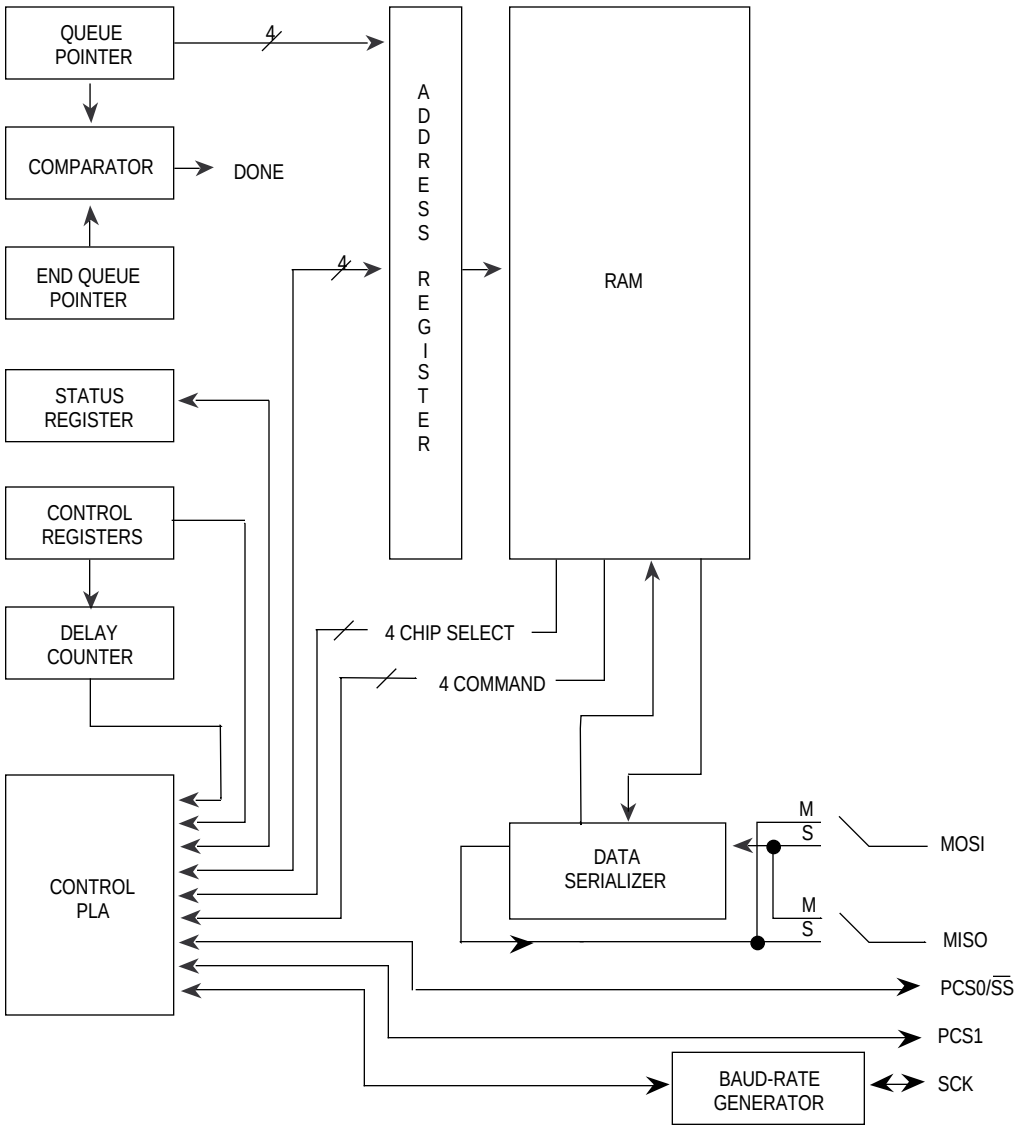

Figure 9-3. QSPI Submodule Diagram

9.5.3 QSPI Pins

Five pins are associated with the QSPI; however, when not needed for a QSPI application, they may be configured as general-purpose I/O pins. Figure 9-3 identifies the QSPI pins.

Table 9-6 lists the QSPI external input and output pins and their functions. QSPM register QDDR determines whether the pins are designated as input or output. The user must initialize QDDR for the QSPI to function correctly.

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Table 9-6. External Pin Inputs/Outputs to the QSPI

Pin Names	Mnemonics	Mode	Function
Master In Slave Out	MISO	Master Slave	Serial Data Input to QSPI Serial Data Output from QSPI
Master Out Slave In	MOSI	Master Slave	Serial Data Output from QSPI Serial Data Input to QSPI
Serial Clock	SCK[1]	Master Slave	Clock Output from QSPI Clock Input to QSPI
Peripheral Chip Select	PCS1	Master	Outputs Select Peripheral
Peripheral Chip Select[2] Slave Select[3]	PCS0/$\overline{SS}$	Master Slave	Output Selects Peripheral Input Selects the QSPI
Slave Select[4]	$\overline{SS}$	Master	May Cause Mode Fault

NOTES:
1. All QSPI pins (except SCK) can be used as general-purpose I/O if they are not used by the QSPI while the QSPI is operating.
2. An output (PCS0) when the QSPI is in master mode.
3. An input ($\overline{SS}$) when the QSPI is in slave mode.
4. An input ($\overline{SS}$) when the QSPI is in master mode; useful in multimaster systems.

9.5.4 Programmer's Model and Registers

The programmer's model (memory map) for the QSPI submodule consists of the QSPM global and pin control registers (refer to **9.4.2 QSPM Global Registers** and **9.4.3 QSPM Pin Control Registers**), four QSPI control registers, one status register, and the 80-byte QSPI RAM. Table 9-7 lists the registers and the QSPI RAM of the programmer's model. All of the registers and RAM can be read and written by the CPU. The four control registers must be initialized, in proper order, before the QSPI is enabled to ensure defined operation. Only the control registers must adhere to the order of sequence prescribed in **9.4.1 Overall QSPM Configuration Summary**. Write register SPCR1 last when setting up the QSPI, as this register contains the QSPI enable bit (SPE). Asserting this bit starts the QSPI. QSPI control registers are reset to a defined state and may then be changed by the CPU. Reset values are shown below each register.

Table 9-7. QSPI Registers

Address	Name	Usage
$818, 9	SPCR0	QSPI Control Register 0
$81A, B	SPCR1	QSPI Control Register 1
$81C, D	SPCR2	QSPI Control Register 2
$81E	SPCR3	QSPI Control Register 3
$81F	SPSR	QSPI Status Register
$900–1F	RAM	QSPI Receive Data (16 Words)
$920–3F	RAM	QSPI Transmit Data (16 Words
$940–4F	RAM	QSPI Command Control (8 Words)

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In general, rewriting the same value into a control register does not affect the QSPI operation with the exception of NEWQP (bits 3–0) in SPCR2. Rewriting the same value to these bits causes the RAM queue pointer to restart execution at the designated location.

If control bits are to be changed, the CPU should halt the QSPI first. With the exception of SPCR2, writing a different value into a control register while the QSPI is enabled may disrupt operation. SPCR2 is buffered, preventing any disruption of the current serial transfer. After completion of the current serial transfer, the new SPCR2 values become effective.

9.5.4.1 QSPI CONTROL REGISTER 0 (SPCR0). SPCR0 contains parameters for configuring the QSPI before it is enabled. Although the CPU can read and write this register, the QSPM has read-only access.

SPCR0 $818

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSTR	WOMQ	BITS				CPOL	CPHA	SPBR							
RESET:															
0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0

MSTR—Master/Slave Mode Select

1 = QSPI is system master and can initiate transmission to external SPI devices.
0 = QSPI is a slave device, and only responds to externally generated serial transfers.

MSTR configures the QSPI for either master or slave mode operation. This bit is cleared on reset and may only be written by the CPU, not the QSPM.

WOMQ—Wired-OR Mode for QSPI Pins

1 = All QSPI port pins designated as output by QDDR function as open-drain outputs and can be wire-ORed to other external lines.
0 = Output pins have normal outputs instead of open-drain outputs.

WOMQ allows the QSPI pins to be wire-ORed, regardless of whether they are used as general-purpose outputs or as QSPI outputs. WOMQ affects the QSPI pins whether the QSPI is enabled or disabled.

BITS—Bits Per Transfer

In master mode, BITS determines the number of data bits transferred for each serial transfer in the queue that has the command control bit, BITSE of the QSPI RAM, equal to one. If BITSE equals zero for a command, 8 bits are transferred for that command regardless of the value in BITS. Data transfers from 8 to 16 bits are supported. Illegal (reserved) values all default to 8 bits. BITSE is not used in slave mode. All transfers are of the length specified by BITS. Table 9-8 shows the number of bits per transfer.

Table 9-8. Bits per Transfer if Command Control Bit BITSE = 1

Bit 13	Bit 12	Bit 11	Bit 10	Bits per Transfer

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0	0	0	0	16
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CPOL—Clock Polarity

1 = The inactive state value of SCK is high.
0 = The inactive state value of SCK is low.

CPOL is used to determine the inactive state value of the serial clock (SCK). CPOL is used in conjunction with CPHA to produce the desired clock-data relationship between master and slave device(s). For an understanding of the QSPI clock/data timing relationship, refer to the timing diagrams in Figures 9-24–9-27.

CPHA—Clock Phase

1 = Data is changed on the leading edge of SCK and captured on the following edge of SCK.
0 = Data is captured on the leading edge of SCK and changed on the following edge of SCK.

CPHA determines which edge of SCK causes data to change and which edge of SCK causes data to be captured. CPHA is used in conjunction with CPOL to produce the desired clock-data relationship between master and slave device(s). Note that CPHA is set at reset.

SPBR—Serial Clock Baud Rate

The QSPI internally generates the baud rate for SCK, the frequency of which is programmable by the user. The clock signal is derived from the MC68341 system clock using a modulus counter. At reset, BAUD is initialized to a 2.1-MHz SCK frequency.

The user programs a baud rate for SCK by writing a baud value from 2 to 255. The following equation determines the SCK baud rate:

$$\text{SCK Baud Rate} = \text{System Clock}/(2 \bullet \text{SPBR}) \qquad (9\text{-}1)$$

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or

$$\text{SPBR} = \text{System Clock}/(2 \bullet \text{SCK Baud Rate Desired}) \qquad (9\text{-}2)$$

where SPBR equals 2, 3, 4, . . . , 255.

Programming SPBR with the values zero or one disables the QSPI baud rate generator. SCK is disabled and assumes its inactive state value. No serial transfers occur. SPBR has 254 active values. Table 9-9 lists several possible baud values and the corresponding SCK frequency based on a 16.78-MHz system clock.

Table 9-9. Examples of SCK Frequencies

System Clock Frequency	Required Division Ratio	Value of SPBR	Actual SCK Frequency
16.78 MHz	4	2	4.19 MHz
	8	4	2.10 MHz
	16	8	1.05 MHz
	34	17	493 kHz
	168	84	100 kHz
	510	255	33 kHz

9.5.4.2 QSPI CONTROL REGISTER 1 (SPCR1). SPCR1 contains parameters for configuring the QSPI before it is enabled. Although the CPU can read and write this register, the QSPM has read access only, except for SPE. This bit is automatically cleared by the QSPI after completing all serial transfers or when a mode fault occurs.

SPCR1 $81A

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPE	DSCKL							DTL							
RESET:															
0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0

SPE—QSPI Enable

1 = The QSPI is enabled and the pins allocated by QSPM register QPAR are controlled by the QSPI.

0 = The QSPI is disabled, and the seven QSPI pins can be used as general-purpose I/O pins, regardless of the values in QPAR.

This bit enables or disables the QSPI Submodule. Setting SPE causes the QSPI to begin operation. If the QSPI is a master, setting SPE causes the QSPI to begin initiating serial transfers. If the QSPI is a slave, the QSPI begins monitoring the PCS0/$\overline{SS}$ pin to respond to the external initiation of a serial transfer.

When the QSPI is disabled, the CPU may use the QSPI RAM. When the QSPI is enabled, both the QSPI and the CPU have access to the QSPI RAM. The CPU has both read and write access capability to all 80 bytes of the QSPI RAM. The QSPI can read

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only the transmit data segment and the command control segment, and can write only the receive data segment of the QSPI RAM.

By clearing SPE, the QSPI turns itself off automatically when it is finished. An error condition called mode fault (MODF) also clears SPE. This error occurs when PCS0/$\overline{SS}$ is configured for input, the QSPI is a system master (MSTR = 1), and PCS0/$\overline{SS}$ is driven low externally.

To stop the QSPI, assert HALT, then wait until HALTA is set. SPE may then be safely cleared to zero, providing an orderly method of quickly shutting down the QSPI after the current serial transfer is completed. The CPU can immediately disable the QSPI by just clearing SPE; however, loss of data from a current serial transfer may result and confuse an external SPI device.

DSCKL—Delay before SCK

This bit determines the length of time the QSPI delays from peripheral chip select (PCS) valid to SCK transition for serial transfers in which the command control bit, DSCK of the QSPI RAM, equals one. PCS may be either of the peripheral chip-select pins. The following equation determines the actual delay before SCK:

$$\text{PCS to SCK Delay} = [\text{DSCKL/System Clock Frequency}] \quad (9\text{-}3)$$

where DSCKL equals {1,2,3, . . . 127}.

NOTE

A zero value for DSCKL causes a delay of 128/system clocks, which equals 7.6 µs for a 16.78-MHz system clock. Because of design limits, a DSCKL value of one defaults to the same timing as a value of two.

If a queue entry's DSCK equals zero, then DSCKL is not used. Instead, the PCS valid-to-SCK transition is one-half SCK period.

DTL—Length of Delay after Transfer

These bits determine the length of time that the QSPI delays after each serial transfer in which the command control bit, DT of the QSPI RAM, equals one. The following equation is used to calculate the delay:

$$\text{Delay after transfer} = [(32 \bullet \text{DTL})/\text{system clock frequency}] \quad (9\text{-}4)$$

where DTL equals {1,2,3, . . . 255}.

NOTE

A zero value for DTL causes a delay-after-transfer value of (32 • 256)/system clock, which equals 488.5 µs with a 16.78-MHz system clock.

If DT equals zero, a standard delay is inserted.

$$\text{Standard Delay-after-Transfer} = [17/\text{System Clock}] \quad (9\text{-}5)$$
$$= 1\ \mu\text{s with a 16.78-MHz System Clock}$$

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Delay after transfer can be used to ensure that the deselect time requirement (for peripherals having such a requirement) is met. Some peripherals must be deselected for a minimum period of time between consecutive serial transfers. A delay after transfer can be inserted between consecutive transfers to a given peripheral to ensure that its minimum deselect time requirement is met or to allow serial A/D converters to complete conversion before the next transfer is made.

9.5.4.3 QSPI CONTROL REGISTER 2 (SPCR2). SPCR2 contains parameters for configuring the QSPI. Although the CPU can read and write this register, the QSPM has read access only. Writes to this register are buffered. A write to SPCR2 that changes any of the bit values (while the QSPI is operating) is ineffective on the current serial transfer, but becomes effective on the next serial transfer. Reads of SPCR2 return the actual current value of the register, not the buffer. Refer to **9.5.5 Operating Modes and Flowcharts** for a detailed description of this register.

SPCR2 $81C

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPIFIE	WREN	WRTO	0	ENDQP				0	0	0	0	NEWQP			
RESET:															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPIFIE—SPI Finished Interrupt Enable

1 = QSPI interrupts enabled
0 = QSPI interrupts disabled

SPIFIE enables the QSPI to generate a CPU interrupt upon assertion of the status flag SFIP. Because of its special buffering, the value written to SPIFIE applies only upon completion of the queue (the transfer of the entry indicated by ENDQP). Thus, if a single sequence of queue entries is to be transferred (i.e., no WRAP), then SPIFIE should be set to the desired state before the first transfer.

If a subqueue (see bit NEWQP) is to be used, the same CPU write that causes a branch to the subqueue may enable or disable the SPIF interrupt for the subqueue. The primary queue retains its own selected interrupt mode, either enabled or disabled.

The SPIF interrupt must be cleared by clearing SPIF. Later interrupts may then be prevented by clearing SPIFIE to zero.

The QSPI has three possible interrupt sources, but only one interrupt vector. These sources are SPIF, MODF, and HALTA. When the CPU responds to a QSPI interrupt, the user must ascertain the exact interrupt cause by reading register SPSR. Any interrupt that was set may then be cleared by writing to SPSR with a zero in the bit position corresponding to the exact interrupt source. Clearing SPIFIE does not immediately clear an interrupt already caused by SPIF.

WREN—Wrap Enable

1 = Wraparound mode enabled
0 = Wraparound mode disabled

WREN enables or disables wraparound mode. If enabled, the QSPI executes commands in the queue through the command contained in ENDQP. Execution

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continues at either address $0 or at the address found in NEWQP, depending on the state of WRTO. The QSPI continues looping until either WREN is negated, HALT is asserted, or SPE is negated. Once WREN is negated, the QSPI finishes executing commands through the command at the address contained in ENDQP, sets the SPIF flag, and stops. When WREN is set, SPIF is set each time the QSPI transfers the entry indicated by ENDQP.

WRTO—Wrap To

When wraparound mode is enabled and after the end of queue has been reached, WRTO determines which address the QSPI executes next. End of queue is determined by an address match with ENDQP. Execution wraps to address $0 if WRTO is not set, or to the address found in NEWQP if WRTO is set.

Bit 12—Not Implemented

ENDQP—Ending Queue Pointer

This field determines the last absolute address in the queue to be completed by the QSPI. After completing each command, the QSPI compares the queue pointer value of the just-completed command with the value of ENDQP. If the two values match, the QSPI assumes it has reached the end of the programmed queue and sets the SPIF flag to so indicate.

The QSPI RAM queue has 16 entries: $0–$F. The user may program the NEWQP to start executing commands, beginning at any of the 16 addresses. Similarly, the user may program the ENDQP to stop execution of commands at any of the 16 addresses.

The queue is a circular data structure. If ENDQP is set to a lower address than NEWQP, the QSPI executes commands through address $F, and then continues execution at address $0 and so on until it stops after executing the command at address ENDQP. A maximum of 16 commands are executed before stopping, unless wraparound mode is enabled or unless the user modifies NEWQP and/or ENDQP.

The user may write a NEWQP value at any time, changing the flow of execution. ENDQP may also be written at any time, changing the length of the queue. Wraparound mode may also be enabled, causing continuous execution until the mode is disabled or the QSPI is halted.

Bits 7–4—Not Implemented

NEWQP—New Queue Pointer Value

NEWQP determines which queue entry the QSPI transfers first. NEWQP should be initialized before the QSPI is enabled with SPE. NEWQP may also be written while the QSPI is operating. When this happens, the QSPI completes transfer of the queue entry in progress and then immediately begins transferring queue entries starting with the entry indicated by the NEWQP.

In this way, NEWQP provides additional functionality to the QSPI by providing a mechanism for supporting multiple queues or subqueues within the QSPI RAM. By changing the value in NEWQP, the user can cause the QSPI to execute a sequence of

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QSPI commands beginning at any location in the queue. Therefore, the user in advance is able to set up separate subqueues for different tasks within the QSPI RAM. By writing to NEWQP, selection between the different subqueues within the QSPI RAM is accomplished.

If wraparound mode is enabled by setting WREN and WRTO in SPCR2, NEWQP assumes an additional function. When the end of the queue is reached, as determined by ENDQP, the address contained in NEWQP is used by the QSPI to wrap around to the first queue entry. The QSPI then re-executes the queued commands repeatedly until halted.

9.5.4.4 QSPI CONTROL REGISTER 3 (SPCR3). SPCR3 contains parameters for configuring the QSPI. The CPU can read and write this register; the QSPM has read-only access.

SPCR3 $81E

15	14	13	12	11	10	9	8	0
0	0	0	0	0	LOOPQ	HMIE	HALT	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
RESET:								
0	0	0	0	0	0	0	0	

Bits 15–11—Not Implemented

LOOPQ—QSPI Loop Mode

1 = Feedback path enabled
0 = Feedback path disabled

LOOPQ enables or disables the feedback path on the data serializer for testing. If enabled, LOOPQ routes serial output data back into the data serializer, instead of received data. If disabled, LOOPQ allows regular received data into the data serializer. LOOPQ does not affect the QSPI output pins.

HMIE—HALTA and MODF Interrupt Enable

1 = HALTA and MODF interrupts enabled
0 = HALTA and MODF interrupts disabled

HMIE enables or disables QSPI interrupts to the CPU caused when either the HALTA status flag or the MODF status flag in SPSR is asserted. When HMIE is set, the assertion of either flag causes the QSPI to send a hardware interrupt to the CPU. When HMIE is clear, the asserted flag does not cause an interrupt.

HALT—Halt

1 = Halt enabled
0 = Halt not enabled

This bit is used by the CPU to stop the QSPI on a queue boundary. The QSPI halts in a known state from which it can later be restarted. When HALT is asserted by the CPU, the QSPI finishes executing the current serial transfer (up to 16 bits) and then halts. While halted, if the command control bit (CONT of the QSPI RAM) for the last command was asserted, the QSPI continues driving the peripheral chip-select pins with the value

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designated by the last command before the halt. If CONT was clear, the QSPI drives the peripheral chip-select pins to the value in QSPM register QPDR.

If HALT is asserted during the last command in the queue, the QSPI completes the last command, asserts both HALTA and SPIF, and clears SPE. If the last queue command has not been executed, asserting HALT does not set SPIF nor clear SPE. QSPI execution continues when the CPU clears HALT.

9.5.4.5 QSPI STATUS REGISTER (SPSR). SPSR contains QSPI status information. Only the QSPI can assert the bits in this register. The CPU reads this register to obtain status information and writes this register to clear status flags. CPU writes to CPTQP have no effect.

SPSR $81F

15	7	6	5	4	3	2	1	0
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX	SPIF	MODF	HALTA	0	CPTQP			
RESET:								
	0	0	0	0	0	0	0	0

SPIF—QSPI Finished Flag

1 = QSPI finished
0 = QSPI not finished

SPIF is set when the QSPI finishes executing the last command determined by the address contained in ENDQP in SPCR2. When the address of the command being executed matches the ENDQP, the SPIF flag is set after finishing the serial transfer.

If wraparound mode is enabled (WREN = 1), the SPIF is set, after completion of the command defined by ENDQP, each time the QSPI cycles through the queue. If SPIFIE in SPCR2 is set, an interrupt is generated when SPIF is asserted. Once SPIF is set, the CPU may clear it by reading SPSR followed by writing SPSR with a zero in SPIF.

MODF—Mode Fault Flag

1 = Another SPI node requested to become the network SPI master while the QSPI was enabled in master mode (MSTR = 1), or the PCS0/$\overline{SS}$ pin was incorrectly pulled low by external hardware.
0 = Normal operation

MODF is asserted by the QSPI when the QSPI is the serial master (MSTR = 1) and the slave select (PCS0/$\overline{SS}$) input pin is pulled low by an external driver. This is possible only if the PCS0/$\overline{SS}$ pin is configured as input by QDDR. This low input to $\overline{SS}$ is not a normal operating condition. It indicates that a multimaster system conflict may exist, that an external device is requesting to become the SPI network master, or simply that the hardware is incorrectly affecting PCS0/$\overline{SS}$. SPE in SPCR1 is cleared, disabling the QSPI. The QSPI pins revert to control by QPDR. If MODF is set and HMIE in SPCR3 is asserted, the QSPI generates an interrupt to the CPU.

The CPU may clear MODF by reading SPSR with MODF asserted, followed by writing SPSR with a zero in MODF. After correcting the mode fault problem, the QSPI can be re-enabled by asserting SPE.

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The PCS0/$\overline{SS}$ pin may be configured as a general-purpose output instead of input to the QSPI. This inhibits the mode fault checking function. In this case, MODF is not used by the QSPI.

HALTA—Halt Acknowledge Flag

1 = QSPI halted
0 = QSPI not halted

HALTA is asserted by the QSPI when it has come to an orderly halt at the request of the CPU, via the assertion of HALT. To prevent undefined operation, the user should not modify any QSPI control registers or RAM while the QSPI is halted.

If HMIE in SPCR3 is set, the QSPI sends interrupt requests to the CPU when HALTA is asserted. The CPU can only clear HALTA by reading SPSR with HALTA set and then writing SPSR with a zero in HALTA.

Bit 4—Not Implemented

CPTQP—Completed Queue Pointer

CPTQP contains the queue pointer value of the last command in the queue that was completed. The value of CPTQP is not updated until the command has been completed entirely. While the first command in a queue is executing, CPTQP contains either the reset value ($0) or the pointer to the last command completed in the previous queue.

If the QSPI is halted, CPTQP may be used to determine which commands have not been executed. The CPTQP may also be used to determine which locations in the receive data segment of the QSPI RAM contain valid received data.

9.5.4.6 QSPI RAM. The QSPI uses an 80-byte block of dual-access static RAM, which can be accessed by both the QSPI and the CPU. Because of sharing, the length of time taken by the CPU to access the QSPI RAM, when the QSPI is enabled, may be longer than when the QSPI is disabled. From one to four CPU wait states may be inserted by the QSPI in the process of reading or writing.

The size and type of access of the QSPI RAM by the CPU affects the QSPI access time. The QSPI is byte, word, and long-word addressable. Only word accesses of the RAM by the CPU are coherent accesses because these accesses are an indivisible operation. If the CPU makes a coherent access of the QSPI RAM, the QSPI cannot access the QSPI RAM until the CPU is finished. However, a long-word or misaligned word access is not coherent because the CPU must break its access of the QSPI RAM into two parts, which allows the QSPI to access the QSPI RAM in between the two accesses by the CPU.

The RAM is divided into three segments: receive data (REC.RAM), transmit data (TRAN.RAM), and command control (COMD.RAM). Receive data is information received from a serial device external to the MC68341. Transmit data is information stored by the CPU for transmission to an external peripheral chip. Command control contains all the information needed by the QSPI to perform the transfer. Figure 9-4 illustrates the organization of the RAM.

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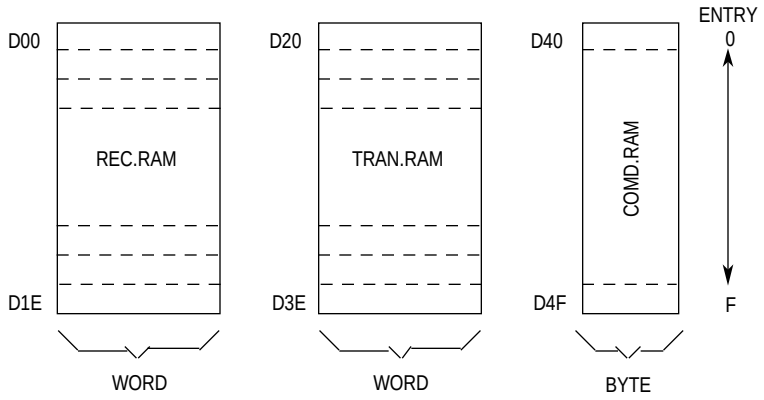

Figure 9-4. Organization of the QSPI RAM

Once the CPU has set up the queue of QSPI commands and enabled the QSPI, the QSPI operates independently of the CPU. The QSPI executes all of the commands in its queue, sets a flag indicating that it is finished, and then either interrupts the CPU or waits for CPU intervention.

9.5.4.6.1 Receive Data RAM (REC.RAM). This segment of the RAM stores the data that is received by the QSPI from peripherals, SPI bus masters, or other SPI devices. The CPU reads this segment of RAM to retrieve the data from the QSPI. Data stored in receive RAM is right-justified, i.e., the least significant bit is always in the right-most bit position within the word (bit 0) regardless of the serial transfer length. Unused bits in a receive queue entry are set to zero by the QSPI upon completion of the individual queue entry. The CPU can access the data using byte, word, or long-word addressing.

The CPTQP value in SPSR shows which queue entries have been executed. The CPU uses this information to determine which locations in receive RAM contain valid data before reading them.

9.5.4.6.2 Transmit Data RAM (TRAN.RAM). This segment of the RAM stores the data that is to be transmitted by the QSPI to peripherals. The CPU normally writes one word of data into this segment for each queue command to be executed. If the corresponding peripheral, such as a serial input port, is used solely to input data, then this segment does not need to be initialized.

Information to be transmitted by the QSPI should be written by the CPU to the transmit data segment in a right-justified manner. The information in the transmit data segment of the RAM cannot be modified by the QSPI. The QSPI merely copies the information to its data serializer for transmission to a peripheral. Information in transmit RAM remains there until it is re-written by the CPU.

9.5.4.6.3 Command RAM (COMD.RAM). The command segment of the QSPI RAM is used only by the QSPI when it is in master mode. The CPU writes one byte of control information to this segment for each QSPI command to be executed. The information in the command RAM cannot be modified by the QSPI. It merely uses the information to perform the serial transfer.

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COMD.RAM consists of 16 bytes. Each byte is divided into two fields. The first, the peripheral chip-select field, activates the correct serial peripheral during the transfer. The second, the command control field, provides transfer options specifically for that command/serial transfer. This feature gives the user more control over each transfer, providing the flexibility to interface to external SPI chips with different requirements (refer to Figure 9-5).

A maximum of 16 commands can be in the queue command control bytes. These bytes are assigned an address from $0–$F. Queue execution by the QSPI proceeds from the address contained in NEWQP through the address contained in ENDQP. Both of these fields are contained in SPCR2.

COMD.RAM—**Command RAM** $940

7	6	5	4	3	2	1	0
CONT	BITSE	DT	DSCK	RSVD	RSVD	PCS1	PCS0 *
—	—	—	—	—	—	—	—
CONT	BITSE	DT	DSCK	RSVD	RSVD	PCS1	PCS0 *
						$94F	
COMMAND CONTROL				PERIPHERAL CHIP SELECT			

*The PCS0 bit represents the dual-function PCS0/$\overline{SS}$.

Figure 9-5. Command RAM

CONT—Continue

1 = Keep peripheral chip selects asserted after transfer is complete.
0 = Return control of peripheral chip selects to QPDR after transfer is complete.

Some peripheral chips must be deselected between every QSPI transfer. Other chips must remain selected between several sequential serial transfers. CONT is designed to provide the flexibility needed to handle both cases.

If CONT = 1 and the peripheral-chip-select pattern for the next command is the same as that of the present command, the QSPI drives the PCS pins to the same value continuously during the two serial transfers. An unlimited number of serial transfers may be sent to the same peripheral(s) without deselecting it (them) by setting CONT = 1.

If CONT = 1 and the peripheral-chip-select pattern for the next command is different from that of the present command, the QSPI drives the PCS pins to the new value for the second serial transfer. Although this case is similar to CONT = 0, a difference remains. When CONT = 1, the QSPI continues to drive the PSC pins using the pattern from the first transfer until it switches to using the pattern for the second transfer.

When CONT = 0, the QSPI drives the PCS pins to the values found in register QPDR between serial transfers.

BITSE—Bits Per Transfer Enable

1 = Number of bits set in BITS field of SPCR0

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0 = 8 bits

DT — Delay After Transfer

A/D converters require a known amount of time to perform a conversion. The conversion time for serial CMOS A/D converters may range from 1–100 µs.

To facilitate interfacing to peripherals with a latency requirement, the QSPI provides a programmable delay at the end of the serial transfer, with the DT field. The user may avoid using this delay option by executing transfers with other peripheral devices in between transfers with the peripheral that requires a delay. This interleaved operation improves the effective serial transfer rate.

The amount of the delay between transfers is programmable by the user via the DTL field in SPCR1. The range may be set from 1-489 µs at 16.78 MHz.

DSCK — PCS to SCK Delay

1 = DSCKL field in SPCR1 specifies value of delay from PCS valid to SCK.
0 = PCS valid to SCK transition is 1/2 SCK.

PCS1–PCS0/$\overline{SS}$—Peripheral Chip Select

The two peripheral chip-select bits can be used directly to select one of two external chips for the serial transfer, or decoded by external hardware to select one of four chip-select patterns for the serial transfer. More than one peripheral chip select may be activated at a time, which is useful for broadcast messages in a multinode SPI system. More than one peripheral chip may be connected to each PCS pin. Care must be taken by the system designer not to exceed the maximum drive capability of the pins as defined in **Section 12 Electrical Characteristics** for QSPM pins.

QSPM register QPDR determines the state of the PCS pins when the QSPI is disabled, and also determines the state of PCS pins that are not assigned to the QSPI when the QSPI is enabled. QPDR determines the state of pins assigned to the QSPI between transfers as well.

To use a peripheral chip-select pin, the CPU assigns the pin to the QSPI in QPAR by writing a one to the appropriate bit. The default value of the PCS pin should be written to QPDR. Next, the pin must be defined as an output in QDDR by setting the appropriate bit, which causes the pin to start driving the default value.

The QSPI RAM may then be initialized for a serial transmission, with the peripheral-chip-select bits of the command control byte appropriately configured to activate the desired PCS pin(s) during the serial transfer. When the command is executed, the PCS pin(s) are driven to the values contained in the appropriate control byte. After completing the serial transfer, the QSPI returns control of the peripheral-chip-select signal(s) (if CONT = 0 in the command control byte) to register QPDR.

9.5.5 Operating Modes and Flowcharts

The QSPI utilizes an 80-byte block of dual-access static RAM accessible by both the QSPI and the CPU. The RAM is divided into three segments: 16 command control bytes, 16 transmit data words of information to be transmitted, and 16 receive data words for data to be received. Once the CPU has a) set up a queue of QSPI commands, b) written

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the transmit data segment with information to be sent, and c) enabled the QSPI, the QSPI operates independently of the CPU. The QSPI executes all of the commands in its queue, sets a flag indicating completion, and then either interrupts the CPU or waits for CPU intervention.

The QSPI operates on a queue data structure contained in the QSPI RAM. Control of the queue is handled by three pointers: the new queue pointer (NEWQP), the completed queue pointer (CPTQP), and the end queue pointer (ENDQP). NEWQP, contained in SPCR2, points to the first command in the queue to be executed by the QSPI. CPTQP, contained in SPSR, points to the command last executed by the QSPI. ENDQP, also contained in SPCR2, points to the last command in the queue to be executed by the QSPI, unless wraparound mode is enabled (WREN = 1).

At reset, NEWQP is initialized to $0, causing QSPI execution to begin at queue address $0 when the QSPI is enabled (SPE = 1). CPTQP is set by the QSPI to the queue address ($0-$F) last executed, but is initialized to $0 at reset. ENDQP is also initialized to $0 at reset, but should be changed by the user to reflect the last queue entry to be transferred before enabling the QSPI. Leaving NEWQP and ENDQP set to $0 causes a single transfer to occur when the QSPI is enabled.

The organization of the QSPI RAM defines that one byte of command control data, one word of transmit data, and one word of receive data all correspond to one queue entry, $0-$F.

After executing the current command, ENDQP is checked against CPTQP for an end-of-queue condition. If a match occurs, the SPIF flag is set and the QSPI stops unless wraparound mode is enabled.

The QSPI operates in one of two modes: master or slave. Master mode is used when the MC68341 originates all data transfers. Slave mode is used when another device or a peripheral to the MC68341 initiates all serial transfers to the MC68341 via the QSPI. Switching between the two operating modes is achieved under software control by writing to the master (MSTR) bit in SPCR0.

In master mode, the QSPI executes the queue of commands as defined by the control bits in each entry. Chip-select pins are activated; data is transmitted, received, and placed in the QSPI RAM.

In slave mode, a similar operation occurs in response to the slave select ($\overline{SS}$) pin activated by an external SPI bus master. The primary differences are a) no peripheral chip selects are generated, and b) the number of bits transferred is controlled in a different manner. When the QSPI is selected, it executes the next queue transfer to correctly exchange data with the external device.

The following flowcharts, Figures 9-6–9-8, outline the operation of the QSPI for both master and slave modes. Note that the CPU must initialize the QSPM global and pin registers and the QSPI control registers before enabling the QSPI for either master or slave operation. If using master mode, the necessary command control RAM should also

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be written before enabling the QSPI. Any data to be transmitted should also be written before the QSPI is enabled. When wrap mode is used, data for subsequent transmissions may be written at any time.

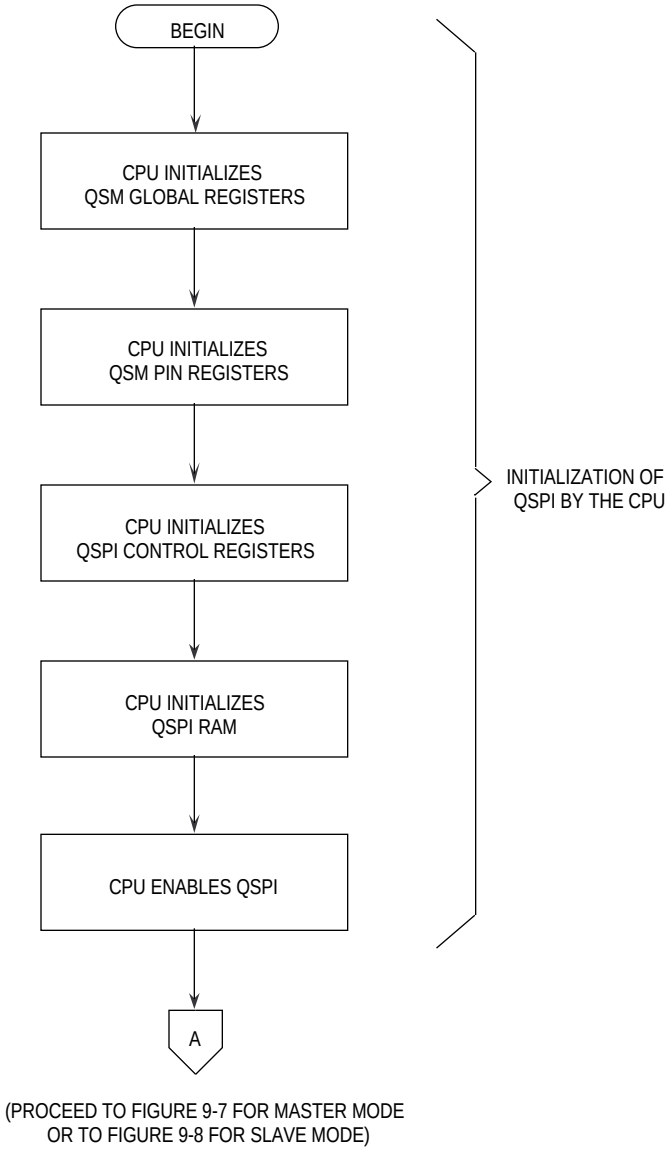

Figure 9-6. Flowchart of QSPI Initialization Operation

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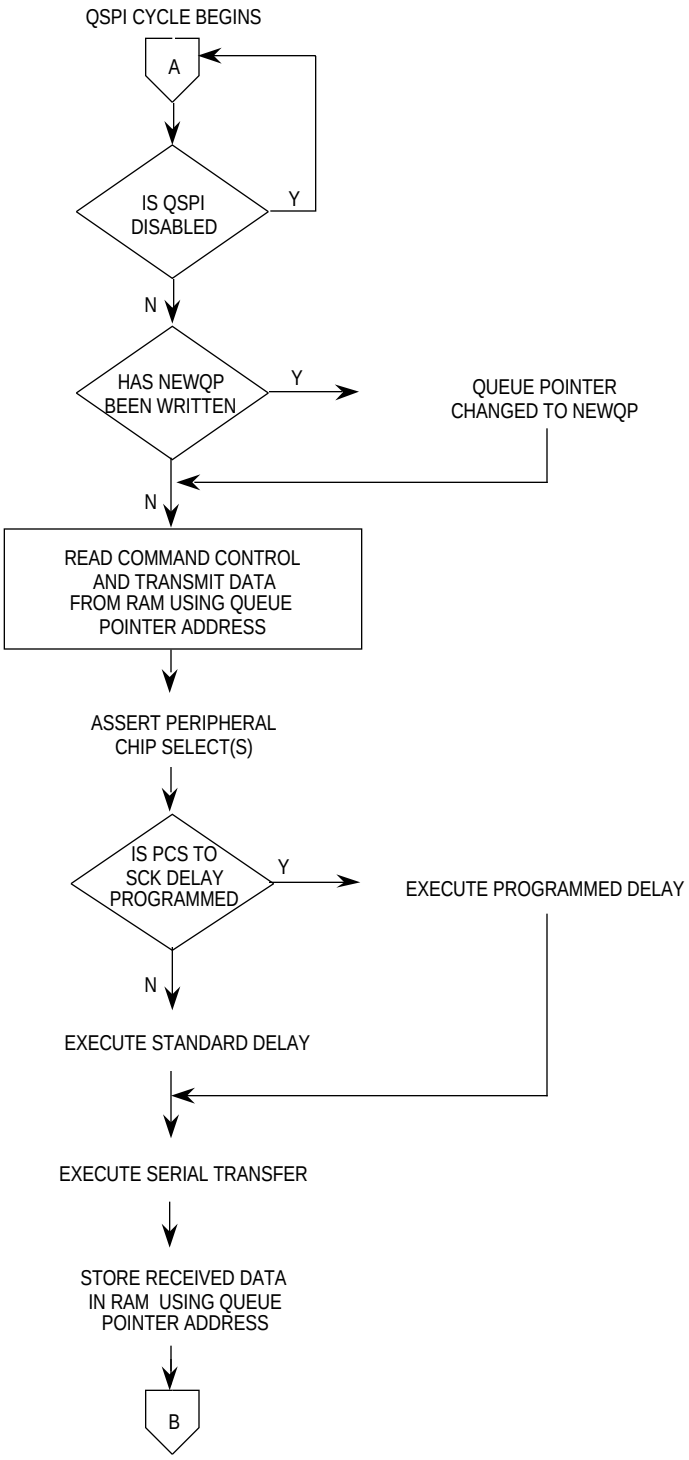

Figure 9-7. Flowchart of QSPI Master Operation (1 of 3)

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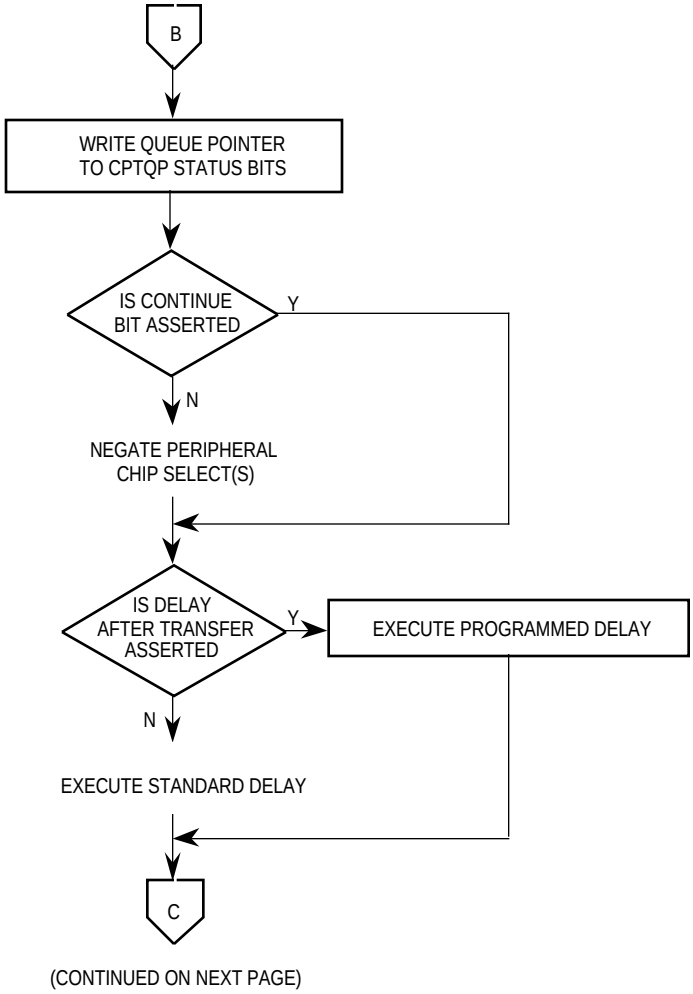

Figure 9-7. Flowchart of QSPI Master Operation (2 of 3)

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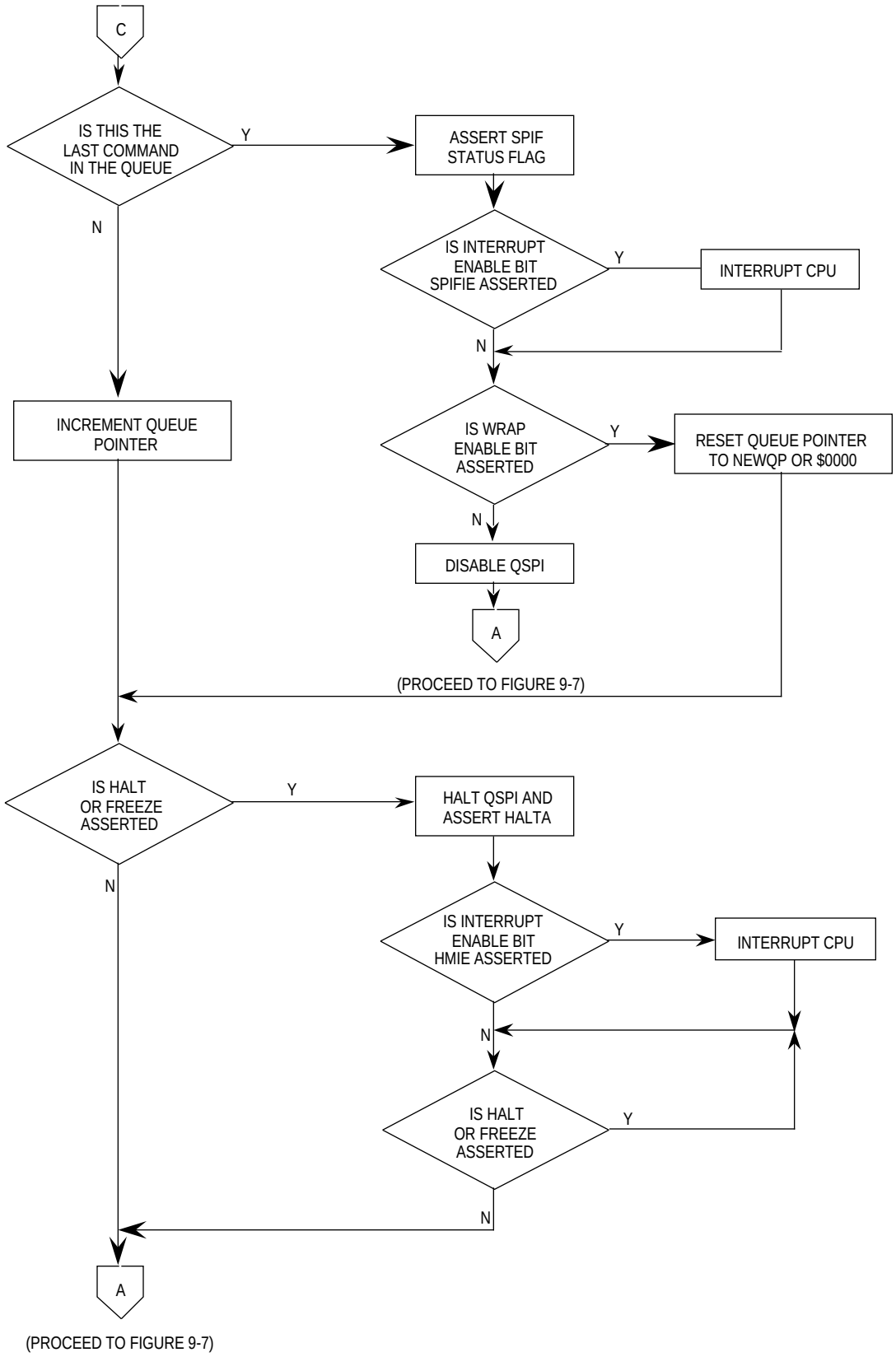

Figure 9-7. Flowchart of QSPI Master Operation (3 of 3)

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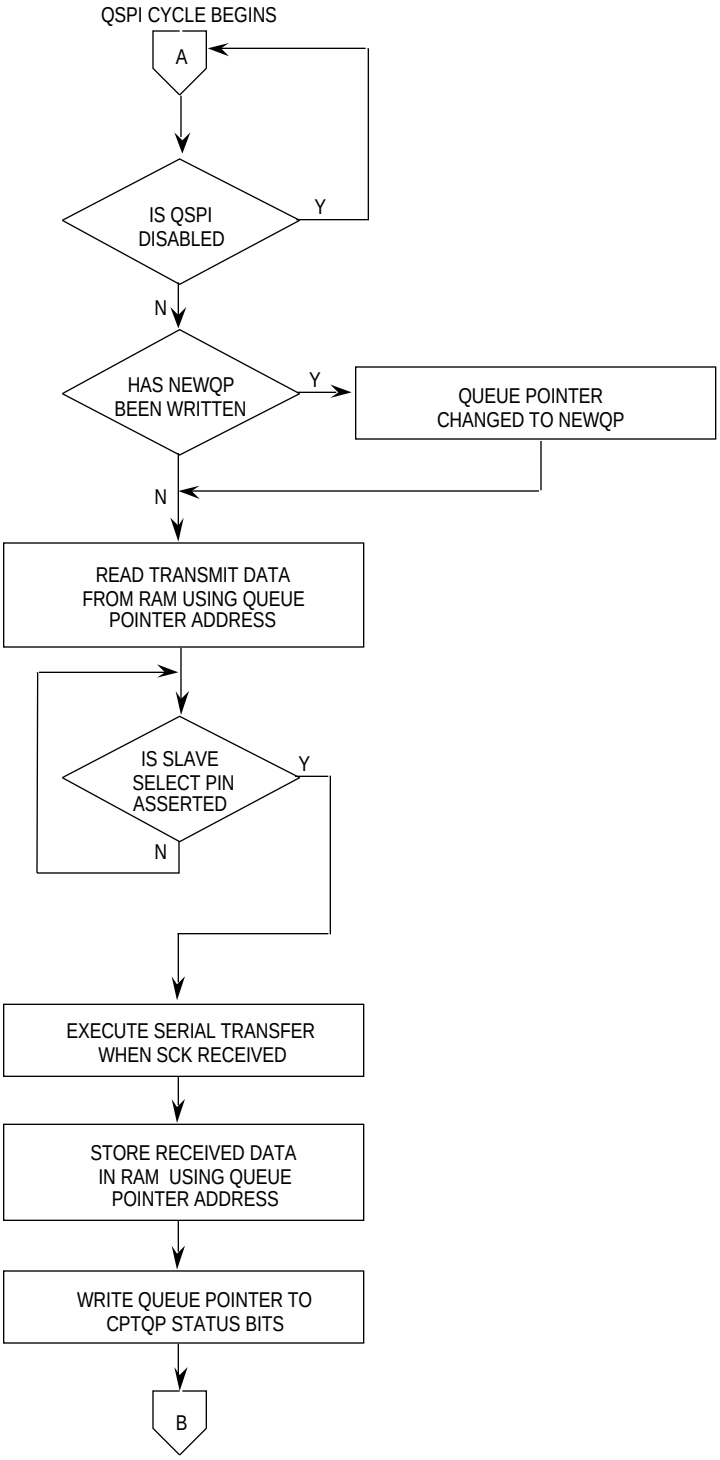

Figure 9-8. Flowchart of QSPI Slave Operation (1 of 2)

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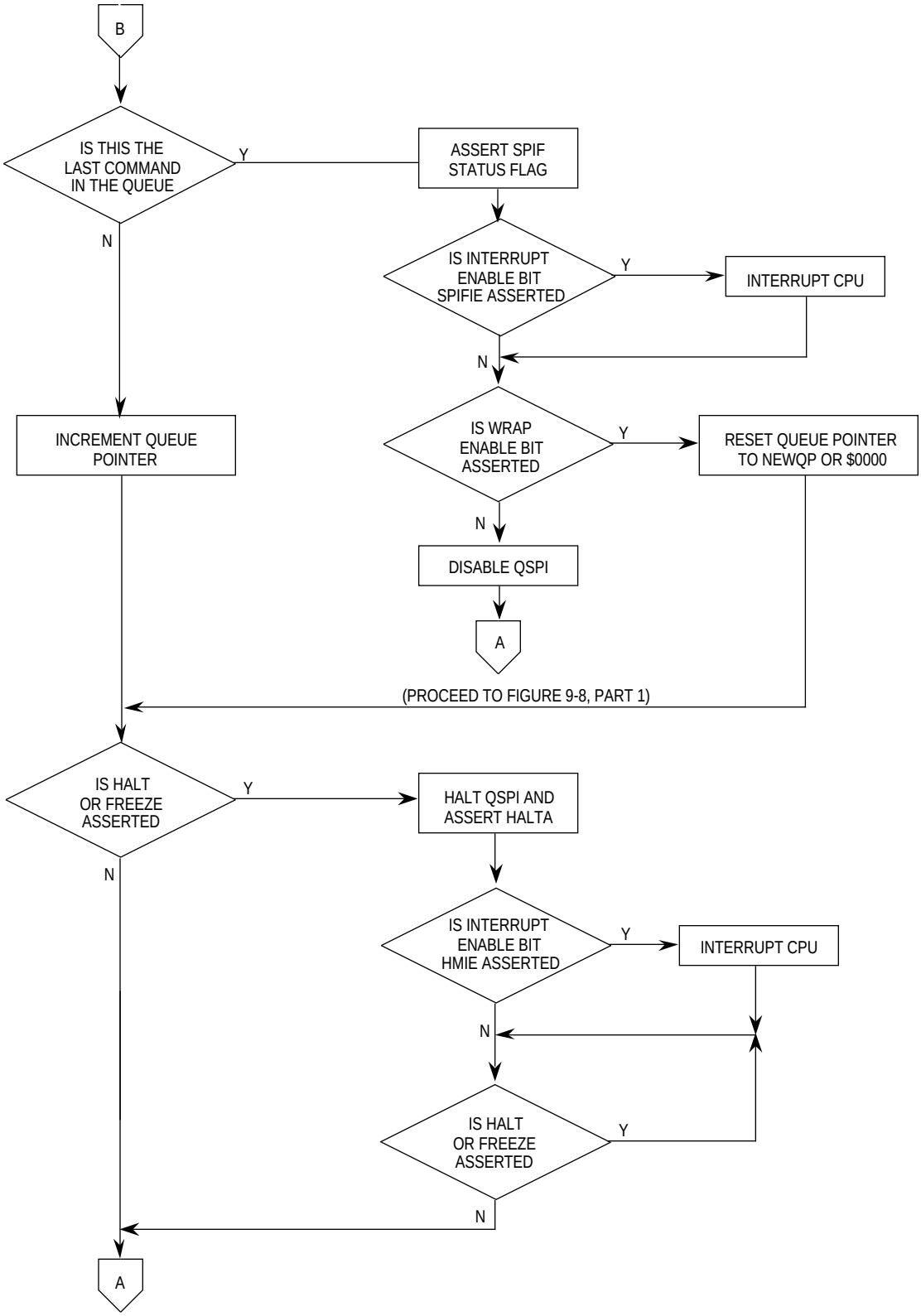

Figure 9-8. Flowchart of QSPI Slave Operation (2 of 2)

Although the QSPI inherently supports multimaster operation, no special arbitration mechanism is provided. The user is given a mode fault flag (MODF) to indicate a request

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for SPI master arbitration; however, the system software must implement the arbitration. Note that unlike previous SPI systems, e.g., on the M68HC11 Family, MSTR is not cleared by a mode fault being set nor are the QSPI pin output drivers disabled; however, the QSPI is disabled when software clears SPE in QSPI register SPCR1.

Normally, the SPI bus performs simultaneous bidirectional synchronous transfers. The serial clock on the SPI bus master supplies the clock signal (SCK) to time the transfer of the bits. Four possible combinations of clock phase and polarity may be employed.

Data is transferred with the most significant bit first. The number of bits transferred per command defaults to eight, but may be programmed to a value from 8–16 bits, using the BITSE field.

Typically, outputs used for the SPI bus are not open drain unless multiple SPI masters are in the system. If needed, WOMQ in S PCR0 may be set to provide open-drain outputs. An external pullup resistor should be used on each output bus line. WOMQ affects all QSPI pins regardless of whether they are assigned to the QSPI or used as general-purpose I/O.

9.5.5.1 MASTER MODE. When operated in master mode, the QSPI may initiate serial transfers. The QSPI is unable to respond to any externally initiated serial transfers. QSPM register QDDR should be written to direct the data flow on the QSPI pins used. The SCK pin should be configured as an output. Pins MOSI, PCS1/$\overline{\text{SS}}$, and PCS0 should be configured as outputs as necessary. MISO should be configured as an input if necessary.

QSPM register QPAR should be written to assign the necessary bits to the QSPI. The pins necessary for master mode operation are MISO and/or MOSI, SCK, and one or more of the PCS pins, depending on the number of external peripheral chips to be selected. MISO is used as the data input pin in master mode, and MOSI is used as the data output pin in master mode. Either or both may be necessary, depending on the particular application. SCK is the serial clock output in master mode.

PCS1/$\overline{\text{SS}}$ and PCS0 are the select pins used to select external SPI peripheral chips for a serial transfer initiated by the QSPI. These pins operate as either active-high or active-low chip selects. Other considerations for initialization are prescribed in **9.4.1 Overall QSPM Configuration Summary**.

9.5.5.1.1 Master Mode Operation. After reset, the QSPM registers and the QSPI control registers must be initialized as described above. In addition to the command control segment, the transmit data segment may, depending upon the application, need to be initialized. If meaningful data is to be sent out from the QSPI, the user should write the data to the transmit data segment before enabling the QSPI.

Shortly after SPE is set, the QSPI commences operation at the address indicated by NEWQP. The QSPI transmits the data found in the transmit data segment at the address indicated by NEWQP, and the QSPI stores received data in the receive data segment at the address indicated by NEWQP. Data is transferred synchronously with the internally generated SCK.

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Transmit data is loaded into the data serializer (refer to **9.5.4.4 QSPI Control Register 3 (SPCR3)**). The QSPI employs control bits, CPHA and CPOL, to determine which SCK edge the MISO pin uses to latch incoming data and which edge the MOSI pin uses to start driving the outgoing data. SPBR of SPCR0 determines the baud rate of SCK. DSCK and DSCKL determine any peripheral chip selects valid to SCK start delay.

The number of bits transferred is determined by BITSE and BITS fields. Two options are available: the user may use the default value of 8 bits, or the user may program the length from 8–16 bits, inclusive.

Once the proper number of bits are transferred, the QSPI stores the received data in the receive data segment, stores the internal working queue pointer value in CPTQP, increments the internal working queue pointer, and loads the next data required for transfer from the queue. The internal working queue pointer address is the next command executed unless the CPU writes a new value first.

If CONT is set and the peripheral-chip-select pattern does not change between the current and the pending transfer, the PCS pins are continuously driven in their designated state during and between both serial transfers. If the peripheral-chip-select pattern changes, then the first pattern is driven out during execution of the first transfer, followed by the QSPI switching to the next pattern of the second transfer when execution of the second transfer begins. If CONT is clear, the deselected peripheral-chip-select values (found in register QPDR) are driven out between transfers.

DT causes a delay to occur after the specified serial transfer is completed. The length of the delay is determined by DTL. When DT is clear, the standard delay (1 µs at a 16.78-MHz system clock) occurs after the specified serial transfer is completed.

9.5.5.1.2 Master Wraparound Mode. When the QSPI reaches the end of the queue, it always sets the SPIF flag whether wraparound mode is enabled or disabled. An optional interrupt to the CPU is generated when SPIF is asserted. At this point, the QSPI clears SPE and stops unless wraparound mode is enabled. A description of SPIFIE may be found in **9.5.4.3 QSPI Control Register 2 (SPCR2).**

In wraparound mode, the QSPI cycles through the queue continuously. Each time the end of the queue is reached, the SPIF flag is set. If the CPU fails to clear SPIF it remains set, and the QSPI continues to send interrupt requests to the CPU (assuming SPIFIE is set). The user may avoid causing CPU interrupts by clearing SPIFIE. As SPIFIE is buffered, clearing it after the SPIF flag is asserted does not immediately stop the CPU interrupts, but only prevents future interrupts from this source. To clear the current interrupt, the CPU must read QSPI register SPSR with SPIF asserted, followed by a write to SPSR with a zero in SPIF (clear SPIF).

Execution continues in wraparound mode, even while the QSPI is requesting interrupt service from the CPU. The internal working queue pointer increments to the next address, and the commands are executed again. SPE is not cleared by the QSPI. New receive data overwrites previously received data in the receive data segment.

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Wraparound mode is properly exited in two ways: a) The CPU may disable wraparound mode by clearing WREN. The next time the end of the queue is reached, the QSPI sets SPIF, clears SPE, and stops; b) The CPU sets HALT. This second method halts the QSPI after the current transfer is completed, allowing the CPU to negate SPE. The CPU can immediately stop the QSPI by clearing SPE; however, this method is not recommended as it causes the QSPI to abort a serial transfer in process.

9.5.5.2 SLAVE MODE. When operating in slave mode, the QSPI may respond to externally initiated serial transfers. The QSPI is unable to initiate any serial transfers. Slave mode is typically used when multiple devices are in an SPI bus network, because only one device can be the SPI master (in master mode) at any given time.

QSPM register QDDR should be written to direct data flow on the QSPI pins used. The MISO and MOSI pins, if needed, should be configured as output and input, respectively. Pins SCK and PCS0/$\overline{SS}$ should be configured as inputs.

QSPM register QPAR should be written to assign the necessary bits to the QSPI. The pins necessary for slave mode operation are MISO and/or MOSI, SCK, and PCS0/$\overline{SS}$. MISO is the data output pin in slave mode, and MOSI is the data input pin in slave mode. Either or both may be necessary depending on the particular application. The serial clock (SCK) is the slave clock input in slave mode. PCS0/$\overline{SS}$ is the slave select pin used to select the QSPI for a serial transfer by the external SPI bus master when the QSPI is in slave mode. The external bus master selects the QSPI by driving PCS0/$\overline{SS}$ low. The command control segment is not implemented in slave mode; therefore, the CPU does not need to initialize it. This segment of the QSPI RAM and any other unused segments may be employed by the CPU as general-purpose RAM. Other considerations for initialization are prescribed in **9.4.1 Overall QSPM Configuration Summary.**

9.5.5.2.1 Description of Slave Operation. After reset, the QSPM registers and the QSPI control registers must be initialized as described above. Although the command control segment is not used, the transmit and receive data segments may, depending upon the application, need to be initialized. If meaningful data is to be sent out from the QSPI, the user should write the data to the transmit data segment before enabling the QSPI.

If SPE is set and MSTR is not set, a low state on the slave select (PCS0/$\overline{SS}$) pin commences slave mode operation at the address indicated by NEWQP. The QSPI transmits the data found in the transmit data segment at the address indicated by NEWQP, and the QSPI stores received data in the receive data segment at the address indicated by NEWQP. Data is transferred in response to an external slave clock input at the SCK pin.

Because the command control segment is not used, the command control bits and peripheral-chip-select codes have no effect in slave mode operation. The QSPI does not drive either of the two peripheral chip selects as outputs. PCS0/$\overline{SS}$ is used as an input.

Although CONT cannot be used in slave mode, a provision is made to enable receipt of more than 16 data bits. While keeping the QSPI selected (PCS0/$\overline{SS}$ is held low), the QSPI stores the number of bits, designated by BITS, in the current receive data segment

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address, increments NEWQP, and continues storing the remaining bits (up to the BITS value) in the next receive data segment address.

As long as PCS0/$\overline{SS}$ remains low, the QSPI continues to store the incoming bit stream in sequential receive data segment addresses, until either the value in BITS is reached or the end-of-queue address is used with wraparound mode disabled. When the end of the queue is reached, the SPIF flag is asserted, optionally causing an interrupt. If wraparound mode is disabled, any additional incoming bits are ignored. If wraparound mode is enabled, storing continues at either address $0 or the address of NEWQP, depending on the WRTO value.

When using this capability to receive a long incoming data stream, the proper delay between transfers must be used. The QSPI requires time, approximately 1 µs at 16.78-MHz system clock, to prefetch the next transmit RAM entry for the next transfer. Therefore, the user may select a baud rate that provides at least a 1 µs delay between successive transfers to ensure no loss of incoming data. If the system clock is operating at a slower rate, the delay between transfers must be increased proportionately.

Because the BITSE option in the command control segment is no longer available, BITS sets the number of bits to be transferred for all transfers in the queue until the CPU changes the BITS value. As mentioned above, until PCS0/$\overline{SS}$ is negated (brought high), the QSPI continues to shift one bit for each pulse of SCK. If PCS0/$\overline{SS}$ is negated before the proper number of bits (according to BITS) is received, the QSPI, the next time it is selected, resumes storing bits in the same receive data segment address where it left off. If more than 16 bits are transferred before negating the PCS0/$\overline{SS}$, the QSPI stores the number of bits indicated by BITS in the current receive data segment address, then increments the address and continues storing as described above. Note that PCS0/$\overline{SS}$ does not necessarily have to be negated between transfers.

Once the proper number of bits (designated by BITS) are transferred, the QSPI stores the received data in the receive data segment, stores the internal working queue pointer value in CPTQP, increments the internal working queue pointer, and loads the new transmit data from the transmit data segment into the data serializer. The internal working queue pointer address is used the next time PCS0/$\overline{SS}$ is asserted, unless the CPU writes to the NEWQP first.

The DT and DSCK command control bits are not used in slave mode. As a slave, the QSPI does not drive the clock line nor the chip-select lines and, therefore, does not generate a delay.

In slave mode, the QSPI shifts out the data in the transmit data segment. The transmit data is loaded into the data serializer (refer to Figure 9-9) for transmission. This serializer shifts the 16 bits of data out in sequence, most significant bit first, as clocked by the incoming SCK signal. The QSPI uses CPHA and CPOL to determine which incoming SCK edge the MOSI pin uses to latch incoming data, and which edge the MISO pin uses to drive the data out.

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The QSPI transmits and receives data until reaching the end of the queue (defined as a match with the address in ENDQP), regardless of whether PCS0/$\overline{SS}$ remains selected or is toggled between serial transfers. Receiving the proper number of bits causes the received data to be stored. The QSPI always transmits as many bits as it receives at each queue address, until the BITS value is reached or PCS0/$\overline{SS}$ is negated.

9.5.5.2.2 Slave Wraparound Mode. When the QSPI reaches the end of the queue, it always sets the SPIF flag, whether wraparound mode is enabled or disabled. An optional interrupt to the CPU is generated when SPIF is asserted. At this point, the QSPI clears SPE and stops unless wraparound mode is enabled. A description of SPIFIE bit can be found in **9.5.4.3 QSPI Control Register 2 (SPCR2)**.

In wraparound mode, the QSPI cycles through the queue continuously. Each time the end of the queue is reached, the SPIF flag is set. If the CPU fails to clear SPIF, it remains set, and the QSPI continues to send interrupt requests to the CPU (assuming SPIFIE is set). The user may avoid causing CPU interrupts by clearing SPIFIE. As SPIFIE is buffered, clearing it after the SPIF flag is asserted does not immediately stop the CPU interrupts, but only prevents future interrupts from this source. To clear the current interrupt, the CPU must read QSPI register SPSR with SPIF asserted, followed by a write to SPSR with zero in SPIF (clear SPIF).

Execution continues in wraparound mode even while the QSPI is requesting interrupt service from the CPU. The internal working queue pointer is incremented to the next address and the commands are executed again. SPE is not cleared by the QSPI. New receive data overwrites previously received data located in the receive-data segment.

Wraparound mode is properly exited in two ways: a) The CPU may disable wraparound mode by clearing WREN. The next time end of the queue is reached, the QSPI sets SPIF, clears SPE, and stops; and, b) The CPU sets HALT. This second method halts the QSPI after the current transfer is completed, allowing the CPU to negate SPE. The CPU can immediately stop the QSPI by clearing SPE; however, this method is not recommended, as it causes the QSPI to abort a serial transfer in process.

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SECTION 10
IEEE 1149.1 TEST ACCESS PORT

The MC68341 includes dedicated user-accessible test logic that is fully compatible with the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*. Problems associated with testing high-density circuit boards have led to development of this proposed standard under the sponsorship of the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The MC68341 implementation supports circuit-board test strategies based on this standard.

The test logic includes a test access port (TAP) consisting of four dedicated signal pins, a 16-state controller, an instruction register, and two test data registers. A boundary scan register links all device signal pins into a single shift register. The test logic, implemented using static logic design, is independent of the device system logic. The MC68341 implementation provides the following capabilities:

a. Perform boundary scan operations to test circuit-board electrical continuity
b. Sample the MC68341 system pins during operation and transparently shift out the result in the boundary scan register
c. Bypass the MC68341 for a given circuit-board test by effectively reducing the boundary scan register to a single bit
d. Disable the output drive to pins during circuit-board testing

NOTE

Certain precautions must be observed to ensure that the IEEE 1149.1 test logic does not interfere with nontest operation. See **10.6 Non-IEEE 1149.1 Operation** for details.

10.1 OVERVIEW

NOTE

This description is not intended to be used without the supporting IEEE 1149.1 document.

The discussion includes those items required by the standard and provides additional information specific to the MC68341 implementation. For internal details and applications of the standard, refer to the IEEE 1149.1 document.

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An overview of the MC68341 implementation of IEEE 1149.1 is shown in Figure 10-1. The MC68341 implementation includes a 16-state controller, a 3-bit instruction register, and two test registers (a 1-bit bypass register and a 155-bit boundary scan register). This implementation includes a dedicated TAP consisting of the following signals:

TCK — a test clock input to synchronize the test logic
TMS — a test mode select input (with an internal pullup resistor) that is sampled on the rising edge of TCK to sequence the TAP controller's state machine
TDI — a test data input (with an internal pullup resistor) that is sampled on the rising edge of TCK.
TDO — a three-state test data output that is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.

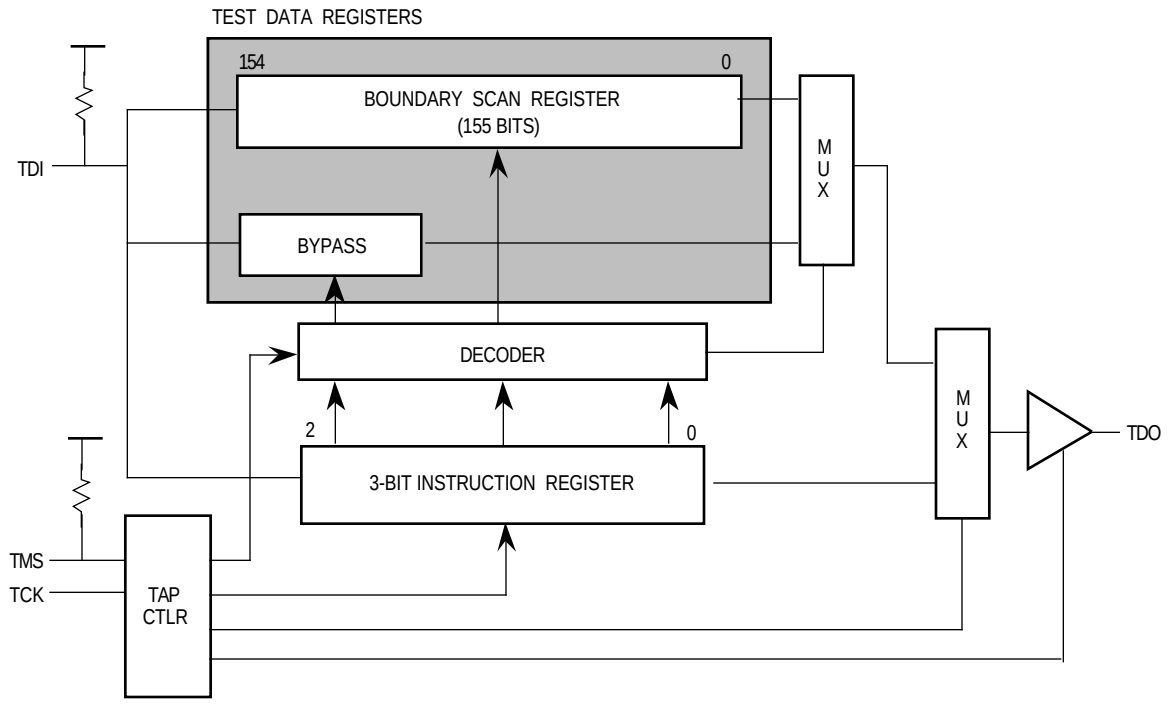

Figure 10-1. Test Access Port Block Diagram

10.2 TAP CONTROLLER

The TAP controller is responsible for interpreting the sequence of logical values on the TMS signal. It is a synchronous state machine that controls the operation of the JTAG logic. The state machine is shown in Figure 10-2; the value shown adjacent to each arc represents the value of the TMS signal sampled on the rising edge of the TCK signal. For a description of the TAP controller states, please refer to the IEEE 1149.1 document.

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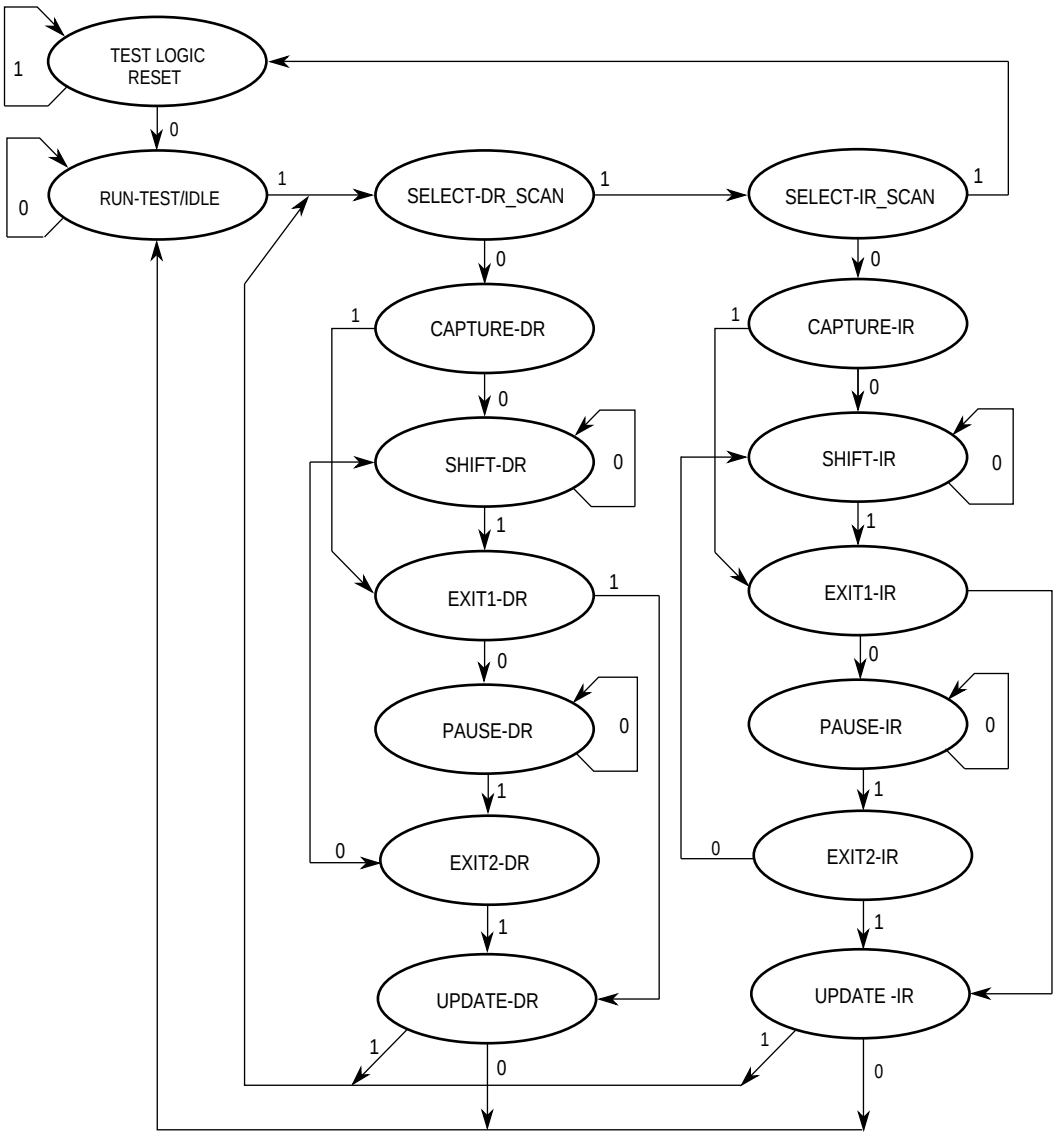

Figure 10-2. TAP Controller State Machine

10.3 BOUNDARY SCAN REGISTER

The MC68341 IEEE 1149.1 implementation has a 155-bit boundary scan register. This register contains bits for all device signal and clock pins and associated control signals. The XTAL, X2, XFC, BSW, EXTAL, and V_{BATT} pins are associated with analog signals and are not included in the boundary scan register.

All MC68341 bidirectional pins, except the open-drain I/O pins ($\overline{DONE1}$, $\overline{DONE2}$, $\overline{HALT}$, and $\overline{RESET}$) and QSM pins (QSCLK, MISO, MOSI, $\overline{PCS1}$, $\overline{PCS0}$) have a single register bit for pin data and an associated control bit in the boundary scan register. All open drain I/O and QSM pins have two register bits, input and output, for pin data and no associated control bit. To ensure proper operation, the open-drain pins require external pullups. Twenty-seven control bits in the boundary scan register define the output enable signal for

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associated groups of bidirectional and three-state pins. The control bits and their bit positions are listed in Table 10-1.

Table 10-1. Boundary Scan Control Bits

Name	Bit Number	Name	Bit Number	Name	Bit Number
ifetch.ctl	152	ab31.ctl	114	berr.ctl	97
modck.ctl	149	ab30.ctl	112	ab.ctl	96
irq1.ctl	131	ab29.ctl	110	cs0.ctl	74
irq2.ctl	129	ab28.ctl	108	tout.ctl	44
irq3.ctl	127	ab27.ctl	106	pcs0.ctl	14
irq4.ctl	125	ab26.ctl	104	pcs1.ctl	11
irq5.ctl	123	ab25.ctl	102	miso.ctl	8
irq6.ctl	121	ab24.ctl	100	mosi.ctl	5
irq7.ctl	119	db.ctl	98	sck.ctl	2

Boundary scan bit definitions are shown in Table 10-2. The first column in Table 10-2 defines the bit's ordinal position in the boundary scan register. The shift register bit nearest TDO (i.e., first to be shifted out) is defined as bit 0; the last bit to be shifted out is 154.

The second column references one of the five MC68341 cell types depicted in Figures 10-3–10-7, which describe the cell structure for each type.

The third column lists the pin name for all pin-related bits or defines the name of bidirectional control register bits. The active level of the control bits (i.e., output driver on) is defined by the last digit of the cell type listed for each control bit. For example, the active level for irq2.ctl (bit 129) is logic zero since the cell type is IO.Ctl0. The active level for ab.ctl (bit 96) is logic one, since the cell type is IO.Ctl1. IO.Ctl0 (see Figure 10-6) differs from IO.Ctl1 (see Figure 10-5) by an inverter in the output enable path.

The fourth column lists the pin type: TS-Output indicates a three-state output pin, I/O indicates a bidirectional pin, and OD-I/O denotes an open-drain bidirectional pin. An open-drain output pin has two states: off (high impedance) and logic zero.

The last column indicates the associated boundary scan register control bit for bidirectional, three-state, and open-drain output pins.

Bidirectional pins include a single scan bit for data (IO.Cell) as depicted in Figure 10-7. These bits are controlled by one of the two bits shown in Figures 10-5 and 10-6. The value of the control bit determines whether the bidirectional pin is an input or an output. One or more bidirectional data bits can be serially connected to a control bit as shown in Figure 10-8. Note that, when sampling the bidirectional data bits, the bit data can be interpreted only after examining the IO control bit to determine pin direction.

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Table 10-2. Boundary Scan Bit Definitions

Bit Num	Cell Type	Pin/Cell Name	Pin Type	Output CTL Cell
154	O.Latch	FREEZE	Output	—
153	I.Pin	$\overline{\text{BKPT}}$	Input	—
152	IO.Ctl0	ifetch.ctl	—	—
151	IO.Cell	$\overline{\text{IFETCH}}$	I/O*	ifetch.ctl
150	O.Latch	$\overline{\text{IPIPE}}$	Output	—
149	IO.Ctl0	modck.ctl	—	—
148	IO.Cell	MODCK	I/O	modck.ctl
147	I.pin	SEXTCLK	Input	—
146	O.Latch	CLKOUT	Output	—
145	I.Pin	$\overline{\text{RESET}}$	OD-I/O	—
144	O.Latch	$\overline{\text{RESET}}$	OD-I/O	—
143	I.Pin	$\overline{\text{HALT}}$	OD-I/O	—
142	O.Latch	$\overline{\text{HALT}}$	OD-I/O	—
141	IO.Cell	$\overline{\text{BERR}}$	I/O**	berr.ctl
140	I.pin	$\overline{\text{BR}}$	Input	—
139	O.Latch	$\overline{\text{BG}}$	Output	—
138	I.Pin	$\overline{\text{BGACK}}$	Input	—
137	IO.Cell	$\overline{\text{AS}}$	I/O*	ab.ctl
136	IO.Cell	$\overline{\text{DS}}$	I/O*	ab.ctl
135	IO.Cell	SIZ0	I/O*	ab.ctl
134	IO.Cell	SIZ1	I/O*	ab.ctl
133	IO.Cell	R/$\overline{\text{W}}$	I/O*	ab.ctl
132	O.Latch	$\overline{\text{RMC}}$	TS-Output	ab.ctl
131	IO.Ctl0	irq1.ctl	—	—
130	IO.Cell	$\overline{\text{IRQ1}}$	I/O	irq1.ctl
129	IO.Ctl0	irq2.ctl	—	—
128	IO.Cell	$\overline{\text{IRQ2}}$	I/O	irq2.ctl
127	IO.Ctl0	irq3.ctl	—	—
126	IO.Cell	$\overline{\text{IRQ3}}$	I/O	irq3.ctl
125	IO.Ctl0	irq4.ctl	—	—
124	IO.Cell	$\overline{\text{IRQ4}}$	I/O	irq4.ctl
123	IO.Ctl0	irq5.ctl	—	—
122	IO.Cell	$\overline{\text{IRQ5}}$	I/O	irq5.ctl
121	IO.Ctl0	irq6.ctl	—	—
120	IO.Cell	$\overline{\text{IRQ6}}$	I/O	irq6.ctl

Bit Num	Cell Type	Pin/Cell Name	Pin Type	Output CTL Cell
119	IO.Ctl0	irq7.ctl	—	—
118	IO.Cell	$\overline{\text{IRQ7}}$	I/O	irq7.ctl
117	IO.Cell	$\overline{\text{DSACK1}}$	I/O**	berr.ctl
116	IO.Cell	$\overline{\text{DSACK0}}$	I/O**	berr.ctl
115	IO.Cell	A0	I/O*	ab.ctl
114	IO.Ctl0	ab31.ctl	—	—
113	IO.Cell	A31	I/O	ab31.ctl
112	IO.Ctl0	ab30.ctl	—	—
111	IO.Cell	A30	I/O	ab30.ctl
110	IO.Ctl0	ab29.ctl	—	—
109	IO.Cell	A29	I/O	ab29.ctl
108	IO.Ctl0	ab28.ctl	—	—
107	IO.Cell	A28	I/O	ab28.ctl
106	IO.Ctl0	ab27.ctl	—	—
105	IO.Cell	A27	I/O	ab27.ctl
104	IO.Ctl0	ab26.ctl	—	—
103	IO.Cell	A26	I/O	ab26.ctl
102	IO.Ctl0	ab25.ctl	—	—
101	IO.Cell	A25	I/O	ab25.ctl
100	IO.Ctl0	ab24.ctl	—	—
99	IO.Cell	A24	I/O	ab24.ctl
98	IO.Ctl1	db.ctl	—	—
97	IO.Ctl0	berr.ctl	—	—
96	IO.Ctl1	ab.ctl	—	—
95	IO.Cell	D15	I/O	db.ctl
94	IO.Cell	D14	I/O	db.ctl
93	IO.Cell	D13	I/O	db.ctl
92	IO.Cell	D12	I/O	db.ctl
91	IO.Cell	D11	I/O	db.ctl
90	IO.Cell	D10	I/O	db.ctl
89	IO.Cell	D9	I/O	db.ctl
88	IO.Cell	D8	I/O	db.ctl
87	IO.Cell	D7	I/O	db.ctl
86	IO.Cell	D6	I/O	db.ctl
85	IO.Cell	D5	I/O	db.ctl

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Table 10-2. Boundary Scan Bit Definitions (Continued)

Bit Num	Cell Type	Pin/Cell Name	Pin Type	Output CTL Cell
84	IO.Cell	D4	I/O	db.ctl
83	IO.Cell	D3	I/O	db.ctl
82	IO.Cell	D2	I/O	db.ctl
81	IO.Cell	D1	I/O	db.ctl
80	IO.Cell	D0	I/O	db.ctl
79	O.Latch	$\overline{68KAS}$	TS-Output	ab.ctl
78	O.Latch	$\overline{LWE}$	TS-Output	ab.ctl
77	O.Latch	$\overline{UWE}$	TS-Output	ab.ctl
76	O.Latch	$\overline{LDS}$	TS-Output	ab.ctl
75	O.Latch	$\overline{UDS}$	TS-Output	ab.ctl
74	IO.Ctl0	cs0.ctl	—	—
73	IO.Cell	$\overline{CS0}$	I/O*	cs0.ctl
72	O.Latch	$\overline{CS1}$	TS-Output	ab.ctl
71	O.Latch	$\overline{CS2}$	TS-Output	ab.ctl
70	O.Latch	$\overline{CS3}$	TS-Output	ab.ctl
69	O.Latch	$\overline{CS4}$	TS-Output	ab.ctl
68	O.Latch	$\overline{CS5}$	TS-Output	ab.ctl
67	O.Latch	$\overline{CS6}$	TS-Output	ab.ctl
66	O.Latch	$\overline{CS7}$	TS-Output	ab.ctl
65	I.Pin	$\overline{DONE2}$	OD-I/O	—
64	O.Latch	$\overline{DONE2}$	OD-I/O	—
63	O.Latch	$\overline{DACK2}$	Output	—
62	I.Pin	$\overline{DREQ2}$	Input	—
61	I.Pin	$\overline{DONE1}$	OD-I/O	—
60	O.Latch	$\overline{DONE1}$	OD-I/O	—
59	O.Latch	$\overline{DACK1}$	Output	—
58	I.Pin	$\overline{DREQ1}$	Input	—
57	I.Pin	X1	Input	—
56	I.Pin	SCLK	Input	—
55	I.Pin	$\overline{CTSB}$	Input	—
54	O.Latch	$\overline{RTSB}$	Output	—
53	O.Latch	TxDB	Output	—
52	I.Pin	RxDB	Input	—
51	O.Latch	$\overline{TxRDYA}$	Output	—
50	O.Latch	$\overline{RxRDYA}$	Output	—

Bit Num	Cell Type	Pin/Cell Name	Pin Type	Output CTL Cell
49	I.Pin	$\overline{CTSA}$	Input	—
48	O.Latch	$\overline{RTSA}$	Output	—
47	O.Latch	TxDA	Output	—
46	I.Pin	RxDA	Input	—
45	I.Pin	TIN	Input	—
44	IO.ctl0	tout.ctl	—	—
43	O.Latch	TOUT	TS-Output	tout.ctl
42	I.Pin	$\overline{TGATE}$	Input	—
41	IO.cell	A1	I/O*	ab.ctl
40	IO.cell	A2	I/O*	ab.ctl
39	IO.cell	A3	I/O*	ab.ctl
38	IO.cell	A4	I/O*	ab.ctl
37	IO.cell	A5	I/O*	ab.ctl
36	IO.cell	A6	I/O*	ab.ctl
35	IO.cell	A7	I/O*	ab.ctl
34	IO.cell	A8	I/O*	ab.ctl
33	IO.cell	A9	I/O*	ab.ctl
32	IO.cell	A10	I/O*	ab.ctl
31	IO.cell	A11	I/O*	ab.ctl
30	IO.cell	A12	I/O*	ab.ctl
29	IO.cell	A13	I/O*	ab.ctl
28	IO.cell	A14	I/O*	ab.ctl
27	IO.cell	A15	I/O*	ab.ctl
26	IO.cell	A16	I/O*	ab.ctl
25	IO.cell	A17	I/O*	ab.ctl
24	IO.cell	A18	I/O*	ab.ctl
23	IO.cell	A19	I/O*	ab.ctl
22	IO.cell	A20	I/O*	ab.ctl
21	IO.cell	A21	I/O*	ab.ctl
20	IO.cell	A22	I/O*	ab.ctl
19	IO.cell	A23	I/O*	ab.ctl
18	IO.cell	FC0	I/O*	ab.ctl
17	IO.cell	FC1	I/O*	ab.ctl
16	IO.cell	FC2	I/O*	ab.ctl
15	IO.cell	FC3	I/O*	ab.ctl

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Table 10-2. Boundary Scan Bit Definitions (Continued)

Bit Num	Cell Type	Pin/Cell Name	Pin Type	Output CTL Cell	Bit Num	Cell Type	Pin/Cell Name	Pin Type	Output CTL Cell
14	IO.ctl0	pcs0.ctl	—	—	6	O.Latch	MISO	I/O	miso.ctl
13	I.Pin	PCS0	I/O	—	5	IO.ctl0	mosi.ctl	—	—
12	O.Latch	PCS0	I/O	pcs0.ctl	4	I.Pin	MOSI	I/O	—
11	IO.ctl0	pcs1.ctl	—	—	3	O.Latch	MOSI	I/O	mosi.ctl
10	I.Pin	PCS1	I/O	—	2	IO.ctl0	sck.ctl	—	—
9	O.Latch	PCS1	I/O	pcs1.ctl	1	I.Pin	SCK	I/O	—
8	IO.ctl0	miso.ctl	—	—	0	O.Latch	SCK	I/O	sck.ctl
7	I.Pin	MISO	I/O	—					

NOTES:
The noted pins are implemented differently than defined in the signal definition description:
* Input during Motorola factory test
** Output during Motorola factory test

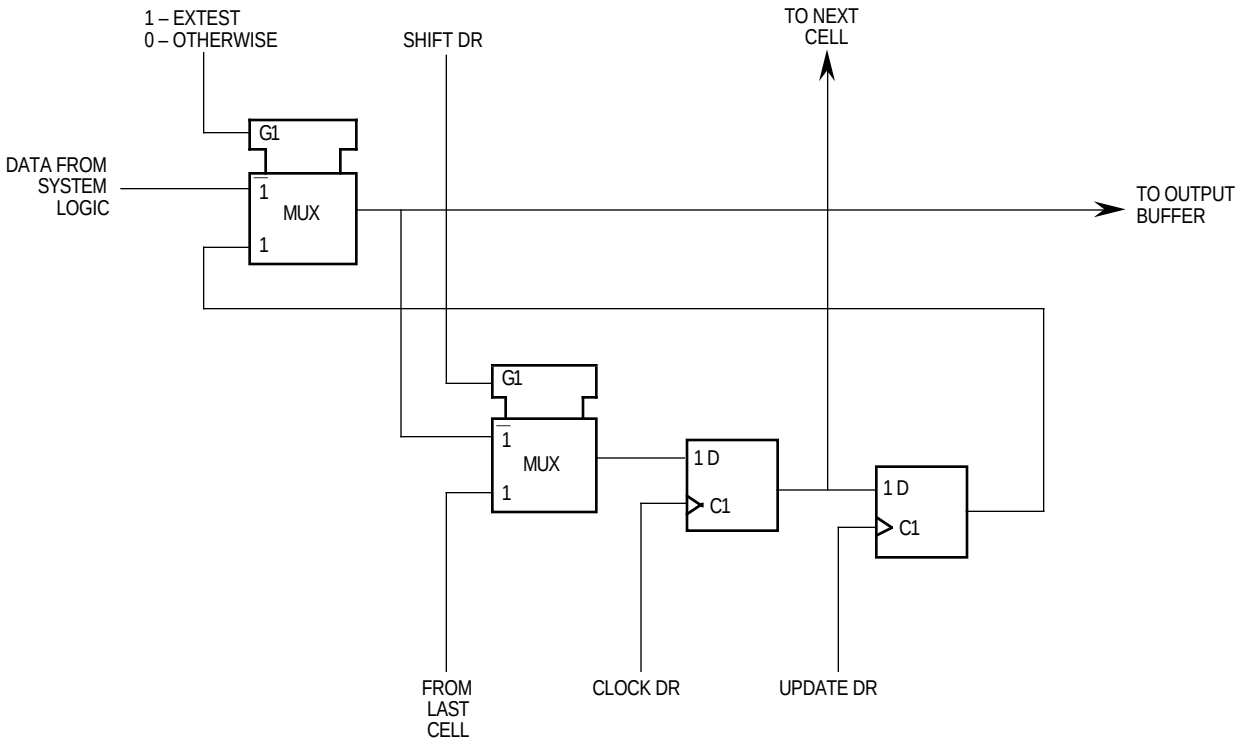

Figure 10-3. Output Latch Cell (O.Latch)

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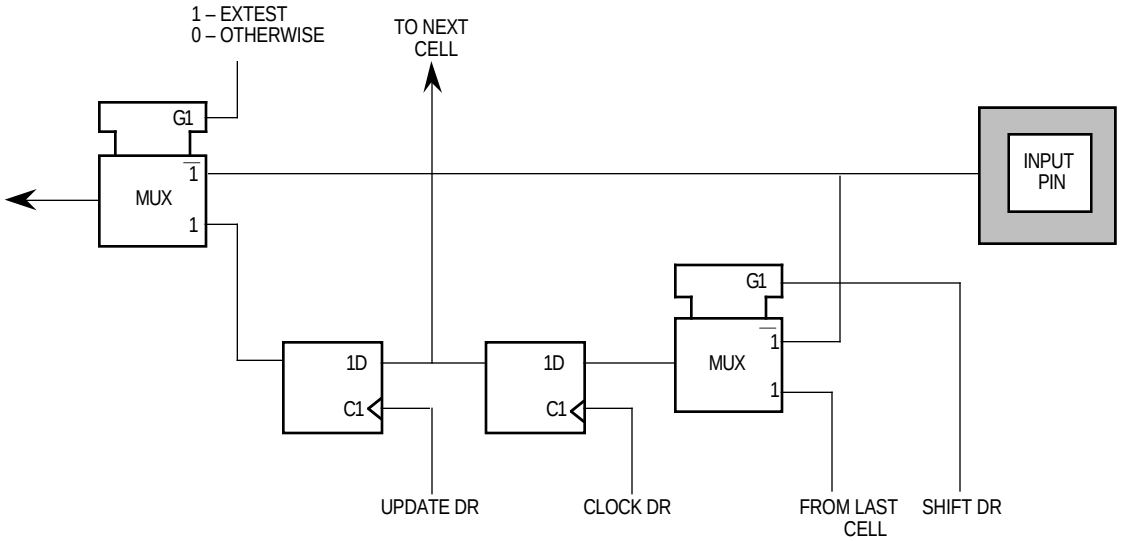

Figure 10-4. Input Pin Cell (I.Pin)

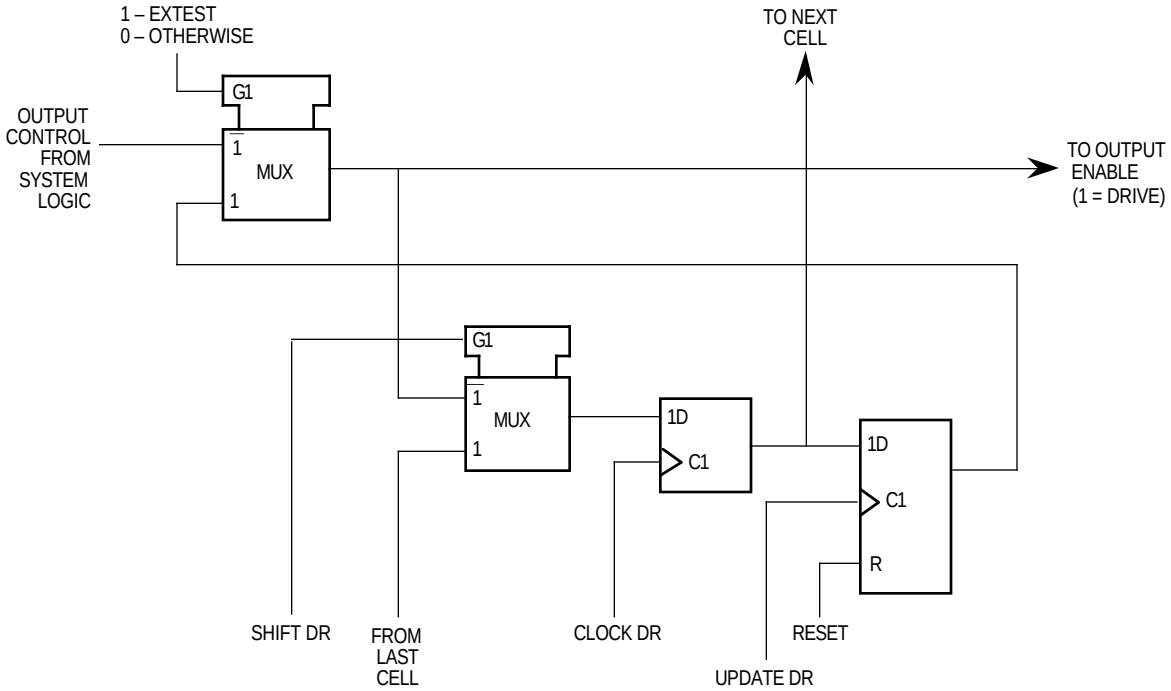

Figure 10-5. Active-High Output Control Cell (IO.Ctl1)

FIG. 9-4

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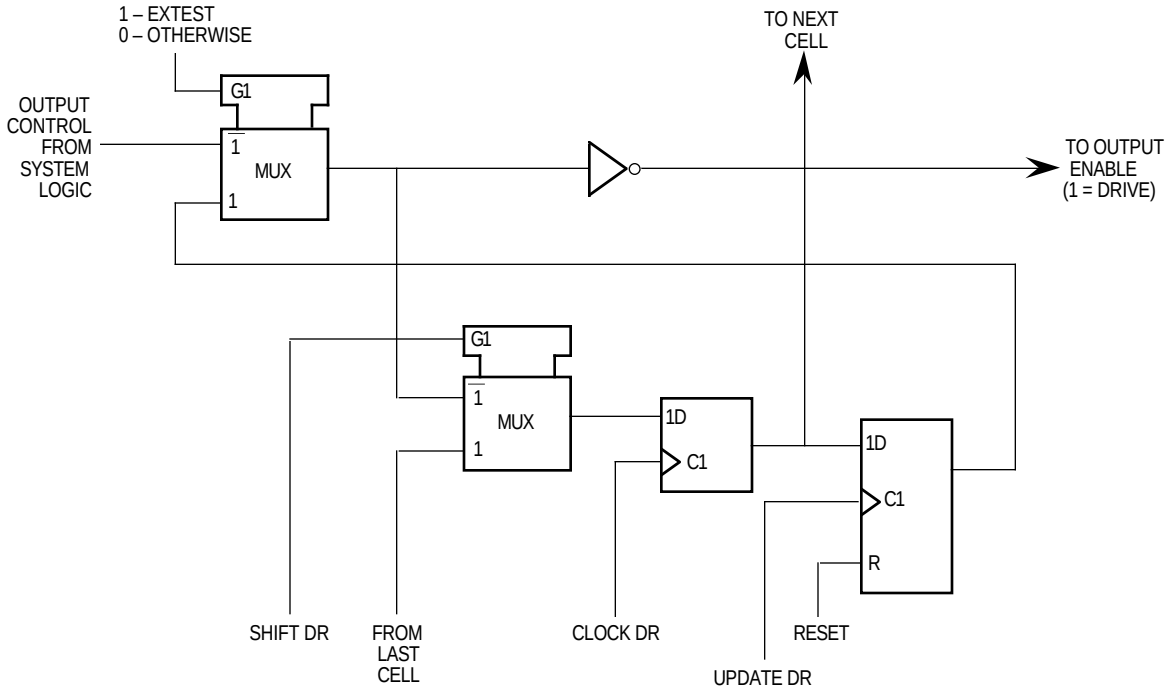

Figure 10-6. Active-Low Output Control Cell (IO.Ctl0)

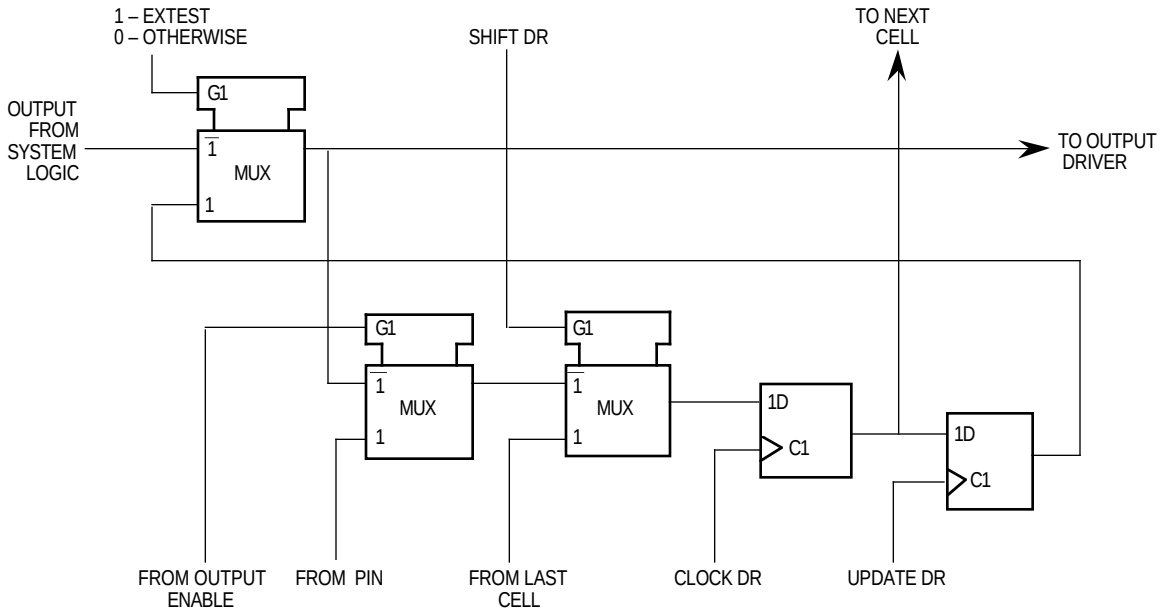

Figure 10-7. Bidirectional Data Cell (IO.Cell)

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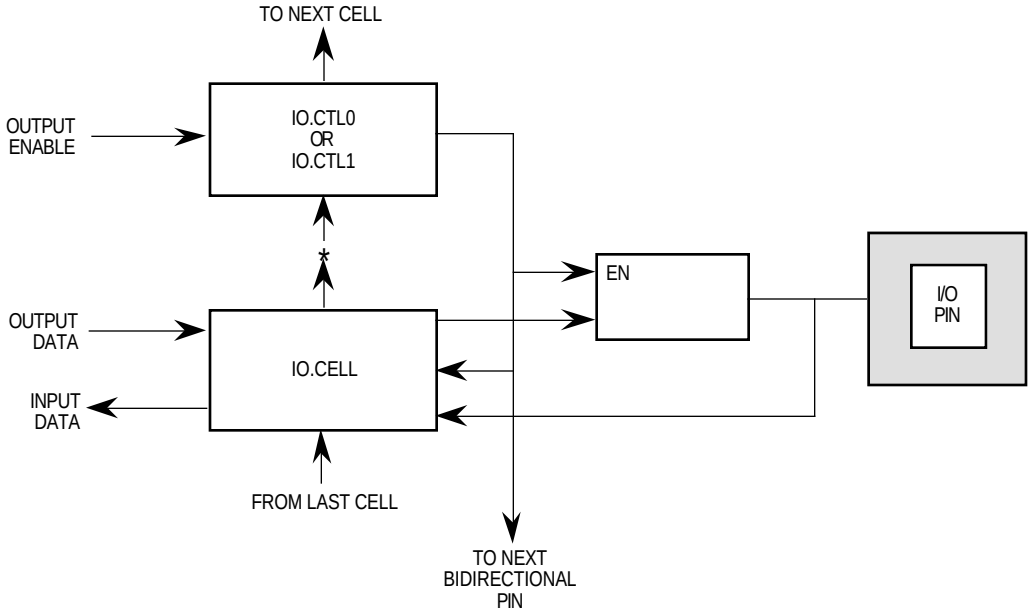

NOTE: More than one IO.Cell could be serially connected and controlled by a single IO.Ctlx cell.

Figure 10-8. General Arrangement for Bidirectional Pins

10.4 INSTRUCTION REGISTER

The MC68341 IEEE 1149.1 implementation includes the three mandatory public instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS), but does not support any of the optional public instructions defined by IEEE 1149.1. One additional public instruction (HI-Z) provides the capability for disabling all device output drivers. The MC68341 includes a 3-bit instruction register without parity, consisting of a shift register with three parallel outputs. Data is transferred from the shift register to the parallel outputs during the update-IR controller state. The three bits are used to decode the four unique instructions listed in Table 10-3.

The parallel output of the instruction register is reset to all ones in the test-logic-reset controller state. Note that this preset state is equivalent to the BYPASS instruction.

Table 10-3. Instructions

Code			Instruction
B2	B1	B0	
0	0	0	EXTEST
0	0	1	SAMPLE/PRELOAD
X	1	X	BYPASS
1	0	0	HI-Z
1	0	1	BYPASS

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During the capture-IR controller state, the parallel inputs to the instruction shift register are loaded with the standard 2-bit binary value (01) into the two least significant bits and the loss-of-crystal (LOC) status signal into bit 2. The parallel outputs, however, remain unchanged by this action since an update-IR signal is required to modify them.

The LOC status bit of the instruction register indicates whether an internal clock is detected when operating with a crystal clock source. The LOC bit is clear when a clock is detected and set when it is not. The LOC bit is always clear when an external clock is used. The LOC bit can be used to detect faulty connectivity when a crystal is used to clock the device.

10.4.1 EXTEST (000)

The external test (EXTEST) instruction selects the 155-bit boundary scan register. EXTEST asserts internal reset for the MC68341 system logic to force a predictable benign internal state while performing external boundary scan operations.

By using the TAP, the register is capable of a) scanning user-defined values into the output buffers, b) capturing values presented to input pins, c) controlling the direction of bidirectional pins, and d) controlling the output drive of three-state output pins. For more details on the function and uses of EXTEST, please refer to the IEEE 1149.1 document.

10.4.2 SAMPLE/PRELOAD (001)

The SAMPLE/PRELOAD instruction selects the 155-bit boundary scan register and provides two separate functions. First, it provides a means to obtain a snapshot of system data and control signals. The snapshot occurs on the rising edge of TCK in the capture-DR controller state. The data can be observed by shifting it transparently through the boundary scan register.

NOTE

Since there is no internal synchronization between the IEEE 1149.1 clock (TCK) and the system clock (CLKOUT), the user must provide some form of external synchronization to achieve meaningful results.

The second function of SAMPLE/PRELOAD is to initialize the boundary scan register output bits prior to selection of EXTEST. This initialization ensures that known data will appear on the outputs when entering the EXTEST instruction.

10.4.3 BYPASS (X1X, 101)

The BYPASS instruction selects the single-bit bypass register as shown in Figure 10-9. This creates a shift-register path from TDI to the bypass register and, finally, to TDO, circumventing the 155-bit boundary scan register. This instruction is used to enhance test efficiency when a component other than the MC68341 becomes the device under test.

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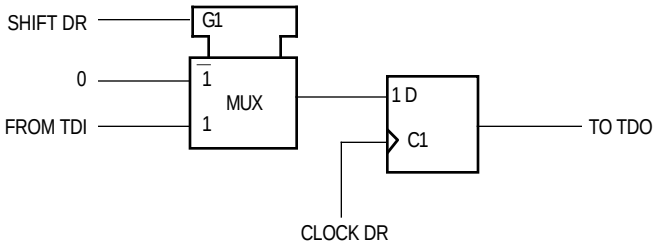

Figure 10-9. Bypass Register

When the bypass register is selected by the current instruction, the shift-register stage is set to a logic zero on the rising edge of TCK in the capture-DR controller state. Therefore, the first bit to be shifted out after selecting the bypass register will always be a logic zero.

10.4.4 HI-Z (100)

The HI-Z instruction is not included in the IEEE 1149.1 standard. It is provided as a manufacturer's optional public instruction to prevent having to backdrive the output pins during circuit-board testing. When HI-Z is invoked, all output drivers, including the two-state drivers, are turned off (i.e., high impedance). The instruction selects the bypass register.

10.5 MC68341 RESTRICTIONS

The control afforded by the output enable signals using the boundary scan register and the EXTEST instruction requires a compatible circuit-board test environment to avoid device-destructive configurations. The user must avoid situations in which the MC68341 output drivers are enabled into actively driven networks. Overdriving the TDO driver when it is active is not recommended.

The MC68341 includes on-chip circuitry to detect the initial application of power to the device. Power-on reset (POR), the output of this circuitry, is used to reset both the system and IEEE 1149.1 logic. The purpose for applying POR to the IEEE 1149.1 circuitry is to avoid the possibility of bus contention during power-on. The time required to complete device power-on is power-supply dependent. However, the IEEE 1149.1 TAP controller remains in the test-logic-reset state while POR is asserted. The TAP controller does not respond to user commands until POR is negated.

The MC68341 features a low-power stop mode that uses a CPU instruction called LPSTOP. The interaction of the IEEE 1149.1 interface with LPSTOP mode is as follows:

1. Leaving the TAP controller test-logic-reset state negates the ability to achieve minimal power consumption, but does not otherwise affect device functionality.
2. The TCK input is not blocked in LPSTOP mode. To consume minimal power, the TCK input should be externally connected to V_{CC} or ground.
3. The TMS and TDI pins include on-chip pullup resistors. In LPSTOP mode, these two pins should remain either unconnected or connected to V_{CC} to achieve minimal power consumption.

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10.6 NON-IEEE 1149.1 OPERATION

In non-IEEE 1149.1 operation, there are two constraints. First, the TCK input does not include an internal pullup resistor and should be pulled up externally to preclude mid-level inputs. The second constraint is to ensure that the IEEE 1149.1 test logic is kept transparent to the system logic by forcing the TAP controller into the test-logic-reset state, using either of two methods. During power-on, POR forces the TAP controller into this state. Alternatively, sampling TMS as a logic one for five consecutive TCK rising edges also forces the TAP controller into this state. If TMS either remains unconnected or is connected to V_{CC}, then the TAP controller cannot leave the test-logic-reset state, regardless of the state of TCK.

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SECTION 11
APPLICATIONS

This section provides guidelines for using the MC68341. Minimum system-configuration requirements and memory interface information are discussed.

11.1 MINIMUM SYSTEM CONFIGURATION

One of the powerful features of the MC68341 is the small number of external components needed to create an entire system. The information contained in the following paragraphs details a simple high-performance MC68341 system (see Figure 11-1). This system configuration features the following hardware:

- Processor Clock Circuitry
- Reset Circuitry
- SRAM Interface
- ROM Interface
- Serial Interface

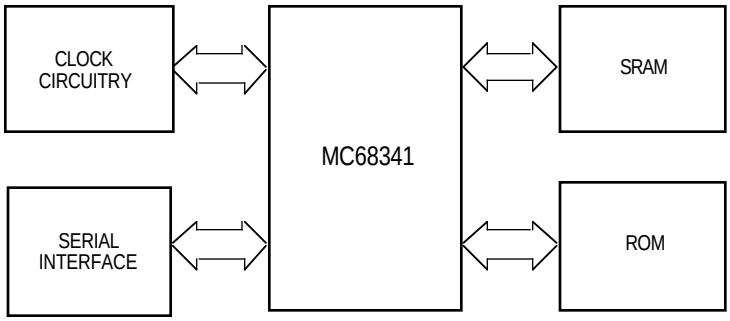

Figure 11-1. Minimum System Configuration Block Diagram

11.1.1 Processor Clock Circuitry

The MC68341 has an on-chip clock synthesizer that can operate from an on-chip phase-locked loop (PLL) and a voltage-controlled oscillator (VCO). The clock synthesizer uses an external crystal connected between the EXTAL and XTAL pins as a reference frequency source. Figure 11-2 shows a typical circuit using an inexpensive 32.768-kHz watch crystal. The 22-M resistor connected between the EXTAL and XTAL pins provides biasing for a faster oscillator startup time. The crystal manufacturer's documentation should be consulted for specific recommendations on external component values.

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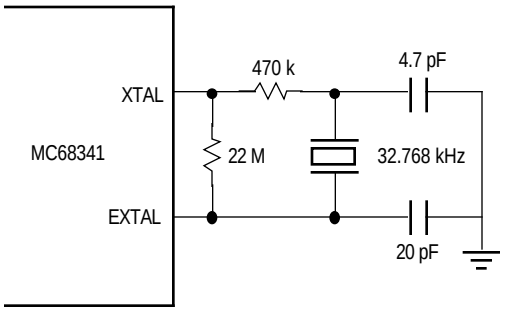

Figure 11-2. Sample Crystal Circuit

The circuit shown in Figure 11-3 is the typical circuit recommended by Statek Corporation, for 32768 kHz crystal, part number CX-IV. It is recommended to start with these values, but parameter values may need to be adjusted to compensate for variables in layout.

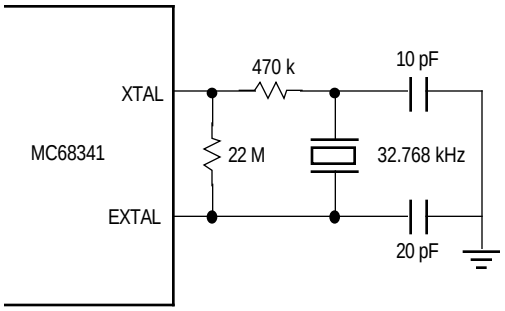

Figure 11-3. Statek Corporation Crystal Circuit

A separate power pin (V_{CCSYN}) is used to provide increased noise immunity for the clock circuits. The source for V_{CCSYN} should be a quiet power supply, and external bypass capacitors (see Figure 11-4) should be placed as close as possible to the V_{CCSYN} pin to ensure a stable operating frequency.

Additionally, the PLL requires that an external low-leakage filter capacitor, typically in the range of 0.01 to 0.1 µF, be connected between the XFC and V_{CCSYN} pins. The XFC capacitor should provide 50-MΩ insulation but should not be electrolytic. For external clock mode without PLL, the XFC pin can be left open. Smaller values of the external filter capacitor provide a faster response time for the PLL, and larger values provide greater frequency stability. Figure 11-4 depicts examples of both an external filter capacitor and bypass capacitors for V_{CCSYN}.

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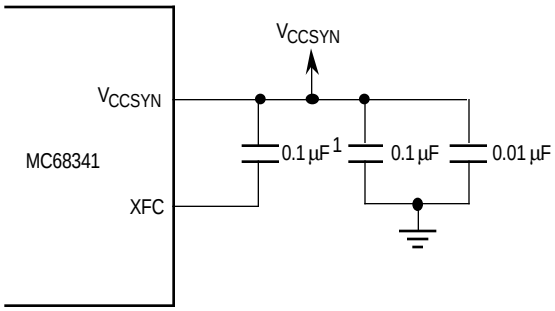

NOTE 1: Must be a low leakage capacitor.

Figure 11-4. XFC and V_{CCSYN} Capacitor Connections

11.1.2 Reset Circuitry

A power-on reset (POR) is generated by the SIM41 module when it detects a positive going V_{CC} transition—the V_{CC} threshold is typically in the range 2.0–2.7V, and varies depending on processing and environmental variables. Hysteresis is included in the reset circuit to prevent reassertion for a monotonically increasing V_{CC} voltage; however, excessively long V_{CC} rise times (>100 ms) may allow the reset logic to release $\overline{\text{RESET}}$ before V_{CC} has stabilized. The reset thresholds provided in the SIM41 should not be relied upon to monitor V_{CC}, since internal logic may fail at voltages between spec V_{CCmin} and the reset trigger threshold. An external low voltage monitor circuit, such as the MC34064, should be used instead.

When the MC68341 is used in crystal clock mode, the simplest external reset logic consists of simply a 1K pullup resistor from RESET to V_{CC}. This solution relies on a monotonically increasing V_{CC} that has a rise time on the order of 100ms or less - the actual allowable rise time is dependent on the startup time of the 32.768kHz oscillator circuit. As noted above, this does not provide rigorous V_{CC} monitoring, and may be susceptible to sags or glitches in the V_{CC} supply voltage.

In external clock mode, either with or without the PLL, the POR time delay of 328 * T_{clkin} does not provide adequate time for V_{CC} to stabilize before allowing reset to negate. Applications using these two clocking modes should include an external reset circuit which generates an appropriate delay for the power source being used, as well as a voltage monitor if needed.

11.1.3 SRAM Interface

SRAM interfacing is very simple when a programmable chip select is used, as shown in Figure 11-5. The chip select provides address decode and controls bus cycle termination, while $\overline{\text{UWE}}$ and $\overline{\text{LWE}}$ are used as byte write strobes. The SRAMs are enabled only during SRAM accesses to minimize system power consumption.

This SRAM interface supports a two-clock access at 16.78-MHz with up to 24ns memory data access time. If buffers are required to reduce signal loading or if slower and less expensive memories are desired, a three-clock bus cycle can be used. Additional

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memories can be used provided the MC68341 specification for load capacitance on the chip-select ($\overline{CSx}$) signal is not exceeded. (Address buffers may be needed, however.)

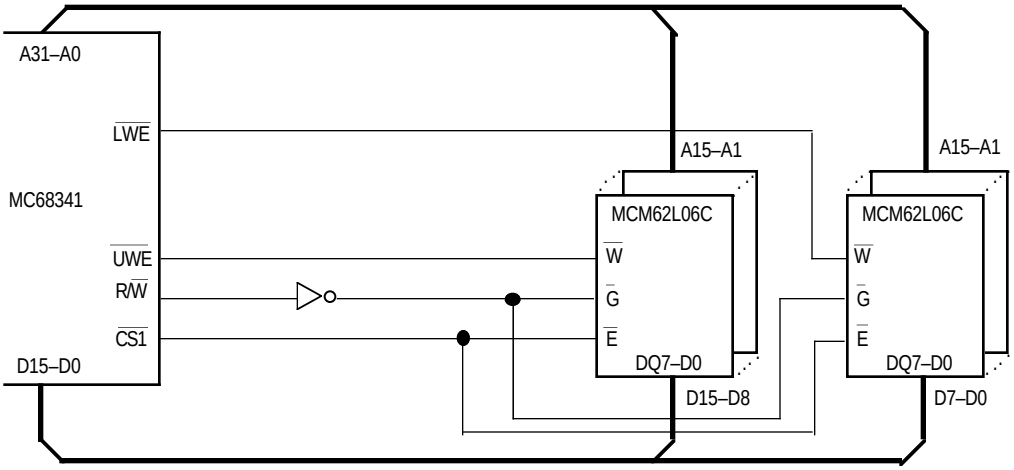

Figure 11-5. SRAM Interface

11.1.4 ROM Interface

Using the programmable chip selects creates a very straightforward ROM interface. As shown in Figure 11-6, no external circuitry is needed. Care must be used, however, not to overload the address bus. Address buffers may be required to ensure that the total system input capacitance on the address signals does not exceed the C_L specification.

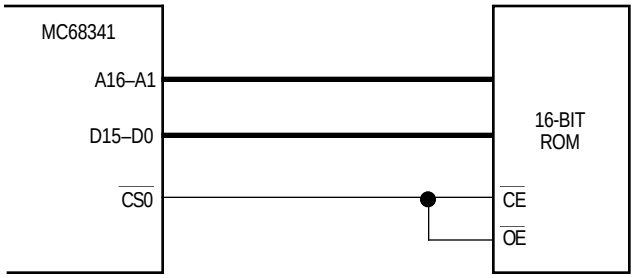

Figure 11-6. ROM Interface

11.1.5 Serial Interface

The necessary circuitry to create an RS-232 interface with the MC68341 includes an external crystal and an RS-232 receiver/driver (see Figure 11-7). The resistor and capacitor values shown are typical; the crystal manufacturer's documentation should be consulted for specific recommendations on external component values. The circuit shown does not include modem support (ready-to-send (RTS) and clear-to-send (CTS) are not shown); however, these signals can be connected to the receiver/driver and to the connector in a similar manner as the connections for TxDx and RxDx.

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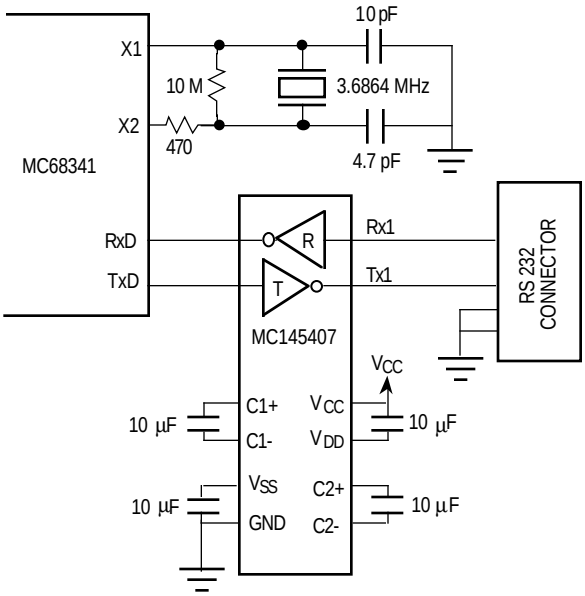

Figure 11-7. Serial Interface

11.2 MEMORY INTERFACE INFORMATION

The following paragraphs contain information on using an 8-bit boot ROM, performing access time calculations, calculating frequency-adjusted outputs, and interfacing an 8-bit device to 16-bit memory using the DMA channel single-address mode.

11.2.1 Using an 8-Bit Boot ROM

Upon power-up, the MC68341 uses $\overline{\text{CS0}}$ to begin operation. $\overline{\text{CS0}}$ is a six-wait-state, 16-bit chip select, until otherwise programmed. If an 8-bit ROM is desired, external circuitry can be added to return an 8-bit $\overline{\text{DSACKx}}$ in five (or less) wait states (see Figure 11-8).

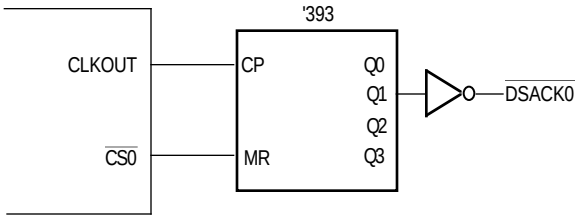

Figure 11-8. External Circuitry for 8-Bit Boot ROM

The `393 is a falling edge-triggered counter; thus, $\overline{\text{CS0}}$ is stable during the time in which it is being clocked. $\overline{\text{CS0}}$ acts as the asynchronous reset—i.e., when it is asserted, the `393 is allowed to count. The falling edge of S2 provides the first counting edge. Q1 does not transition on this falling edge, but transitions to a logic one on the subsequent edge. $\overline{\text{DSACK0}}$ is Q1 inverted; thus, on the next falling edge, $\overline{\text{DSACK0}}$ is seen as asserted, indicating an 8-bit port. When $\overline{\text{CS0}}$ is negated, Q1 is again held in reset and $\overline{\text{DSACK0}}$ is negated. The timing diagram in Figure 11-9 illustrates this operation.

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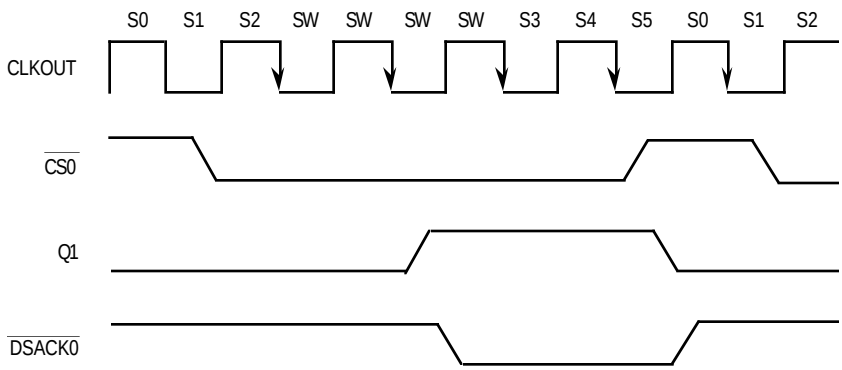

Figure 11-9. 8-bit Boot ROM Timing

11.2.2 Access Time Calculations

The two time paths that are critical in an MC68341 application using the $\overline{CSx}$ signals are shown in Figure 11-10. The first path is the time from address valid to when data must be available to the processor; the second path is the time from $\overline{CSx}$ asserted to when data must be available to the processor. Note that the $\overline{CSx}$ timing shown in these examples is for M68300 bus cycles; timing for 68000 bus cycles can be derived in a similar manner.

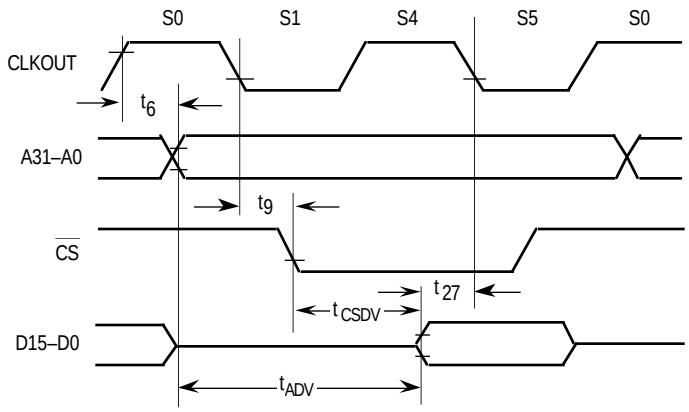

Figure 11-10. Access Time Computation Diagram

As shown in the diagram, an equation for the address access time, t_{ADV}, can be developed as follows:

$$t_{ADV} = t_{cyc}(N_c - 0.5) - t_{s9} - t_{s27}$$

where:

t_{cyc} = system CLKOUT period

N_c = number of clocks per bus cycle

t_{s6} = CLKOUT high to address valid = 30 ns maximum at 16.78 MHz

t_{s27} = data-in valid to CLKOUT low setup = 5 ns minimum at 16.78 MHz

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An equation for the chip select access time, t_{CSDV}, can be developed as follows:

$$t_{CSDV} = t_{cyc}(N_c - 1) - t_{s9} - t_{s27}$$

where:

t_{cyc} = system clock period

N_c = number of clocks per access

t_{s9} = CLKOUT low to $\overline{CSx}$ asserted = 30 ns maximum at 16.78 MHz

t_{s27} = data-in valid to CLKOUT low setup = 5 ns minimum at 16.78 MHz

Using these equations, the memory access times at 16.78 MHz are shown in Table 11-1. See **Section 12 Electrical Characteristics** for more timing information.

Table 11-1. Memory Access Times at 16.78 MHz

Access Time	N = 2	N = 3	N = 4	N = 5	N = 6
t_{ADV}	54 ns	114 ns	173 ns	233 ns	292 ns
t_{CSDV}	24 ns	84 ns	143 ns	203 ns	263 ns

The values can be used to determine how many clock cycles an access will take, given the access time of the memory devices and any delays through buffers or external logic that may be needed.

11.2.3 Calculating Frequency-Adjusted Output

The general relationship between the CLKOUT and most input and output signals is shown in Figure 11-11. Most outputs transition off of a falling edge of CLKOUT, but the same principle applies to those outputs that transition off of a rising edge.

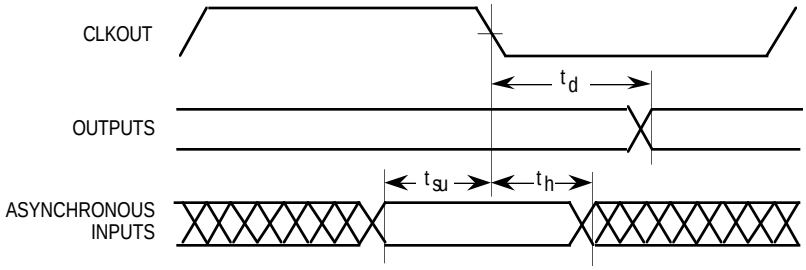

Figure 11-11. Signal Relationships to CLKOUT

For outputs that are referenced to a clock edge, the propagation delay (t_d) does not change as the frequency changes. For instance, specification 6 in the electrical characteristics, shown in **Section 12 Electrical Characteristics**, shows that address, function code, and size information is valid 3 to 30 ns after the rising edge of S0. This specification does not change even if the device frequency is less than 16.78 MHz. Additionally, the relationship between the asynchronous inputs and the clock edge, as shown in Figure 11-11, does not change as frequency changes.

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A second type of specification indicates the minimum amount of time a signal will be asserted. This type of specification is illustrated in Figure 11-12.

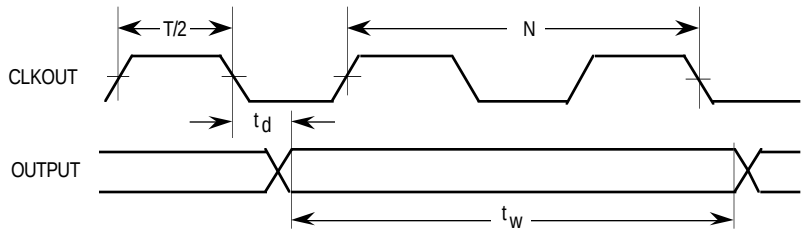

Figure 11-12. Signal Width Specifications

The method for calculating a frequency-adjusted t_W is as follows:

$$t_W' = t_W + N\,(T_f'/2 - T_f/2) + (T_f'/2 - t_d)$$

where:

t_W' = the frequency-adjusted signal Frequency-Adjusted Signal:width

t_W = the signal width at 16.78 MHz

N = the number of full one-half clock periods in t_W

$T_f'/2$ = one-half the new clock period

$T_f/2$ = one-half the clock period at full speed

t_d = the propagation time from the clock edge

The following calculation uses a 16.78-MHz part, specification 14, $\overline{AS}$ width asserted, at 12.5 MHz as an example:

t_W = 100 ns

N = 3

$T_f'/2$ = 80/2 = 40 ns

$T_f/2$ = 60/2 = 30 ns

t_d = 30 ns maximum

therefore:

$$t_W' = 100 + 3(40 - 30) + (40 - 30) = 140 \text{ ns}$$

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The third type of specification used is a skew between two outputs (see Figure 11-13).

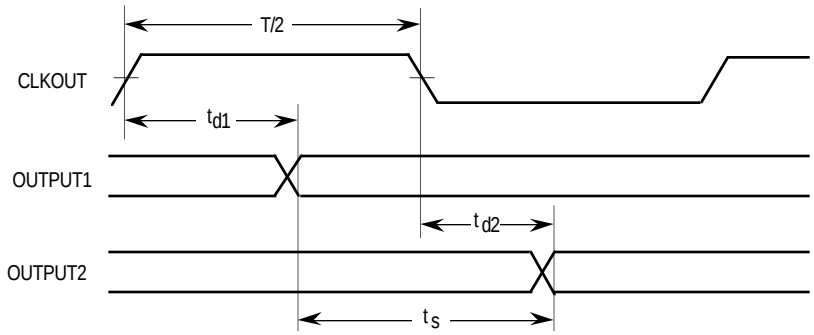

Figure 11-13. Skew between Two Outputs

The method for calculating a frequency-adjusted t_S is as follows:

$$t_S' = t_S + N\,(T_f'/2 - T_f/2) + (T_f'/2 - t_{d1})$$

where:

t_S' = the frequency-adjusted skew

t_S = the skew at full speed

N = the number of full one-half clock periods in t_S, if any

$T_f'/2$ = one-half the new clock period

$T_f/2$ = one-half the clock period at full speed

t_{d1} = the propagation time for the first output from the clock edge

The following calculation uses a 16.78-MHz port, specification 21, R/$\overline{W}$ high to $\overline{AS}$ asserted, at 8 MHz as an example:

t_S = 15 ns minimum

N = 0

$T_f'/2$ = 125/2 = 62.5 ns

$T_f/2$ = 60/2 = 30 ns

t_{d1} = 30 ns maximum

therefore:

$$t_S' = 15 + 0(62.5 - 30) + (62.5 - 30) = 47.5 \text{ ns minimum}$$

In this manner, new specifications for lower frequencies can be derived for an MC68341.

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11.2.4 Interfacing an 8-Bit Device to 16-Bit Memory Using Single-Address DMA Mode

One of the requirements of single-address mode is that the source and destination must be the same port size. However, the MC68341 can perform direct memory accesses in single-address mode between an 8-bit device and 16-bit memory. The port size must be specified as 8 bits, and some external logic is required as shown in Figure 11-14.

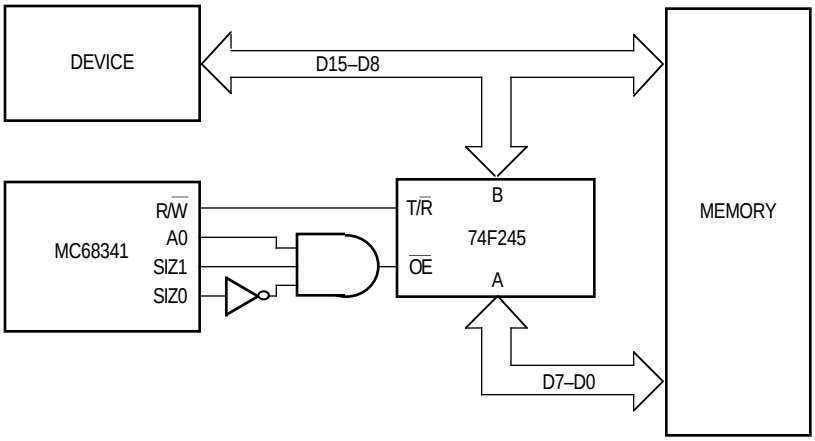

Figure 11-14. Circuitry for Interfacing 8-Bit Device to 16-Bit Memory in Single-Address DMA Mode

During even-byte accesses, the data is transferred directly on D15–D8. However, during odd-byte accesses, the data must be routed on D15–D8 for the 8-bit device and on D7–D0 for the 16-bit memory.

11.3 POWER CONSUMPTION CONSIDERATIONS

The MC68341 can be designed into low-power applications that involve high-performance processing capability (32-bits), high functional density, small size, portable capability, and battery operation.

The MC68341 fits into the following types of applications:

- "Palmtop" Computers
  - — Stylus Input
  - — Voice Input
  - — Image Input
- Transaction Tracking
  - — Car Rental
  - — Cargo
  - — Courier
  - — Handheld
- Bar Code Scanners
- Telephony
  - — Cordless Phones
  - — Cellular Phones
- CD-I, CD-ROM
- Defense Industry
  - — Guidance Systems
  - — Tracking Systems
- Data Entry
- Instruments
- Handheld Games

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11.4 MC68341V (3.3 V)

The MC68341V can operate with a 3.3-V power supply for significant power savings. The formula for power dissipation is

$$P_d \approx V^2 \times f + dc$$

Table 11-2 shows typical electrical characteristics for both the MC68341 and MC68341V.

Table 11-2. Typical Electrical Characteristics

Parameter	MC68341 (5.0 V)	MC68341V (3.3 V)
Clock Frequency	0–16.78 MHz 0–25 MHz	0–8.39 MHz 0–16.78 MHz
Typical Current (16 MHz)	TBD	TBD
Typical Current (8 MHz)	TBD	TBD
Standby Current	TBD	TBD

Running at 3.3 V saves 66% of the power consumption.

The 3.3 V operation provides the following user advantages:

Advantage	Benefit
Lower Supply Voltage	Fewer Batteries
Fewer Batteries	Less Weight Smaller Size
Lower Current Drain	Extended Battery Life
Less Heat Generated	No Fan No Fan Noise
Less EMF Radiation	Easier FCC Certification Less Crosstalk Closer PCB Traces
High Functional Integration	All-In-One 3.3 V Part: Processor Peripherals Glue Logic

These advantages result in a much more portable system.

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SECTION 12
ELECTRICAL CHARACTERISTICS - PRELIMINARY

This section contains preliminary information on power considerations, DC/AC electrical characteristics, and AC timing specifications of the MC68341. Refer to **Section 13 Ordering Information and Mechanical Data** for specific part numbers corresponding to voltage, frequency, and temperature ratings.

12.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage [1, 2]	V_{CC}	–0.3 to +6.5	V
Input Voltage[1, 2]	V_{in}	–0.3 to +6.5	V
Operating Temperature Range Commercial	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C

NOTES:
1. Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

The above ratings define a range of conditions in which the device will operate without being damaged. However, sections of the device may not operate normally while being exposed to the electrical extremes.

12.2 THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance—Junction to Case Plastic 160-Pin PQFP	θ_{JC}	TBD	°C/W
Thermal Resistance—Junction to Ambient Plastic 160-Pin PQFP	θ_{JA}	43*	°C/W

* Estimated

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12.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \qquad (1)$$

where:

T_A	=	Ambient Temperature, °C
θ_{JA}	=	Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D	=	$P_{INT} + P_{I/O}$
P_{INT}	=	$I_{CC} \times V_{CC}$, Watts—Chip Internal Power
$P_{I/O}$	=	Power Dissipation on Input and Output Pins—User Determined

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C)$$

Solving Equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equations (1) and (2) iteratively for any value of T_A.

12.4 AC ELECTRICAL SPECIFICATION DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 12-1. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in the figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs are specified with minimum setup and hold times and are measured as shown. Finally, the measurement for signal-to-signal specifications are shown.

Note that the testing levels used to verify conformance to the AC specifications do not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.

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The MC68341V low voltage part can operate up to 16.78 MHz with a 3.3 V ±0.3 V supply. Separate part numbers are used to distinguish the operation of the parts according to the supply voltage- refer to **Section 13 Ordering Information and Mechanical Data** for the part numbering schemes. MC68341 is used throughout this section to refer to the 16.78- or 25.16-MHz parts at 5.0 V ±5%. MC68341V is used throughout this section to refer to the 16.78-MHz part at 3.3 V ±0.3 V.

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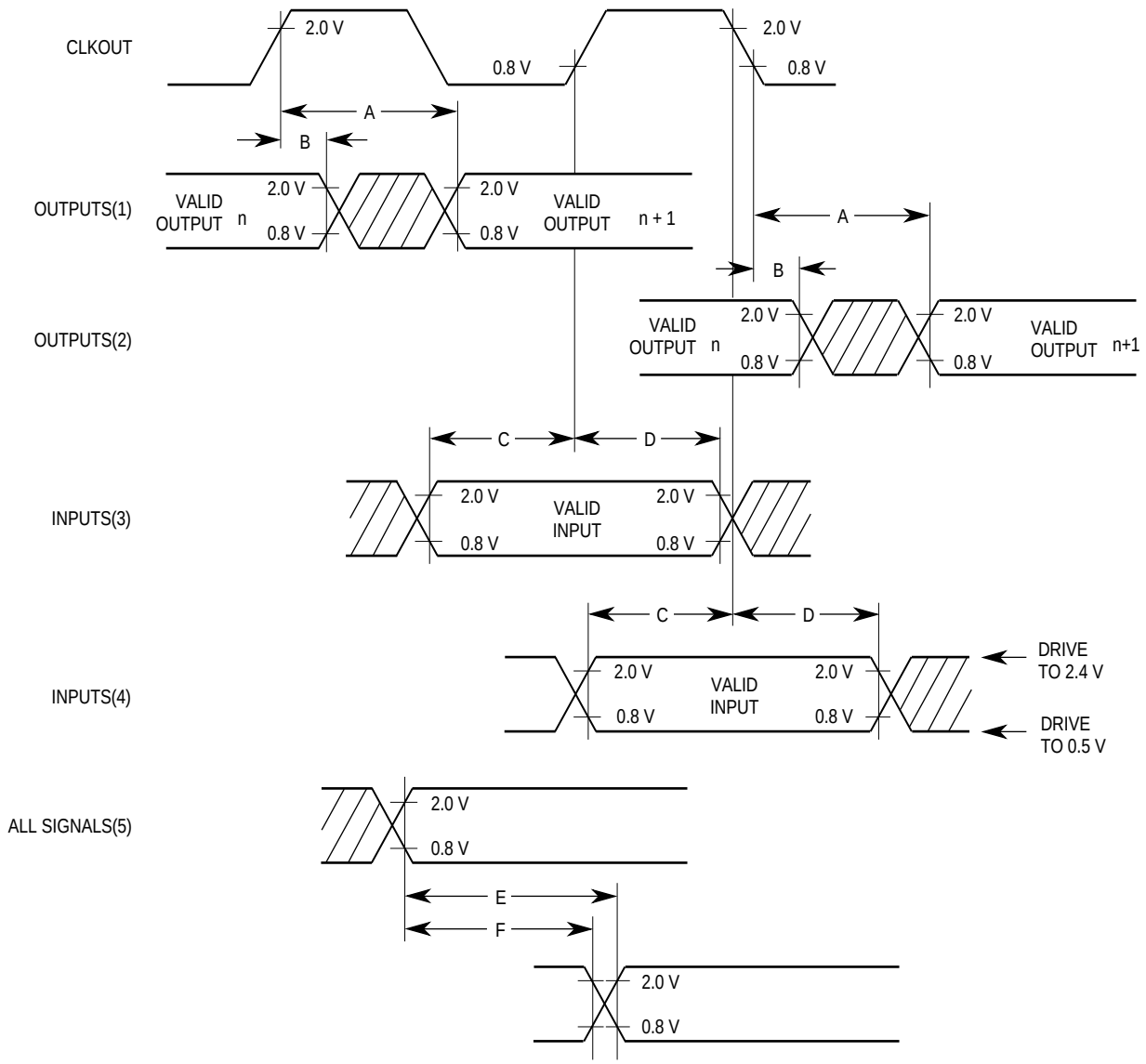

NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 12-1. Drive Levels and Test Points for AC Specifications

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12.5 DC ELECTRICAL SPECIFICATIONS - PRELIMINARY

(GND = 0 Vdc, TA = 0 to 70°C; see numbered notes)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage (except clocks)	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Clock Input High Voltage (EXTAL, EXTCLK, SCLK)	V_{IHC}	$0.7*(V_{CC})$	$V_{CC}+0.3$	V
Undershoot	—	—	–0.8	V
Input Leakage Current (All Input Only Pins) $V_{in} = V_{CC}$ or GND	I_{in}	–2.5	2.5	µA
Hi-Z (Off-State) Leakage Current (All Noncrystal Outputs and I/O Pins) V_{in} = 0.5/2.4 V[1]	I_{OZ}	–20	20	µA
Signal Low Input Current TMS, TDI V_{IL} = 0.8 V Signal High Input Current TMS, TDI V_{IH} = 2.0 V	I_L I_H	–0.015 –0.015	0.2 0.2	mA mA
Output High Voltage[1, 2] I_{OH} = –0.8 mA All Noncrystal Outputs except $\overline{DONE2}$, $\overline{DONE1}$, RTCOUT, $\overline{HALT}$, $\overline{RESET}$. I_{OH} = –20 µA[3] RTCOUT	V_{OH}	2.4	—	V
Output Low Voltage[1] I_{OL} = 2.0 mA CLKOUT, FREEZE, $\overline{IPIPE}$, $\overline{IFETCH}$ I_{OL} = 3.2 mA A23–A0, D15–D0, FC3–FC0, SIZ1, SIZ0 I_{OL} = 5.3 mA All Other Output Only and Group 2 I/O Pins I_{OL} = 15.3 mA $\overline{HALT}$, $\overline{RESET}$	V_{OL}	—	 0.5 0.5 0.5 0.5	V
Total Supply Current at 5 V +5% @ 16.78 MHz RUN LPSTOP (VCO Off)	 I_{CC} S_{ICC}	—	 TBD TBD	 mA µA
Power Dissipation at 5 V +5% @ 16.78 MHz[4]	P_D	—	TBD	mW
Total Supply Current at 3.3 V + 0.3 V @ 16.78 MHz RUN LPSTOP (VCO Off)	 I_{CC} S_{ICC}	—	 TBD TBD	 mA µA
Power Dissipation at 3.3 V +0.3 V @ 16.78 MHz[4]	P_D	—	TBD	mW
RTC Battery Voltage	V_{BATT}	2.0	V_{CC}	V
RTC Battery Supply Current	I_{BATT}	—	TBD	µA
Input Capacitance[5] All Input-Only Pins All I/O Pins	C_{in}	—	 10 20	pF
Load Capacitance	C_L	—	100	pF

NOTES:

1. Input-Only Pins: $\overline{BERR}$, $\overline{BG}$, $\overline{BKPT}$, $\overline{BR}$, $\overline{CTSB}$, $\overline{CTSA}$, $\overline{DREQ2}$, $\overline{DREQ1}$, $\overline{DSACK1}$, $\overline{DSACK0}$, EXTAL, RxDB, RxDA, SCLK, TCK, TDI, $\overline{TGATE}$, TIN, TMS,EXTCLK, $\overline{BSW}$.
   Output-Only Pins: A23–A0, $\overline{AS}$, $\overline{AS68K}$, $\overline{BG}$, CLKOUT, $\overline{CS7}$–$\overline{CS1}$, $\overline{DACK2}$, $\overline{DACK1}$, $\overline{DS}$, FC3–FC0, FREEZE, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{LDS}$, $\overline{LWE}$, $\overline{RMC}$, $\overline{RTSB}$, $\overline{RTSA}$, R/$\overline{W}$, RxRDYA, SIZ1, SIZ0, TDO, TOUT, TxDB, TxDA, $\overline{TxRDYA}$, $\overline{UDS}$, $\overline{UWE}$.
   Input/Output Pins:
   Group 1: D15–D0.
   Group 2: A31–A24, $\overline{CS0}$, $\overline{DONE2}$, $\overline{DONE1}$, $\overline{IRQ7}$–$\overline{IRQ1}$, MODCK
   Group 3: $\overline{HALT}$, $\overline{RESET}$.
   Group 4: $\overline{MISO}$, $\overline{MOSI}$, $\overline{PCS1}$, $\overline{PCS0}$, $\overline{QSCLK}$
2. V_{OH} specification for $\overline{HALT}$, $\overline{RESET}$, $\overline{DONE2}$, and $\overline{DONE1}$ is not applicable because they are open-drain pins.
3. $\overline{RMC}$/RTCOUT can source 20µA when configured as RTCOUT, 0.8mA when configured as $\overline{RMC}$.
4. Power dissipation measured with all modules active.
5. Capacitance is periodically sampled rather than 100% tested.

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12.6 CLOCK AC ELECTRICAL SPECIFICATIONS - PRELIMINARY

(GND = 0 Vdc, TA = 0 to 70°C; see numbered notes)

CLOCK SPECIFICATIONS - Crystal Mode

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
	System Frequency - Crystal Mode[1]	f_{sys}	0.13	16.78	0.13	25.16	MHz
	Crystal Frequency[2]	f_{XTAL}	25	50	25	50	kHz
	External Clock Input Frequency[3]	f_{EXT}	25	50	25	50	kHz
	External Clock Duty Cycle		20	80	20	80	%
	VCO Frequency Range	f_{VCO}	0.1	51.2	0.1	51.2	MHz
	PLL Start-up Time[4]	t_{rc}	—	20	—	20	ms
	Limp Mode CLKOUT Frequency[5] SYNCR X-bit = 0 and Z-bit = 0 SYNCR X-bit = 1 and Z-bit = 0	f_{limp}	 — —	 8.39 16.78	 — —	 8.39 16.78	MHz
	CLKOUT stability[6]	Δ_{CLK}	—	±1	—	±1	%
1	CLKOUT Period	t_{cyc}	59.6	—	39.7	—	ns
	CLKOUT Duty Cycle		47	53	47	53	%
2,3	CLKOUT Pulse Width	t_{CW}	28	—	19	—	ns
4,5	CLKOUT Rise and Fall Times	t_{Crf}	—	5	—	4	ns

NOTES:

1. All crystal mode clock specifications are based on using a 32.768-kHz crystal for the input.
2. The RTC requires a 32.768 kHz crystal or external clock for proper operation.
3. EXTAL can be direct driven by an external oscillator source - refer to the DC Electrical Characteristics for VIL/VIH requirements.
4. Assumes that a stable V_{CCSYN} is applied, that an external filter capacitor with a value of 0.1 µF is attached to the XFC pin, and that the crystal oscillator is stable. This specification also applies to the period required for PLL lock after changing the W or Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after exiting LPSTOP.
5. The X-bit in the SYNCR controls a divide-by-two scaler on the system clock output.
6. CLKOUT stability is the average deviation from programmed frequency measured at maximum f_{sys}. Measurement is made with a stable external clock input applied using the PLL.

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CLOCK SPECIFICATIONS - External Clock With PLL Mode

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
	System Frequency External Clock with PLL Mode	f_{sys}	0.1	16.78	0.1	25.16	MHz
1C	External Clock Input Period	t_{EXTcyc}	59.6	10µS	39.7	10µS	ns
	External Clock Duty Cycle		20	80	20	80	%
	External Clock Input Period with ÷2	t_{EXTcyc}	TBD	—	TBD	—	ns
	External Clock Duty Cycle with ÷2		TBD	—	TBD	—	%
	VCO Frequency Range	f_{VCO}	0.1	33.6	0.1	51.2	MHz
	PLL Start-up Time[1]	t_{rc}	—	20	—	20	ms
	Limp Mode CLKOUT Frequency	f_{limp}	—		—		kHz
	CLKOUT stability[2]	Δ_{CLK}	—	±1	—	±1	%
	CLKOUT Duty Cycle		47	53	47	53	%
2C, 3C	CLKOUT Pulse Width	t_{EXTCW}	28	—	19	—	ns
4,5	CLKOUT Rise and Fall Times	t_{Crf}	—	5	—	4	ns
	Clock Input to CLKOUT Skew (Rising Edges)		—	±5	—	±5	ns

NOTES:

1. Assumes that a stable V_{CCSYN} is applied, that an external filter capacitor with a value of 0.1 µF is attached to the XFC pin, and that the crystal oscillator is stable. This specification also applies to the period required for PLL lock after changing the W or Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after exiting LPSTOP.
2. CLKOUT stability is the average deviation from programmed frequency measured at maximum f_{sys}. Measurement is made with a stable external clock input applied using the PLL.

CLOCK SPECIFICATIONS - External Clock Mode (Without PLL)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
	System Frequency[1] External Clock Without PLL Mode	f_{sys}	dc	16.78	dc	25.16	MHz
1B	External Clock Input Period	t_{EXTcyc}	59.6	—	39.7	—	ns
	External Clock Pulse Width		TBD	—	TBD	—	ns
	External Clock Input Period with ÷2	t_{EXTcyc}	TBD	—	TBD	—	ns
	External Clock Pulse Width with ÷2		TBD	—	TBD	—	ns
2B, 3B[9]	CLKOUT Pulse Width	t_{EXTCW}	TBD	—	TBD	—	ns
4,5	CLKOUT Rise and Fall Times	t_{Crf}	—	5	—	4	ns
	Clock Input to CLKOUT Skew (Rising Edges)		TBD	TBD	TBD	TBD	ns

1. All internal registers retain data at 0 Hz.

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12.7 AC TIMING SPECIFICATIONS - PRELIMINARY

(GND = 0 Vdc, TA = 0 to 70°C; see numbered notes; see Figures 12-2–12-13)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
6	CLKOUT High to Address, FC, SIZ Valid	t_{CHAV}	0	30	0	20	ns
6A	CLKOUT High to FC3, $\overline{RMC}$ Valid	t_{CHAVB}	0	35	0	25	ns
7	CLKOUT High to Address, Data, FC, SIZ, $\overline{RMC}$ High Impedance	t_{CHAZx}	0	60	0	40	ns
8	CLKOUT High to Address, FC, SIZ, $\overline{RMC}$ Invalid	t_{CHAZn}	0	—	0	—	ns
9[9]	CLKOUT Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{IACKx}$ Asserted	t_{CLSA}	3	30	3	20	ns
9A[2]	$\overline{AS}$ to $\overline{DS}$ or $\overline{CS}$ Asserted (Read)	t_{STSA}	–15	15	–6	6	ns
9B	CLKOUT High to $\overline{AS68K}$, $\overline{CS}$, $\overline{UDS}$, $\overline{LDS}$ Asserted		3	30	3	20	ns
9C	$\overline{AS68K}$ to $\overline{UDS}$, $\overline{LDS}$, or $\overline{CS}$ Asserted (Read)		–15	15	–6	6	ns
11	Address, FC, SIZ, $\overline{RMC}$ Valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Asserted	t_{AVSA}	15	—	10	—	ns
11A	Address, FC, SIZ, $\overline{RMC}$ Valid to $\overline{AS68K}$, $\overline{CS}$ (and $\overline{UDS}$ /$\overline{LDS}$ Read) Asserted	t_{AVSKA}	45	—	30	—	ns
12	CLKOUT Low to $\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{IFETCH}$, $\overline{IPIPE}$, $\overline{AS68K}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{LWE}$, $\overline{UWE}$ Negated	t_{CLSN}	3	30	3	20	ns
13	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{AS68K}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{UWE}$, $\overline{LWE}$, $\overline{IACKx}$ Negated to Address, FC, SIZ Invalid (Address Hold)	t_{SNAI}	15	—	10	—	ns
14	$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SWA}	100	—	70	—	ns
14A	$\overline{DS}$ Width Asserted (Write)	t_{SWAW}	45	—	30	—	ns
14B	$\overline{AS}$, $\overline{CS}$, $\overline{IACKx}$ (and $\overline{DS}$ Read) Width Asserted (Fast Termination Cycle)	t_{SWDW}	40	—	30	—	ns
14C	$\overline{AS68K}$, $\overline{CS}$ (and $\overline{UDS}$/ $\overline{LDS}$ Read) Width Asserted	t_{SWA}	70	—	50	—	ns
14D	$\overline{UDS}$, $\overline{LDS}$ Width Asserted (3-Clock Write)	t_{SWBW}	15	—	10	—	ns
15[3]	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$ Width Negated	t_{SN}	40	—	30	—	ns
16	CLKOUT High to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, $\overline{AS68K}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{UWE}$, $\overline{LWE}$ High Impedance	t_{CHSZ}	—	60	—	40	ns
17	$\overline{AS}$, $\overline{DS}$, $\overline{CS}$, $\overline{AS68K}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{UWE}$, $\overline{LWE}$, Negated to R/$\overline{W}$ High	t_{SNRN}	15	—	10	—	ns
18	CLKOUT High to R/$\overline{W}$ High	t_{CHRH}	0	30	0	20	ns
20	CLKOUT High to R/$\overline{W}$ Low	t_{CHRL}	0	30	0	20	ns
21[9]	R/$\overline{W}$ High to $\overline{AS}$, $\overline{CS}$ Asserted	t_{RAAA}	15	—	10	—	ns
21A	R/$\overline{W}$ High to $\overline{AS68K}$, $\overline{CS}$ Asserted	t_{RABA}	45	—	30	—	ns
22	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RASA}	70	—	47	—	ns
22A	R/$\overline{W}$ Low to $\overline{LDS}$, $\overline{UDS}$ Asserted (Write)	t_{RADA}	100	—	67	—	ns
23	CLKOUT High to Data-Out Valid	t_{CHDO}	—	30	—	20	ns

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12.7 AC TIMING SPECIFICATIONS - PRELIMINARY (Continued)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
24	Data-Out Valid to Negating Edge of $\overline{AS}$, $\overline{CS}$, (Fast Termination Write)	t_{DVASN}	15	—	10	—	ns
25	$\overline{DS}$, $\overline{CS}$, $\overline{UDS}$, $\overline{LDS}$ Negated to Data-Out Invalid (Data-Out Hold)	t_{SNDOI}	15	—	10	—	ns
26	Data-Out Valid to $\overline{DS}$ Asserted (Write)	t_{DVSA}	15	—	10	—	ns
26A	Data-Out Valid to $\overline{UDS}$, $\overline{LDS}$ Asserted (Write)	t_{DVBSA}	45	—	30	—	ns
27	Data-In Valid to CLKOUT Low (Data Setup)	t_{DICL}	5	—	5	—	ns
27A	Late $\overline{BERR}$, $\overline{HALT}$, $\overline{BKPT}$ Asserted to CLKOUT Low (Setup Time, no 68K Bus)	t_{BELCL}	20	—	10	—	ns
28	$\overline{AS}$, $\overline{DS}$ $\overline{AS68K}$, $\overline{UDS}$, $\overline{LDS}$ Negated to $\overline{DSACKx}$, $\overline{BERR}$, $\overline{HALT}$ Negated	t_{SNDN}	0	80	0	50	ns
29[4]	$\overline{DS}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{CS0}$ Negated to Data-In Invalid (Data-In Hold)	t_{SNDI}	0	—	0	—	ns
29A[4]	$\overline{DS}$, $\overline{CS}$, $\overline{UDS}$, $\overline{LDS}$ Negated to Data-In High Impedance	t_{SHDI}	—	60	—	40	ns
30[4]	CLKOUT Low to Data-In Invalid (Fast Termination Hold)	t_{CLDI}	15	—	10	—	ns
30A[4]	CLKOUT Low to Data-In High Impendance	t_{CLDH}	—	90	—	60	ns
31[5]	$\overline{DSACKx}$ Asserted to Data-In Valid	t_{DADI}	—	50	—	32	ns
31A	$\overline{DSACKx}$ Asserted to $\overline{DSACKx}$ Valid (Skew)	t_{DADV}	—	30	—	20	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	t_{HRrf}	—	200	—	140	ns
33	CLKOUT Low to $\overline{BG}$ Asserted	t_{CLBA}	—	30	—	20	ns
34	CLKOUT Low to $\overline{BG}$ Negated	t_{CLBN}	—	30	—	20	ns
35[6]	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted ($\overline{RMC}$ Not Asserted)	t_{BRAGA}	1	—	1	—	CLKOUT
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GAGN}	1	2.5	1	2.5	CLKOUT
39	$\overline{BG}$ Width Negated	t_{GH}	2	—	2	—	CLKOUT
39A	$\overline{BG}$ Width Asserted	t_{GA}	1	—	1	—	CLKOUT
46	R/$\overline{W}$ Width Asserted (Write or Read)	t_{RWA}	150	—	100	—	ns
46A	R/$\overline{W}$ Width Asserted (Fast Termination Write or Read)	t_{RWAS}	90	—	60	—	ns
47A[8]	Asynchronous Input Setup Time	t_{AIST}	8, 5	—	5	—	ns
47B	Asynchronous Input Hold Time	t_{AIHT}	15	—	10	—	ns
48[5,7]	$\overline{DSACKx}$ Asserted to $\overline{BERR}$, $\overline{HALT}$ Asserted	t_{DABA}	—	30	—	20	ns
53	Data-Out Hold from CLKOUT High	t_{DOCH}	0	—	0	—	ns
54	CLKOUT High to Data-Out High Impedance	t_{CHDH}	—	30	—	20	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RADC}	40	—	25	—	ns
56	$\overline{RESET}$ Pulse Width (Reset Instruction)	t_{HRPW}	512	—	512	—	CLKOUT
56A	$\overline{RESET}$ Pulse Width (Input from External Device)	t_{RPWI}	590	—	590	—	CLKOUT
57	$\overline{BERR}$ Negated to $\overline{HALT}$ Negated (Rerun)	t_{BNHN}	0	—	0	—	ns

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12.7 AC TIMING SPECIFICATIONS - PRELIMINARY (Continued)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
70	CLKOUT Low to Data Bus Driven (Show Cycle)	t_{SCLDD}	0	30	0	20	ns
71	Data Setup Time to CLKOUT Low (Show Cycle)	t_{SCLDS}	15	—	10	—	ns
72	Data Hold from CLKOUT Low (Show Cycle)	t_{SCLDH}	10	—	6	—	ns
80	DSI Input Setup Time	t_{DSISU}	15	—	10	—	ns
81	DSI Input Hold Time	t_{DSIH}	10	—	6	—	ns
82	DSCLK Setup Time	t_{DSCSU}	15	—	10	—	ns
83	DSCLK Hold Time	t_{DSCH}	10	—	6	—	ns
84	DSO Delay Time	t_{DSOD}	—	t_{cyc} + 25	—	t_{cyc} + 16	ns
85	DSCLK Cycle	t_{DSCCYC}	2	—	2	—	CLKOUT
86	CLKOUT High to FREEZE Asserted	t_{FRZA}	0	50	0	35	ns
87	CLKOUT High to FREEZE Negated	t_{FRZN}	0	50	0	35	ns
88	CLKOUT High to $\overline{\text{IFETCH}}$ High Impedance	t_{IFZ}	0	50	0	35	ns
89	CLKOUT High to $\overline{\text{IFETCH}}$ Valid	t_{IF}	0	50	0	35	ns

NOTES:

1. All AC timing is shown with respect to 0.8 V and 2.0 V levels unless otherwise noted.
2. This number can be reduced to 5 ns if strobes have equal loads.
3. If multiple chip selects are used, the $\overline{\text{CS}}$ width negated (#15) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select.
4. These hold times are specified with respect to $\overline{\text{DS}}$ or $\overline{\text{CS}}$ on asynchronous reads and with respect to CLKOUT on fast termination reads. The user is free to use either hold time for fast termination reads.
5. If the asynchronous setup time (#47) requirements are satisfied, the $\overline{\text{DSACKx}}$ low to data setup time (#31) and $\overline{\text{DSACKx}}$ low to $\overline{\text{BERR}}$ low setup time (#48) can be ignored. The data must only satisfy the data-in to CLKOUT low setup time (#27) for the following clock cycle: $\overline{\text{BERR}}$ must only satisfy the late $\overline{\text{BERR}}$ low to CLKOUT low setup time (#27A) for the following clock cycle.
6. To ensure coherency during every operand transfer, $\overline{\text{BG}}$ will not be asserted in response to $\overline{\text{BR}}$ until after cycles of the current operand transfer are complete and $\overline{\text{RMC}}$ is negated.
7. In the absence of $\overline{\text{DSACKx}}$, $\overline{\text{BERR}}$ is an asynchronous input using the asynchronous setup time (#47).
8. Specification #47A for 16.78 MHz @ 3.3 V ±0.3V will be 8 ns.
9. During interrupt acknowledge cycles up to two wait states may be inserted by the processor between states S0 and S1.

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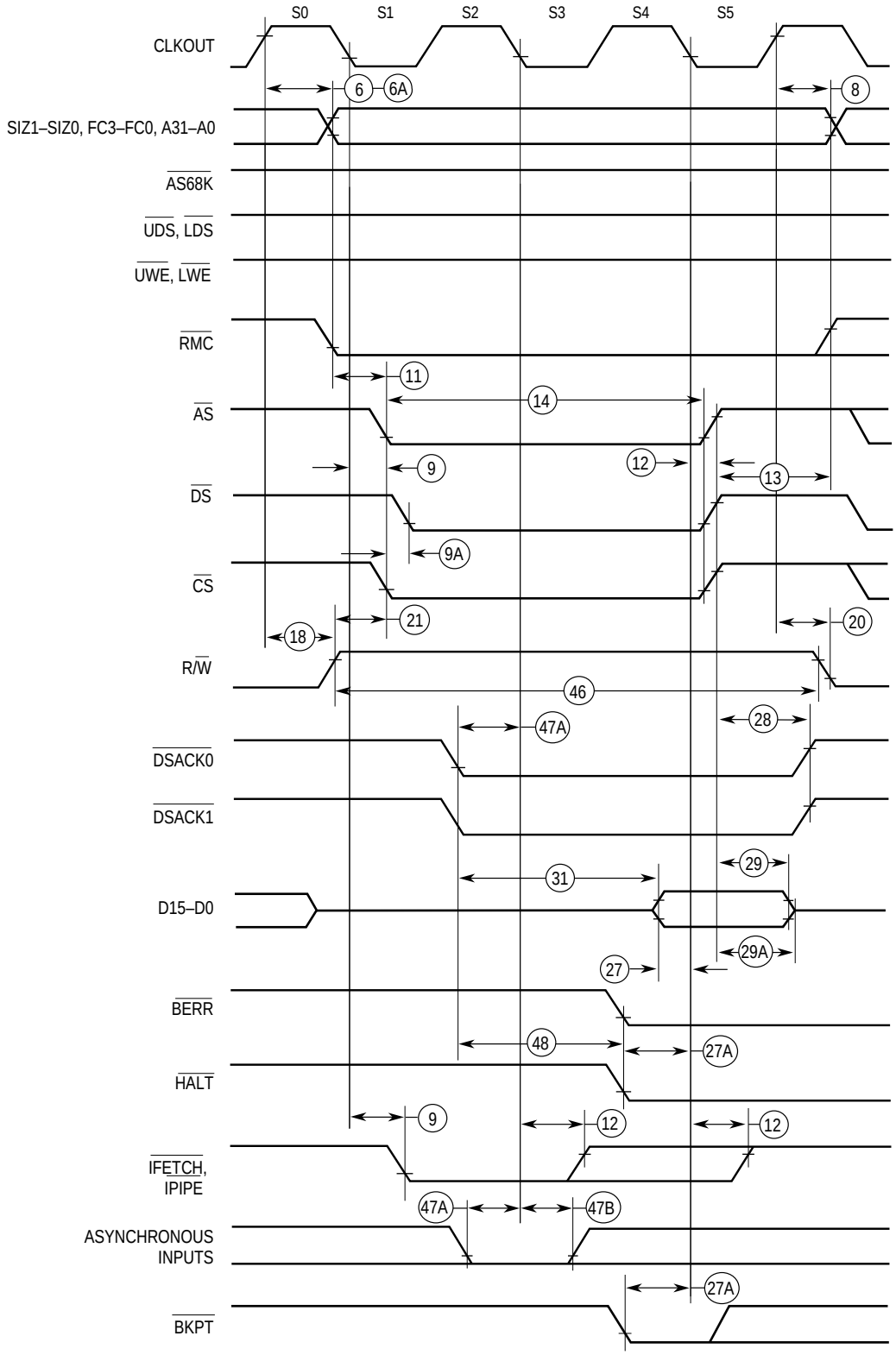

NOTE: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 12-2. M68300 Read Cycle Timing Diagram

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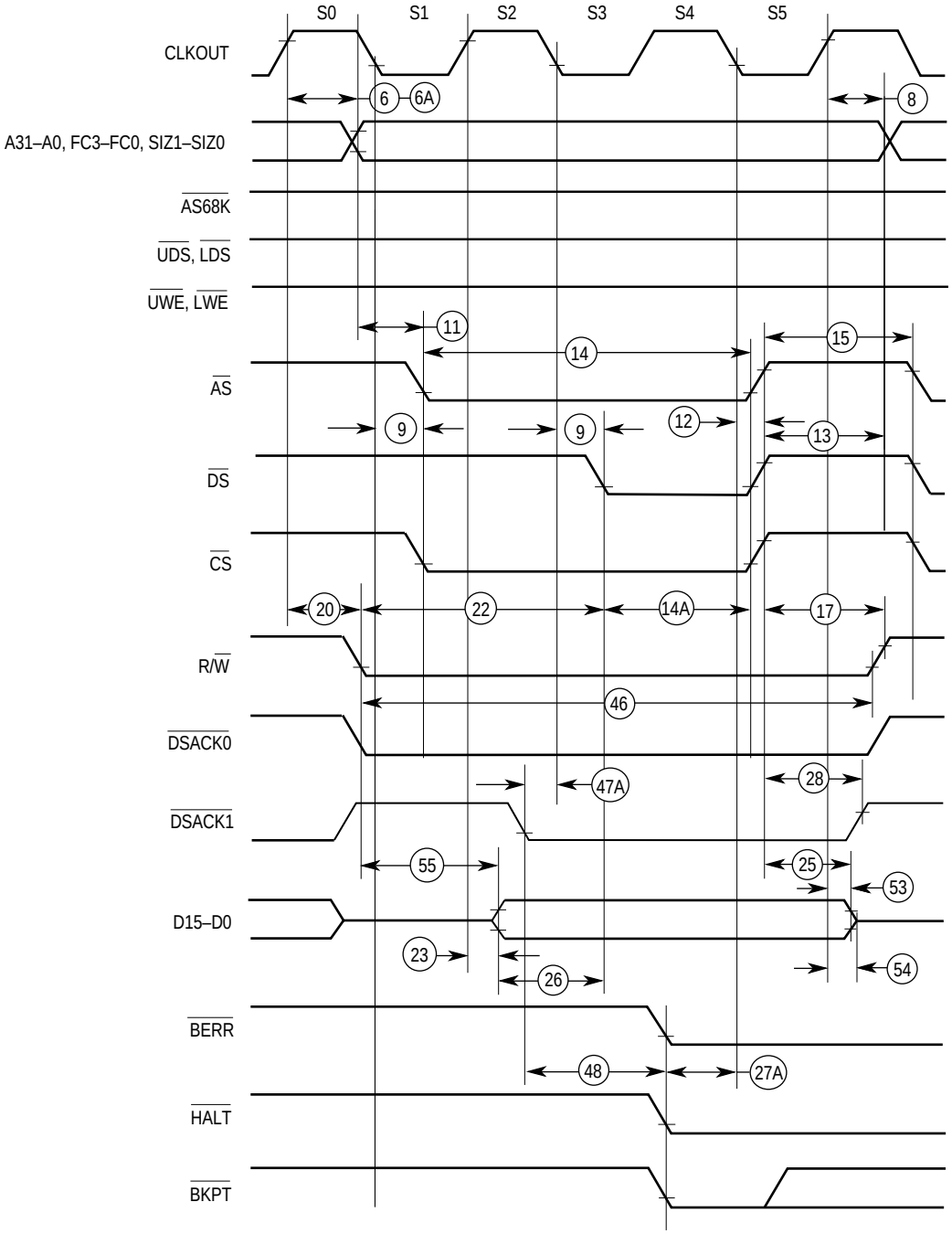

NOTE: All timing is shown with respect to 0.8-V and 2.0-V levels.

Figure 12-3. M68300 Write Cycle Timing Diagram

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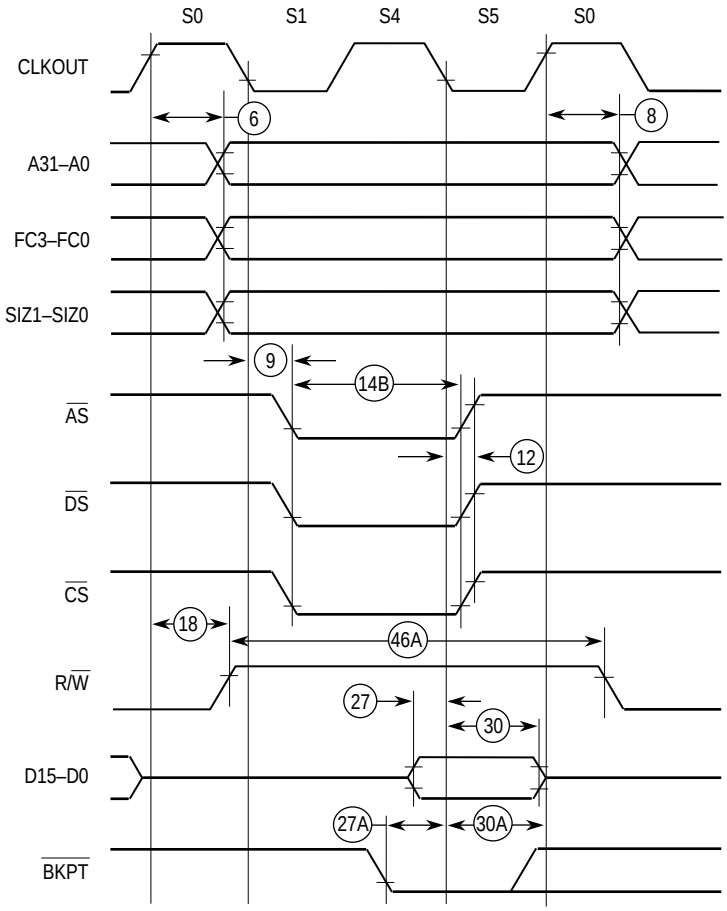

Figure 12-4. M68300 Fast Termination Read Cycle Timing Diagram

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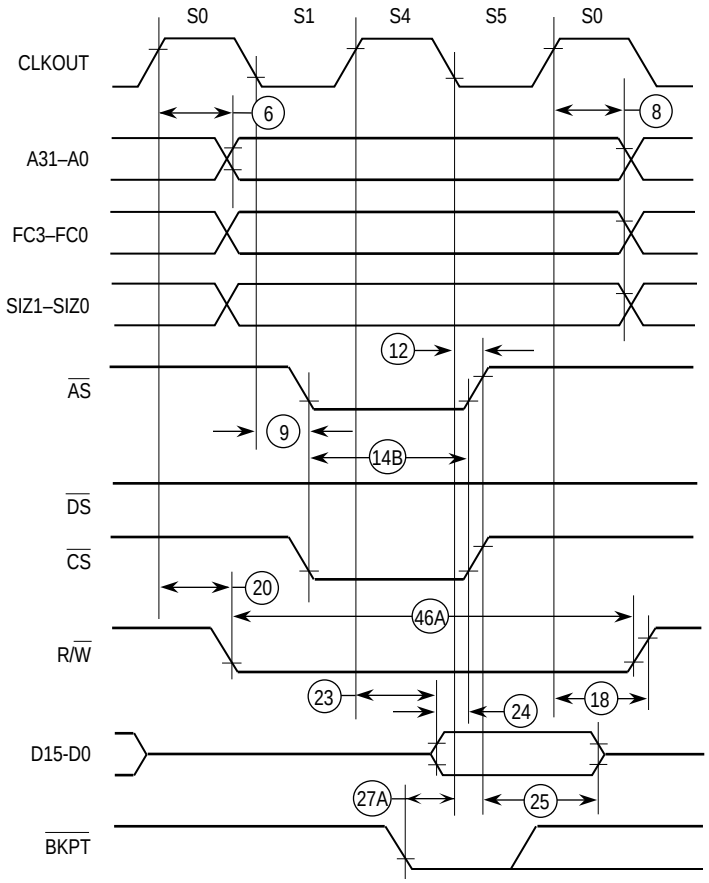

Figure 12-5. M68300 Fast Termination Write Cycle Timing Diagram

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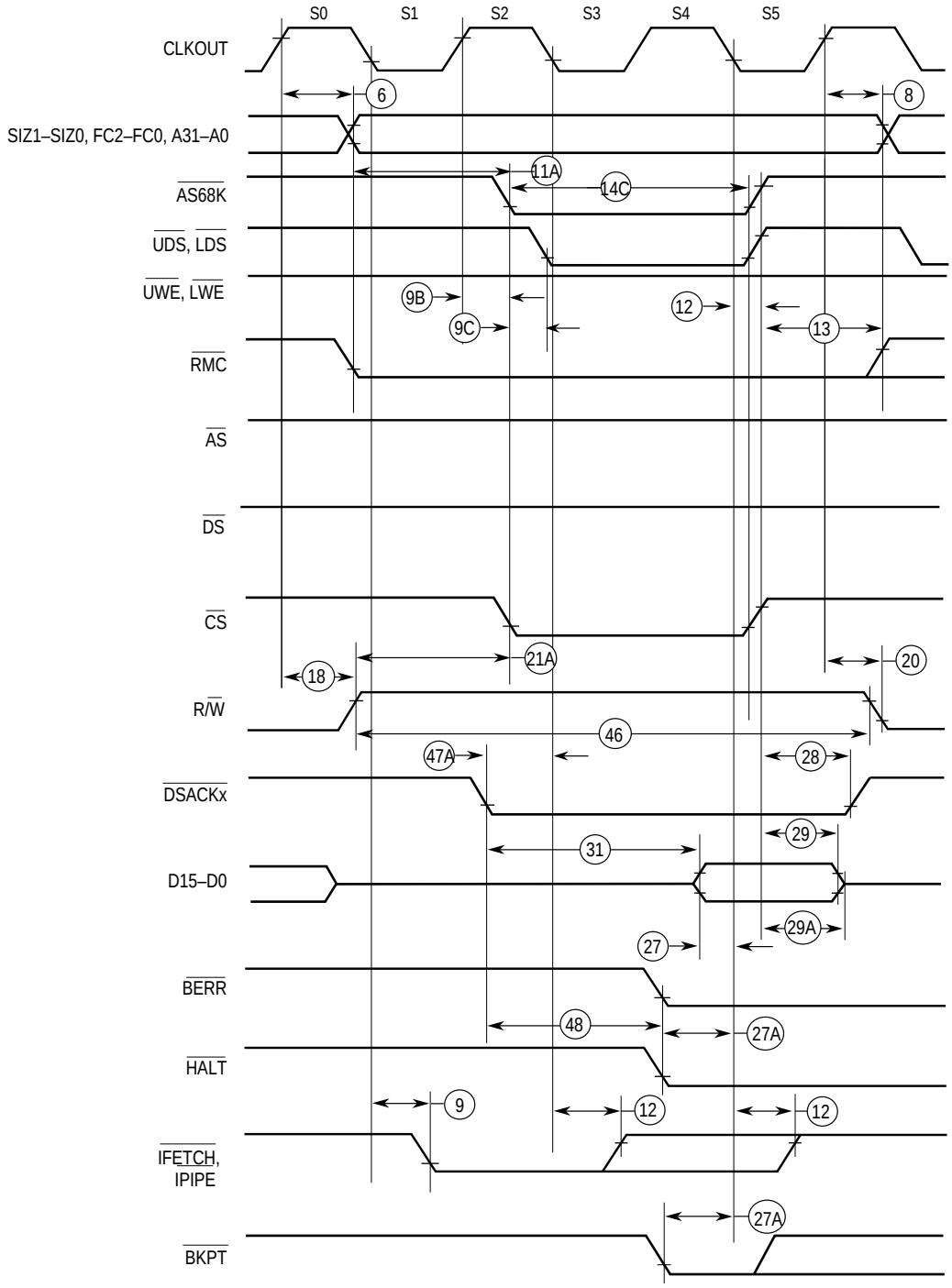

NOTE: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 12-6. 68000 Three-Clock Read Cycle Timing Diagram

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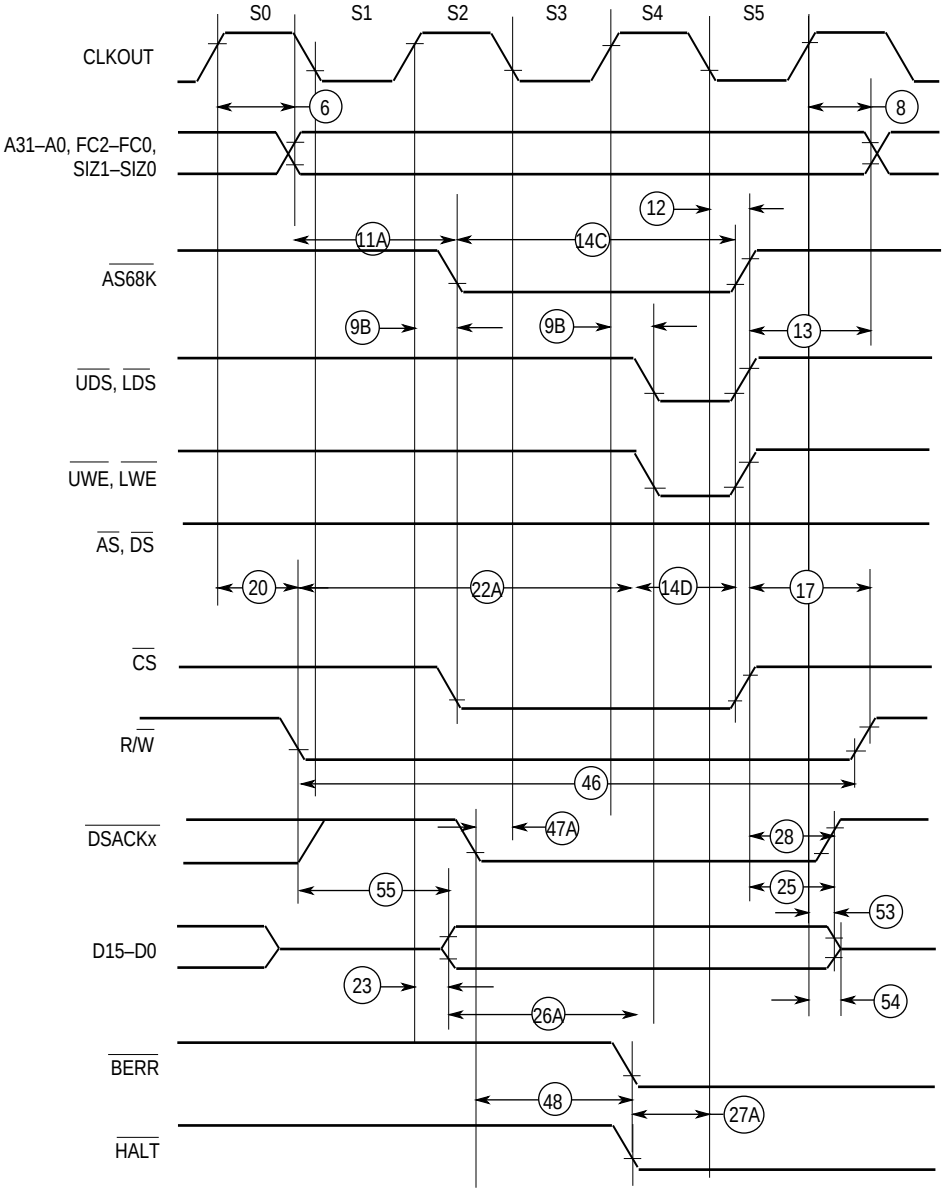

NOTE: All timing is shown with respect to 0.8V and 2.0V levels.

Figure 12-7. 68000 Three-Clock Write Cycle Timing Diagram

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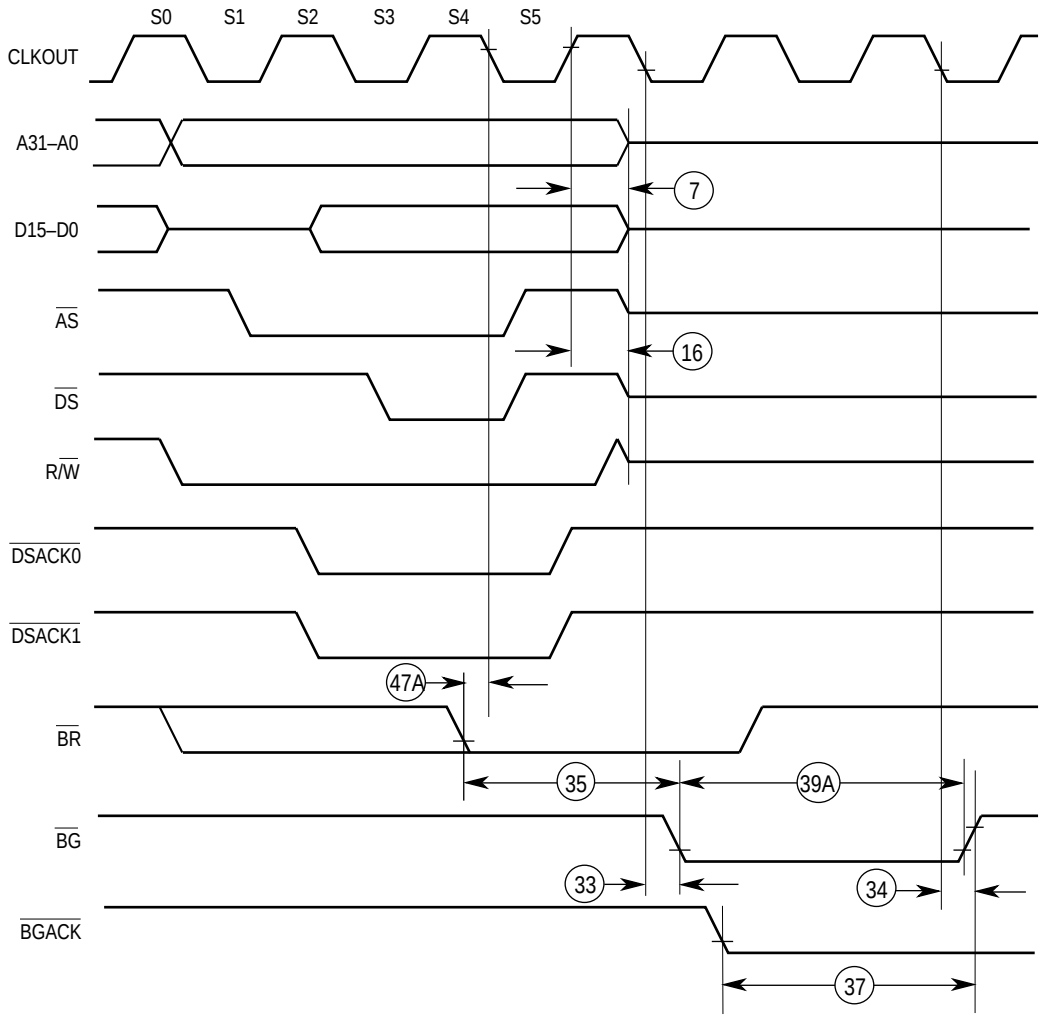

Figure 12-8. Bus Arbitation Timing—Active Bus Case

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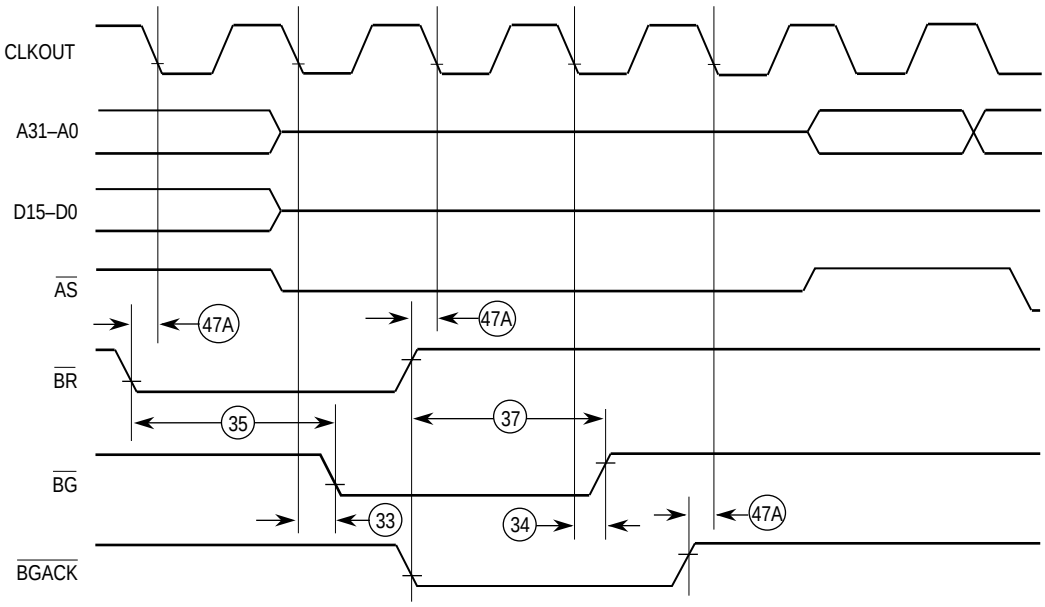

Figure 12-9. Bus Arbitration Timing—Idle Bus Case

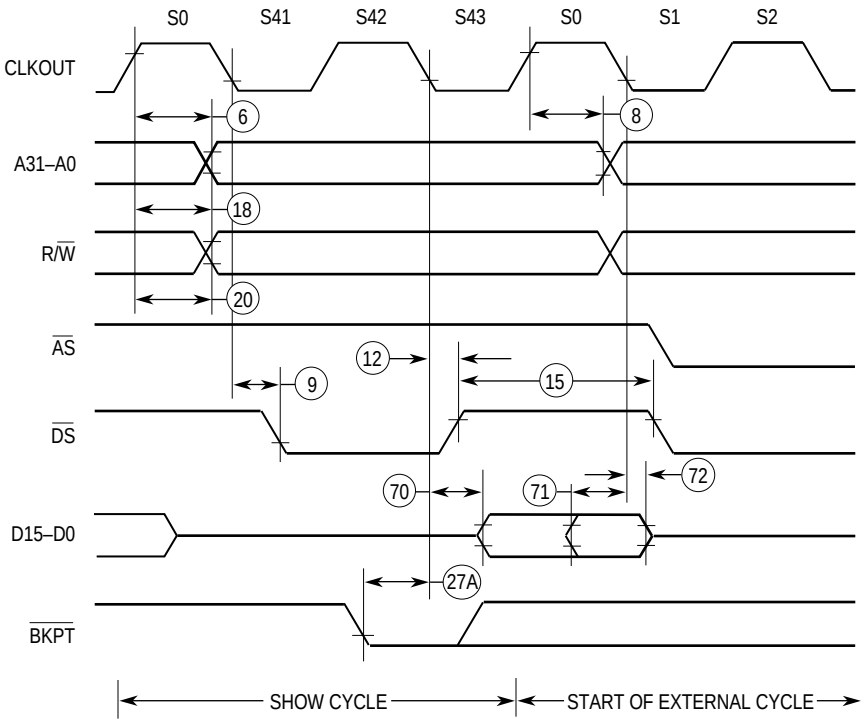

Figure 12-10. Show Cycle Timing Diagram

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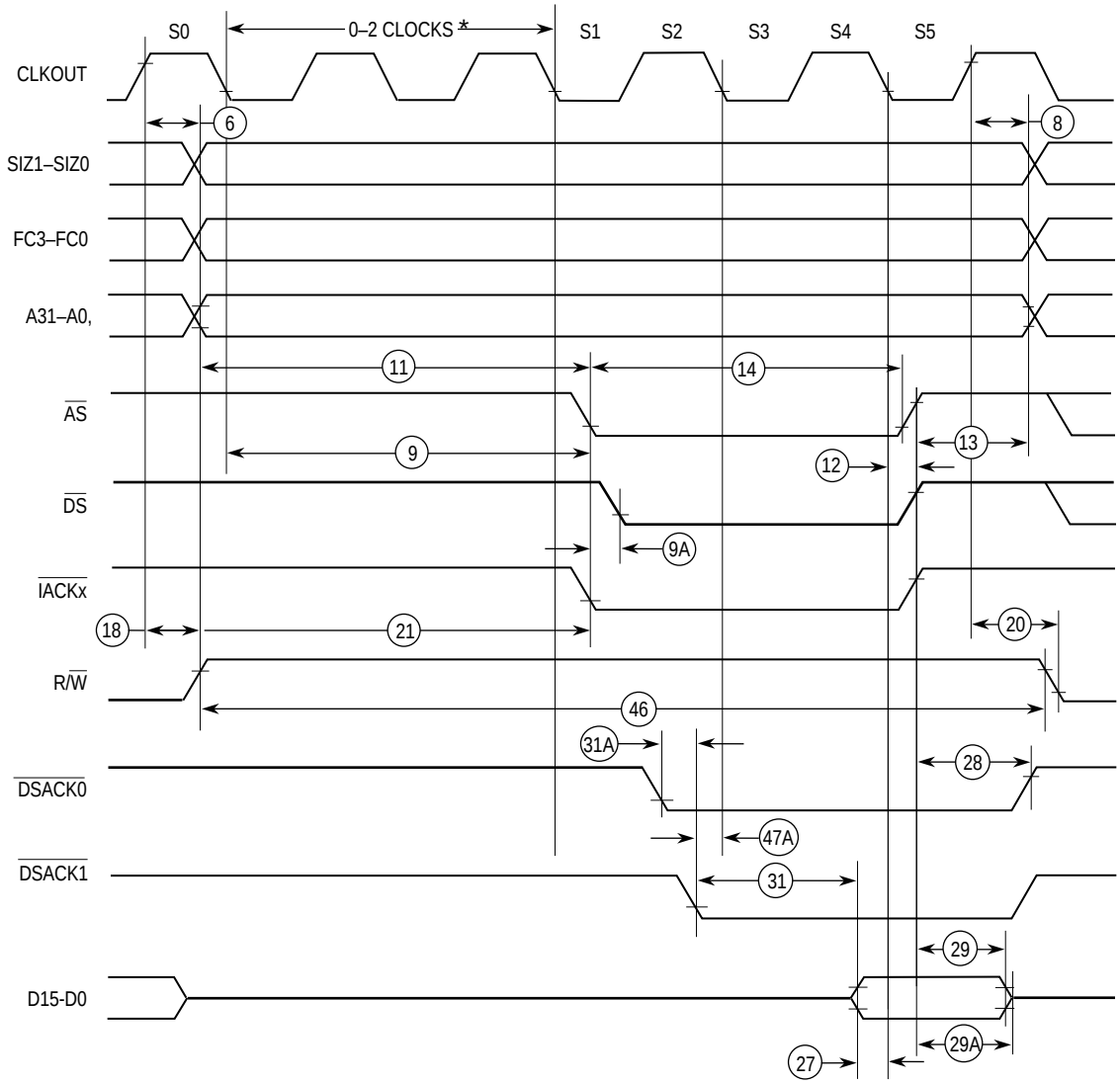

*Up to two wait states may be inserted by the processor between states S0 and S1.

Figure 12-11. IACK Cycle Timing Diagram

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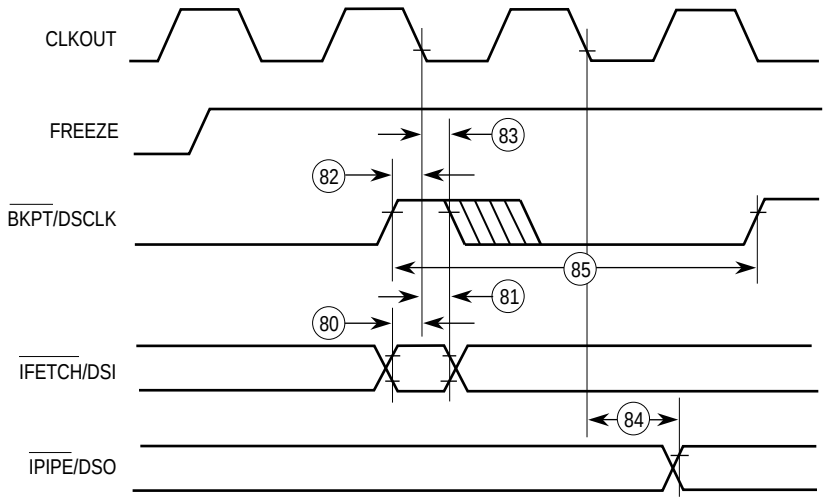

Figure 12-12. Background Debug Mode Serial Port Timing

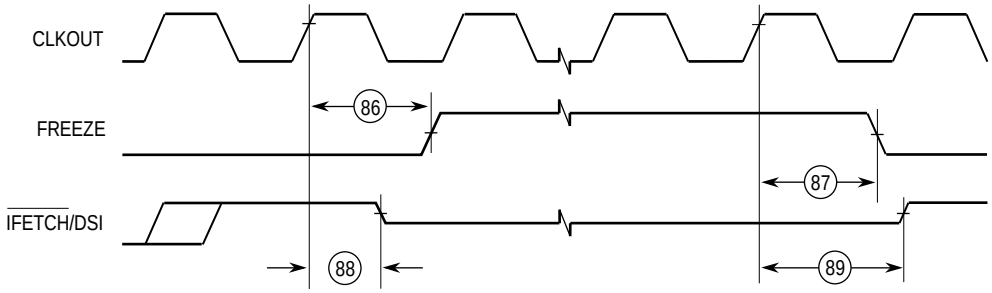

Figure 12-13. Background Debug Mode FREEZE Timing

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12.8 DMA MODULE AC ELECTRICAL SPECIFICATIONS - PRELIMINARY

(GND = 0 Vdc, TA = 0 to 70°C; see Figure 12-14 and 12-15)

Num.	Characteristic	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
1	CLKOUT Low to $\overline{AS}$, $\overline{DACK}$, $\overline{DONE}$ Asserted	—	30	—	20	ns
2	CLKOUT Low to $\overline{AS}$, $\overline{DACK}$ Negated	—	30	—	20	ns
3	$\overline{DREQx}$ Asserted to $\overline{AS}$ Asserted (for DMA Bus Cycle)	$3t_{cyc} + t_{AIST} + t_{CLSA}$				ns
4[1]	Asynchronous Input Setup Time to CLKOUT Low	8, 5	—	5	—	ns
5	Asynchronous Input Hold Time from CLKOUT Low	15	—	10	—	ns
6	$\overline{AS}$ to $\overline{DACK}$ Assertion Skew	–15	15	–10	10	ns
7	$\overline{DACK}$ to $\overline{DONE}$ Assertion Skew	–15	15	–8	8	ns
8	$\overline{AS}$, $\overline{DACK}$, $\overline{DONE}$ Width Asserted	100	—	70	—	ns
8A	$\overline{AS}$, $\overline{DACK}$, $\overline{DONE}$ Width Asserted (Fast Termination Cycle)	40	—	28	—	ns
9	CLKOUT High to $\overline{DTC}$ Asserted	—	30	—	20	ns
10	CLKOUT High to $\overline{DTC}$ Negated	—	30	—	20	ns

NOTES:
1. Specification #4 for 16.78 MHz @ 3.3 V ±0.3 V will be 8 ns.

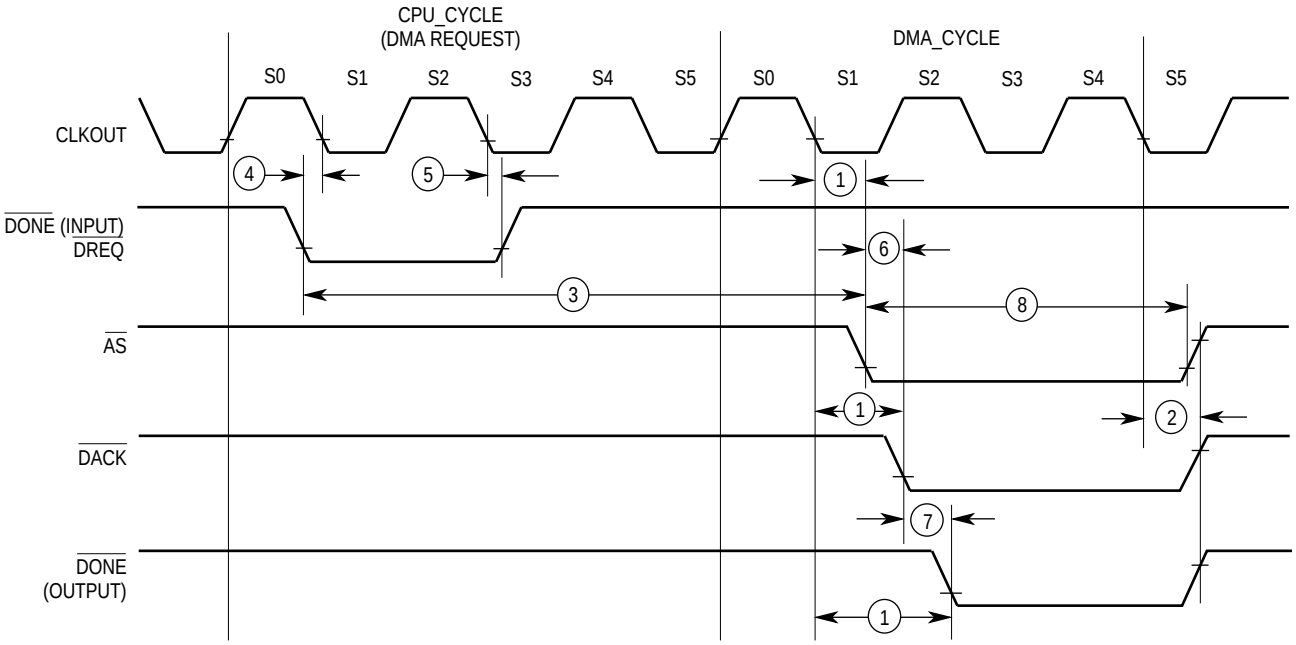

Figure 12-14. DMA Signal Timing Diagram

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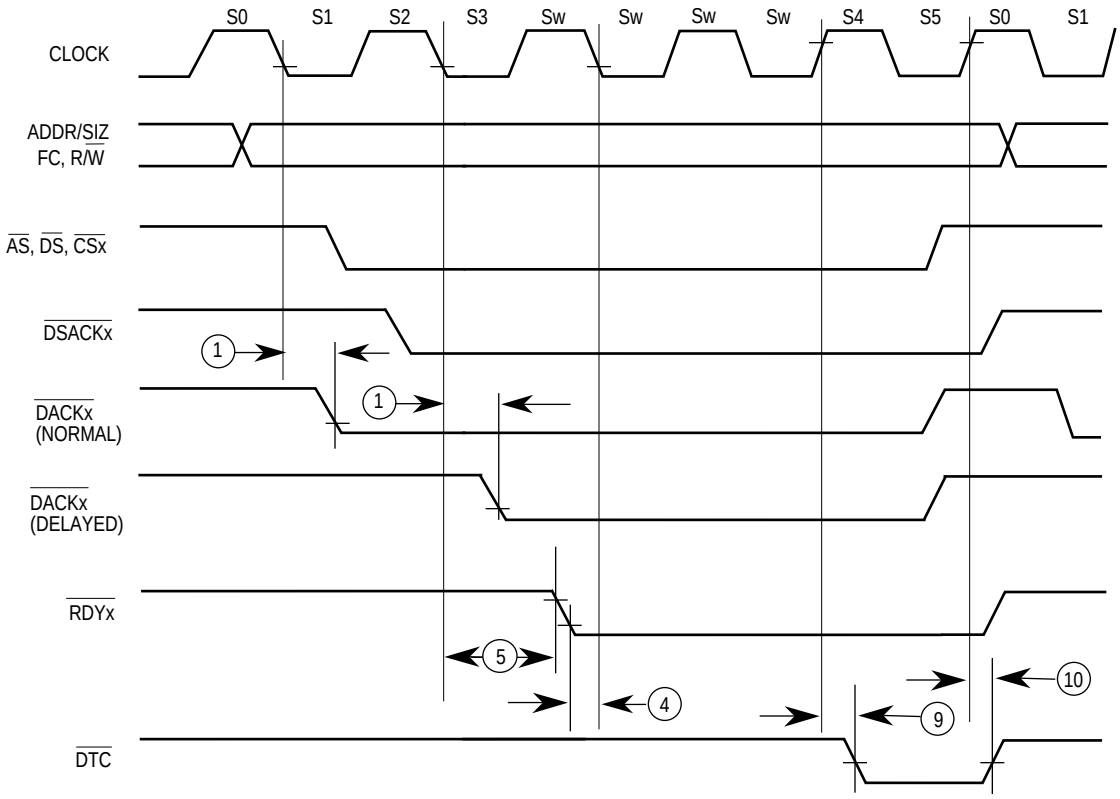

Figure 12-15. DMA Enhancements Timing Diagram

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12.9 TIMER MODULE ELECTRICAL SPECIFICATIONS - PRELIMINARY

(GND = 0 Vdc, TA = 0 to 70°C; see Figures 12-16 and 12-17)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25MHz Min	5.0 V 25MHz Max	Unit
1	CLKOUT Period in Crystal Mode	t_{cyc}	59.6	—	40	—	ns
2	Clock Rise and Fall Time	t_{rf}	—	10	—	5	ns
3	TIN/$\overline{\text{TGATE}}$ High or Low Time, Minimum Pulse Width	—	t_{cyc}+20	—	t_{cyc}+12	—	ns
4[1]	Asynchronous Input Setup Time to CLKOUT Low	—	8, 5	—	5	—	ns
5	Asynchronous Input Hold Time from CLKOUT Low	—	15	—	8	—	ns
6	Asynchronous Input Setup Time to CLKOUT High	—	5	—	3	—	ns
7	Asynchronous Input Hold Time from CLKOUT High	—	15	—	8	—	ns
8	CLKOUT High to TOUT Valid	t_{TO}	3	30	3	20	ns

NOTES:
1. Specification #4 for 16.78 MHz @ 3.3 V ±0.3 V will be 8 ns.

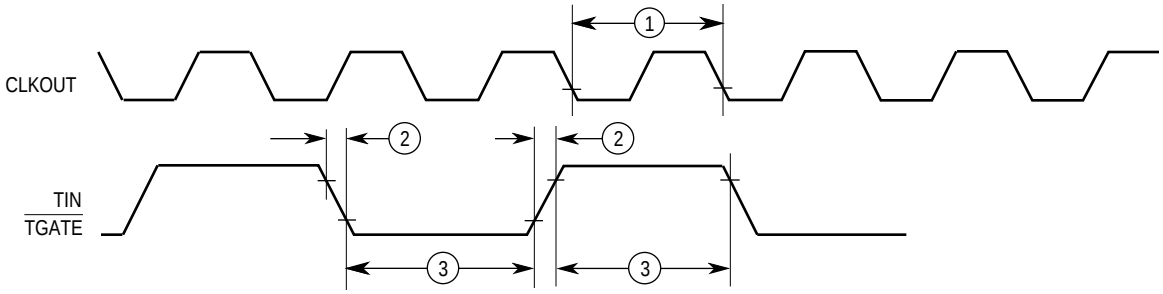

Figure 12-16. Timer Module Clock Signal Timing Diagram

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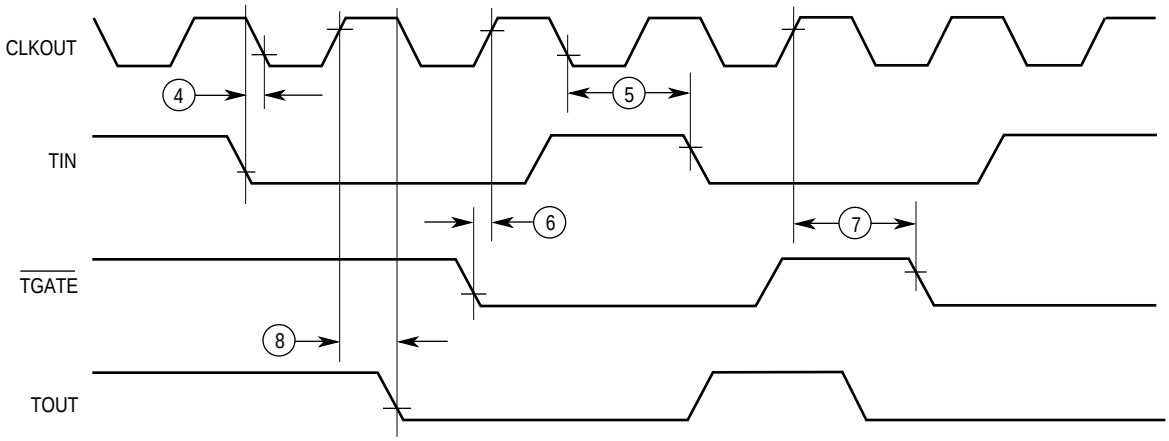

Figure 12-17. Timer Module Signal Timing Diagram

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12.10 SERIAL MODULE ELECTRICAL SPECIFICATIONS - PRELIMINARY

(GND = 0 Vdc, TA = 0 to 70°C; see numbered notes; see Figures 12-18–12-21)

Num.	Characteristic	Symbol	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
1	CLKOUT Cycle Time	t_{cyc}	59.6	—	40	—	ns
2	Clock Rise or Fall Time	t_{rf}	—	10	—	5	ns
3[2]	Clock Input (X1 or SCLK) Synchronizer Setup Time	t_{CS}	8, 5	—	5	—	ns
4	Clock Input (X1 or SCLK) Synchronizer Hold Time	t_{CH}	15	—	8	—	ns
5	TxD Data Valid from CLKOUT High	t_{VLD}	0.5 t_{cyc}				Max
6	X1 Cycle Time	t_{X1}	2.25 t_{cyc}				Min
7	X1 High or Low Time	t_{X1HL}	0.55 t_{cyc} + 0.75(t_{CS} + t_{CH})				Min
8	SCLK High or Low Time, Asynchronous (16x) Mode	t_{AHL}	t_{cyc} + t_{CS} + t_{CH}				Min
9[1]	SCLK High Time, Synchronous (1x) Mode	t_{SH}	t_{cyc}(Gx) + t_{CS}(Gx) + t_{CH}(Gx)				Min
10	SCLK Low Time, Synchronous (1x) Mode	t_{SL}	greater of ({1.5t_{cyc}(Tx) + t_{CS}(Tx) + t_{VLD}(Tx)} + 0.5t_{cyc}(Rx) + t_{CS}(Rx) + t_{CH}(Rx)}) or t_{SH}				Min
11	TxD Data Valid from SCLK Low, Synchronous (1x) Mode	$t_{T \times D}$	1.5t_{cyc}(Tx) + t_{CS}(Tx) + t_{VLD}(Tx)				Max
12	RxD Setup Time to SCLK High, Synchronous (1x) Mode	$t_{R \times S}$	0.5t_{cyc}(Rx) + t_{CS}(Rx) + t_{CH}(Rx)				Min
13	RxD Hold Time from SCLK High, Synchronous (1x) Mode	$t_{R \times H}$	0.5t_{cyc}(Rx) + t_{CS}(Rx) + t_{CH}(Rx)				Min

NOTES:

1. Asynchronous operation numbers take into account a receiver and transmitter operating at different clock frequencies. (Rx) refers to receiver value. (Tx) refers to transmitter value. (Gx) refers to the value that is greater, either receiver or transmitter.
2. Specification #3 for 16.78 MHz @ 3.3 V ±0.3 V will be 8 ns.

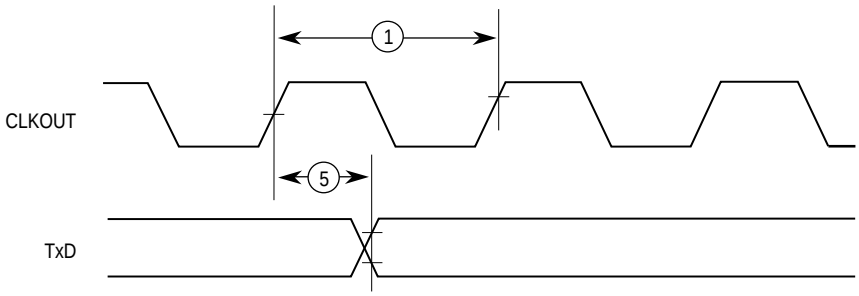

Figure 12-18. Serial Module General Timing Diagram

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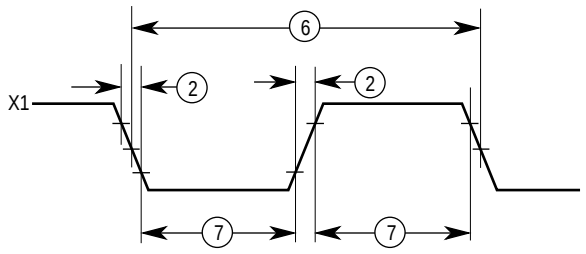

Figure 12-19. Serial Module Asynchronous Mode Timing (X1)

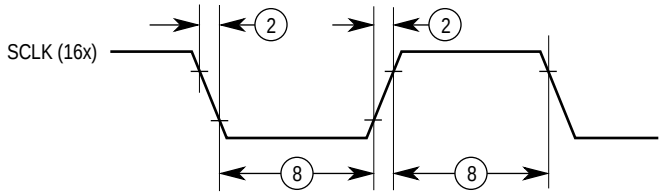

Figure 12-20. Serial Module Asynchronous Mode Timing (SCLK–16X)

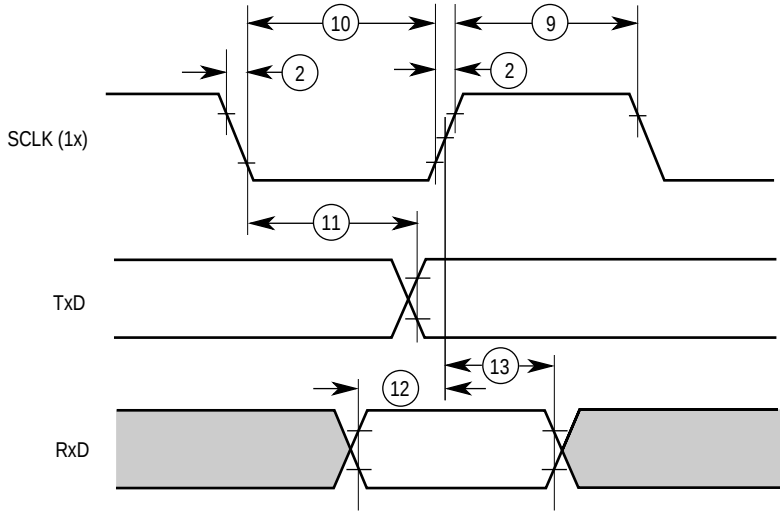

Figure 12-21. Serial Module Synchronous Mode Timing Diagram

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12.11 QSPM ELECTRICAL SPECIFICATIONS - PRELIMINARY

(GND = 0 Vdc, TA = 0 to 70°C; see Figures 12-22–12-25)

Num	Function	Min	Max	Unit
	Operating Frequency			
	Master	DC	1/4	System Clock Frequency
	Slave	DC	1/4	System Clock Frequency
1	Cycle Time			
	Master	4	510	System Clocks
	Slave	TBD	—	System Clocks
2	Enable Lead Time			
	Master	2	128	System Clocks
	Slave	TBD	—	System Clocks
3	Enable Lag Time			
	Master	1/2	1/2	SCK
	Slave	TBD	—	SCK
4	Clock (SCK) High or Low Time			
	Master	2	255	System Clocks
	Slave	2	—	System Clocks
5	Sequential Transfer Delay			
	Master	17	8192	System Clocks
	Slave (Does Not Require Deselect)	13	—	System Clocks
6	Data Setup Time (Inputs)			
	Master Nominal 50	TBD	—	ns
	Slave Nominal 50	TBD	—	ns
7	Data Hold Time (Inputs)			
	Master Nominal 50	TBD	—	ns
	Slave Nominal 50	TBD	—	ns
8	Access Time		1/4	
	Slave	—		SCK
9	MISO Disable Time			
	Slave	—	1/2	SCK
10	Data Valid (after SCK Edge)* Nominal 50			
	Master	—	TBD	ns
	Slave	—	TBD	ns
11	Data Hold Time (Outputs)			
	Master	0	TBD	ns
	Slave	0	TBD	ns
12	Rise Time*			
	Outputs (SCK, MOSI, MISO, PCS1–PCS0)	—	TBD	ns
	Inputs (SCK, MOSI, MISO, SS)	—	TBD	µs
13	Fall Time*			
	Outputs (SCK, MOSI, PCS1–PCS0, MISO)	—	TBD	ns
	Inputs (SCK, MOSI, MISO, SS)	—	TBD	µs

*Assumes 200 pF load on all QSPI pins

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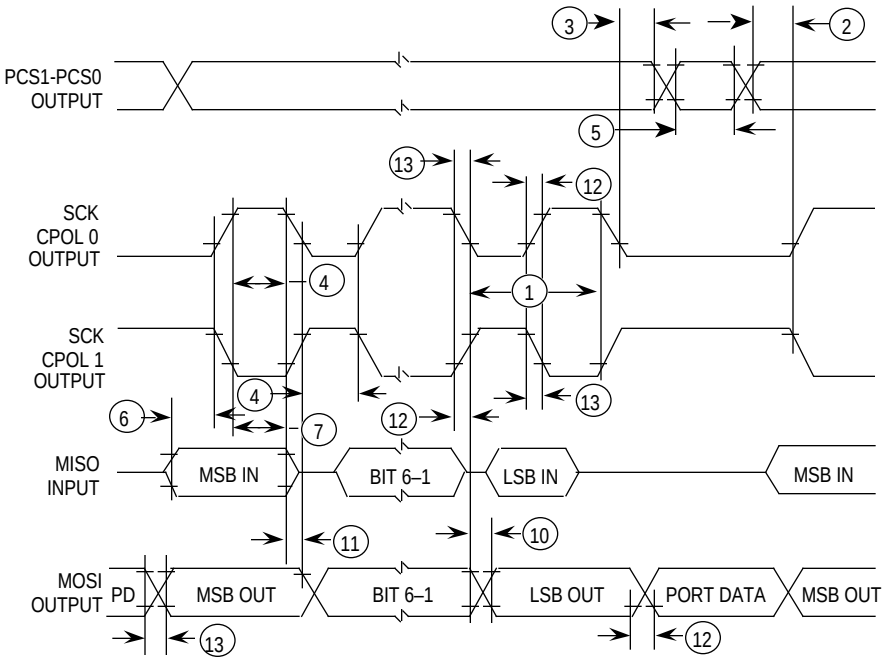

Figure 12-22. QSPI Timing Master, CPHA 0

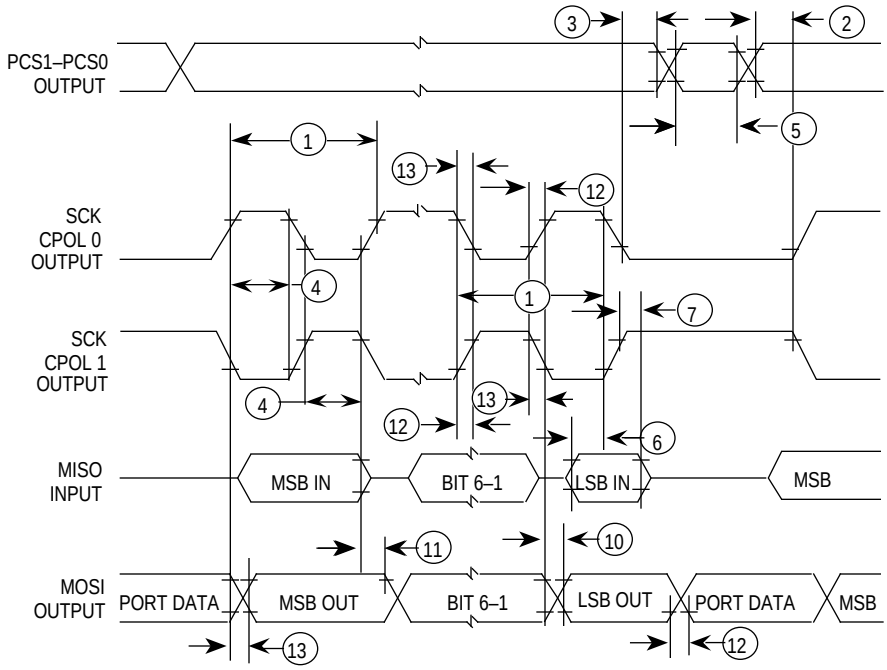

Figure 12-23. QSPI Timing Master, CPHA 1

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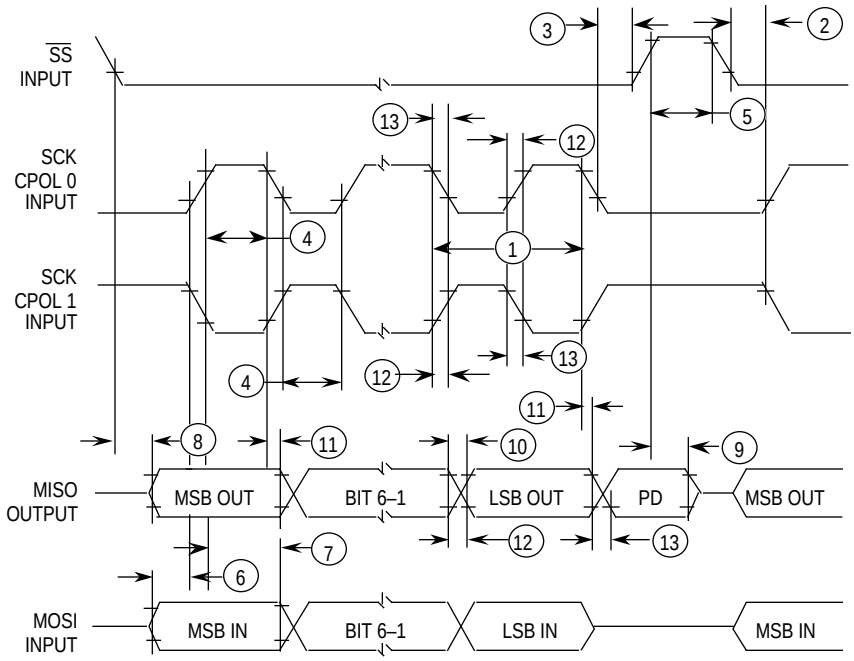

Figure 12-24. QSPI Timing Slave, CPHA 0

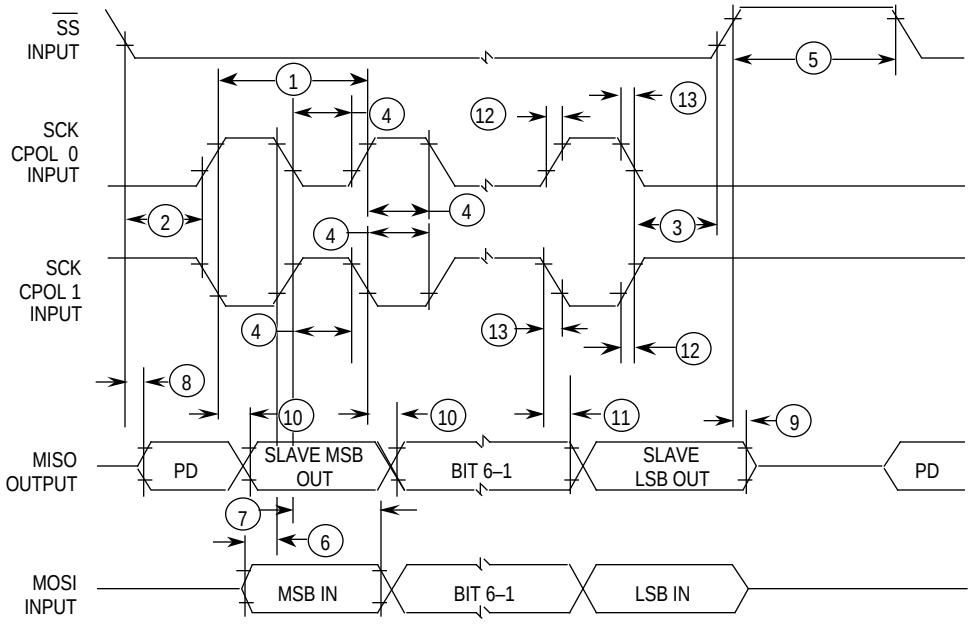

Figure 12-25. QSPI Timing Slave, CPHA 1

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12.12 IEEE 1149.1 ELECTRICAL SPECIFICATIONS

(GND = 0 Vdc, TA = 0 to 70°C; see Figures 12–26—12-28)

Num.	Characteristic	3.3 V or 5.0 V 16.78 MHz Min	3.3 V or 5.0 V 16.78 MHz Max	5.0 V 25.16 MHz Min	5.0 V 25.16 MHz Max	Unit
	TCK Frequency of Operation	0	16.78	0	25	MHz
1	TCK Cycle Time in Crystal Mode	59.6	—	40	—	ns
2	TCK Clock Pulse Width Measured at 1.5 V	28	—	18	—	ns
3	TCK Rise and Fall Times	0	5	0	3	ns
6	Boundary Scan Input Data Setup Time	16	—	10	—	ns
7	Boundary Scan Input Data Hold Time	26	—	18	—	ns
8	TCK Low to Output Data Valid	0	40	0	26	ns
9	TCK Low to Output High Impedance	0	60	0	40	ns
10	TMS, TDI Data Setup Time	15	—	10	—	ns
11	TMS, TDI Data Hold Time	15	—	10	—	ns
12	TCK Low to TDO Data Valid	0	25	0	16	ns
13	TCK Low to TDO High Impedance	0	25	0	16	ns

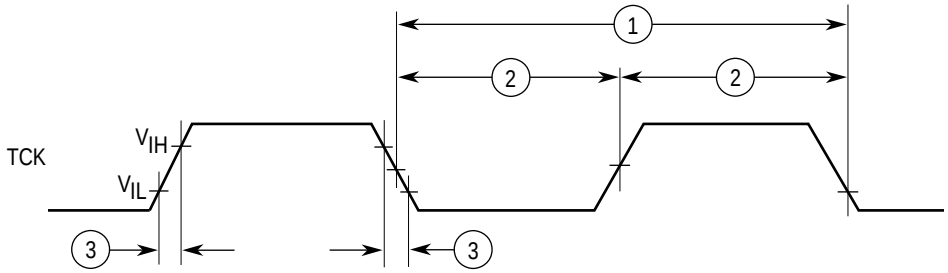

Figure 12-26. Test Clock Input Timing Diagram

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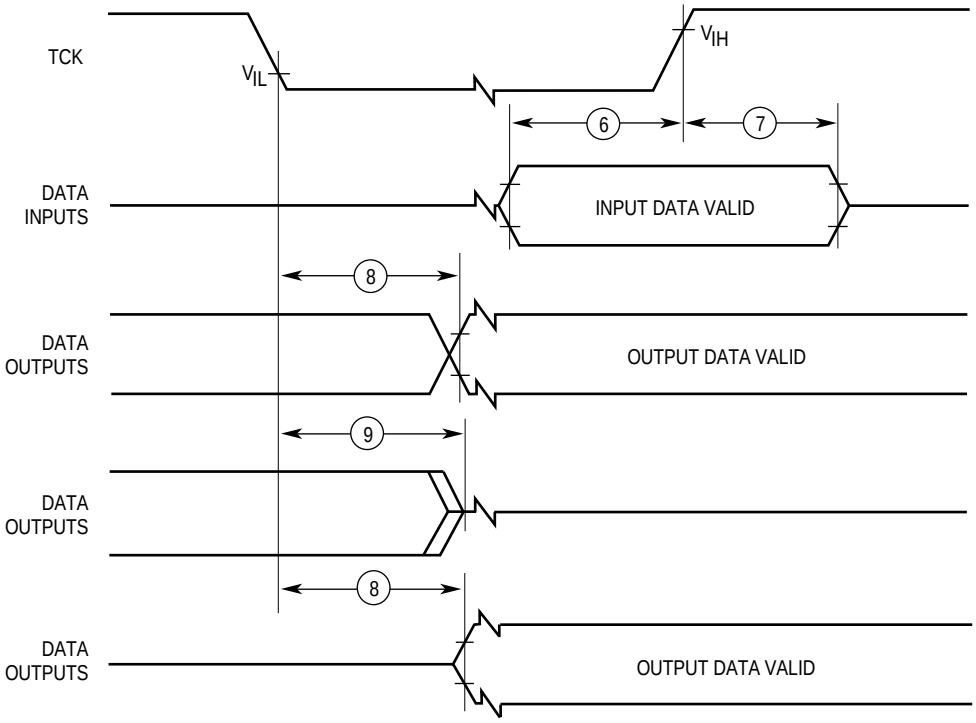

Figure 12-27. Boundary Scan Timing Diagram

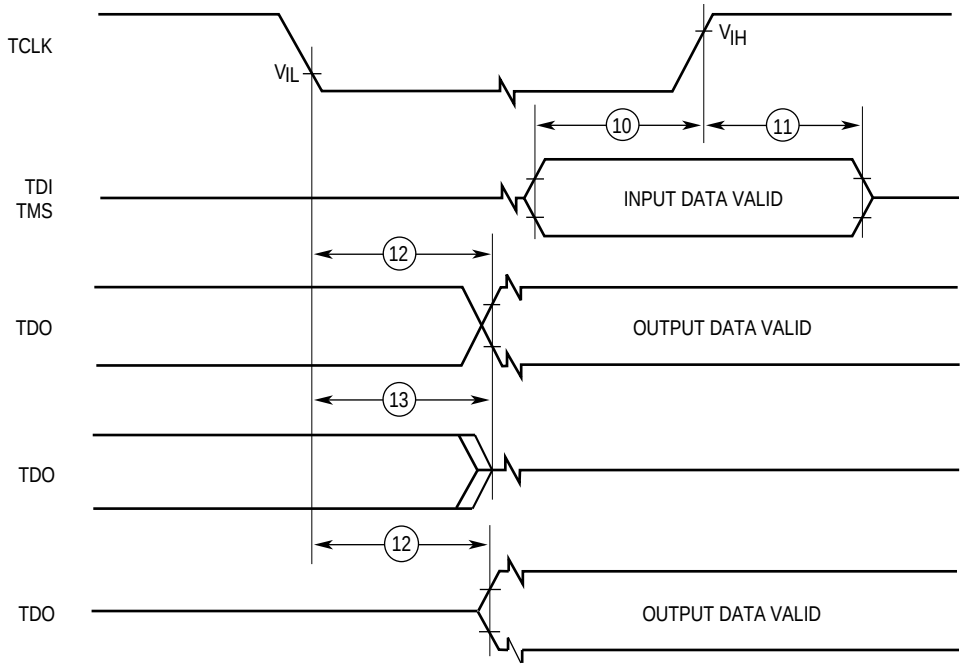

Figure 12-28. Test Access Port Timing Diagram

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SECTION 13
ORDERING INFORMATION AND MECHANICAL DATA

This section contains ordering information, pin assignments and package dimensions of the MC68341.

13.1 STANDARD MC68341 ORDERING INFORMATION

Supply Voltage	Package Type	Frequency (MHz)	Temperature	Order Number
5.0 V	Plastic Quad Flat Pack FT Suffix	0 – 25	0°C to +70°C	MC68341FT25
5.0 V	Plastic Quad Flat Pack FT Suffix	0 – 16.78	0°C to +70°C	MC68341FT16
3.3 V	Plastic Quad Flat Pack FT Suffix	0 – 16.78	0°C to +70°C	MC68341FT16V

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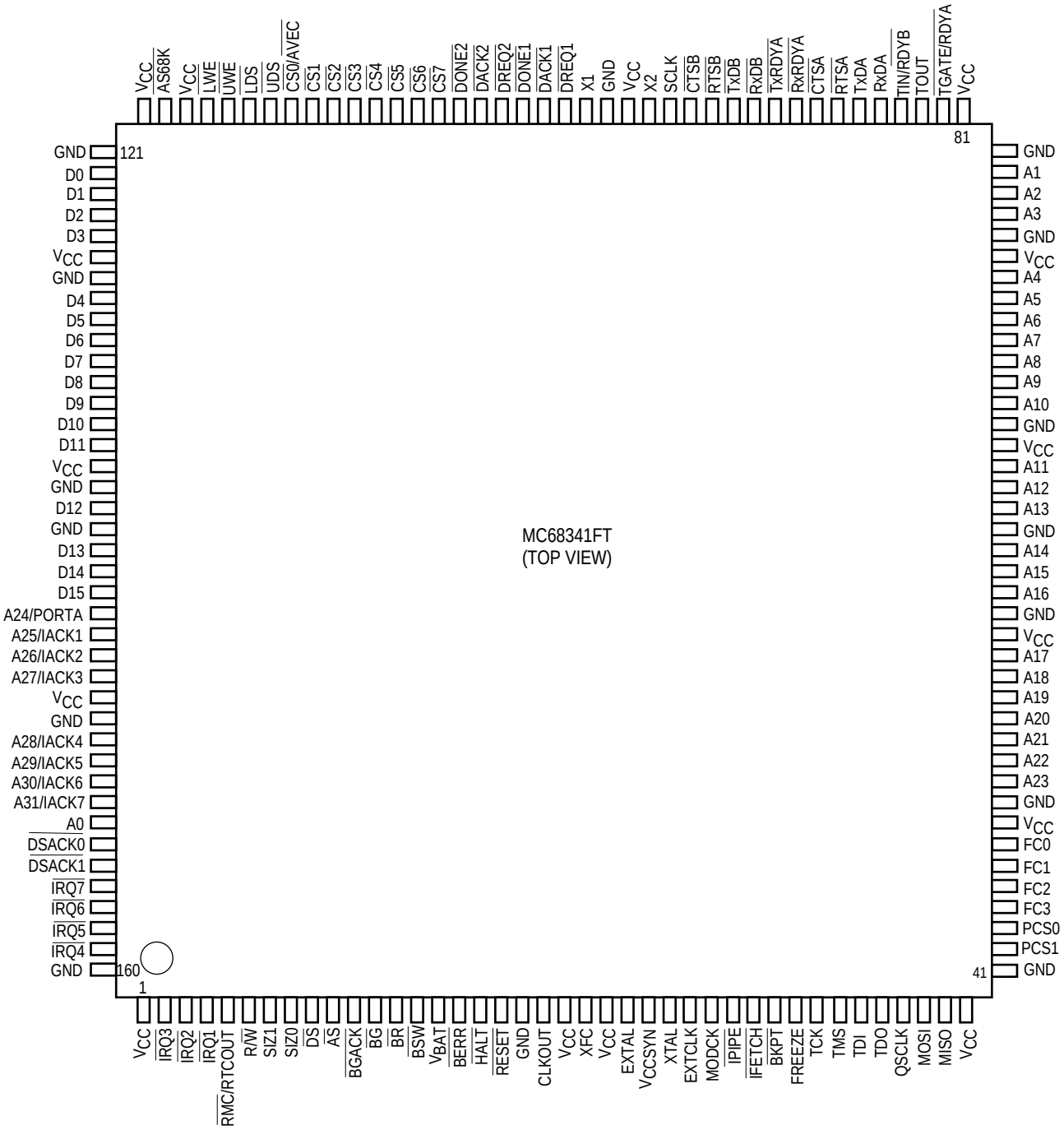
13.2 PIN ASSIGNMENT — PLASTIC SURFACE MOUNT

13.2.1 160-Lead Plastic Quad Flat Pack (FT Suffix)



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13.3 PACKAGE DIMENSIONS

13.3.1 FT Suffix

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