Errata to
MC68302 Integrated Multiprotocol Processor User's Manual

March 19, 1992

This errata applies to the MC68302UM/AD REV2, *Integrated Multiprotocol Processor User's Manual* . The following pages have been amended.

Page:

3-13 In the last sentence of the External Burst Mode paragraph, "before $\overline{\text{DTACK}}$ is asserted" should be replaced by "one setup time (see spec 80) before the S5 falling edge".

In the last two sentences of the External Cycle Steal paragraph, "before $\overline{\text{DTACK}}$ is asserted" and "the time $\overline{\text{DTACK}}$ has been asserted" should be replaced by "one setup time (see spec 80) before the S5 falling edge".

3-14 In the second sentence of the External Device Termination paragraph, "while $\overline{\text{DTACK}}$ is asserted" should be replaced by "one setup time prior to the S5 falling edge (i.e., before or with $\overline{\text{DTACK}}$)".

3-15 In the second paragraph of section 3.1.6, "see Figure 3-9" should be "see Figure 3-12".

3-28 In the description of the ET7—IRQ7 bit, change the note as follows:

"The M68000 always treats level 7 as an edge-sensitive interrupt. Normally, users should not select the level-triggered option. The level-triggered option is useful when it is desired to make the negation of $\overline{\text{IRQ7}}$ cause the IOUT2–IOUT0 pins to cease driving a level 7 interrupt request when the MC68302 is used in the disable CPU mode. This situation is as follows:

For a slave-mode MC68302, when it is triggered by $\overline{\text{IRQ1}}$, $\overline{\text{IRQ6}}$, or $\overline{\text{IRQ7}}$ to generate an interrupt, its interrupt controller will output the interrupt request on pins IOUT2–IOUT0 to another processor (MC68302, MC68020, etc.). For cases when the slave MC68302 does not generate a level 4 vector (i.e., VGE bit is cleared), one must set the ET1, ET6, and ET7 bits to level-triggered and then negate the $\overline{\text{IRQ1}}$, $\overline{\text{IRQ6}}$, and $\overline{\text{IRQ7}}$ lines externally in the interrupt handler code. If the ET1, ET6, and ET7 bits are set to edge-triggered and the VGE bit is clear, the IOUT2–IOUT0 pins will never be cleared."

3-41 In the last paragraph, "either starts a new time count immediately or continues to run." should be "either resets to zero on the next clock or continues to run.".

3-47 In the second paragraph, "see Figure 6-13" should be "see Figure 6-14".

3-53 In the last paragraph, "R = 700kW" should be "R = 700kΩ".

3-60 In item 2 of section 3.8.4, the second sentence should be "When $\overline{BG}$ is sampled as low by the MC68302, it waits for AS, BERR, HALT and BGACK to be negated, and then asserts BGACK and performs one or more bus cycles."

3-63 Add a note to Table 3-9:
"4. The bus arbitration priority for IDMA in the two rightmost columns of the table applies only to the case when the IDMA request is internally generated; for the cases of external request, the bus arbitration priority of IDMA is right below that of SDMA."

3-63 At the end of the first sentence of the third paragraph that ends "... provided BCLM in the SCR is set", add "and the IDMA request is internally generated."

4-3 In the second paragraph, "see 3.8.9" should be "see 3.9".

4-6 In the first paragraph, change the second to the last sentence to “The CP-reset resets the SCCs to the state following hardware reset, but it does not affect the serial interface (the parallel I/O, the configuration of the SIMODE and SIMASK registers, and the SCON register).”

4-10 In Figure 4-4, the labels "SCC2" and "SCC3" should be switched.

4-29 In the descriptions of TCS and RCS, "After reset" should be "After system reset".

4-34 In the description of automatic echo, add a sentence: "The CD must be asserted for the receiver to receive data".

4-41 In the last paragraph, "and before the ENTER HUNT MODE" should be "and after the ENTER HUNT MODE".

4-57 At the end of the description of the ENTER HUNT MODE command, add a new sentence "In the UART mode, none of the data received in the FIFO is lost when ENTER HUNT MODE command is issued; however, this command does reset the receive FIFO in other protocols, e.g., HDLC."

4-83 "18-bit HDLC address recognition" should be 8-bit.

4-133 In the TX bit description for DDCMP mode, "transmission of the last" should be "transmission of the second-to-last".

4-154 In the TX bit description for transparent mode, "on the last bit" should be "on the second - to-last bit".

5-7 In the DISCPU pin description, add a new sentence: "The disable CPU (slave) mode will not take effect until the third clock edge during a power-on reset sequence."

5-9 In the first paragraph, add a new sentence "When the $\overline{UDS}$/A0 pin is used as A0 (i.e., the BUSW pin is low), then the pin takes on the timing of the other address pins, as opposed to the strobe timing."

5-19 In the last paragraph, add two sentences "The BRG clock output on the BRG pins is 180 degrees out of phase with the BRG clock output on the RCLK and TCLK pins. This statement applies to all BRG pins: BRG1, BGR2, and BRG3."

6-6 In spec 29, the value for 20 MHz Max should be " — ", not "95".

6-11 Spec. 62 is correct in page 6-7. In Figure 6-4, it is shown one half cycle too early.

6-13 Note 3 should say "$\overline{BR}$ will not be asserted while $\overline{BG}$, $\overline{HALT}$, or $\overline{BERR}$ is asserted."

6-13 In the description of spec 97, "Clock High" should be "Clock Low".

6-14 In Figure 6-6, spec 97 should be modified to be measured at the S5 falling edge, not at the S4 rising edge as shown.

6-15 The bubble labelled "6" should be labelled "84".

6-34 In the description of spec 302, "Falling Edge" should be "Rising Edge".

In note 2, add the following sentences:

"This note should only be used if the user can guarantee that only one sync pin (L1SY0 and L1SY1) is changed at a time in the selection andde-selection of the desired PCM channel time slot. A safe example of this is using only PCM CH-1.
Another example is using CH-1 and CH-2 only, whereCH-1 and CH-2 are not contiguous on the PCM highway."

D-14 On the third line from the bottom, the comment, "Normal mode, v7 – v5 = 3" should be "Normal mode, v7 – v5 = 5".

D-15 On the seventh line from the top, the comment, " * v7 – v5 = 3 ..." should be
" * v7 – v5 = 5, v4 – v0 = $0d => vector = $ad => Exception vector = ($ad- 4) = $2b4".

D-25 The line "Move.W #$0, $7006aa ;UADDR2=0000" should be
"Move.W #$0, $7006ac ;UADDR2=0000".

Add one more instruction for the setting of the control character:

"Move.W #$0000,$7006be ; No flow control character to transmit.

D-53 In Figure D-19:
- The resistor connected to the master's A23 should be 4K instead of 1K.
- The resistor connected to the slave's A23 should be 2K instead of 1K.
- The DISCPU pin of the master should be tied to ground, not +5V.
- The DISCPU pin of the slave should be pulled high, not grounded.
- The resistor on the $\overline{BR}$ line should be 820 instead of 1K.

D-57 In Figure D-21, the labels "SCC2" and "SCC3" should be switched.

D-74 Before the last paragraph, add the following paragraph:

"In the transparent operation, assertion of $\overline{RTS1}$ is slightly different from that of $\overline{RTS2}$ and $\overline{RTS3}$. The description of $\overline{RTS}$ in Table D-4, the text on D-73, Figure D-29, and the text on D-74 is correct for $\overline{RTS2}$ and $\overline{RTS3}$, but not exactly correct for $\overline{RTS1}$. $\overline{RTS1}$ has the

opposite polarity in PCM mode. $\overline{RTS1}$ goes low when SIMODE is programmed as the PCM mode, and then goes high when the SCC is about ready to transmit."

E-6 RCS should refer to RCLK pin, rather than to TCLK pin.