Peripheral Bus Control CPLD

Wireless Solutions Division

Eyal Liser

Version 0.5

May 3, 2005

freescale semiconductor

Revision Table

Notes	Author	Date	Version
Initial version. Applied appropriate changes to ZAS PBC document to fit Tortola ADS	Eyal Liser	March 25, 2005	Revision 0.0
Interrupt controller added to the document.	Eyal Liser	April 14, 2005	Revision 0.1
Interrupt description revised	Eyal Liser	April 18, 2005	Revision 0.2
Some power up defaults changed, formatting revised,	Eyal Liser	May 2, 2005	Revision 0.3
Revised interrupt section per OS teams requests	Eyal Liser	May 3, 2005	Revision 0.4
UART selects Default changed. Vibrator default value changed. PCMCIA_EN bit added on BCTRL4(5)	Eyal Liser	May 24, 2005	Revision 0.5

1.1 Introduction

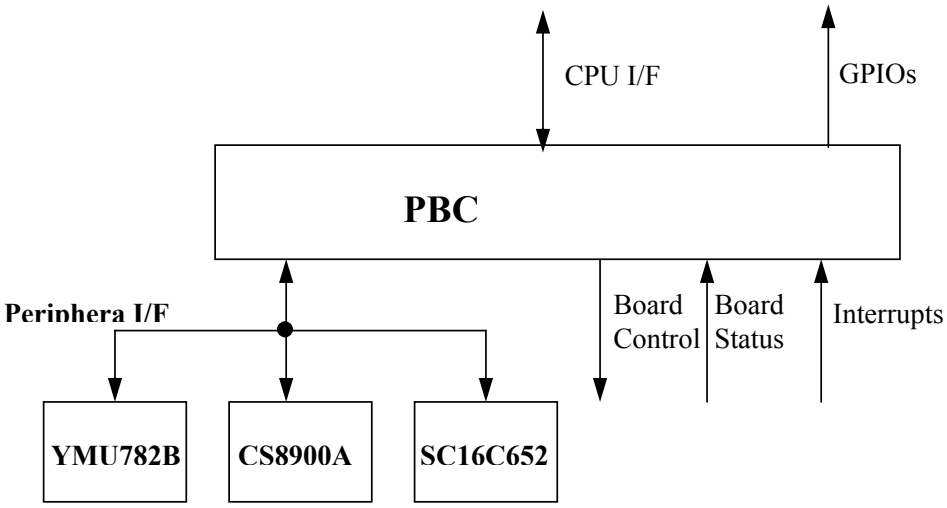
The Tortola EVB main board requires some glue logic for peripheral bus address decoding, board control and status signals, board revision registers, and other miscellaneous functions. This glue logic is implemented with a Complex Programmable Logic Device (CPLD). This document describes the functionality and requirements for the Peripheral Bus Control CPLD (PBC).

1.2 Features

The key features provided by the PBC include:

- Provide a 16-bit slave interface to the CPU data bus
- Provide address decode and control for Ethernet controller
- Provide address decode and control for external UART controller
- Provide address decode for Audio Synthesizer.
- Provide control and status registers for various board functions.
- Provide control and muxing for interrupt sources from various sources.

1.3 Block Diagram



1.4 CPU Interface

The Tortola CPU WEIM interface, referred in this document as the CPU Interface, has the capability to connect low to mid-range memories and peripherals with asynchronous and synchronous protocols. Several chip select signals are provided by the CPU, which can be configured for different memory types. The PBC uses the chip select signal CS4, with the following requirements:

- CS4 occupies a 32Mbyte window in the address space
- CS4 must be configured for 16-bit bus width, asynchronous transfers.
- CS4 assertion window must be at least 150nsec.
- Byte enables must be asserted at CS4 assertion time.
- Byte enables must be negated at least 1/2 clock before CS4 negation during write cycles.
- Multiplexed transfers and synchronous transfers are not supported.

Table 1 CPU Signal Interface

Signal	DIR	Description
A[25:0]	In	Address bus (not all address lines are used)
D[15:0]	In/Out	Data bus
CS4_B	In	Chip select 4 used for peripheral access
BE0_B	In	Byte Enable 0, which corresponds with D[7:0]
BE1_B	In	Byte Enable 1, which corresponds with D[15:8]
OE_B	In	Output Enable
RW_B	In	Read/write signal
RSTIN_B	In	Reset signal
DMAREQ	Out	DMA Request to CPU

1.5 Peripheral Interface

The peripheral interface provides address decode and control for the CS8900A Ethernet controller the SC16C652 dual UART (DUART) controller and the YMU782B Audio Synthesizer.

Table 2 Peripheral Interface

Signal	DIR	Description
PBA[2:0]	Out	Peripheral Bus Address
PBD[7:0]	InOut	Peripheral Bus Data, used for DUART, board version, switches
IOR_B	Out	IO Read is asserted during I/O read transfers and DMA transfers
IOW_B	Out	IO Write is asserted during I/O write transfers
MEMR_B	Out	Memory read to Ethernet controller is asserted during memory read transfers.
MEMW_B	Out	Memory write to Ethernet controller is asserted during memory write transfers.
AEN	Out	DMA Address enable, asserted during Ethernet controller DMA transfers
ENET_DMAREQ	In	DMA request from Ethernet controller
ENET_DMACK_B	Out	DMA acknowledge to Ethernet controller
ENET_CS_B	Out	Ethernet chip select
UA_CS_B	Out	UART A chip select
UB_CS_B	Out	UART B chip select
SYNTH_CS	Out	Synthesizer chip select

1.5.1 Peripheral Bus Cycles

The following peripheral bus cycles are implemented.

Table 3 Bus Cycles

Cycle	Transfer size	Description
IOREAD	Byte, Word	Used to read 8/16-bit data from peripheral registers with IOR_B signal.
IOWRITE	Byte, Word	Used to write 8/16-bit data to peripheral registers with IOW_B signal.
MEMREAD	Byte, Word	Used to read 8/16-bit data from peripheral memory using MEMR_B signal.
MEMWRITE	Byte, Word	Used to write 8/16-bit data to peripheral memory using MEMW_B signal.
DMAREAD	Word	Used during Ethernet DMA transfers to read 16-bit data from Ethernet controller memory buffer using ENET_DMACK_B signal.

1.5.2 DMA operation

The CS8900A supports DMA slave transfers for received data frames. The PBC supports these DMA transfers using a single DMAREQ signal to the processor and a special DMA address space in the memory map. The ENET_DMAREQ signal from the CS8900A is forwarded to the CPU I/F and used as a qualifier for DMA transfers. Qualified read transfer to the DMA address space will generate the ENET_DMACK_B signal to the CS8900A.

1.5.3 SC16C652C UART Decode

The PBC provides address decodes and data path control for the SC16C652C dual UART controller. Data is transferred through the PBC to and from the SC16C652C. The PBC hardware provides byte steering logic to transfer the correct byte to the SC16C652C during data transfers. The following points must be followed for accessing the SC16C652C

1.5.4 SCS8900A Ethernet Decode

The PBC provides address decode and control for the CS8900A Ethernet controller. Both 16-bit I/O mode and memory mode are supported. Memory mode operation allows direct access to the CS8900A internal registers and frame buffer. A single DMA request line is provided for DMA transfers from the CS8900A buffer to system memory for increased performance.

The following points must be followed for accessing the CS8900A:

- Provide a transition of the SBHE input after reset. This is done with a dummy byte read to an odd location, as for example a byte read to $B400_0007.
- All reads and writes to the CS8900A must be 16-bits.
- For memory mode operation, the MEMORY BASE ADDRESS REGISTER (Offset $002C) must be set to $1000. Note that this is a 20 bit register, and the upper 4 bits must be 0.

1.5.5 YMU782B Audio Synthesizer Decode

The PBC provides address decode and data path control for the YMU782B Audio Synthesizer. Data is transferred through the PBC to and from the YMU782B. The PBC hardware provides byte steering logic to transfer the correct byte to the YMU782B during data transfers. The following points must be followed for accessing the YMU782B:

- All reads and writes to the YMU782B must be 8-bits.

1.6 UART Muxing

UARTC has one DTR line coming from the UART transceiver. This line is muxed to either UART1 or UART2 of the CPU. The muxing is made according to UARTC_SEL (BCTRL2.2) .

1.7 Memory Map

Table 4 PBC Memory Map

Name	Description	Address
VERSION	Version register	B400_0000
BSTAT2	Board status register 2	B400_0002
BCTRL1	Board control register 1 set address	B400_0004
	Board control register 1 clear address	B400_0006
BCTRL2	Board control register 2 set address	B400_0008
	Board control register 2 clear address	B400_000A
BCTRL3	Board control register 3 set address	B400_000C
	Board control register 3 clear address	B400_000E
BCTRL4	Board control register 4 set address	B400_0010
	Board control register 4 clear address	B400_0012
BSTAT1	Board status register 1	B400_0014
INT STATUS	Interrupt status register address	B400_0016
INT CURRENT STATUS	Interrupt CURRENT STATUS register	B400_0018
INT MASK	Interrupt mask register set address	B400_001A
	Interrupt mask register clear address	B400_001C
SC16C652	External UART port A	B401_0000
	External UART port B	B401_0010
CS8900A	Ethernet Controller I/O base address	B402_0000
	Ethernet Controller Memory base address	B402_1000
	Ethernet Controller DMA base address	B402_2000
YMU782B	Audio synthesizer port	B403_0000
CODE_B	Code test debug enable	B407_0000

1.8 Register descriptions

1.8.1 Version register

The version register contains three fields with the version of the PBC, CPU board, and BASE board. The PBC version is an 8-bit hardwired field that will be changed with design changes to the PBC. The CPU and BASE fields are implemented as two 4-bit fields and configured with external input signals connected to pull up and pull down resistors. The CPU and BASE fields are muxed on the Peripheral Data bus.

Table 5 Version Register

NAME	VERSION															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	PBC								CPU				BASE			
OPER	R								R				R			

1.9 Board status registers

1.9.1 Board Status Register 1

BSTAT1 contains several bits that represent the board status from different places on the board. These registers are read only.

Table 6 Board Status Register 1

NAME	BSTAT1															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RSV	RSV	RSV	ATLAS_ IN	PTT	FLIP_ SENSE2	FLIP_ SENSE1	SD2_ WP	SD1_ WP	PWR_ RDY	ATA_ DASP	ATA_ CBLID	ATA_ IOCS16	LIGHT_ SENSE	KP_ ON	NF_ DET
OPER	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
RESET	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-	-
IN/OUT	-	-	-	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN

Table 7 Board Status Register 1 Bit Definitions

Name	Description	Settings
NF_DET Bit 0	**Nand Flash Detect—** indicates Nand Flash card insertion.	0 = Nand Flash card is inserted 1 = Nand Flash card is not inserted
KP_ON Bit 1	**Keypad On/Off—** indicates if keypad is on/off	0 = Keypad is ON 1 = Keypad is OFF
LIGHT_SENSE Bit 2	**Light sense—** This signal reflects the light sense output from the keypad	0 = Light sense is 0 1 = Light sense is 1
ATA_IOCS16 Bit 3	**ATA IOCS16 –** This bit reflects the status of pin IOCS16 on the ATA connector	0 – IOCS16 state is 0 1 – IOCS16 state is 1
ATA_CBLID Bit 4	**ATA CBLID –** This bit reflects the status of pin CBLID on the ATA connector	0 – CBLID state is 0 1 – CBLID state is 1
ATA_DASP Bit 5	**ATA DASP –** This bit reflects the status of pin DASP on the ATA connector	0 – DASP state is 0 1 – DASP state is 1
PWR_RDY Bit 6	**Power Ready—** Power ready indication from Atlas board.	0 = Atlas power is not ready 1 = Atlas power is ready
SD1_WP Bit 7	**SD1 Write Protect —**This bit reflects the Write Protect on SD1 card.	0 = SD1 card is Write Protected 1 = SD1 card is not Write Protected
SD2_WP	**SD2 Write Protect —**This bit reflects the Write Protect on	0 = SD2 card is Write Protected

Name	Description	Settings
Bit 8	SD2 card.	1 = SD2 card is not Write Protected
FLIP_SENSE1 Bit 9	**Flip Sense 1 –** This bit reflects the status of pin Flip_Sense1 on the keypad connector	0 = Flip Sense 1 on keypad is 0. 1 = Flip Sense 1 on keypad is 1.
FLIP_SENSE2 Bit 10	**Flip Sense 2 –** This bit reflects the status of pin Flip_Sense2 on the keypad connector	0 = Flip Sense 2 on keypad is 0. 1 = Flip Sense 2 on keypad is 1.
PTT Bit 11	**PTT button –** This bit reflects the status of pin PTT on the keypad connector	0 = PTT signal on keypad is 0. 1 = PTT signal on keypad is 1.
ATLAS_IN Bit 12	**ATLAS IN** – This bit indicates if the power management board (Atlas) is placed on the board.	0 = Atlas board is placed 1 = Atlas board is not placed
RSV Bits 13:15	**Reserved**- For future use	Always reads 0

1.9.2 Board Status Register 2

BSTAT2 contains several bits that represent the board status from different places on the board. These registers are read only.

Table 8 Board Status Register

NAME	BSTAT2															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RSV	RSV	RSV	RSV	RSV	RSV	RSV	DMA_REQ	DSW							
OPER	R	R	R	R	R	R	R	R	R							

Table 9 Board Status Register 1 Bit Definitions

Name	Description	Settings
DSW Bits 7:0	**Debug switch**—This 8-bit field contains the value of the debug DIP switch.	0 (each bit) = switch is closed 1(each bit) = switch is open
DMA_REQ Bit 8	**DMA Request** – this bit reflects the DMA request to CPU from the Ethernet controller	0 = DMA Request is low 1 = DMA Request is high
RSV Bits 9:15	**Reserved**—These bits are reserved for future use.	Always read as 0

1.9.3 Board Control Register 1

BCTRL1 contains several fields to control various board functions. This register is implemented as a set register and a clear register. To set a bit, the set address is used, writing a 1 to the desired bit. To clear a bit, the clear address is used, writing a 1 to the desired bit.

Table 10 Board Control Register 1

NAME	BCTRL1															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	LCDON	BEND	CCTL2			CCTL1			LED1_B	LED0_B	IRDA_EN_B	UCE_EN_B	UB_EN_B	UA_EN_B	XUART_RST	ENET_RST
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
IN/OUT	OUT/OD	-	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT	OUT	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT	OUT

Table 11 Board Control Register 1 Bit Definitions

Name	Description	Settings
ENET_RST Bit 0	**Ethernet Reset—**Reset the Ethernet controller. This bit must be set for the desired duration of the reset signal, then cleared to remove the reset signal.	0 = Ethernet controller reset signal negated. 1 = Ethernet controller reset signal asserted.
XUART_RST Bit 1	**External UART Reset—**Reset external UART controller. This bit must be set for the desired duration of the reset signal, then cleared to remove the reset signal.	0 = UART controller reset signal negated. 1 = UART controller reset signal asserted.
UA_EN_B Bit 2	**UART A Enable—**Enable UART A transceiver.	0 = UART A transceiver enabled. 1 = UART A transceiver disabled
UB_EN_B Bit 3	**UART B Enable—**Enable UART B transceiver	0 = UART B transceiver enabled. 1 = UART B transceiver disabled
UCE_EN_B Bit 4	**UART C Enable—**Enable UART C transceiver.	0 = UART C transceiver enabled. 1 = UART C transceiver disabled
IRDA_EN_B Bit 5	**IRDA Enable—**Used to enable the IRDA transmitter.	0 = IRDA transmitter enabled 1 = IRDA transmitter disabled
LED0_B Bit 6	**LED 0 on—**Used to turn LED 0 on. This is used as a general purpose status indicator.	0 = LED 0 is off 1 = LED 0 is on.

Name	Description	Settings
LED1_B Bit 7	**LED 1 on—**Used to turn LED 1 on. This is used as a general purpose status indicator.	0 = LED 1 is off. 1 = LED 1 is on.
CCTL1[2:0] Bits 8-10	**CSI1 Control —**CSI1 control provides a three bit field for control of user defined functions on the CSI connector	xxx = User defined function.
CCTL2[2:0] Bits 11-13	**CSI2 Control —**CSI2 control provides a three bit field for control of user defined functions on the CSI connector	xxx = User defined function.
BEND	Internal register used as endian indicator	
LCDON Bit 15	**LCD ON—**Used to turn the QVGA dumb LCD display on.	0 = LCD is off 1 = LCD on

1.9.4 Board Control Register 2

BCTRL2 contains several bits to control various board functions. This register is implemented as a set register and a clear register. To set a bit, the set address is used, writing a 1 to the desired bit. To clear a bit, the clear address is used, writing a 1 to the desired bit.

Table 12 Board Control Register 2

NAME	BCTRL2															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	VCC_EN	VPP_EN	CT_CS	LCDIO_EN	LCD_RST2	LCD_RST1	LCD_RST0	IRDA_MOD	ATA_SEL	ATA_EN	CSI_EN	UMOD ENC	UMOD ENA	USELC	USELB	USELA
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	1	1	1	1	1	0	0	1	1	1	1	1	0	1
IN/OUT	OUT	OUT	OUT	OUT/OD	OUT/OD	OUT/OD	OUT/OD	OUT	OUT	OUT	OUT	OUT	OUT	OUT/OD	OUT/OD	OUT/OD

Table 13 Board Control Register 2 Bit Definitions

Name	Description	Settings
USELA Bit 0	**UART A SELECT—**Select UART A source on the CPU.	0 = the source is UART1 signals. 1 = the source is UART5 signals
USELB Bit 1	**UART B SELECT—**Select UART B source on the CPU.	0 = the source is UART3 signals. 1 = the source is UART4 signals
USELC	**UART C SELECT—**Select UART C source on the CPU.	0 = the source is UART2 signals.

Name	Description	Settings
Bit 2		1 = the source is UART1 signals
UMODENA Bit 3	**UART A MODEM Enable**—Enables UART A MODEM signals.	0 = UART C MODEM signals enabled 1 = UART C MODEM signals disabled
UMODENC Bit 4	**UART C MODEM Enable**—Enables UART C MODEM signals	0 = UART C MODEM signals enabled 1 = UART C MODEM signals disabled
CSI_EN Bit 5	**CSI Enable**—Used to enable the CSI Interface.	0 = CSI enabled 1 = CSI disabled
ATA_EN Bit 6	**ATA_Enable**—Enables ATA interface.	0 = ATA enabled 1 = ATA disabled
ATA_SEL Bit 7	**ATA Select**— Selects the signals of the cpu that will connect to the ATA interface.	0 = group A is connected to ATA interface 1 = group B is connected to ATA interface
IRDA_MOD Bit 8	**IRDA Mode** —this bit selects the bandwidth of the IRDA Transceiver.	A transition from high to low while IRDA_TXD is low – SIR/MIR bandwidth A transition from high to low while IRDA_TXD is high – FIR bandwidth
LCDRST0 Bit 9	**LCD 0 Reset** —This bit resets the smart parallel LCD #1	0 = smart parallel LCD #1 reset signal negated 1 = smart parallel LCD #1 reset signal asserted
LCDRST1 Bit 10	**LCD 1 Reset** —This bit resets the smart parallel LCD #2	0 = smart parallel LCD #2 reset signal negated 1 = smart parallel LCD #2 reset signal asserted
LCDRST2 Bit 11	**LCD 2 Reset** —This bit resets the smart serial LCD	0 = smart serial LCD reset signal negated 1 = smart serial LCD reset signal asserted
LCDIO_EN Bit 12	**LCD GPIO Enable –** Enables GPIO1 and GPIO2 interface with the LCD connectors for general purpose use.	0= connection with GPIO1 and GPIO2 is enabled 1= connection with GPIO1 and GPIO2 is disabled
RSV Bit 13	**Reserved**- For future use	Always reads 0
VPPEN Bit 14	**VPP Enable –** enables VPP power towards the PCMCIA.	0= PCMCIA VPP power is off 1= PCMCIA VPP power is VCC power (3.3V)
VCCEN Bit 15	**VCC Enable -** enables VCC power towards the PCMCIA.	0= PCMCIA VCC power is off 1= PCMCIA VCC power is 3.3V

1.9.5 Board Control Register 3

BCTRL3 contains several bits to control various board functions. This register is implemented as a set register and a clear register. To set a bit, the set address is used, writing a 1 to the desired bit. To clear a bit, the clear address is used, writing a 1 to the desired bit.

Table 14 Board Control Register 3

NAME	BCTRL3															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	SPI3_ RESET	VESIM _EN	VSIM_ EN	SYNTH_ RST	CARD2_ SEL	CARD1_ SEL	FSH_ VBUS_ EN	OTG_ VBUS_ EN	OTG_ HS_EN	FSH_ MOD	HSH_ EN	HSH_ SEL	FSH_ EN	FSH_ SEL	OTG_ FS_EN	OTG_ FS_SEL
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	1	0	0	1	0	0	1	1	1	0	1	0	1	0	1	1
IN/OUT	OUT	OUT/OD	OUT/OD	OUT	OUT	OUT	OUT/OD	OUT/OD	OUT/OD	OUT	OUT	OUT	OUT	OUT	OUT	OUT

Table 15 Board Control Register 3 Bit Definitions

Name	Description	Settings
OTG_FS_SEL Bit 0	**USB OTG Full Speed Select—**Select The source of the USB OTG Full speed interface.	0 = the source is the ATLAS board. 1 = the source is the CPU.
OTG_FS_EN Bit 1	**USB OTG Full Speed Enable —** Enables the USB OTG Full speed interface on the CPU.	0 = OTG Full Speed Interface enabled 1 = OTG Full Speed Interface disabled
FSH_SEL Bit 2	**USB Full Speed Host Select—** Select The source of the USB Full speed Host interface.	0 = Group A on the CPU 1 = Group B on the CPU
FSH_EN Bit 3	**USB Full Speed Host Enable—** Enables the USB Full speed Host interface.	0 = Full Speed Host Interface enabled 1 = Full Speed Host Interface disabled
HSH_SEL Bit 4	**USB High Speed Host Select—** Select The source of the USB High speed Host interface.	0 = Group A on the CPU 1 = Group B on the CPU
HSH_EN Bit 5	**USB High Speed Host Enable—** Enables the USB High speed Host interface.	0 = High Speed Host Interface enabled 1 = High Speed Host Interface disabled
FSH_MODE Bit 6	**USB Full Speed Host Mode—** Selects Single ended/ differential mode on USB Host Full Speed interface.	0 = Single ended mode 1 = Differential mode
OTG_HS_EN Bit 7	**USB OTG High Speed Enable —** Enables the USB OTG High speed interface on the CPU.	0 = OTG High Speed Interface enabled 1 = OTG High Speed Interface disabled
OTG_VBUS_EN	**USB OTG VBUS Enable —** Enables VBUS regulator on	0 = OTG VBUS regulator is enabled

Name	Description	Settings
Bit 8	USB OTG interface PHY.	1 = OTG VBUS regulator is disabled
FSH_ VBUS_EN Bit 9	**USB Full Speed Host VBUS Enable —** Enables VBUS regulator on USB Full speed Host interface PHY.	0 = Full Speed Host VBUS regulator is enabled 1 = Full Speed Host VBUS regulator is disabled
CARD1_SEL Bit 10	**Card1 Select—** Mux select pin for SD1 / MS1 lines	0 = lines are dedicated to SD1 interface 1 = lines are dedicated to MS1 interface
CARD2_SEL Bit 11	**Card2 Select—** Mux select pin for PCMCIA & SD2 / MS2 lines	0 = lines are dedicated to PCMCIA &SD2 interface 1 = lines are dedicated to MS2 interface
SYNTH_RST Bit 12	**Audio Synthesizer Reset –** Reset signal towards Audio Synthesizer	0= Reset audio Synthesizer 1= Normal operation
VSIM_EN Bit 13	**VSIM Enable—** Enables VSIM regulator on the ATLAS board.	0 = VSIM regulator is disabled 1 = VSIM regulator is enabled
VESIM_EN Bit 14	**VESIM Enable—** Enables VESIM regulator on the ATLAS board.	0 = VESIM regulator is disabled 1 = VESIM regulator is enabled
SPI3_RESET Bit 15	**CSPI3 Connector Reset —** Reset signal towards CSPI3 connector	0 = CSPI3 is reset 1 = Normal operation

1.9.6 Board Control Register 4

BCTRL4 contains several bits to control various board functions. This register is implemented as a set register and a clear register. To set a bit, the set address is used, writing a 1 to the desired bit. To clear a bit, the clear address is used, writing a 1 to the desired bit.

Table 16 Board Control Register 4

NAME	BCTRL4															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	RSV	CLR_ POE	PCMCIA_ EN	VIB_ EN	USER_ OFF	REGEN_ SEL	CSI_ MSB_EN
OPER	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	1
IN/OUT	-	-	-	-	-	-	-	-	-	-	OUT	OUT	OUT/OD	OUT/OD	OUT/OD	OUT/OD

Table 17 Board Control Register 4 Bit Definitions

Name	Description	Settings
CSI_MSB_EN Bit 0	**CSI MSB Enable -** Enables bits CSI_Data[3:0] from CSI interface.	0 = CSI_Data[3:0] enabled 1 = CSI_Data[3:0] disabled
REGEN_SEL Bit 1	**Regulator Enable Select—** This bit selects predefined programming for Atlas regulators.	0 = REGEN_SEL is active 1 = REGEN_SEL is not active
USER_OFF Bit 2	**User Off Indication —** This signal is sent to the Atlas board to confirm user off mode after a power fail.	0 = normal operation 1 = user off confirmation
VIB_EN Bit 3	**Vibrator Enable —** Enables the Vibrator regulator on the Atlas board.	0 = Vibrator regulator is disabled 1 = Vibrator regulator is enabled
PCMCIA_EN Bit 4	**PCMCIA Enable —** Enables the PCMCIA buffer	0 = PCMCIA buffer enabled 1 = PCMCIA buffer disabled
CLR_POE Bit 5	**PCMCIA Output Enable Clear —** Clears the PCMCIA Output enable	0 = PCMCIA OE 1 = PCMCIA buffer disabled
USB_HS_PHY_EN Bit 6	**USB High Speed PHY Enable —** Enables the PHY of the USB High Speed	0 = USB High Speed PHY enabled 1 = USB High Speed PHY disabled
RSV	**Reserved-** For future use	Always reads 0

Bits 7:15		

1.10 Interrupts

The Tortola ADS has several interrupt sources that the CPU must handle. The number of interrupt sources is larger than the number of GPIO pin available on the CPU. Therefore all interrupt sources are routed through the CPLD where some of them are grouped. An Interrupt Mask Register can disable each interrupt source.

1.10.1 Interrupt Status/Clear Register

The Interrupt Status Register reflects the status of each interrupt source on the ADS. There are two interrupt types, level and edge triggered. Edge triggered interrupts generate an interrupt whenever the source signal changes from high to low, or low to high. The user may reset these by writing a one (high) to the associated bit. Writing a zero (low) will leave the status bit unaffected. Level interrupts are generated when the chosen active level (high or low) is detected. These require a software service routine to reset the interrupt signal back to the inactive state at the source. Writing to level sensitive interrupt status bits will not change the bit. It is assumed in Table 18 that the RESET status of all level sensitive interrupts will be inactive.

The register may be read at any time.

Table 18 Interrupt Status/Clear Register

NAME	Interrupt Status Register															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RES	CE_INT2	CE_INT1	SYNTH_IRQ	XUART_INTB	XUART_INTA	OTG_FS_INT	ENET_INT	RES	RES	RES	RES	FSH_OVR	OTG_FS_OVR	PB_IRQ	LOW_BAT
OPER	-	R	R	R	R	R	R	R	-	-	-	-	R/W1C	R/W1C	R/W1C	R/W1C
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 19 Interrupt Status/Clear Register Bit Definitions

Name	Description	Settings
LOW_BAT Bit 0	**Low Battery—** Low Battery signal from Atlas has changed state.	0 – No interrupt pending 1- Interrupt active, write a one to clear

Name	Description	Settings
PB_IRQ Bit 1	**Push Button IRQ —** Push button switch circuit output has changed state.	0 – No interrupt pending 1- Interrupt active, write a one to clear
OTG_FS_OVR Bit 2	**USB OTG Full Speed Over Current —**The USB OTG Full Speed Over Current bit has changed state.	0 – No interrupt pending 1- Interrupt active, write a one to clear
FSH_OVR Bit 3	**USB Full Speed Host Over Current —** The USB Full Speed Host interface. Overcurrent bit has changed state.	0 – No interrupt pending 1- Interrupt active, write a one to clear
RES Bits 4,5,6,7, & 15	Reserved for future use	N/A
ENET_INT Bit 8	**Ethernet Interrupt -** interrupt signal from Ethernet controller	0= no interrupt from Ethernet controller 1= Interrupt received from Ethernet controller
OTG_FS_INT Bit 9	**USB Host Full Speed Interrupt —**This bit is the interrupt indication from USB Host full speed interface.	0= no interrupt from USB Host full speed interface. 1= Interrupt received from USB Host full speed interface.
XUART_INTA Bit 10	**External UART A interrupt –** interrupt signal from External UART A.	0= no interrupt from External UART A 1= Interrupt received from External UART A
XUART_INTB Bit 11	**External UART B interrupt –** interrupt signal from External UART B.	0= no interrupt from External UART B 1= Interrupt received from External UART B
SYNTH_IRQ Bit 12	**Audio Synthesizer IRQ –** interrupt signal from Audio Synthesizer	0= no interrupt from Audio Synthesizer 1= Interrupt received from Audio Synthesizer
CE_INT1 Bit 13	**Communication Engine Interrupt 1—**	0 = No interrupt from CE_INT1 1 = Interrupt received from CE_INT1
CE_INT2 Bit 14	**Communication Engine Interrupt 2—** .	0 = No interrupt from CE_INT2 1 = Interrupt received from CE_INT2

1.10.2 Interrupt Signal Current State Status Register

This register represents the current state of each edge triggered interrupt source. This register is a read only register.

Table 20 Interrupt Signal Current State Status Register

NAME	Interrupt Current State Status Register															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	FSH_ OVR	OTG_ FS_ OVR	PB_ IRQ	LOW_B AT

Table 21 Interrupt Current Status Register Bit Definitions

Name	Description	Settings
LOW_BAT Bit 4	**Low Battery—** Low Battery Indicator signal from Atlas Board.	0 - Low Battery indication 1- Normal operation
PB_IRQ Bit 5	**Push Button IRQ —** Push button switch circuit.	0 – Push button is pressed 1- Push button is not pressed
OTG_FS_OVR Bit 6	**USB OTG Full Speed Over Current —**USB OTG Full Speed Over Current indication.	0 – Over Current indication 1- No Over Current indication
FSH_OVR Bit 7	**USB Full Speed Host Over Current —** The USB Full Speed Host interface. Over current indication.	0 – Over Current indication 1- No Over Current indication

1.10.3 Interrupt Mask Register

The Interrupt Mask Register enables/disables the corresponding interrupt source. A high (one) will enable the associated interrupt source. A low (zero) will mask (disable) the associated interrupt source. Even if the interrupt is masked the associated status register bit will still indicate whether or not an interrupt is pending from each source. However a masked interrupt will not cause an interrupt signal to be generated to the GPIO pin it is associated with. Modifying the Mask Register to enable an interrupt that is pending will immediately cause an interrupt to be generated.
This register is implemented as a set register and a clear register. To set a bit, the set address is used, writing a 1 to the desired bit. To clear a bit, the clear address is used, writing a 1 to the desired bit.

Table 22 Interrupt Mask Register

NAME	Interrupt Mask Register															
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MASKED INTERRUPT FEILD	RES	CE_ INT2	CE_ INT1	SYNTH_ IRQ	XUART_ INTB	XUART _ INTA	OTG_ FS_ INT	ENET_ INT	RES	RES	RES	RES	FSH_ OVR	OTG_ FS_ OVR	PB_ IRQ	LOW_ BAT
OPER	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

1.10.3 GPIO Interrupt Grouping and Non Registered Interrupts

Some interrupt signals are not associated with any CPLD register but are instead directly routed (inside the CPLD) to a GPIO pin. The SD and Memory Stick detect functions are logically ORed together since only one or the other should be implemented at any given time.
The interrupt are grouped in the following way:

GPIO	Interrupt sources
GPIO1_1	SD1_DET + MS1_DET
GPIO1_2	SD2_DET + MS2_DET
GPIO1_3	PRI_INT (ATLAS)
GPIO1_4	XUART_INTA, XUART_INTB, ENET_INT, LOW_BAT, PB_IRQ, OTG_FS_OVR, OTG_FS_INT, FSH_OVR, SYNTH_IRQ, CE_INT1, CE_INT2

Table 23 GPIO Interrupt Bit Descriptions

Name	Description	Settings
GPIO1_1	SD1 OR MS1 memory card detect status	0 – No Card is inserted 1- A card has been detected
GPIO1_2	SD2 OR MS2 memory card detect status	0 – No Card is inserted 1- A card has been detected
GPIO1_3	Atlas' Primary Interrupt output status bit	0 – No interrupt pending 1- Interrupt active
GPIO1_4	Registered Interrupt Status bit	0 – No interrupt pending 1- Interrupt active

1.14 References

[1] ZAS peripheral Bus Control CPLD, November 30, 2004, Version 2.0, Freescale Semiconductor.

[2] CS8900A ISA Ethernet Controller Data Sheet, April 2001, Cirrus Logic.

[3] SC16C652 Dual UART Controller, June 20, 2003, Rev 04, Philips Semiconductors.

[4] ISA System Architecture, October 1993, Mindshare, In