LLC Resonant AC/DC Switched-Mode Power Supply using the MC56F8013 and MC56F8257

MC56F80xx and MC56F82xx Digital Signal Controllers

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Chapter 1
Introduction

1.1 Application outline

This reference design describes an off-line AC/DC switched-mode power supply (SMPS) using an LLC resonant converter topology.

This document focuses on the digital control of key parts of the off-line AC/DC SMPS system. It includes control of a power factor correction (PFC), a DC/DC LLC resonant converter, and a DC/DC buck converter. The AC/DC switch mode power supply is fully digitally controlled. The digital control is based on two Freescale digital signal controllers (DSC). The primary side (PFC) is controlled by the MC56F8013 DSC and the secondary side, the LLC resonant converter and buck converter is controlled by the MC56F8257 DSC.

The reference design incorporates both hardware and software parts of the system including hardware schematics.

1.2 Resonant converter topologies and features

The off-line AC/DC switched-mode power supplies uses a large number of circuit topologies (flyback, forward, push-pull, boost, buck, half bridge, full bridge, and so on). The circuit topology selection depends on many parameters like output power, input voltage, output/input voltage ratio, and so on. The selected circuit topology is also compromised in the size, price, and efficiency.

The demand for increasing power density of switched-mode power supplies pushes designers to use a higher switching frequency. But a very high switching frequency significantly increases switching losses at pulse width modulated (PWM) converters. It brings decreasing efficiency and also the space saved by using smaller passive components is wasted by larger heating or forced cooling. Therefore the SMPS designers are looking for solutions for decreasing switching losses.

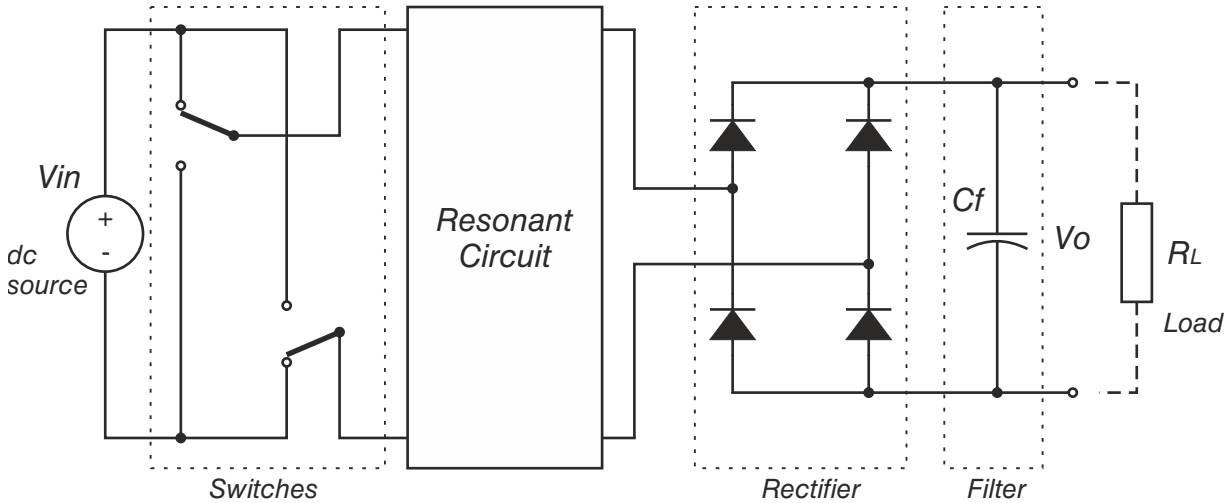

Figure 1-1. Resonant converter principle

One of the possible solutions is the use of resonant converter topologies. The resonant converter uses a resonant circuit in the conversion path. The typical structure of the resonant converter can be seen in Figure 1-1. The switching network generates a square wave voltage output with a 50% duty cycle. This voltage pattern feeds the resonant tank. The resonant tank consists of a serial or a parallel combination of L and C passive components. There are several combinations of two or three L and C passive components used in the resonant tank. The type of resonant tank and its connection to the load defines the resonant converter behaviors. Due to the resonant tank, the semiconductor switches can operate at zero voltage or current switching condition. This phenomenon significantly reduces switching losses and allows the converter operation at high switching frequencies.

The most common known resonant topologies are a serial resonant converter (SRC) and parallel resonant converter (PRC). The serial resonant converter can be seen in Figure 1-2. The resonant tank consists of a serial connected inductor L_r and capacitor C_r. The load R_L is also connected in series with the resonant tank. In the serial resonant converter, the resonant tank and load creates a voltage divider. Because the resonant tank impedance is frequency dependent, the output voltage of the serial resonant converter can be controlled by switching frequency. At the DC or low switching frequency the resonant tank has high impedance in comparison with the load impedance and the output voltage is low. Increasing the switch frequency also increases the output voltage. At the resonant frequency, the voltage drop on the resonant tank is equal to zero and thus the output voltages are equal to the the input voltage. Continuing over the resonant frequency the output voltage starts to decrease, this is because the resonant tank impedance increases against to load impedance. The operation over the resonant frequency is preferred, even if the output voltage regulation is possible both over or below resonant frequency. The inductive character of the resonant frequency allows to achieve zero voltage switching (ZVS), which is preferred for MOSFET transistors.

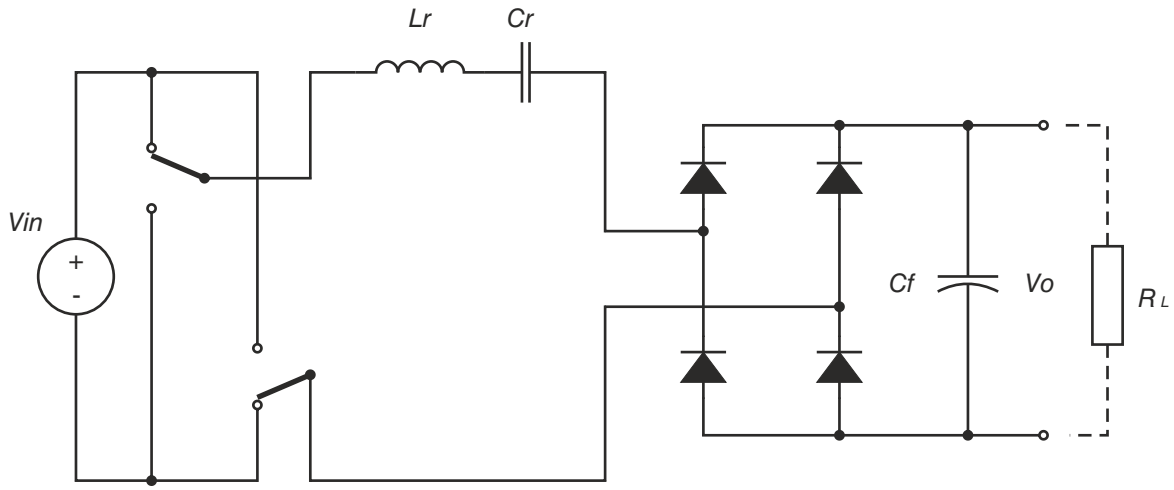

Figure 1-2. Serial resonant converter topology (SRC)

The output voltage regulation is also limited by the load value. If the load is very low, the load impedance is high in comparison with the resonant tank. To keep the desired voltage at the output becomes difficult. Theoretically the switching frequency can be infinite, but practically there is some maximal frequency limit. Therefore the output voltage regulation at light or no load condition is very limited.

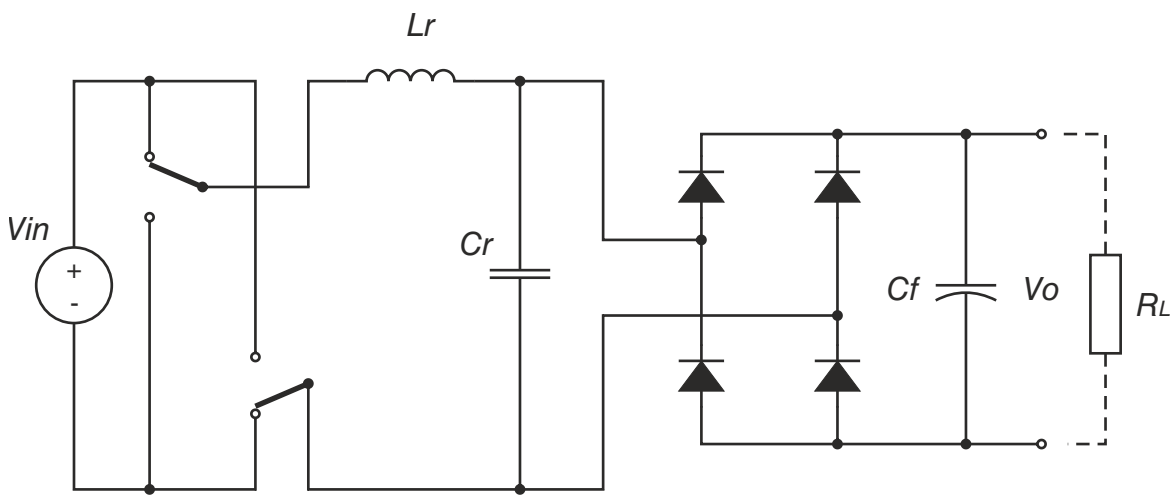

Figure 1-3. Parallel resonant converter topology (PRC)

Another well know topology — Parallel resonant converter can be seen in Figure 1-3. The parallel converter uses the same resonant tank as the serial resonant converter, the serial connection of inductor L_r and capacitor C_r. The parallel resonant converter differs in load connection to the resonant tank. In this case, the load is connected in parallel with the capacitor C_r. In this configuration the voltage divider consists of impedance of the inductor L_r and impedance of parallel combination of the capacitor C_r and the load R_L. This means that both parts top and bottom impedance of the voltage divider are frequency dependent. At DC or low switching the output voltage of the parallel resonant converter is equal to input voltages. Increasing the switching frequency the output voltage also

increases due to the characteristic of the resonant tank. The maximal output voltage is achieved at a resonant frequency, where the output voltage is Q times higher than the input voltage. The Q is a quality factor of the resonant tank. Over the resonant frequency the output voltage falls, because the inductor impedance becomes more dominant against the capacitor impedance.

The parallel resonant converter can control the output voltage even at no load conditions. In this case the load is comprised of a resonant tank only. On the other hand, the permanent connection of the resonant tank to the switch network brings some drawbacks at nominal operation. At nominal load the parallel converter operates close to the resonant frequency and thus the resonant tanks have the lowest impedance. This also means a high circulating current through the resonant tank. The parallel converter also operates over the resonant frequency due to ZVS conditions.

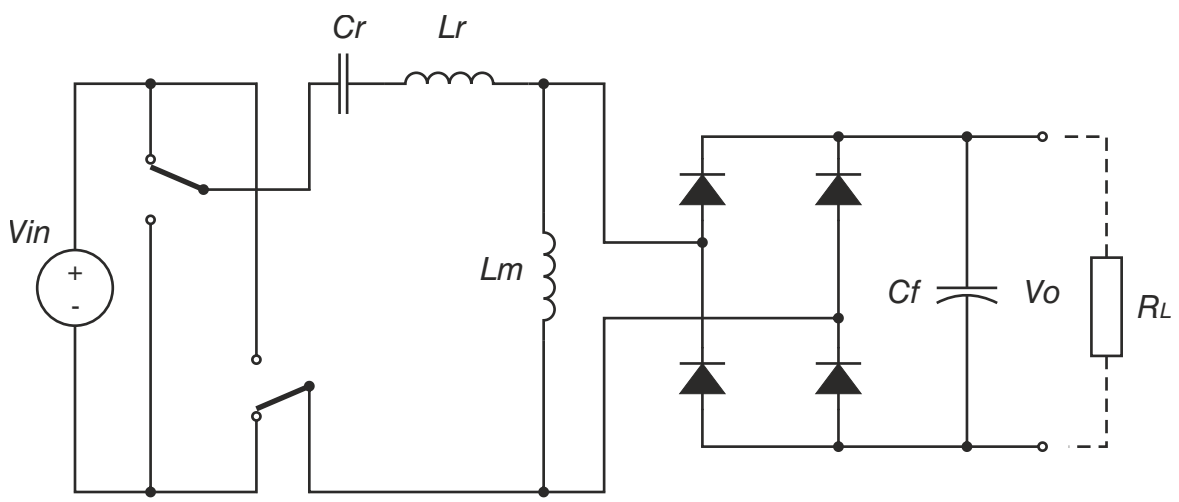

Figure 1-4. LLC resonant converter topology

Other than the two part resonant tanks, there are almost 40 possibilities of three part resonant tanks. The most popular member of three part tanks is the LLC resonant converter. The resonant tank consists of two inductors L_r, L_m and one capacitor C_r (see Figure 1-4). The load is connected in parallel to the inductor L_m. The LLC resonant converter solves all drawbacks mentioned above. At no load conditions the output voltage can still be controlled by a voltage drop over inductor L_m. Also at resonant frequency the current is limited by the L_m inductor, therefore the circulating current through the resonant circuit can be kept on an acceptable level. Another advantage of the LLC resonant converter is that it can operate under ZVS condition over the whole load

range. The behaviors of the LLC resonant converter will be discussed in more detail in the Section Resonant converter description. The summary of the key features of all the mentioned resonant converters can be seen in Table 1-1.

Table 1-1. Resonant converters comparison

	SRC	PRC	LLC
ZVS operation	Above f_r only	Above f_r only	Yes
Operation without load	No	Yes, but high losses	Yes
Operation at f_r	No (close to f_r)	No (close to $f_{r)}$	Yes
Operation at wide input range	High losses	High losses	Yes

1.3 Freescale MC56F80xx controller advantages and features

The Freescale MC56F80xx family is suited for switch mode power supplies (SMPS) control, motor control, and combining the DSP's calculation capability with the MCU's controller features on a single chip. These hybrid controllers offer many dedicated peripherals such as pulse width modulation (PWM) modules, analogue-to-digital converters (ADC), timers, communication peripherals (SCI, SPI, I^2C), and on-board flash and RAM.

The MC56F80xx family provides the following peripheral blocks:

- One PWM module with PWM outputs, fault inputs, fault-tolerant design with dead time insertion, supporting center-aligned, and edge-aligned modes
- 12-bit ADC, supports two simultaneous conversions; ADC and PWM modules can by synchronized
- One dedicated 16-bit general purpose quad timer module
- One serial peripheral interface (SPI)
- One serial communication interface (SCI) with LIN slave functionality
- On-board 3.3 V to 2.5 V voltage regulator for powering internal logic and memories
- Integrated power on reset and low-voltage interrupt module
- All pins multiplexed with general purpose input/output (GPIO) pins
- Computer operating properly (COP) watchdog timer
- External reset input pin for hardware reset

- JTAG/On-Chip Emulation (OnCE^{TM}) module for unobtrusive processor-speed-independent debugging
- Phase-locked loop (PLL) based frequency synthesizer for the hybrid controller core clock with on-chip relaxation oscillator

Table 1-2. Memory configuration

Memory Type	MC56F8013
Program flash	16 Kbyte
Unified data/program RAM	4 Kbyte

The SMPS and motor control benefit from the flexible PWM module, fast ADC, and quad timer module.

The PWM offers flexibility in its configuration, enabling an efficient three-phase motor control. The PWM module is capable of generation asymmetric PWM duty cycles in a center-aligned configuration. The PWM reload SYNC signal can be generated to provide synchronization with other modules (ADC, Quad-timer).

The PWM block has the following features:

- Three complementary PWM signal pairs, six independent PWM signals (or a combination)
- Complementary channel operation features
- Independent top and bottom dead time insertion
- Separate top and bottom pulse width correction via current status inputs or software
- Separate top and bottom polarity control
- Edge-aligned or center-aligned PWM reference signals with a 15-bit resolution
- Half-cycle reload capability
- Integral reload rates from one to sixteen periods
- Mask/swap capability
- Individual, software-controlled PWM output
- Programmable fault protection
- Polarity control
- 10 mA or 16 mA current sink capability on PWM pins
- Write-protectable registers

The application uses the PWM module for generating two duty cycles for the interleaved boost converter MOSFET transistors.

The ADC module has the following features:

- 12-bit resolution
- Dual ADCs per module; three input channels per ADC

- Maximum ADC clock frequency of 5.33 MHz with a 187 ns period
- Sampling rate of up to 1.78 million samples per second
- Single conversion time of 8.5 ADC clock cycles (8.5 x 187 ns = 1.59 µs)
- Additional conversion time of six ADC clock cycles (6 x 187 ns = 1.125 µs)
- Eight conversion in 26.5 ADC clock cycles (26.5 x 187 ns = 4.97 µs) using parallel mode
- Ability to use the SYNC input signal to synchronize with the PWM (if the integration allows the PWM to trigger a timer channel connected to the SYNC input)
- Ability to sequentially scan and store up to eight measurements
- Ability to scan and store up to four measurements on each of two ADCs operating simultaneously and in parallel
- Ability to scan and store up to four measurements on each of two ADCs operating asynchronously to each other in parallel
- Interrupt generating capabilities at the end of a scan when an out-of-range limit is exceeded and on a zero crossing
- Optional sample correction by subtracting a pre-programmed offset value
- Signed or unsigned results
- Single-ended or differential inputs
- PWM outputs with hysteresis for three of the analogue inputs

The application uses the ADC block in simultaneous mode scan. It is synchronized to the Quadrature timer. This configuration allows the simultaneous conversion of the required analogue values for the input current, input voltage, and output voltage within the required time.

The Quadrature timer is an extremely flexible module, providing all required services relating to time events. It has the following features:

- Four 16-bit counters/timers
- Count up/down
- Counters are cascadable
- Programmable count modulus
- Four 16-bit counters/timers
- Maximum count rate equal to the peripheral clock/2, when counting external events
- Maximum count rate equal to the peripheral clock/1, when using internal clocks
- Count once or repeatedly
- Counters are preloadable
- Counters can share available input pins
- Each counter has as separate precaler
- Four 16-bit counters/timers
- Each counter has a capture and compare capability

The application uses two channels of the quad timer for synchronization PWM to ADC and one channel for application timing.

1.4 Freescale MC56F82xx controller advantages and features

The MC56F825x/MC56F824x is a member of the 56800E core-based family of digital signal controllers (DSCs). It combines on a single chip, the processing power of a DSP, and the functionality of a microcontroller with a flexible set of peripherals to create a cost-effective solution. Because of its low cost, configuration flexibility, and compact program code, it is well-suited for many applications. The MC56F825x/MC56F824x includes many peripherals that are especially useful for cost-sensitive applications, like industrial control, home appliances, solar inverters, battery chargers and management, switched–mode power supplies and power management, power metering, motor control (ACIM, BLDC, PMSM, SR, and stepper), and others.

The MC56F825x/MC56F824x family provides the following on-chip features:

- 60 MHz operation frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- On-chip memory
  - 56F8245/46 — 48 KB (24K x 16) flash memory; 6 KB (3K x 16) unified data/program RAM
  - 56F8247 — 48 KB (24K x 16) flash memory; 8 KB (4K x 16) unified data/program RAM
  - 56F8255/56/57 — 64 KB (32K x 16) flash memory; 8 KB (4K x 16) unified data/program RAM
- eFlexPWM with up to 9 channels, including 6 channels with high (520 ps) resolution NanoEdge placement
- Two 8-channel, 12-bit analog-to-digital converters (ADCs) with dynamic x2 and x4 programmable amplifier, conversion time as short as 600 ns, and input current-injection protection
- Three analog comparators with integrated 5-bit DAC references
- Cyclic Redundancy Check (CRC) Generator
- Two high-speed queued serial communication interface (QSCI) modules with LIN slave functionality
- Queued serial peripheral interface (QSPI) module
- Two SMBus–compatible inter-integrated circuit (I2C) ports
- Freescale’s scalable controller area network (MSCAN) 2.0 A/B module
- Two 16-bit quad timers (2 x 4 16-bit timers)
- Computer operating properly (COP) watchdog module
- On-chip relaxation oscillator — 8 MHz (400 kHz at standby mode)

- Crystal/resonator oscillator
- Integrated power-on reset (POR) and low-voltage interrupt (LVI) and brown-out reset module
- Inter-module crossbar connection
- Up to 54 GPIOs
- 44-pin LQFP, 48-pin LQFP, and 64-pin LQFP packages
- Single supply — 3.0 V to 3.6 V

The switched-mode power supply applications benefit greatly from the flexible eFlexPWM module, fast ADC module, on-chip analog comparator module, and inter-module crossbar.

The Enhanced Flex Pulse Width Modulator (eFlexPWM) module has the following features:

- Up to nine output channels
- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Each complementary pair can operate with its own PWM frequency based and deadtime values
  - 4 time base
  - Independent top and bottom deadtime insertion
- PWM outputs can operate as complimentary pairs or independent channels
- Independent control of both edges of each PWM output
- 6-channel NanoEdge high resolution PWM
  - Fractional delay for enhanced resolution of the PWM period and edge placement
  - Arbitrary eFlexPWM edge placement — PWM phase shifting
  - NanoEdge implementation— 520 ps PWM frequency resolution
- 3 Channel PWM with full input capture features
  - Three PWM Channels — PWMA, PWMB, and PWMX
  - Enhanced input capture functionality
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
  - Integral reload rates from 1 to 16
  - Half cycle reload capability
- Multiple output trigger events can be generated per PWM cycle via hardware
- Support for double switching PWM outputs
- Up to four fault inputs can be assigned to control multiple PWM outputs
  - Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Individual software-control for each PWM output
- All outputs can be programmed to change simultaneously via a FORCE_OUT event
- PWMX pin can optionally output a third PWM signal from each submodule

- Channels not used for PWM generation can be used for buffered output compare functions
- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- The option to supply the source for each complementary PWM signal pair from any of the following:
  - Crossbar module outputs
  - External ADC input, taking into account values set in ADC high and low limit registers

The eFlexPWM offers flexibility in its configuration, enabling efficient control of any SMPS topology. The eFlexPWM module is capable of free control of rising and falling edges for each PWM output and includes automatic complementary signal generation and dead time insertion. Due to NanoEdge placement the eFlexPWM can generate duty cycles and frequencies with high a resolution of up to 520 ps. The eFlexPWM module can also generate up to 6 synchronization events per sub-module to provide synchronization with other modules (ADC, Quad-timer).

The application uses the eFlexPWM module for generating four PWM signals for LLC resonant converter and two PWM signals for synchronous buck converter. The PWM signals for the LLC converter have a variable frequency and constant duty cycle at 50 %. The synchronous buck PWM signals have a fixed frequency of 500 kHz and variable duty cycle.

The ADC converter has the following features:

- Two independent 12-bit analog-to-digital converters (ADCs)
  - 2 x 8 channel external inputs
  - Built-in x1, x2, x 4 programmable gain pre-amplifier
- Maximum ADC clock frequency — Up to 10 MHz
  - Single conversion time of 8.5 ADC clock cycles (8.5 x 100 ns = 850 ns)
  - Additional conversion time of 6-ADC clock cycles (6 x 100 ns = 600 ns)
- Sequential, parallel, and independent scan mode
- First 8 samples have Offset, Limit, and zero-crossing calculation supported
- ADC conversions can be synchronized by eFlexPWM and timer modules via the internal crossbar module
- Support for simultaneous and software triggering conversions
- Support for multi-triggering mode with a number of programmable conversions on each trigger

The application uses the ADC module in independent scan mode. The first ADC converter is synchronized with LLC resonant converter PWM signals. It samples output voltage and output current of LLC resonant converter. The second ADC converter is synchronized with synchronous buck PWM signals and converts output voltage and output current of synchronous buck converter.

The Inter-Module Crossbar Switch (XBAR) has the following features:

- Programmable internal module connections between and among the eFlexPWM, ADCs, Quad Timers, 12-bit DAC, HSCMPs, and package pins
- User-defined input/output pins for PWM fault inputs, timer input/output, ADC triggers, and comparator outputs

The application uses the inter-module crossbar switch to provide interconnection between the eFlexPWM module and ADC module, interconnection between the input pin (fault signal) and on-chip comparator, and interconnection between comparator's output and eFlexPWM fault input.

The application also uses other peripherals like a QTimer module for the software timer, the I^2C module for communication with the temperature sensor, 2xSCI module for communication with the primary side and remote control via PC, the SPI module for communication via the SMBUS, and the MSCAN module for communication via CAN bus.

Chapter 2
System Description

2.1 System concept

The SMPS reference design can be divided into two main parts from the concept point of view—primary and secondary side.

This application system which belongs to the primary side incorporates the EMI input filter, two phase interleaved PFC stage, drivers, input relay stage, fan power stage, quantities sensing circuitry, over-current circuitry, heat-sink temperature sensing, and the primary MCU controller board.

The application system that belongs to the secondary side incorporates the LLC resonant converter, synchronous rectifier, buck converter, quantities sensing circuitry, communication between host PC using USB/SCI interface, PM Bus communication, CAN communication, drivers, temperature board sensing, and the secondary MCU controller board.

The auxiliary power supply stage and isolated communication between MCUs on the primary and secondary side are at the edge between both sides.

The overall system design concept is shown in Figure 2-1.

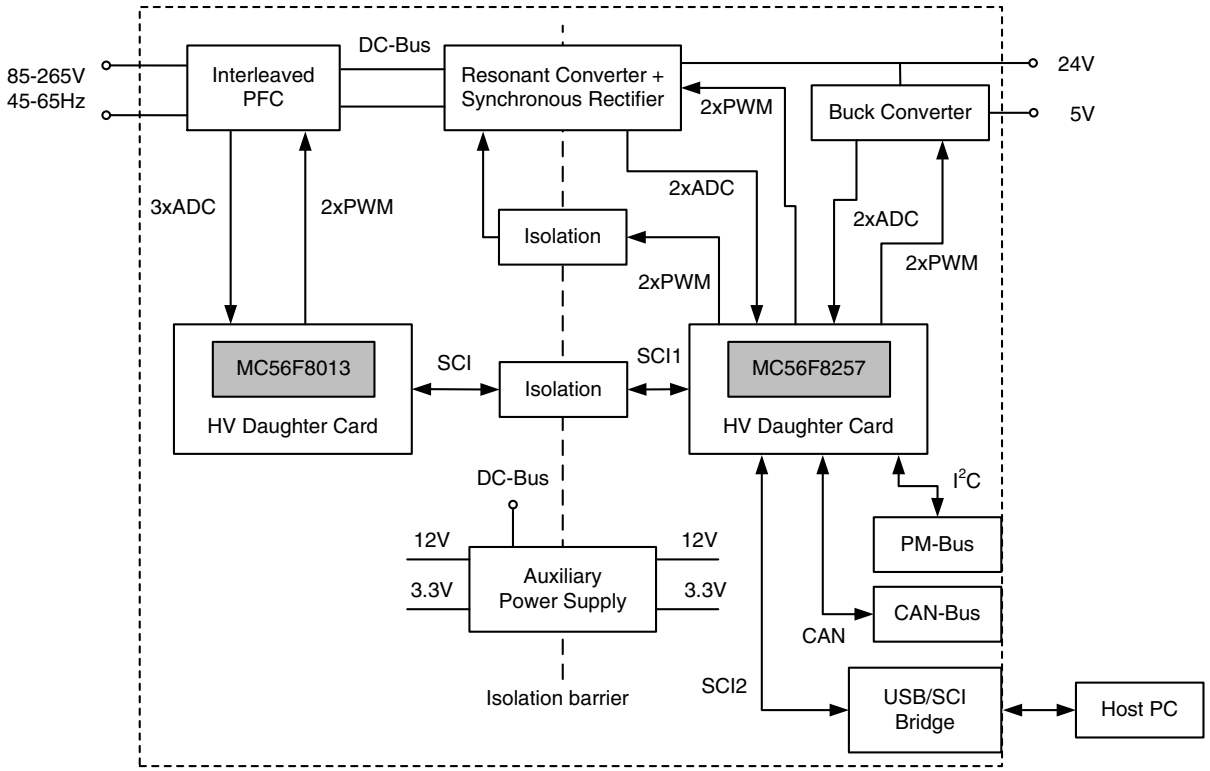

Figure 2-1. Block diagram

As mentioned above the interleaved PFC stage consists of two parallel connected boost converters operating in continuous conduction mode. It provides sinusoidal current shape at input with the input voltage phase while keeping output voltage at the required level. The interleaved PFC approach has more components than a single boost converter.The control algorithm is also complicated, but on the other hand the components are smaller with lower operating limits and can reach a better overall performance of the PFC circuit.

The EMI input filter provides filtering for common and differential noise which is generated under high current switching in the PFC circuit. The EMI filter eliminates these interference signals from the interleaved boost converter stage at the input of mains.

The fan power stage provides the adjustable voltage output to power the fan. The speed of the fan can then be set according to the temperature at heat-sink on the primary side, or the board temperature on the secondary side.

The input relay stage together with two resistors substitute the thermistor in circuits dedicated to limit current peak surge after mains is applied. After a set time the resistors are disconnected which leads to an efficiency increase of the primary stage.

The sensing circuitries are used for sensing input voltage, output voltage and input current, and accommodating them to the MCU controller acceptable voltage level.

The drivers are used for amplification of driving the PWM signal for the boost converters MOSFET transistors.

Heat-sink temperature measurement is used for evaluation of over-temperature state and for fan speed control. If heat-sink reaches an over-temperature level the whole system switches off.

The core of the primary side is the MC56F8013 controller. It is situated on the MCU controller board and connected via a daughter card connector. The MCU controls all the circuits mentioned above. The Primary controller operates in slave serial communication mode in this design.

The main part of the secondary side is the LLC resonant converter. In fact, part of the converter is situated on the primary side, but belongs to the secondary side from the concept point of view. Isolation between the primary and secondary side is formed by the transformer of the resonant converter. The synchronous rectifier as part of the LLC resonant converter rectifies the output voltage to the 24 V level.

The buck converter is used for generating 5 V from 24 V at the output of the synchronous rectifier.

The sensing circuitries are used for sensing two output voltages, two output currents, and accommodating them to the secondary MCU controller acceptable voltage level.

The temperature of the board is read, evaluated as over-temperature, and sent to the primary side for fan speed control. If the board temperature reaches an over-temperature level, the whole system switches off.

The isolated drivers are on the edge between the primary and secondary side and are used for amplification of the driving signal for the resonant converter MOSFET's on the primary side.

Non-isolated drivers are used for amplification of driving PWM signals for the buck converter MOSFET transistors.

The core of the secondary side is the MC56F8257 controller that is situated on the MCU controller board and connected via a daughter card. The MCU controls all circuits on the secondary side and this controller is master for the whole application.

The secondary controller is also used for communication with the host PC via USB. The conversion between USB and SCI signals is made using the USB/SCI bridge. The MC9S08JS16 creates this communication bridge.

The board is ready and all necessary signals are connected for implementation of PM-BUS protocol. Software support is not implemented at this moment.

The board is also ready for implementation of CAN protocol. Software support is not implemented at this moment either.

2.2 System_specification

The SMPS reference design operating with universal input voltage, generates two isolated voltages 24 V and 5 V with a total output power of 350 W. All specific parameters are summarized in the Table 2-1.

This application meets the following performance specification:

- Hardware used:
  - Main board with PFC, resonant converter and buck converter
  - Auxiliary power supply board
  - MC56F8013 daughter card board
  - MC56F8257 daughter card board
- Control techniques incorporates:
  - SW primary side — PFC control, cooling fan control based on measured temperatures, input relay control, and serial communication with secondary side
  - SW secondary side — LLC resonant converter with synchronous rectifier control, buck converter control, serial communication with primary side, serial communication with host PC, and temperature evaluation
- Manual plus FreeMASTER interface and monitor:
  - ON/OFF switch
  - FreeMASTER software graphical control page
  - User LEDs indicating 5 V and 24 V at output
- Fault protection:
  - D.C. bus over-voltage and under-voltage
  - Input over-current
  - Input over-voltage and under-voltage
  - Output over-current for synchronous rectifier
  - Output over-current for buck converter
  - Output over-voltage for synchronous rectifier
  - Output over-voltage for buck converter
  - Over-temperature at the heat-sink on primary side
  - Over-temperature of the board on secondary side

Table 2-1. SMPS parameters

Parameter	Value
Input frequency	45-65 Hz
Input voltage	85-265 V
Input current	5 A
Output voltage 1	24 V

Table continues on the next page...

Table 2-1. SMPS parameters (continued)

Parameter	Value
Output current 1	14.6 A
Output voltage 2	5 V
Output current 2	20 A
Output total power	350 W
Power factor	—
Total harmonic distortion	—

Each part of the system is described in the following sections.

2.3 Interleaved PFC description

A single boost converter is used mainly as a power factor correction circuit. It meets all requirements put on these types of circuits, including international regulations IEC61000-3-2. Nowadays, improved MCU performance with more peripherals allow use of more resources demanded by improving application behavior and reaching better parameters. Therefore, an interleaved PFC approach is well suited for this application with a better performance result comparing to the single boost converter solution. The interleaved PFC consists of two boost converters connected in parallel. Benefits of this approach comes from the ripple current elimination in inductors, because currents are 180° out of phase, and therefore eliminate each other - see explanation in Figure 2-2. This has impact on the used components design. Compared to the single boost converter there are PFC inductors calculated for twice a smaller current, as well as boost MOSFETs and diodes. This leads to an improved power density per watt. Furthermore, the power factor can be increased at lower power levels using only one leg of the converter. On the other hand, the control structure implemented in the software is more complicated.

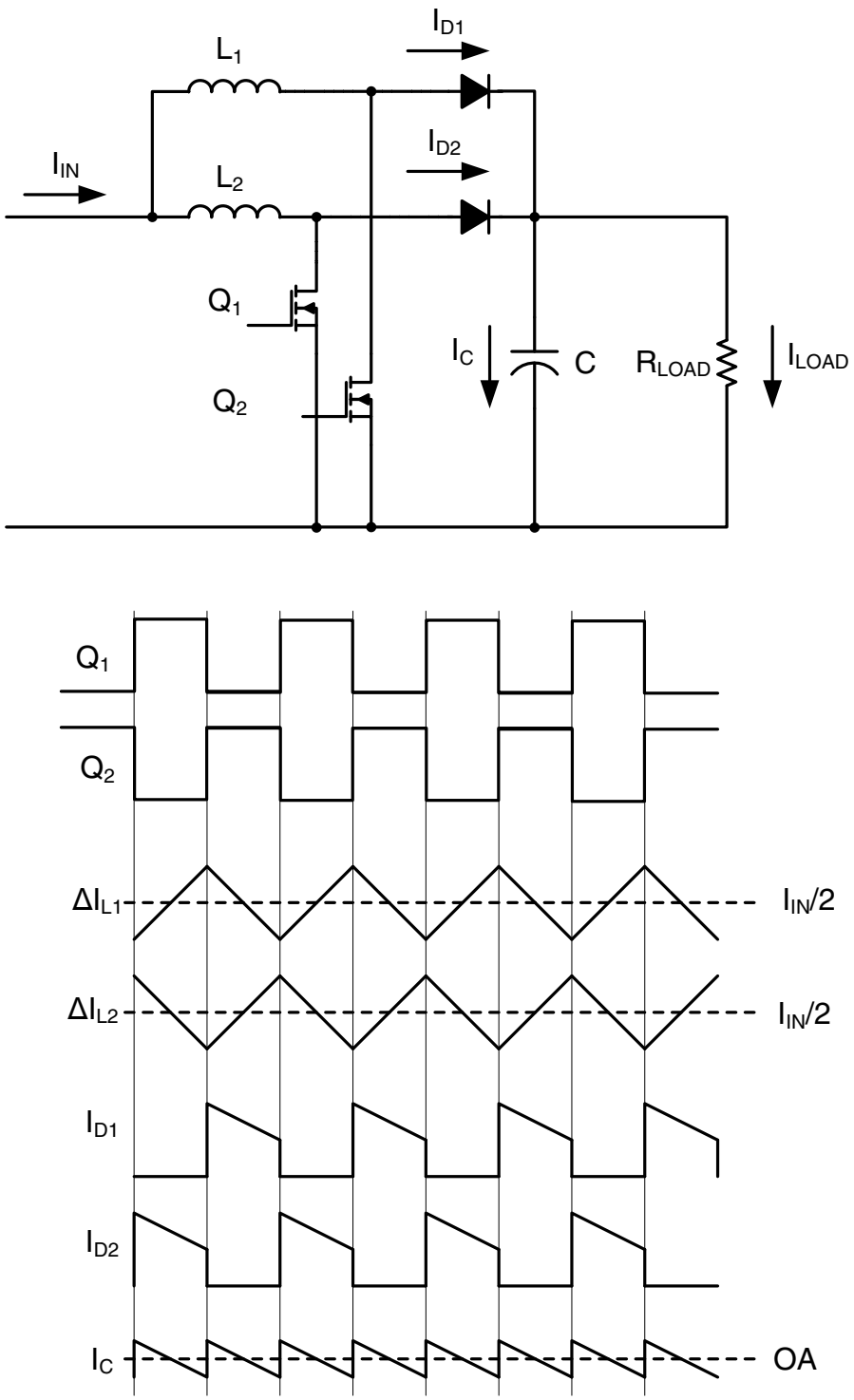

Figure 2-2. Interleave PFC — Current shape

The control structure of the interleaved PFC can be seen in Figure 2-3. In this application there are three quantities measured: input current, input rectified voltage, and output voltage. All quantities are measured the same way as in a single boost converter design. In some approaches, also the currents in each leg of the converter are measured. The control structure is more complicated in this case. It includes two current controllers and

an additional block for compensating differences in each leg of the boost converter. This design comes from the fact that due to MOSFET positive temperature coefficient small differences in both PFC legs are compensated.

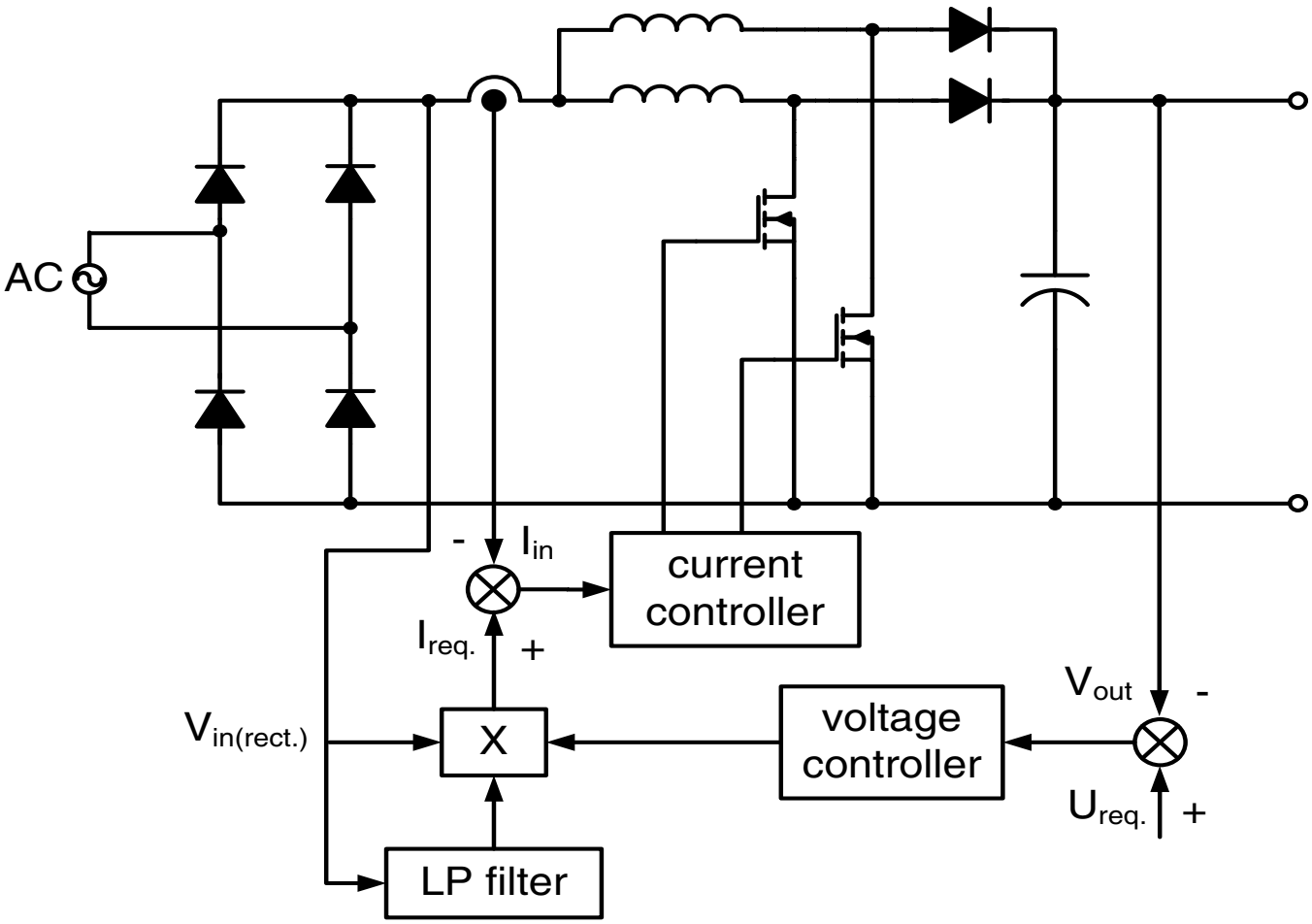

Figure 2-3. PFC Control structure

The software implements a control structured consisting of two control loops. In the outer control loop, the actual DC-bus voltage is compared with the desired one. The control error is processed by the PI (proportional-integral) controller that generates the amplitude of the reference current signal. The input rectified voltage is multiplied by the input rectified RMS voltage and the output of the voltage controller. This multiplied value is the reference current. This signal is compared to the actual one measured on the shunt resistor. The difference between them is processed in the PI current controller. The output from this controller is the PWM signal for one PFC MOSFET transistor. The PWM signal for the second transistor is shifted by 180° against the generated PWM signal.

The input current is controlled using the PFC switches to achieve the desired input current shape and the desired level of d.c. output voltage on bus capacitors. The inner current control loop should be fast enough to track current changes. The bandwidth of the current controller has to be set above 8 kHz to have sufficient response. Therefore, the

current controller algorithm has to be executed at least once every 60 µs. The outer voltage loop is used for keeping voltage on the required level. The MCU performance requirement for the voltage control loop is low. The bandwidth of the voltage control loop is set below 20 Hz, and therefore the MCU performance is not a limiting factor in this part of the PFC algorithm.

2.4 Resonant converter description

The LLC resonant topology has many advantages as opposed to other resonant topologies mentioned briefly in the Section Resonant converter topologies and features. The majority of switched mode power supplies use the transformer to provide galvanic isolation or input/output voltage adjustment. Using the transformer in LLC resonant topology brings another advantage, see Figure 2-4.

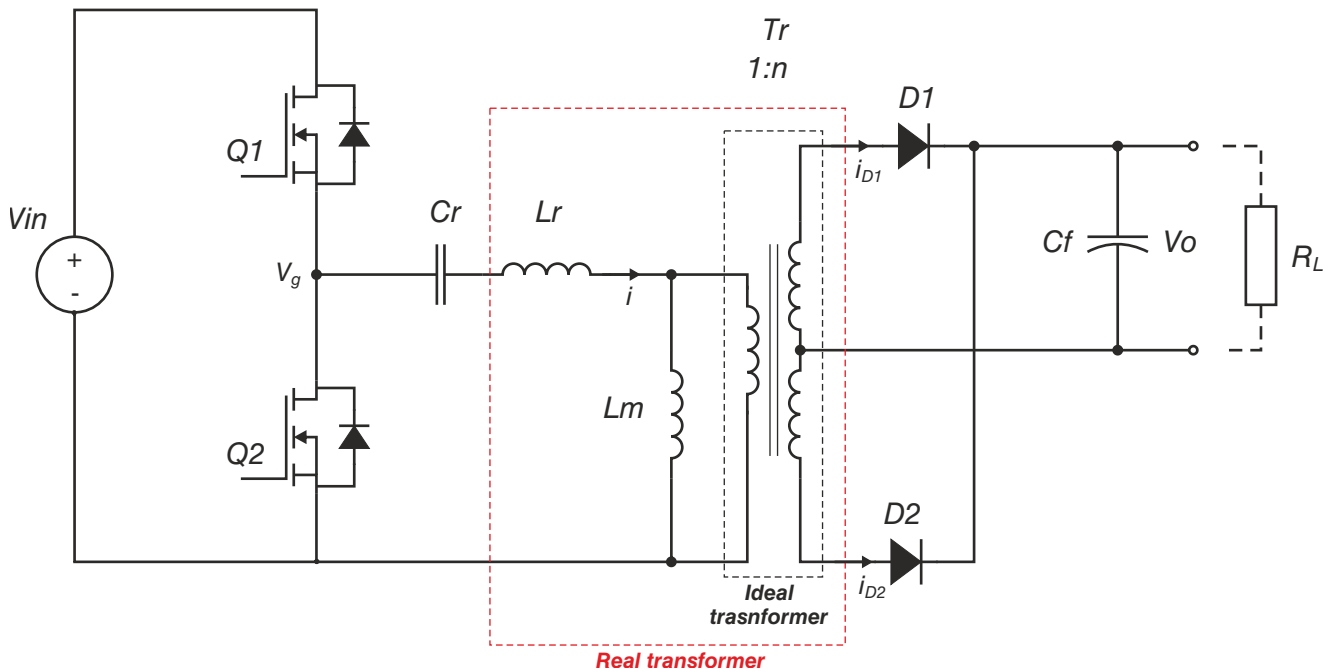

Figure 2-4. LLC resonant converter with transformer

The real transformer can be defined as an ideal transformer with magnetizing and leakage inductances (L_m, L_r). These inductances can be used as elements of the resonant circuit. This eliminates needs for additional inductances for the resonant circuit of the LLC resonant converter. There are also techniques for integrating a parasitic capacitor into a transformer. Therefore components necessary for a resonant circuit are built into the transformer. The only drawback of this approach is a limited variability of components values.

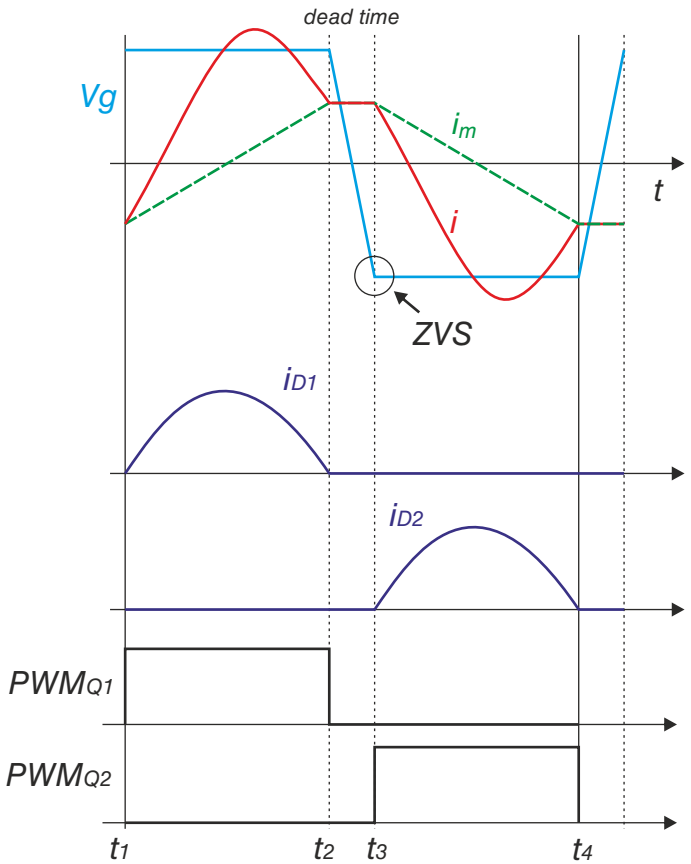

Figure 2-5. LLC resonant converter waveforms at resonant frequency

The typical waveforms of the LLC resonant converter can be seen in Figure 2-5. The square wave voltage V_g is generated by a half bridge consisting of transistors Q1 and Q2. The transistors are switched in a complementary manner with 50 % of duty cycle. The magnetizing current starts to increase from it's minimal value together with the load current. If the LLC converter operates in resonant frequency, the load current achieves zero value at the end of Q1 PWM pulse. At this moment the magnetizing current also reaches it's maximum. After the transistor Q1 is switched off, the magnetizing current continues to flow through the internal output capacitance of transistor Q1. To ensure correct ZVS operation the dead-time has to be long enough to allow to completely charge the internal MOSFET capacitance of transistor Q1 to the DC bus voltage. At the end of the dead-time the drain-source voltage of the transistor Q2 equals zero. Therefore, the transistor Q2 can be switched on at ZVS condition. The second half period is similar to the first half period. After transistor Q2 is switched on the magnetizing current starts to fall. The load current flows in an opposite polarity. At the end of the period the load current achieves zero and the magnetizing current its minimal value. Consequential dead-time ensures the ZVS condition for the transistor Q1. After the drain to the source voltage of transistor Q1 is zero, the operation can then start from the beginning. The Figure 2-5

shows the LLC converter operation in resonant frequency. At this frequency the load current on both the primary and secondary part goes to zero value, thus the switching losses are minimized as much as possible.

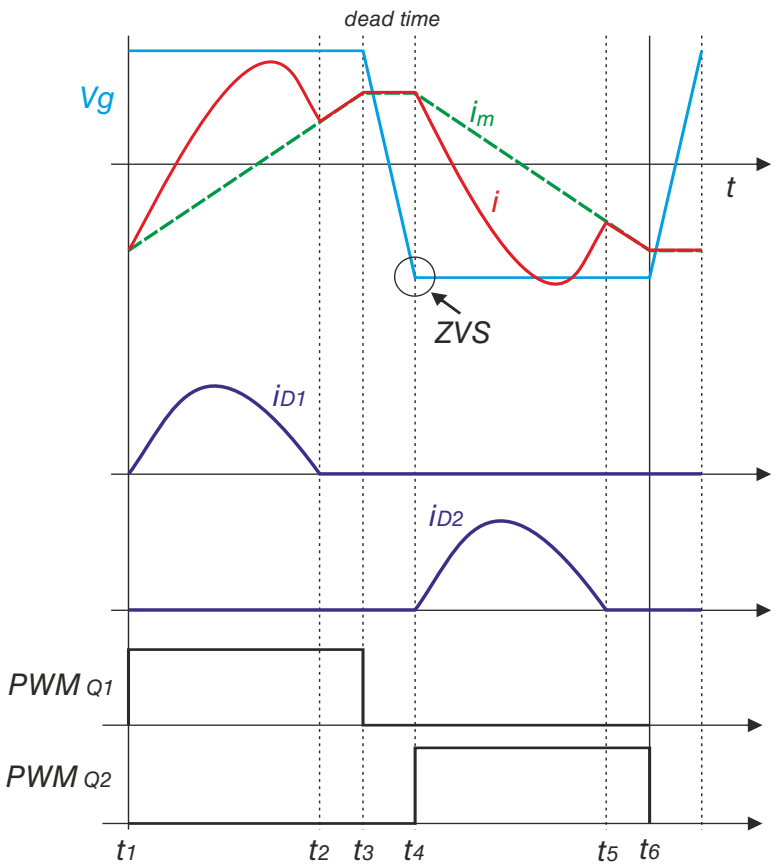

Figure 2-6. LLC resonant converter waveform below resonant frequency

The operation under resonant frequency (Figure 2-6) is similar to the operation at resonant frequency. In addition there is an interval (t_2-t_3), where the load current is zero.

In this last case, operation above resonant frequency, the load current is forced to fall to zero at the end of half period. This leads to increased reverse recovery losses (see Figure 2-7.).

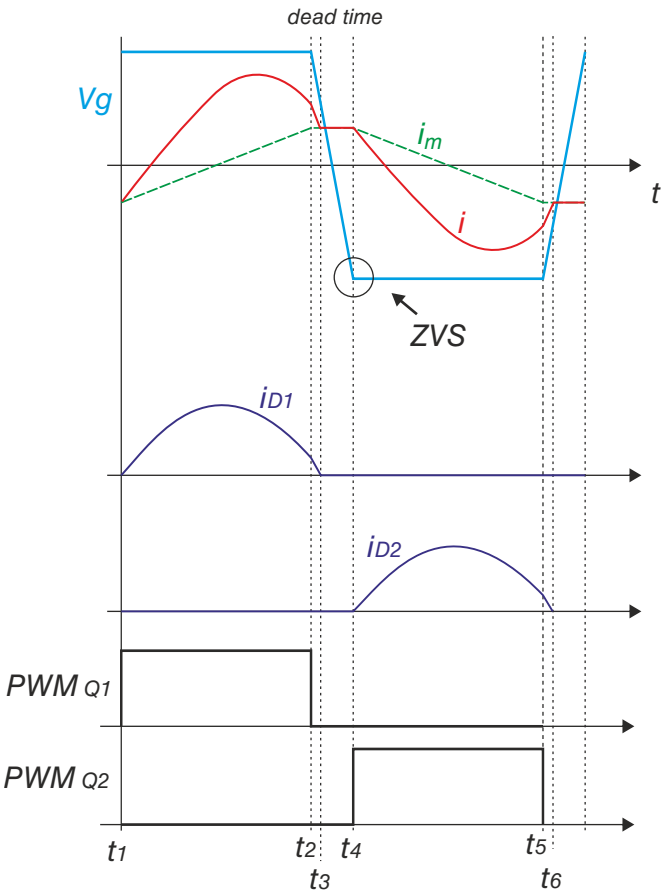

Figure 2-7. LLC resonant converter waveform above resonant frequency

To analyze the LLC resonant converter behavior you can re-draw the circuit on Figure 2-4 with the equivalent circuit on Figure 2-8.

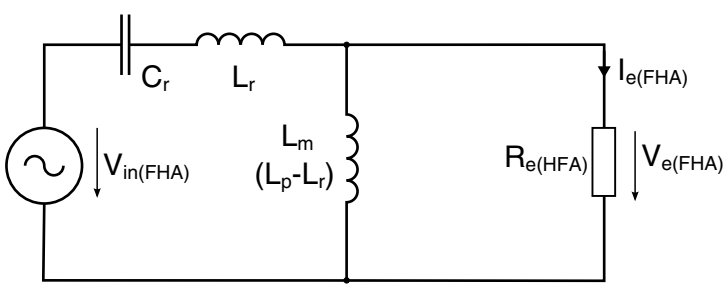

Figure 2-8. Equivalent circuit of LLC resonant converter

There are two approaches used in publications for LLC resonant converter analysis. The first one is omitting the leakage inductance on the secondary side of the transformer. The second one considers this inductance. In this designer reference manual the second approach is used considering the secondary leakage. Figure 2-8 and Figure 2-9.

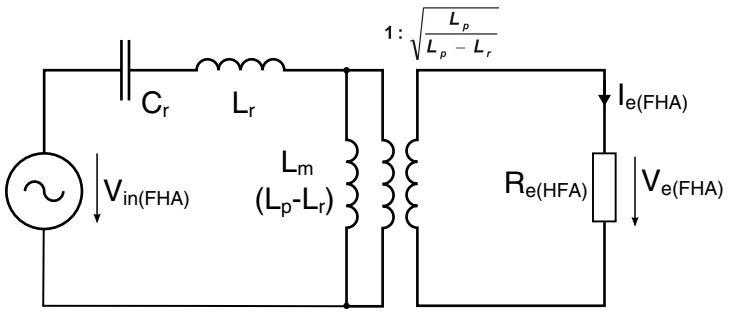

Figure 2-9. Updated Equivalent Circuit of LLC Resonant Converter

Assuming that the power is transfered mainly by a fundamental component of voltages and currents, the First Harmonic Approximation (FHA) approach can be used to analyze the LLC resonant converter behavior. Thus output quantities can be transformed to V_O, I_O, and R_O to $V_{e(FHA)}$, $I_{e(FHA)}$ and $R_{e(FHA)}$ according to Equation 1, Equation 2 and Equation 3 .

Equation 1:

$$V_{e(\mathrm{FHA})} = \frac{4V_O}{\pi}\sin(\omega t)$$

Equation 2:

$$I_{e(\mathrm{FHA})} = \frac{\pi I_O}{2\pi}\sin(\omega t)$$

Equation 3:

$$R_{e(\mathrm{FHA})} = \frac{8V_0}{\pi^2 I_O} = \frac{8}{\pi^2}R_0$$

Considering the transformer ratio $M_{TR}=\sqrt{(L_p/(L_p–L_r))}$, the equivalent load resistant on the primary side can be written as:

Equation 4:

$$R_{e(\mathrm{FHA})} = \frac{8n^2R_O}{\pi^2 M_{\mathrm{Tr}}^2}$$

Then the LLC resonant converter output transfer function can be obtained:

Equation 5:

$$M = \frac{2nV_0}{V_{\mathrm{in}}} = \left|\frac{\left(\frac{\omega}{\omega_0}\right)^2(m-1)M_{\mathrm{Tr}}}{\left(\frac{\omega^2}{\omega_p^2}-1\right)+j\left(\frac{\omega}{\omega_0}\right)\left(\frac{\omega^2}{\omega_0^2}-1\right)(m-1)Q_e}\right|$$

Where

$$Q_e = \sqrt{\frac{L_r}{C_r}}\frac{1}{R_{e(\mathrm{FHA})}},\ \omega_0 = \frac{1}{\sqrt{L_rC_r}},\ \omega_p = \frac{1}{\sqrt{L_pC_r}}$$

Figure 2-10 shows the output transfer function (gain) for different values of the quality factor Q_e. As can be seen, the gain of the LLC resonant converter changes with the load. For the resonant frequency, the gain is constant regardless of the load variation defined by M_{Tr} ratio.

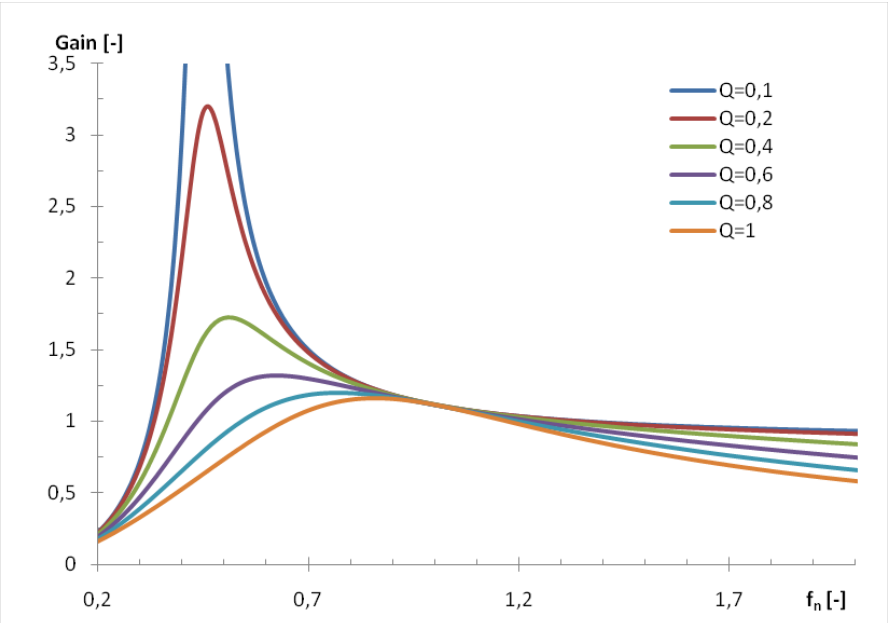

Figure 2-10. Output transfer function (Gain) for LLC resonant converter

The control of the LLC resonant converter is executed by the DSC MC56F8247 located on the secondary side of the switched mode power supply. The DSC measures the ADC converter output voltage and current. The ADC input ANB1 is also shared with built in comparator. Therefore, the output current is compared with the maximal allowed current. In case of an overload condition, the LLC resonant converter is switched off, since the output of comparator CMPB is internally connected to fault input of eFlexPWM module

The difference of the output voltage and the required voltage inputs into PI controller. The voltage mode control using the PI controller is implemented. The output of the PI controller corresponds to the switching frequency of the LLC resonant converter. The PWM signals (PWMQ1-Q4) are generated by the eFlexPWM module based on the output of the PI controller. The signal connections between the LLC resonant converter circuit and the DSC MC56F80247 can be seen in Figure 2-11.

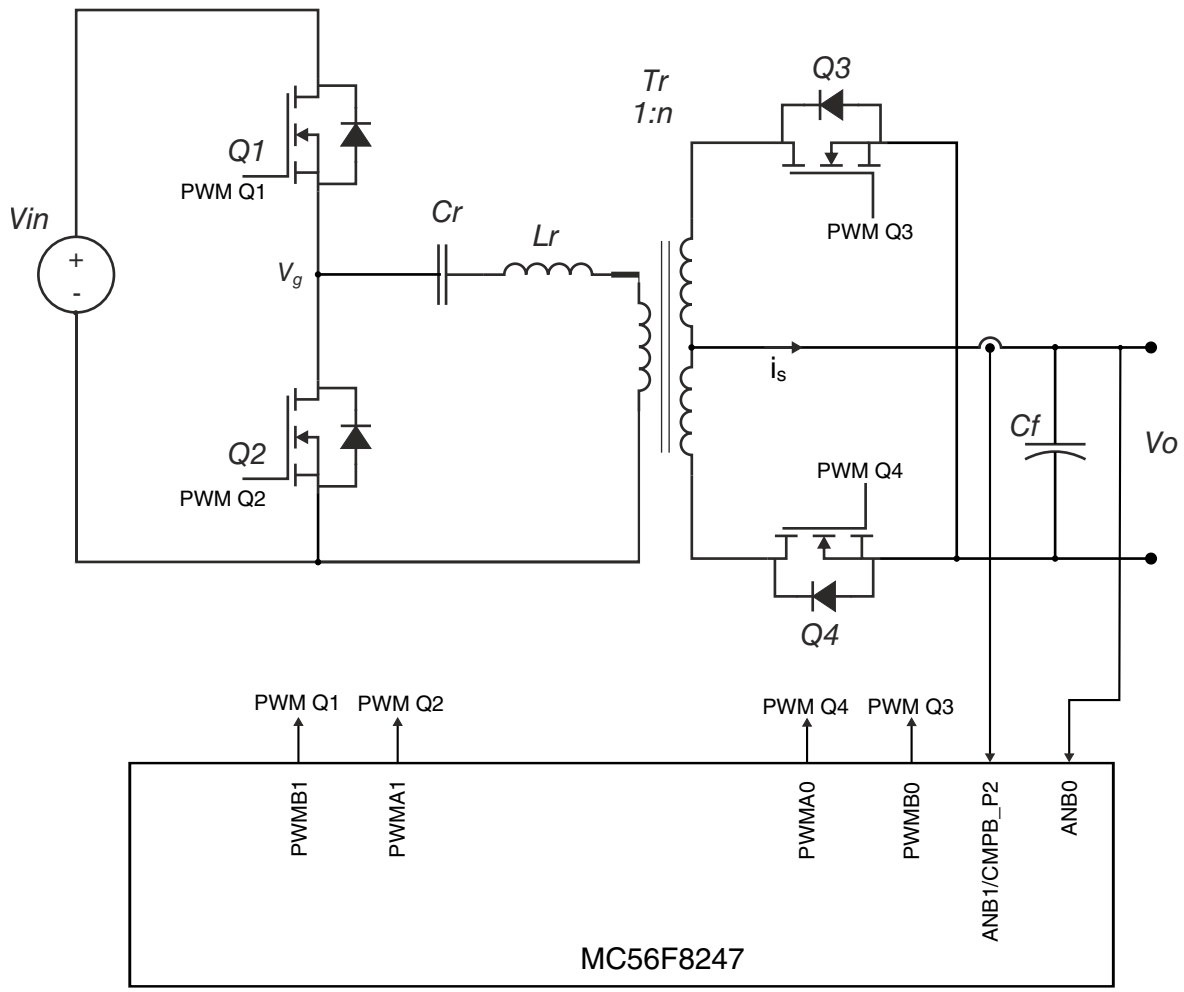

Figure 2-11. LLC resonant converter control diagram

2.5 Synchronous buck converter description

The synchronous buck converter represents a non-isolated step-down converter that converts input voltage to any lower output voltage. In this case, it generates an additional output level of 5 V from the 24 V output of the LLC resonant converter. The structure of the synchronous converter and its operation can be seen in Figure 2-12 and Figure 2-13.

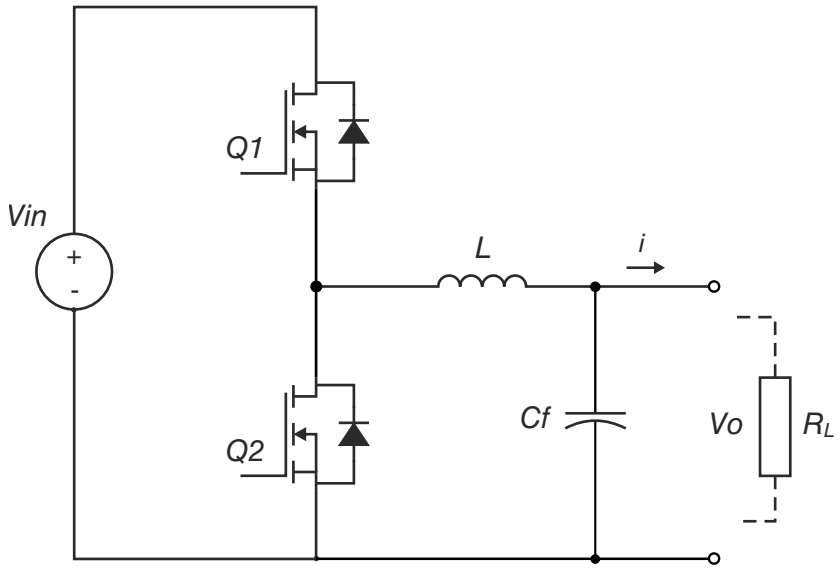

Figure 2-12. Synchronous buck converter

During the buck converter operation both MOSFET transistors are switched to complementary. When the transistor Q1 is switched on, the current flows through it, inductor L, and is divided between the filter capacitor C_f and R_L load. The current slope is defined by $(V_{in}–V_o)/L$. After the transistor Q1 is switched off, the current path is closed through a freewheeling diode on the bottom of transistor Q2. Because transistor Q2 is switched to complementary it helps to reduce conduction losses during this phase. The current slope is defined by $–V_o/L$. In case of a continuous current operation as shown in Figure 3 10, the output voltage of the buck converter is defined as:

Equation 6:

$$V_0 = DV_{in}$$

Where D is duty cycle of a PWM control signal.

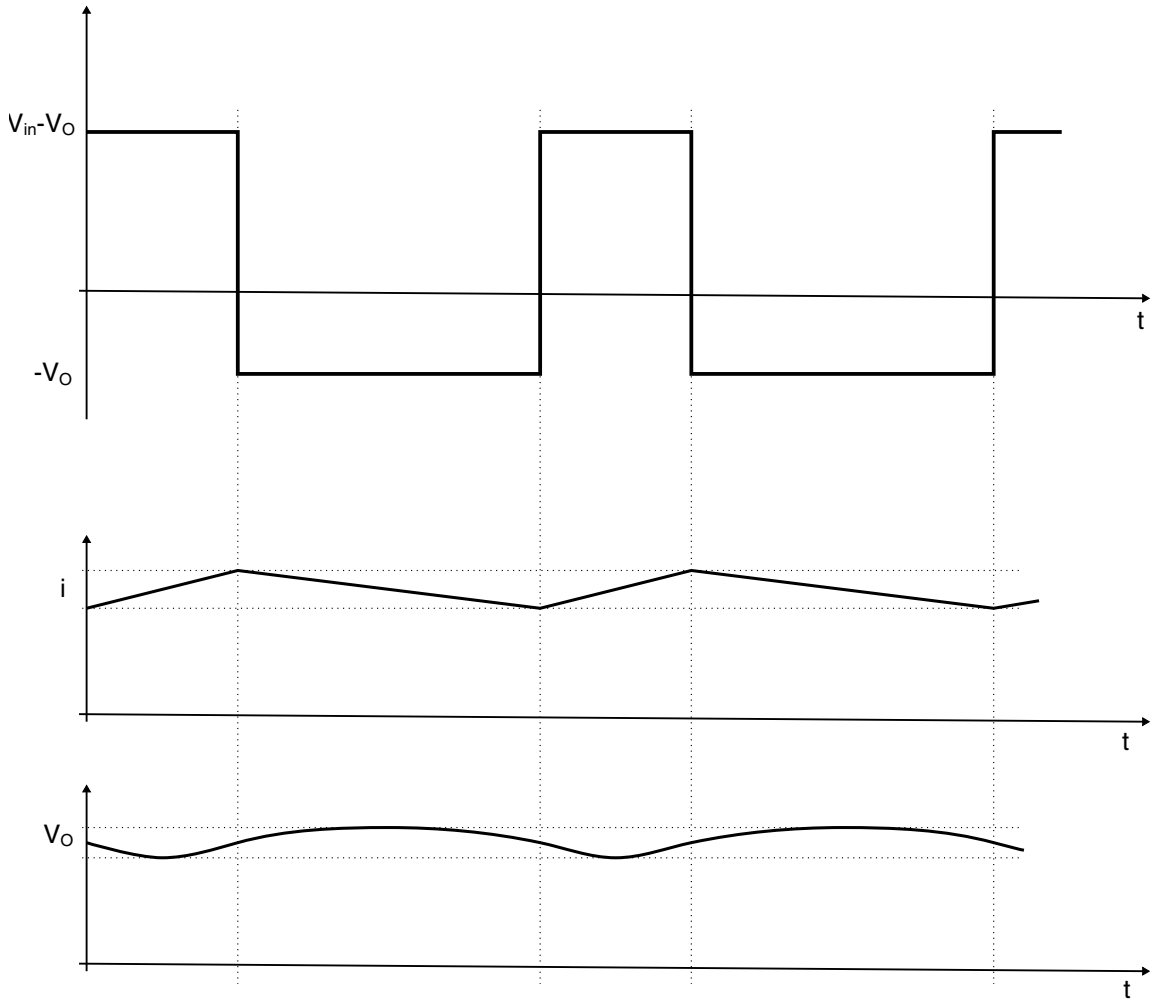

Figure 2-13. Buck converter waveforms

Control of the synchronous buck converter is executed by the DSC MC56F8247 located on the secondary side of the switched mode power supply. The DSC measures the output voltage and current with the ADC converter. The ADC input ANA1 is also shared with a built in comparator. Therefore the output current is also compared with the maximal allowed current. In case of the overload condition, the synchronous converter is switched off, because the output of comparator CMPA is internally connected to the fault input of the eFlexPWM module.

The difference of output voltage and required voltage inputs into PI controller. The voltage mode control using the PID controller is implemented. The output of the PID controller corresponds to the duty cycle of the synchronous buck converter. The PWM signals (PWM Q1-Q2) are generated by the eFlexPWM module based on the output of the PID controller. The signal connections between the synchronous buck converter circuit and the DSC MC56F80247 can be seen in Figure 2-14.

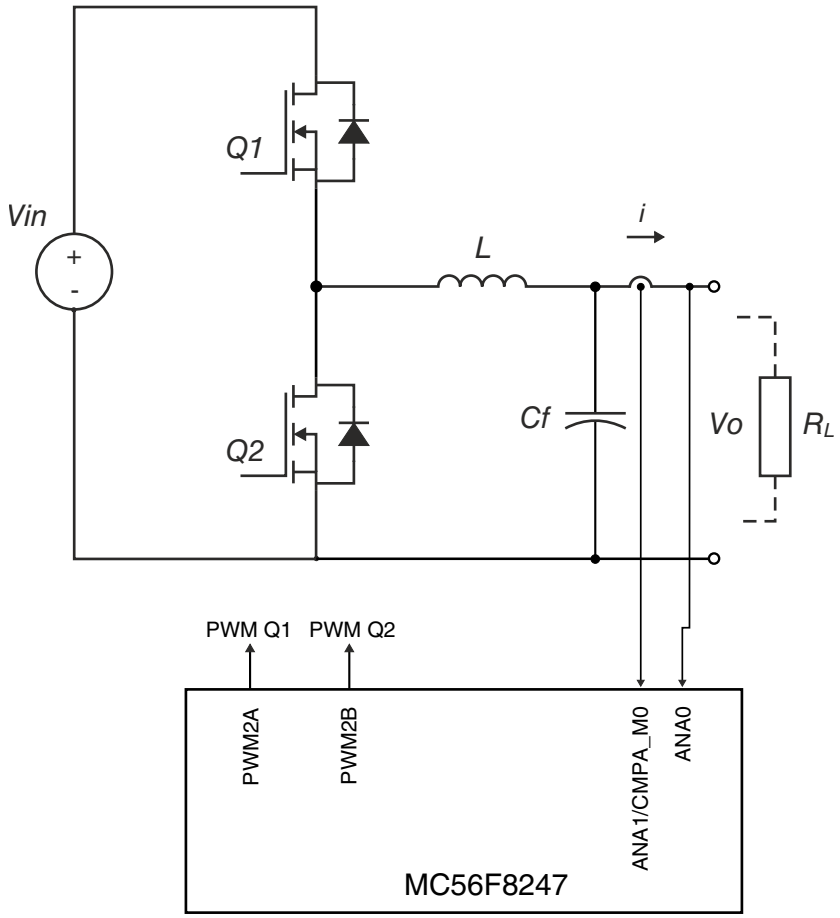

Figure 2-14. Synchronous buck converter control diagram

2.6 MC56F80xx high voltage daughter card

The MC56F80xx high voltage daughter card was designed to be a part of the platform for developing high voltage applications. The board is dedicated for a direct plug into the matching connector on the arbitrary main board. The matching connector is PCI express 64. The board can be populated with different controllers, these controllers are the MC56F8013, MC56F8023, and MC56F8006. These controllers belong to the 56800E digital signal controller family. See the differences in each part's corresponding data sheet. Figure 2-15 is an illustration of this board, populated here with the MC56F8013.

Figure 2-15. MC56F80xx high voltage daughter board card

The MC56F80xx high voltage daughter board setup is simple and straightforward. Plug the board into the PCI express 64 connector available on the main board. The board can be powered from the external power supply through power connector J1 or from the main board via main connector J3. The external power supply needs to be in a range of 5.5 to 30 volt d.c. If external power supply source is selected short header J2 uses jumper to power the board with 3.3 V. If the board is powered from the main board via the main connector then no jumper on J2 is needed.

Warning

Check the power supply voltage on the PCI express 64 connector before plugging in the MC56F80xx high voltage daughter board. If the voltage is higher than the allowed maximum power supply voltage, the controller and other components on the board can be damaged.

Warning

Load code into the controller only if the board is powered from an external power supply. Otherwise, the daughter board include other boards in the system can be damaged. The controller pins state changes during loading code and therefore the whole system's behavior is not guaranteed.

All necessary signals are available on the 64-pin main connector J3. In fact, the main connector is bottom part of the board. Figure 2-16 shows the pin assignment. This figure shows the physical layout of the PCI express 64 connector. Table 2-2 contains the list of signal descriptions for connector J3. JTAG header J4 serves for program uploading or debugging onto the controller. Signals are described in Table 2-3.

Table 2-2. Daughter card main connector J3 — Signal descriptions

Pin number	Description	Analog +3.3 V power supply
A2	GNDA1	Analog ground
A3	AN1	Analog signal connected to the ADC input
A4	AN3	Analog signal connected to the ADC input
A5	AN5	Analog signal connected to the ADC input
A6	AN7	No connect
A7	AN9	No connect
A8	AN11	No connect
A9	AN13	No connect
A10	+15VA	No connect
A11	GNDA4	Analog ground
A12	+5V	No connect
A13	GND2	Digital ground
A14	PWM0	One of the six PWM output signals
A15	PWM1	One of the six PWM output signals
A16	PWM2	One of the six PWM output signals
A17	PWM3	One of the six PWM output signals
A18	PWM4	One of the six PWM output signals
A19	PWM5	One of the six PWM output signals
A20	PWM6	No connect
A21	PWM7	No connect
A22	PWM8	No connect
A23	PWM9	No connect
A24	GND4	Digital ground
A25	FAULT_1	Fault input signal
A26	FAULT_2	Fault input signal
A27	SDA	No connect
A28	SCL	No connect

Table continues on the next page...

Table 2-2. Daughter card main connector J3 — Signal descriptions (continued)

Pin number	Description	Analog +3.3 V power supply
A29	I/O_6	No Connect
A30	I/O_7	No connect
A31	I/O_8/SCI1_TxD	No connect
A32	I/O_9/SCI1_RxD	No connect
B1	+5VA	No connect
B2	GNDA2	Analog ground
B3	AN0	Analog signal connected to the ADC input
B4	AN2	Analog signal connected to the ADC input
B5	AN4	Analog signal connected to the ADC input
B6	AN6	No connect
B7	AN8	No connect
B8	AN10	No connect
B9	AN12	No connect
B10	AN14	No connect
B11	GNDA3	Analog ground
B12	+3.3V	Digital +3.3 V power supply
B13	GND1	Digital ground
B14	TM0	Timer input signal
B15	TM1	Timer input signal
B16	TM2	No connect
B17	TM3	No connect
B18	TM4	No connect
B19	TM5	No connect
B20	I/O_1	General purpose input/output signal
B21	MISO	SPI Master In Slave Out signal
B22	MOSI	SPI Master Out Slave In signal
B23	SCLK	SPI clock source signal
B24	/SS	SPI pin chip select signal
B25	I/O_2	General purpose input/output signal
B26	SCI_TxD	SCI receive data input signal
B27	SCI_RxD	SCI transmit data output signal
B28	I/O_3	No connect
B29	I/O_4	No connect
B30	I/O_5	No connect
B31	+15V	No connect
B32	GND3	Digital ground

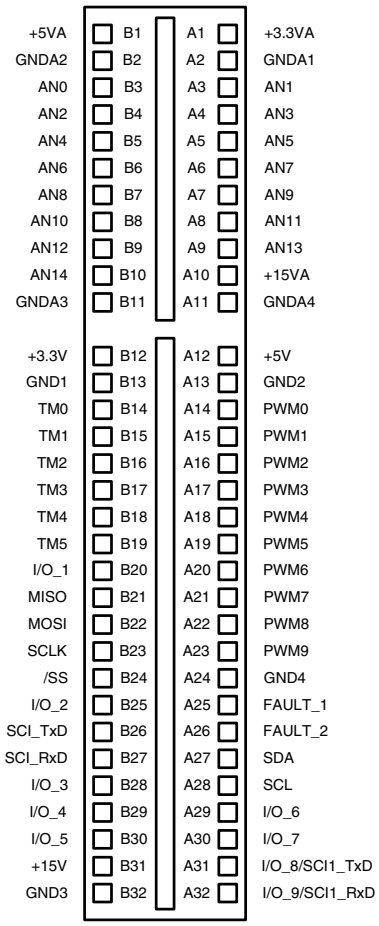

Figure 2-16. Main board connector—Physical view

Table 2-3. JTAG header J4—signal descriptions

Pin number	Signal name	Description
1	TDI	Test data input signal
2	GND	Digital ground
3	TDO	Test data output signal
4	GND	Digital ground
5	TCK	Test clock input signal
6	GND	Digital ground
7	No connect	—
8	No connect	—
9	/RESET	Reset signal
10	TMS	Test mode select input signal
11	+3.3 V	Digital +3.3–volt power supply
12	No connect	—
13	No connect	—
14	No connect	—

Resistors R6, and R8 are populated only if the MC56F8006 controller is attached.

2.7 MC56F82xx high voltage daughter card

The MC56F82xx high voltage daughter card was designed to be a part of a platform for developing high voltage applications. The board is dedicated for a direct plug into the matching connector on the arbitrary main board. The matching connector is PCI express 64. The board can be populated with different controllers. These controllers are the MC56F8247 and MC56F8257. These controllers belong to the 56800E digital signal controller family. See the differences in each part's corresponding datasheet. Figure 2-17 is an illustration of this board — populated here with the MC56F8257.

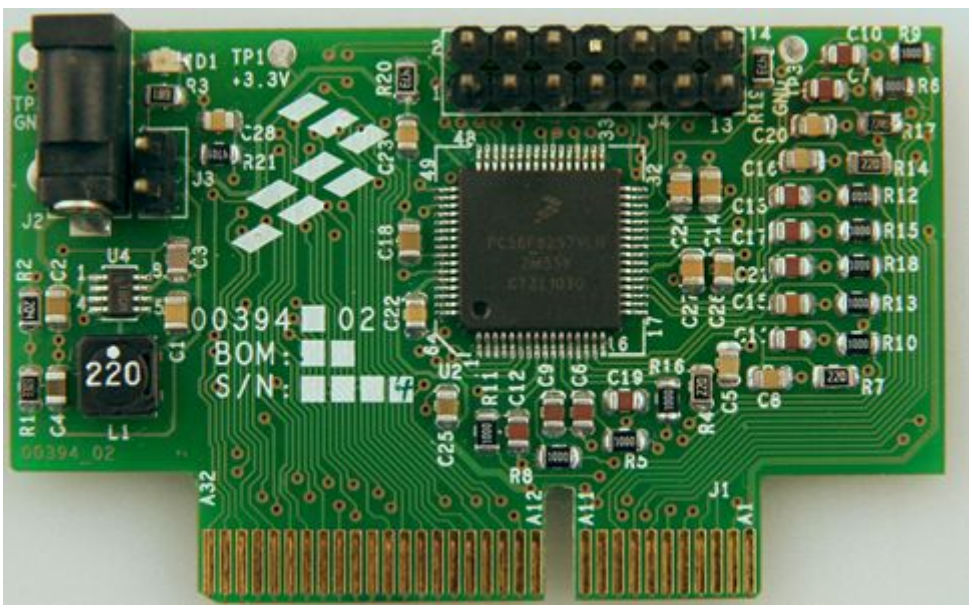

Figure 2-17. MC56F82xx High voltage daughter card board

The MC56F82xx high voltage daughter board setup is simple and straightforward. Plug the board into the PCI express 64 connector available on the main board. The board can be powered from the external power supply through the power connector J2 or from the main board via main connector J1. The external power supply needs to be in a range of 5.5 to 30 volt d.c. If the external power supply source is selected short header J3 uses the jumper to power the board with 3.3 V. If the board is powered from the main board via the main connector no jumper on J3 is needed. In that case, the power supply on the main board needs to be on.

Warning

Check the power supply voltage on the PCI express 64 connector before plugging in the MC56F82xx high voltage daughter board. If the voltage is higher than allowed maximum power supply voltage, the controller and other components on the board can be damaged.

Warning

Load code into the controller only if the board is powered from an external power supply. Otherwise, the daughter board and including other boards in the system can be damaged. The controller pins state changes during loading code and therefore the whole system's behavior is not guaranteed.

All necessary signals are available on the 64-pin main connector J1. The main connector is the bottom part of the board. Figure 2-18 shows the pin assignment. This figure shows the physical layout of the PCI express 64 connector. Table 2-4 contains the list of signal descriptions for the connector J1. The JTAG header J4 serves for program uploading or debugging onto the controller. Signals are described in Table 2-5.

Table 2-4. Daughter card main connector J1 — Signal Descriptions

Pin number	Signal name	Description
A1	+3.3 VA	Analog +3.3 V power supply
A2	GNDA1	Analog ground
A3	AN1	Analog signal connected to the ADC input
A4	AN3	Analog signal connected to the ADC input
A5	AN5	Analog signal connected to the ADC input
A6	AN7	Analog signal connected to the ADC input
A7	AN9	Analog signal connected to the ADC input
A8	AN11	Analog signal connected to the ADC input
A9	AN13	Analog signal connected to the ADC input
A10	+15VA	No connect
A11	GNDA4	Analog ground
A12	+5V	No connect
A13	GND2	Digital ground
A14	PWM0	One of the eight PWM output signals
A15	PWM1	One of the eight PWM output signals
A16	PWM2	One of the eight PWM output signals
A17	PWM3	One of the eight PWM output signals
A18	PWM4	One of the eight PWM output signals

Table continues on the next page...

Table 2-4. Daughter card main connector J1 — Signal Descriptions (continued)

Pin number	Signal name	Description
A19	PWM5	One of the eight PWM output signals
A20	PWM6	One of the eight PWM output signals
A21	PWM7	One of the eight PWM output signals
A22	PWM8	No connect
A23	PWM9	No connect
A24	GND4	Digital ground
A25	FAULT_1	Fault input signal
A26	FAULT_2	Fault input signal
A27	SDA	I^2C serial data line signal
A28	SCL	I^2C serial clock signal
A29	I/O_6	General purpose input and output signal
A30	I/O_7	General purpose input and output signal
A31	I/O_8/SCI1_TxD	General purpose input and output or SCI transmit data input signal
A32	I/O_9/SCI1_RxD	General purpose input and output or SCI receive data input signal
B1	+5VA	No connect
B2	GNDA2	Analog ground
B3	AN0	Analog signal connected to the ADC input
B4	AN2	Analog signal connected to the ADC input
B5	AN4	Analog signal connected to the ADC input
B6	AN6	Analog signal connected to the ADC input
B7	AN8	Analog signal connected to the ADC input
B8	AN10	Analog signal connected to the ADC input
B9	AN12	Analog signal connected to the ADC input
B10	AN14	Analog signal connected to the ADC input
B11	GNDA3	Analog ground
B12	+3.3V	Digital +3.3V power supply
B13	GND1	Digital ground
B14	TM0	Timer input signal
B15	TM1	Timer input signal
B16	TM2	Timer input signal
B17	TM3	No connect
B18	TM4	No connect

Table continues on the next page...

Table 2-4. Daughter card main connector J1 — Signal Descriptions (continued)

Pin number	Signal name	Description
B19	TM5	No connect
B20	I/O_1	General purpose input and output signal
B21	MISO	SPI Master in slave out signal
B22	MOSI	SPI Master in slave out signal
B23	SCLK	SPI Clock source signal
B24	/SS	SPI Pin chip select signal
B25	I/O_2	General purpose input/output signal
B26	SCI_TxD	SCI receive data input signal
B27	SCI_RxD	SCI transmit data output signal
B28	I/O_3	General purpose input and output signal
B29	I/O_4	General purpose input and output signal
B30	I/O_5	General purpose input and output signal
B31	+15V	No connect
B32	GND3	Digital ground

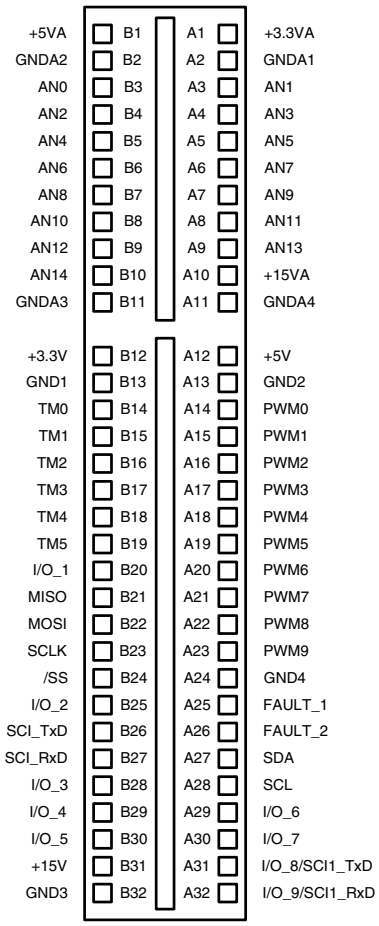

Figure 2-18. Main board connector physical view

Table 2-5. JTAG Header J4 — Signal descriptions

Pin number	Signal name	Description
1	TDI	Test data input signal
2	GND	Digital ground
3	TDO	Test data output signal
4	GND	Digital ground
5	TCK	Test clock input signal
6	GND	Digital ground
7	No connect	—
8	No connect	—
9	/RESET	Reset signal
10	TMS	Test mode select input signal
11	+3.3 V	Digital +3.3–volt power supply
12	No connect	—
13	No connect	—
14	No connect	—

Chapter 3
Hardware Design

3.1 Overview

This chapter describes the design of the application hardware. The hardware incorporates five main parts:

- Interleaved PFC
- LLC resonant converter and buck converter
- Auxiliary power supply
- MC56F8013 daughter card board
- MC56F8257 daughter card board

This chapter focuses on the design of the interleaved PFC, LLC resonant converter, buck converter, and auxiliary power supply. The MC56F8013 and MC56F8257 daughter cards designed are described in the user's manual MC56F8013HVDCUM and MC56F8257HVDCUM.

3.2 Interleaved PFC hardware design

This section of the design reference manual describes main components of the interleaved PFC circuit. They are PFC inductor, MOSFET switch, boost diode and D.C. link capacitor. As interleaved PFC consists of two identical parallel connected boost converters the calculated values are for both legs of converter identical. There is a lot of technical literatures explaining the design of power factor correction circuits.There is no need to go into detail in components design. Literature used for this design is mentioned in this manual, in section References.

3.2.1 PFC Inductor design

The compromise between the PFC inductor size and the ripple current influences the inductor design. Other parameters like switching frequency f_s, and THD need to be taken into consideration. Inductor value calculation starts from calculating input current peak I_{PK} per one leg of the converter.

Equation 7:

$$I_{PK} = \frac{\sqrt{2} P_{OUT}}{n V_{IN(MIN)}}$$

Where:

P_{OUT}— Output power

n — Number of interleaved phases

$V_{IN(MIN)}$— Minimum input voltage

Next step is to calculate ripple current value. The current ripple ratio chosen is 20% of the input current peak. Then the current ripple ΔI_L is:

Equation 8:

$$\Delta I_L = k_{RIPPLE} I_{PK}$$

Where:

k_{RIPPLE}— Ripple current ratio, 20% selected

Finally, you can calculate the inductance using formula:

Equation 9:

$$L = \frac{V_{OUT}}{4 \Delta I_L f_S}$$

Where:

V_{OUT}— D.C. link output voltage

f_s— Switching frequency

Switching frequency was selected based on fastest interrupt service routine execution time (QT3Isr). Maximum execution time of routine is 6 us. There is also a need to have more time for a slower interrupt routine execution (QT0Isr). Finally, 100 kHz switching frequency was selected. Possible optimization of both ISR time execution give some space for increasing switching frequency. Switching losses are increasing with the increasing switching frequency, therefore optimization can be made in terms of losses, efficiency, or size if these parameters are strictly required for the overall system design.

3.2.2 PFC Transistor design

The MOSFET transistor selection depends on input peak current I_{PK} and output voltage V_{OUT}. The k_{RIPPLE} in the equation represents current variations. Maximum MOSFET current must be higher than I_{LPK} and the drain-source voltage must be higher than V_{OUT}. Equation for inductor peak current calculation is mentioned in Equation 10. Voltage rating of MOSFET transistor must be higher than d.c. link output voltage V_{OUT}. The RMS value of the MOSFET forward current should be higher than the value calculated in Equation 11.

Equation 10:

$$I_{LPK} = \frac{\sqrt{2}P_{OUT}}{nV_{IN(MIN)}}(1+k_{RIPPLE})$$

Equation 11:

$$I_F = \frac{P_{OUT}}{\eta \times V_{IN(MIN)}} \times \sqrt{D}$$

3.2.3 Boost diode design

The diode selection depends on reverse recovery time t_{rr}, operating current, and voltage. Reverse recovery time t_{rr} of the selected diode should be as small as possible to minimize power losses in the diode. The reverse recovery voltage value must be higher than output voltage V_{OUT}. Diode maximum forward current must be higher than the inductor peak current from Equation 10. The diode forward current must be higher than value calculated using Equation 12. Most suitable diodes with a very low t_{rr} time are SiC technology based on diodes.

Equation 12:

$$I_D = \frac{P_{OUT}}{nV_{IN(MIN)}}\sqrt{1-D}$$

3.2.4 D.C. Link capacitor tank design

The output capacitor is calculated based on the hold-up time.

Equation 13:

$$C \geq \frac{2P_{OUT}t_{hup}}{(1.1V_{OUT})^2-(0.9V_{OUT})^2}$$

Where:

t_{hup}— Hold-up time selected 20 ms

Minimum value of the output capacitor tank is 400 uF. 20% capacity tolerance was taken into consideration. Eight 56 uF capacitors to create the D.C. link capacitor tank was selected and connected in parallel. For this output capacitor the value of the voltage ripple is at the converter output:

Equation 14:

$$V_{RIPPLE} = \frac{P_{OUT}}{2\pi V_{OUT} f_{MIN} C_{OUT}}$$

Where:

f_{min}— Minimum mains frequency

C_{OUT}— D.C. link capacitor tank value

Other parameters for proper capacitors selection must be taken into consideration. Those parameters are low frequency current and high frequency current. These parameters should be available in the capacitor's datasheet and the calculated values from equations Equation 15 and Equation 16.

Equation 15:

$$I_{COUT\_LF} = \frac{P_{OUT}}{\eta V_{OUT}\sqrt{2}}$$

and

Equation 16:

$$I_{COUT\_HF} = \sqrt{\left(\frac{P_{OUT}}{\eta V_{OUT}}\sqrt{\frac{16V_{OUT}}{6\pi\sqrt{2}V_{IN(MIN)}} - \eta^2}\right)^2 - I_{COUT\_LF}^2}$$

3.3 LLL resonant converter hardware design

This chapter describes a design procedure for the LLC resonant converter. The inputs used for calculations are as follows:

3.3.1 LLC resonant converter specification

Output power (P_O) — 350 W

Output voltage (V_O) — 24 V

Diode voltage drop (V_F) — 0.3V

Min. DC Bus Voltage (V_{min}) — 300 V

Max. DC Bus Voltage (V_{max}) — 400 V

Resonant switching frequency (f_O) — 200 kHz

L_p/L_r ratio (m) — 5

3.3.2 Resonant network design

Most of the parameters are given by requirements of the power supply requirements. The first design parameter that must be chosen, is the L_p/L_r ratio (m). According to the LLC resonant converter behavior analysis, the recommended value of m must be kept in a range of 5 – 10. If using the transformer leakage inductance as resonant inductance, there is a limited possibility of m choice, that is because the L_p/L_r ratio is defined by the mechanical construction of the transformer. The required gain of the LLC resonant converter is calculated and can be derived at a resonant frequency from the converter minimal gain. See Equation 17.

Equation 17:

$$M_{min} = \sqrt{\frac{m}{m-1}} = \frac{5}{5-1} = 1.12$$

For the minimal input voltage V_{min}, the maximal gain can be calculated as:

Equation 18:

$$M_{max} = \frac{V_{max}}{V_{min}} M_{min} = \frac{400}{300} 1.12 = 1.49$$

Knowing the minimal and maximal gain the transformer turns ratio can be calculated according to Equation 19.

Equation 19:

$$n = \frac{N_p}{N_s} = \frac{V_{max}}{2(V_0 + V_F)} M_{min} = \frac{400}{2 \cdot (24+0.3)} 1.12 = 9.20$$

Next step is calculating the equivalent load resistance, which is needed for resonant network calculation. It can be obtained as:

Equation 20:

$$R_{e(FHA)} = \frac{8 n^2 v_0^2}{n^2 P_0} = \frac{8 \cdot 9.2^2 24^2}{n^2 350^2} = 113\Omega$$

The resonant circuit consists of resonant capacitor C_r and resonant inductor L_r. The resonant capacitor can be calculated as:

Equation 21:

$$C_r = \frac{1}{2\pi Q_e f_0 R_{e(FHA)}}$$

As can be seen from Equation 5, the quality factor Q_e also depends on Cr. Therefore, the behavior of the resonant converter has to be analyzed for different values of Q_e . Using Equation 5 and changing the quality factor of the Q_e value from 0.1 to 1 results in different gain characteristics of the LLC resonant converter. Considering the maximum gain only, the Peak gain versus Q_e graph can be drawn, as Figure 3-1. Since the maximal required gain M_{max} is already known (see Equation 18), the Q_e value can be taken from the graph. To ensure safe LLC converter operation, the maximal gain should be increased by 10-20%. Then the maximal gain is equal to 1.71 taking onto consideration a 15% margin. The quality factor Q_e can be read from the graph on Figure 3-1, where Qe=0.41.

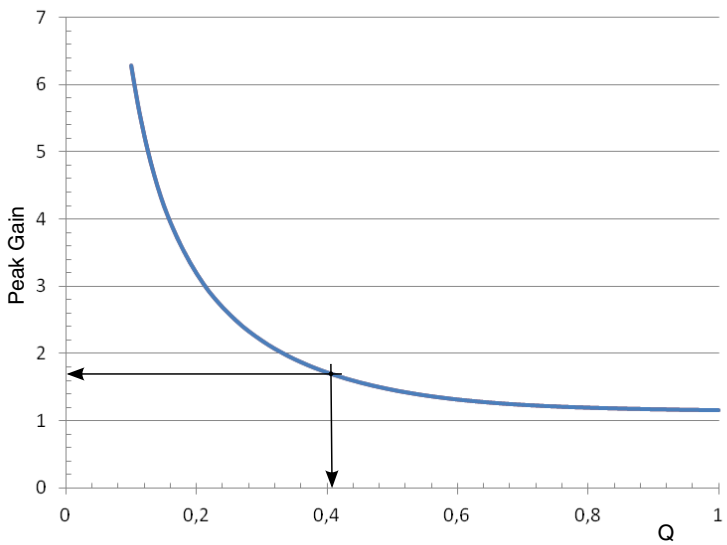

Figure 3-1. Peak gain versus Q_e for m=5

Now the resonant capacitor C_r can be calculated as:

Equation 22:

$$C_r = \frac{1}{2\pi \cdot 0.41 \cdot 200 \cdot 10^3 \cdot 113} = 17.2\text{nF}$$

Because the ratio between the primary transformer inductance, the resonant inductance (m) was defined at the beginning of the design. The primary winding inductance can be calculated as:

Equation 23:

$$L_p = mL_r = 5 \cdot 36.8 = 184\mu\text{H}$$

3.3.3 Transformer design

The size of the transformer depends on the operating frequency. Since the LLC resonant converter operates with a variable switching frequency, the minimal switching frequency must be obtained. The minimal switching frequency can be obtained from Equation 5 (see Figure 3-2). From this graph, the minimal switching frequency f_{min} is 128 kHz. This operation point corresponds to an operation at a minimal DC bus voltage and full load.

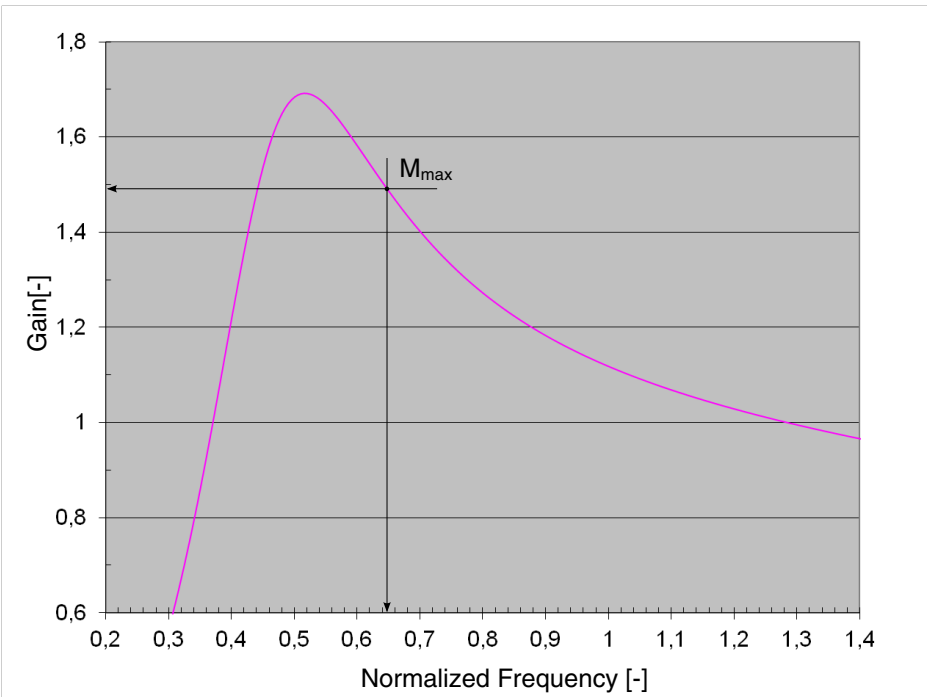

Figure 3-2. Gain at full load

The minimal number of turns of the primary winding can now be obtained as:

Equation 24:

$$N_{pmin} = \frac{n(V_0 + V_F)}{2f_{min} \cdot M_{min} \cdot \Delta B \cdot A_e}$$

To finalize the primary turns calculation, the cross-sectional area of the transformer core and maximum flux density swing has to be chosen. The transformer uses an ETD34 core from N87 material. For this core the $A_e = 97.1 \times 10^{-6}$ m^2. The maximum flux density swing can be chosen up to 0.4 T for ferrite material, but in this case 0.2 T was chosen to reduce losses in the magnetic core. The minimal number of primary turns can then be obtained as:

Equation 25:

$$N_{pmin} = \frac{9.2(24+0.3)}{2 \cdot 128 \cdot 10^3 \cdot 0.2 \cdot 97.1 \cdot 10^{-6}} = 30.2 \text{turns}$$

For the number of secondary turns to be valid, $n.N_s > N_{p\ min}$. The 3 secondary turns makes N_p=28 turns. This is slightly below the $N_{p\ min}$, therefore the final flux density swing is 0.215 T, which is still far from being the allowed limit.

To build the transformer, there are two sections bobbin used. The two sections bobbin allows increase leakage inductance, which is used as the resonant inductor. The first section is used for primary winding, the second one for secondary winding. The primary winding uses Litz wire 1x120x0.071 mm. The secondary winding uses three strands in parallel of the same Litz wire (1x120x0.071 mm). The last step in the transformer construction selecting a proper core gap. Standard gaps for a selected core are available in ranges from 0 to 2 mm. The required primary inductance L_p was obtained for g=0.5 mm. Observe that the leakage inductance is almost constant, even if gap has changed. Finally the one core with g=0 mm and one core with g=0.5 mm are selected. For this core combination L_p=188 µH and Lr=38 µH. Because the leakage inductance depends on mechanical construction (winding layout), it may be difficult to achieve the desired ratio L_p and L_r. In this case some input parameters can be slightly changed (f_0, L_p/L_r, min/max DC Bus voltage) if the application allows. The second possibility is to use a separate inductor for the resonant circuit.

3.4 Synchronous Buck Converter Design

3.4.1 Synchronous buck converter specification

Input voltage (V_{in}) — 24 V

Output Voltage (V_O) — 5 V

Output power (P_O) — 100 W / Output Current (I_O): 20 A

Switching frequency (f) — 234 kHz

Current ripple — 20% I_O

Voltage ripple — 50 mV

3.4.2 Synchronous buck converter design

The synchronous buck converter calculation starts with a duty cycle calculation:

Equation 26:

$$D = \frac{V_0}{V_{in}} = \frac{5}{24} = 0.20833$$

The inductor value can be obtained from:

Equation 27:

$$L = \frac{(V_{in} - V_0) \cdot \Delta t}{\Delta i}$$

Equation 27 can be rewritten as:

$$L = \frac{(V_{in} - V_0) \cdot D}{f \cdot \Delta i} = \frac{(24-5) \cdot 0.20833}{234 \cdot 10^3 \cdot 4} = 4.22\,\mu H$$

Closest value 4 µH (available as a standard value) was chosen. The capacitor value is selected to meet the desired voltage ripple on the output of buck converter. The voltage ripple is the sum of the voltage drop over an effective series resistance (R_{ESR}), and voltage variation due to charging and discharging the capacitor, see Equation 28.

Equation 28:

$$\Delta V = \Delta I \left(R_{ESR} + \frac{D}{f \cdot C} \right)$$

Equation 28 can be rearranged, then the capacitor value is equal to:

Equation 29:

$$C = \frac{\Delta I \cdot D}{f(\Delta V - \Delta I \cdot R_{ESR})}$$

The equation Equation 29 still contains one unknown variable R_{ESR}. To ensure that equation Equation 29 makes physical sense, the following condition has to be met:

Equation 30:

$$\Delta V > \Delta I \cdot R_{ESR}$$

Therefore before capacitance calculation a capacitor with a proper R_{ESR} has to be selected. In this case $R_{ESR} < \Delta V/\Delta I = 0.05/4 = 0.0125\ \Omega$. Selected capacitor 1500 μF with R_{ESR} = 0.010 Ω. Now the capacitor value can be calculated as:

Equation 31:

$$C = \frac{4 \cdot 0.28033}{234 \cdot 10^3 \cdot (0.05 - 0.010 \cdot 4)} = 480\mu F$$

The result shows that any capacitor with capacitance higher than 480 µF and R_{ESR} < 0.010Ω is suitable to meet 50 mV of the output voltage ripple.

3.5 Auxiliary power supply hardware design

The auxiliary power supply provides supply voltages for signal, control, digital, and driving circuits on the primary and secondary side. The power supply is based on fly-back topology, suitable for low power ratings with an isolation barrier between the

primary and secondary side. The main part of this power supply is the off-line switcher from the Power Integrations TNY275 with a power capability of up to 15 W which is sufficient for this purpose. Input parameters necessary for all component calculations in the PI expert design software can be seen in Table 3-1.

Table 3-1. Input design parameters

Parameter	Value
Input voltage	300 – 400 VDC
Output Voltage 1 / Output Current 1	12V / 0.15 A
Output Voltage 2 / Output Current 2	6V/0.3 A
Total Output Power	7.2 W

As described in detail, each component calculation is part of this tool and further explanation is not needed. The tool is free and available at www.powerint.com. The power supply block diagram is shown in Figure 3-3.

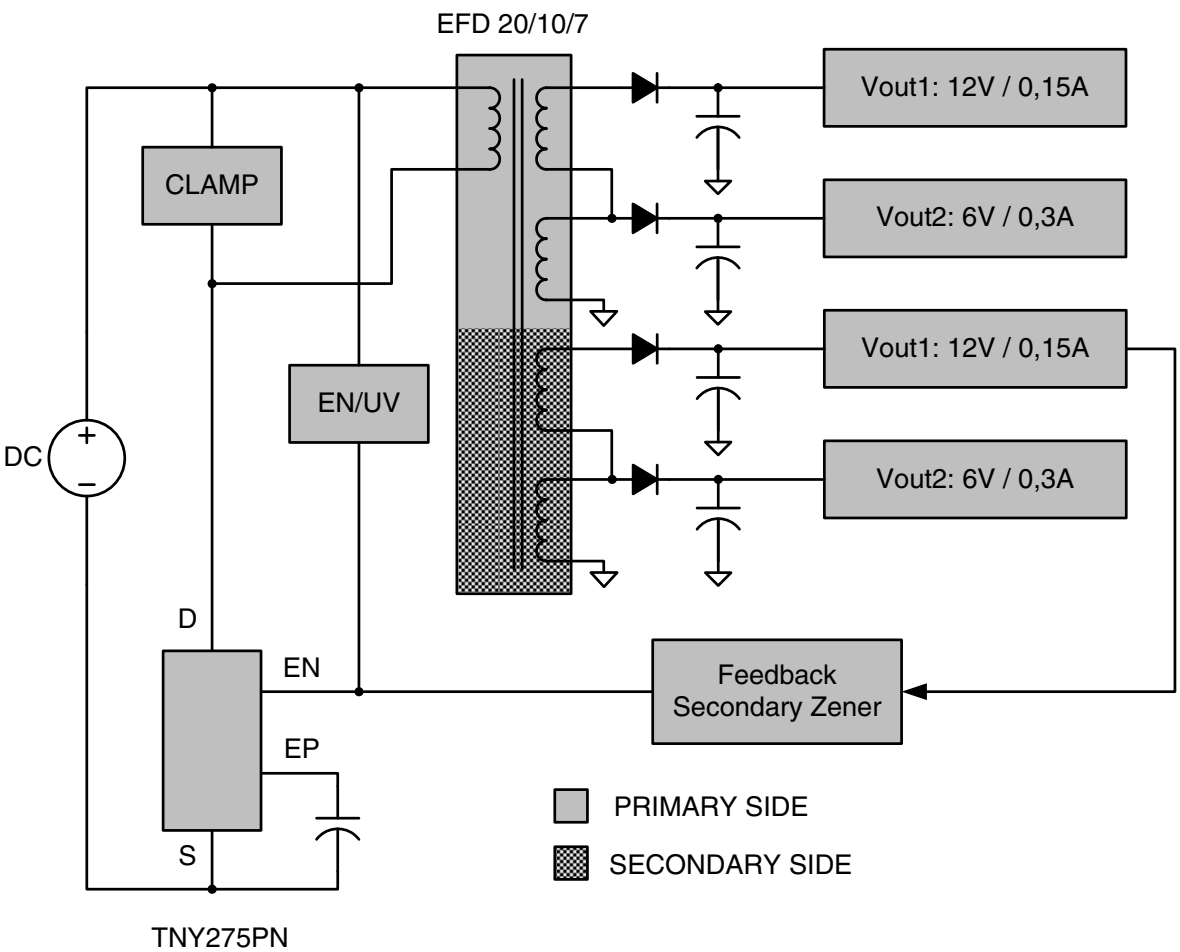

Figure 3-3. Auxiliary power supply block diagram

The power supply provides two levels of equal voltages, for the primary and secondary side –12 V and 3.3 V. A 12 V power supply voltage is used for supplying drivers on both sides, the fan, and the input relay on the primary side is directly gained at the output of the transformer after rectification and filtering. The 3.3 V power supply voltage precise value is critical for system behavior. Therefore, this power supply is generated using the voltage regulator. The source for the voltage regulator is derived from 6 V which is generated on the winding stacked with winding generated 12 V power supply on the fly-back transformer.

The image shows that feedback is taken only from secondary side. Therefore, minimum load on the secondary side is necessary for correct power supply generation on the primary side. Proper positions of primary to secondary winding can eliminate this effect, therefore manufacturing of the fly-back transformer is an important task. Winding positions and parameters can be seen in Figure 3-4.

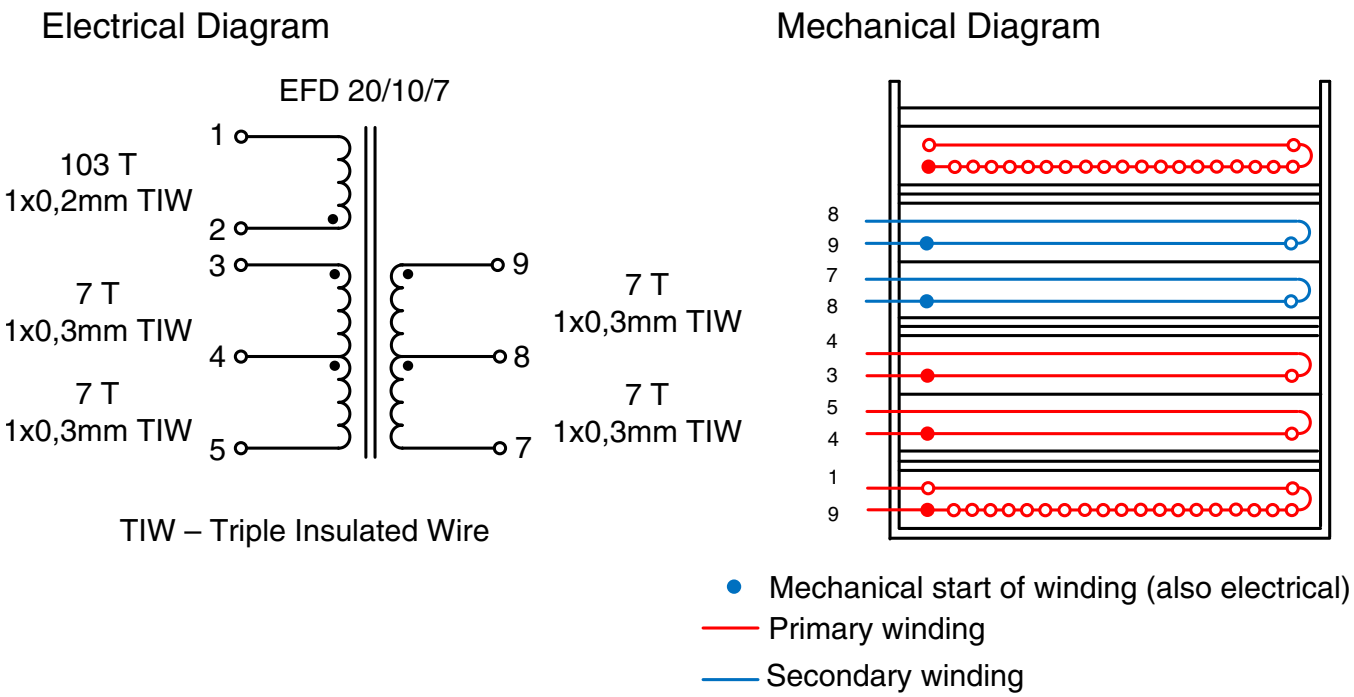

Figure 3-4. Transformer construction

Chapter 4
Software Design

4.1 Overview

This section describes the design of the software blocks for the SMPS. As mentioned earlier there are two MCU controllers which control all tasks like the interleaved PFC control, resonant converter control, buck converter control, current reference calculation, fan control, various type of communications, and others. The software described in the following sections is divided into two main parts—primary and secondary software.

4.2 Primary side software design

The primary side core is the MC56F8013 digital signal controller (DSC). This low-cost DSC has many peripherals and features suitable for implementation of full digital power supplies. The main task for the primary controller is to control the interleaved boost converter. Minor tasks are the fan speed control, heat-sink temperature measurement, overall temperature control, and serial communication with the secondary side.

The software is written in C language using Metrowerks CodeWarrior software. Some time-critical algorithms are written in the assembler. The program consists of initialization process followed by never-ending background loop and two periodic and one event driven interrupt service routine (ISR).

The software state diagram can be seen in Figure 4-1. After the reset, the application state machine executes the DSC peripherals and application initialization (AppInit state). After the whole application is initialized, the application state machines continues into AppVinchecking state. This state detects input voltage level. If the input voltage is within the allowed limits then the application continues into the AppStart state. Otherwise goes into AppError state. In AppStart state, the required D.C. link voltage value is ramped up until it reaches the required value. After the output voltage reaches nominal value, the application enters the AppRun state. In case of any error condition the application state machine enters AppError state.

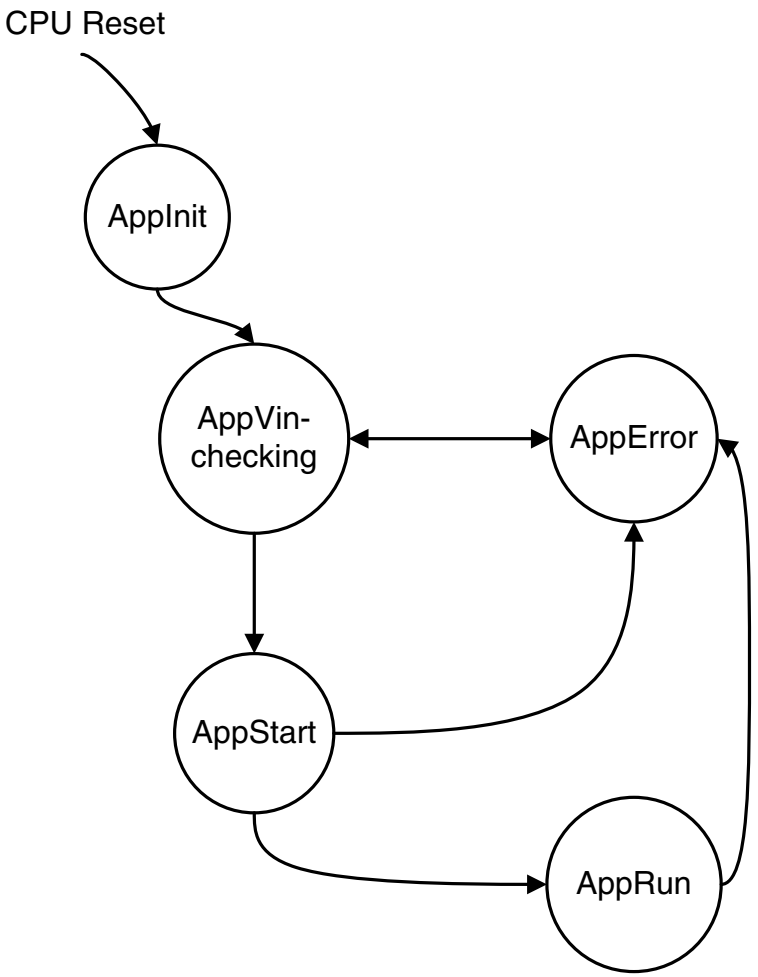

Figure 4-1. Primary software state diagram

The faster of the periodic ISRs (QT3Isr) is executed every 10 us with highest execution priority. This is a time critical routine and therefore the routine is written in the assembler to minimize the total execution time. Most of the time this ISR is consumed by the current PI controller execution and the current reference calculation. The software flow of this ISR can be seen in Figure 4-2. Execution of the interrupt relates to PWM switching frequency, that means that the current controller is executed every PWM period. The QT3Isr is executed every rising edge of the PWM sync signal. This ensures that the ADC conversion is performed in the middle of the PWM period. All quantities are measured at the same time, but read on different places in interrupts QT3Isr and QT0Isr. In this ISR input current and input voltage are read.

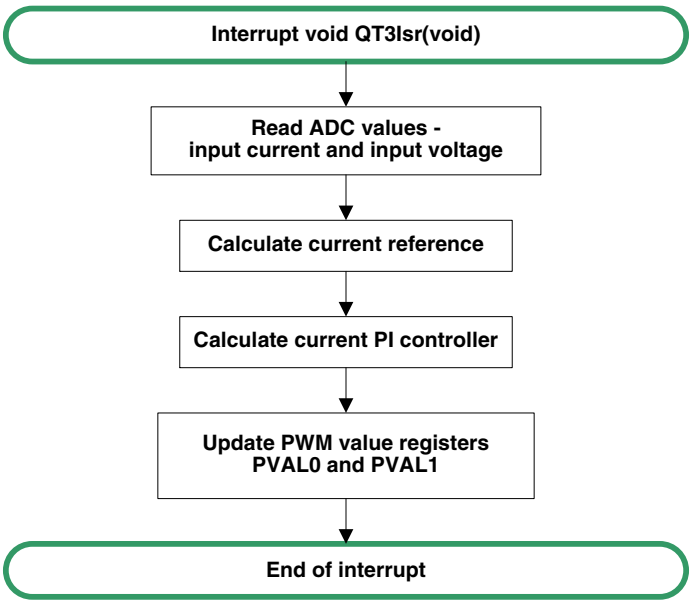

Figure 4-2. QT3 Isr

The slower ISR called QT0Isr is executed every 500 us. This ISR services other tasks. Structure of this ISR is shown in Figure 4-3. This routine executes DC bus voltage PI controller, filtering of input voltage, SCI communication with secondary stage, temperature measurement and fan control.

The serial communication includes ON/OFF state, fault state, and other status informations in direction from primary to secondary. In opposite way it includes board temperature on the secondary side, fault state on secondary side, and other status information. The fan speed is regulated by means of the averaged value from temperatures on heat-sink on the primary side and board temperature on the secondary side, located near the buck converter. Finally, limits of input and output voltage are checked and the watchdog is fed as runaway code protection.

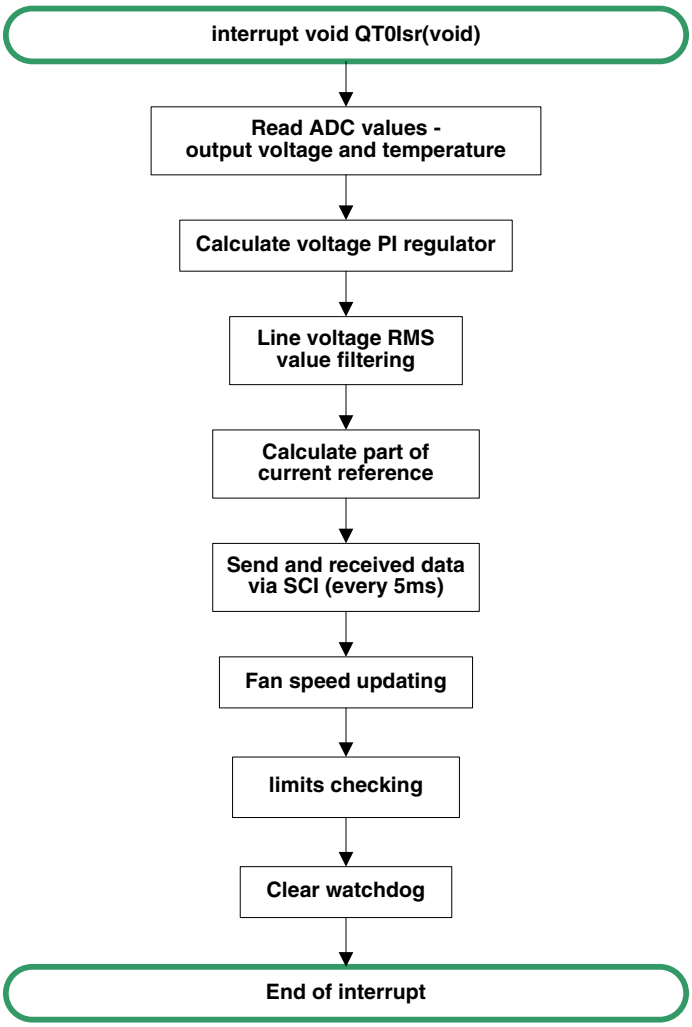

Figure 4-3. QT0Isr

The last one, even driven, ISR in this application is faultISR. It is executed when current overcomes the over-current value which is set by the resistor divider R24 and R28. Immediately after the interrupt is launched, the PWMs are disabled and the application jumps into the AppError state.

Execution time of both interrupt routines were measured. Times were captured using oscilloscope in Figure 4-4 and values were put into Table 4-1.

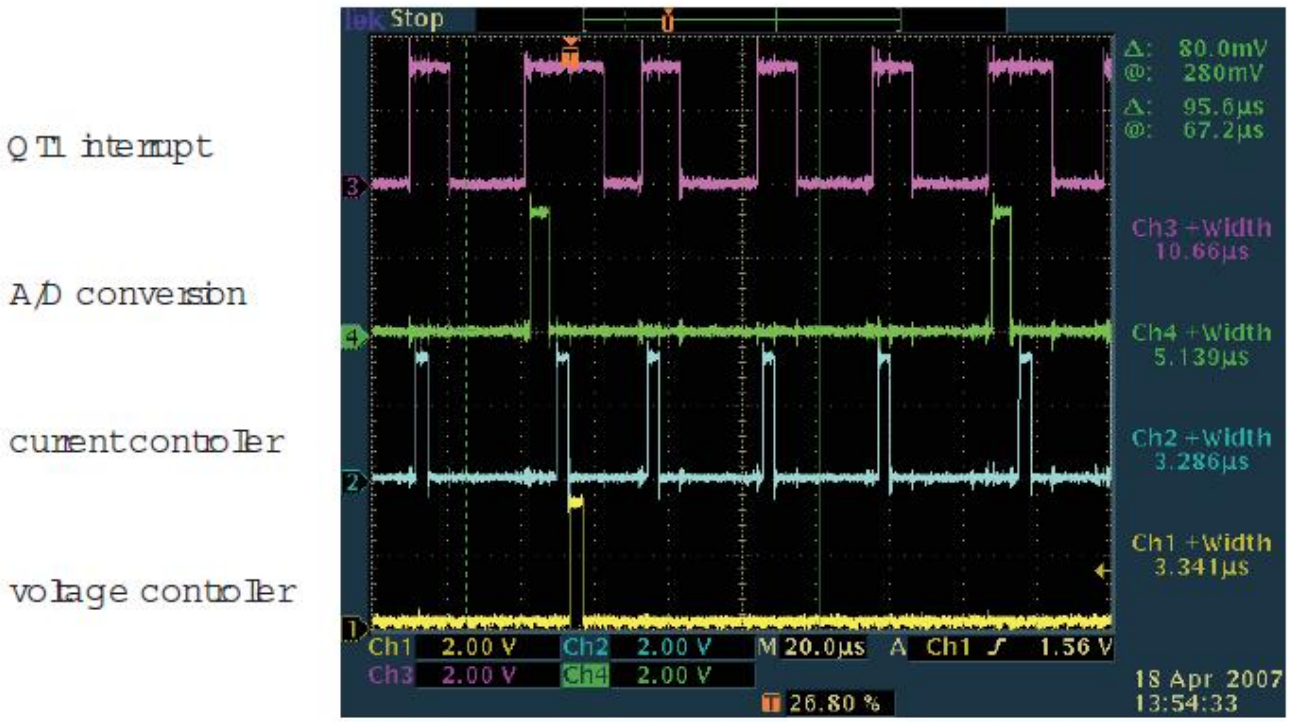

Figure 4-4. CPU Load

Table 4-1. Execution time of interrupt service routines

Name	Execution period	Minimum execution time	Maximum execution time
QT3Isr	10 µs	3 µs	6 µs
QT0Isr	500 µs	12 µs	25 µs

4.3 Secondary side software design

The secondary side of the LLC resonant converter is controlled by the digital signal controller MC56F8247/57. The DSC ensures operation of the LLC resonant converter, operation of synchronous buck converter, communication with primary side, and communication with the PC and the PCB temperature measurement. This chapter describes configuration of the MC56F8247 peripherals and software structure.

4.3.1 MC56F8247/57 Use of Peripherals

4.3.1.1 ADC converter

The ADC module consists of two independent A/D converters. The A/D converters are set to run independently. The ADC B converts the LLC resonant converter output voltage (ANB0) and output current (ANB1). The ADC A converts synchronous buck converter output voltage (ANA0) and output current (ANA1). The ADC B is synchronized with eFlexPWM sub-module 0 via Trigger4 and ADC A is synchronized with eFlexPWM sub-module 2 via Trigger4. The Trigger signals connection between eFlexPWM and ADC is provided by a cross bar switch module.

4.3.1.2 Quad timer module A channel 0

The quad timer A channel 0 is configured to generate a periodical interrupt every 1 ms.

4.3.1.3 Pulse width modulator eFlexPWM sub-module 0

The eFlexPWM sub-module 0 generates two complementary signals for a half bridge of the LLC resonant converter. The PWM outputs have variable frequency with the duty cycle set to 50 %. Comparator VAL4 is used to generate trigger signal for ADC B. There is also fault signal Fault 0, which disables PWM outputs of eFlexPWM sub-module 0 and 1. The fault signal is routed from the high speed comparator HSCMP B.

4.3.1.4 Pulse width modulator eFlexPWM sub-module 1

The eFlexPWM sub-module 1 generates two complementary signals for the synchronous rectifier of the LLC resonant converter. The PWM outputs have the variable frequency with the duty cycle set to 50 %. During operation below resonant frequency the MOSFET transistors have to be switched off earlier as the secondary current falls to zero. This means the falling edge comes earlier in comparison with primary PWM signals. Therefore the sub-module 1 is set to independent mode. The complementary signals include dead time and are generated by SW. The sub-module 1 is synchronized with sub-module 0 to run on the same frequency. There is also fault signal Fault 0, which disables PWM outputs of eFlexPWM sub-module 0 and 1. The fault signal is routed from the high speed comparator HSCMP B.

4.3.1.5 Pulse width modulator eFlexPWM sub-module 2

The eFlexPWM sub-module 2 generates two complementary signals for the synchronous buck converter. The PWM outputs have fixed switching frequency 234 kHz with duty cycle control. Comparator VAL4 is used to generate the trigger signal for ADC A. There is also fault signal Fault 1, which disables PWM outputs of the eFlexPWM sub-module 0, 1, and 2. The fault signal is routed from the high speed comparator HSCMP A.

4.3.1.6 High speed comparator HSCMP A and voltage reference VREF A

The build-in high speed comparator A is used to detect over current condition of synchronous buck converter. The one of the comparator's inputs is shared with ANA1 so the measured current can be concurrently monitored for fault condition. The fault threshold can be set by VREF A.

4.3.1.7 High sspeed comparator HSCMP B and voltage reference VREF B

The build-in high speed comparator A is used to detect over current condition of the LLC resonant converter. The one of the comparator's inputs is shared with ANB1 so the measured current can be concurrently monitored for fault condition. The fault threshold can be set by VREF B.

4.3.1.8 Serial communication interface SCI 0

The serial communication interface SCI 0 is used for communication with the primary side.

4.3.1.9 Serial communication interface SCI 1

The serial communication interface SCI 1 is used for communication with the PC. There is also a SCI -> USB converter on the board, and communication with PC finally goes via USB interface.

4.3.1.10 I2C interface IIC 0

The I2C interface is used for communication with the temperature sensor placed on the PCB close to synchronous MOSFET switches.

4.3.1.11 GPIO pins

There are two GPIO outputs used to drive the status LEDs. The green LED is connected to GPIO F5 and the red LED is connected to GPIO F4. Other GPIO pins used by peripherals are set to the peripheral mode.

4.3.2 Software description

The secondary side software consists of three periodical interrupts and a background loop. Two periodic interrupts IsrAdcBComplete() and IsrBuckReload() are driven by the ADC converter. The third one (isrQTA0Compare()) is called every 1 ms by the compare event from Quad Timer QTA channel 0. The background loop executes the application state machine, communication with the primary side via SCI interface, and communication with the temperature sensor via I2C interface. The background loop also handles FreeMASTER communication.

4.3.2.1 IsrAdcBComplete() routine

The IsrAdcBComplete() routine is called at the end of the conversion of ADC B. This ADC converts output voltage and current of LLC resonant converter. This routine is configured as a fast interrupt with the highest priority. The ADC conversion is started at the middle of the first half period so the execution period of this routine is equal to switching frequency of the LLC resonant converter. The interrupt routine stores ADC converter results into the corresponding variables. The whole routine written is assembler.

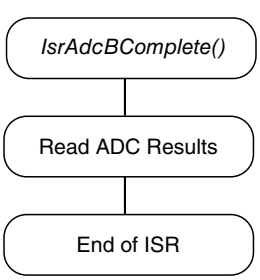

Figure 4-5. IsrAdcBComplete routine

4.3.2.2 IsrBuckReload() Routine

The IsrBuckReload() routine is called at the beginning of every third PWM period of the synchronous buck converter (every 12.8 us). The routine starts with the voltage control loop calculation for the LLC resonant converter. The output of the PI controller corresponds to the required switching frequency. This required frequency is recalculated into the PWM period. The PWM compare registers of sub-modules 0 and 1 are updated with new values. After the LLC resonant converter loop calculation the results of ADC A are ready and can be stored into the corresponding variables. Then, the routine continues to calculate a synchronous buck conversion control loop. The output of the PI controller corresponds to the duty cycle of the PWM output. Thus the PWM compare registers of sub-modules 2 are updated by new values. At the end of the IsrBuckReload() routine there is software over voltage detection. If the output of the LLC resonant converter exceeds the allowed limit, the PWM outputs are disabled.

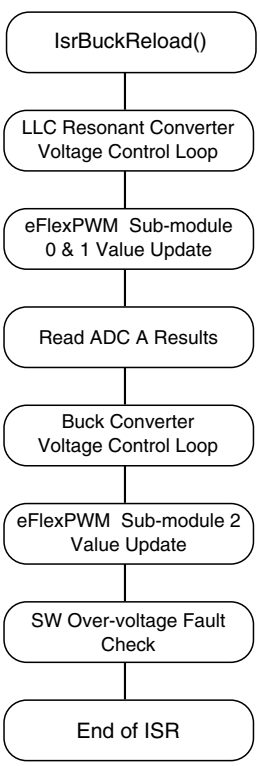

Figure 4-6. IsrBuckReload Routine

4.3.2.3 IsrQTA0Compare() Routine

The isrQTA0Compare() routine is executed every 1 ms and manages the software timer used for power on of the power supply. This interrupt has the lowest (0) interrupt priority.

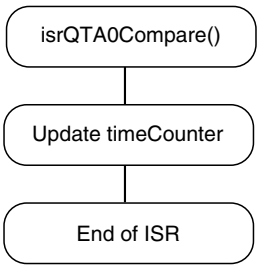

Figure 4-7. IsrQTA0Compare Routine

4.3.2.4 Background loop

The software in the background loop runs in a never ending loop. It includes the application state machine, communication with primary side and PC (FreeMASTER), and communication with temperature sensor.

4.3.2.5 Application state machine

After reset the DSC configures all peripherals and enters a never ending loop including an application state machine. The application state machine goes through the AppInit state (this state is empty) into a Stop state. In the Stop state the application state machine regularly checks the primary side communication. After the command “Primary side OK” is received the application state machine continues into the AppStartLLC state. In this state the LLC resonant converter starts to run with maximal switching frequency and minimal duty cycle. The duty cycle is increased following the ramp until a certain output voltage level is reached. After the certain output voltage level is reached or the duty cycle equals 50% the LLC resonant converter switches into variable frequency mode and the voltage control loop closes.

If there is no fault condition during start up of the LLC resonant converter the application state machine continues into AppStartBuck state. In this state the synchronous buck converter outputs are enabled includes a voltage control loop. After both converters are running the application state machine continues into AppRun state. In AppRun state the application state machine checks fault events from both the primary and secondary side. If a fault condition is detected on the secondary side the application state machine enters AppError state. If the fault condition is received from the primary side the application state machine enters AppStop state. The AppRun and AppError states are indicated on the front panel by red and green LED diodes.

If the application state machine enters AppError state, it stays in a never ending loop and outputs of both converters are disabled. To restart the power supply it has to be switched off and after the DC bus capacitor is fully discharged it can be switched on again.

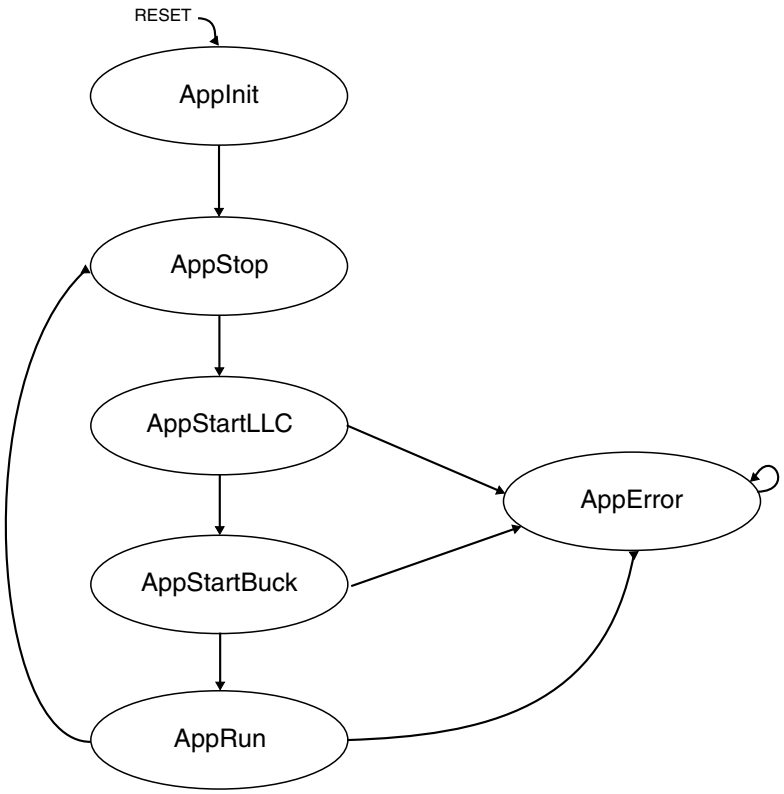

Figure 4-8. Application state machine

Appendix A
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1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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