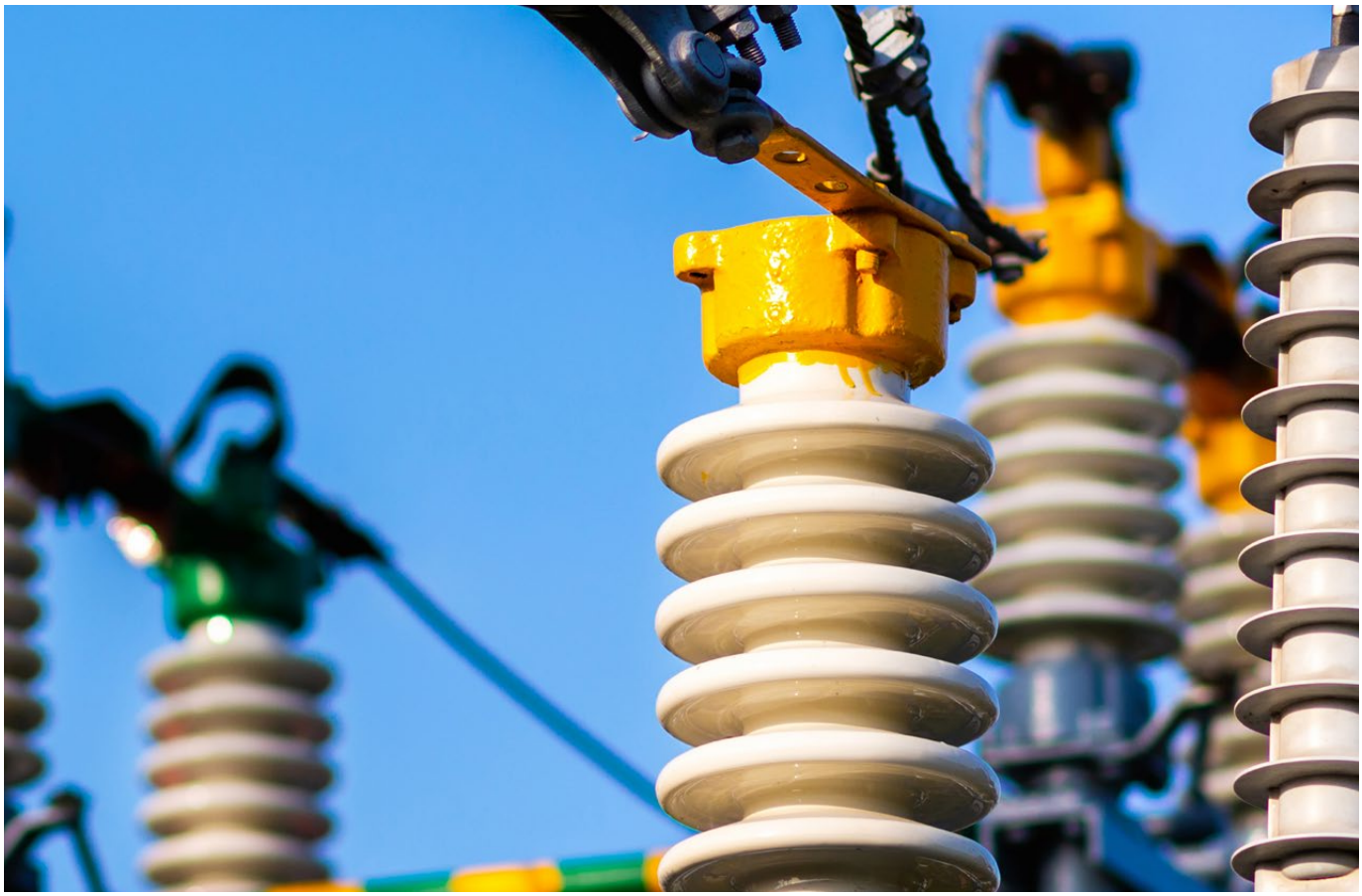
Selector Guide

Voltage translation

How to manage mixed voltage designs with NXP level translators



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Why voltage translation matters

In recent years, voltage translation has become an important part of electronic design, especially in portable applications. That's because the latest data and application processors for mobile applications are typically produced in advanced, low-power CMOS process technologies that use a supply voltage of 1.2 V or lower. But the peripherals they connect to, including memories, image sensors, relays and RF transceivers, are more likely to use older, lower-cost process technologies that operate at higher levels, at or above 3 V or 5 V. Voltage level translators **(Figure 1)** enable these different devices to work together, without producing damaging current flow or signal loss, so the system operates more efficiently and saves power.

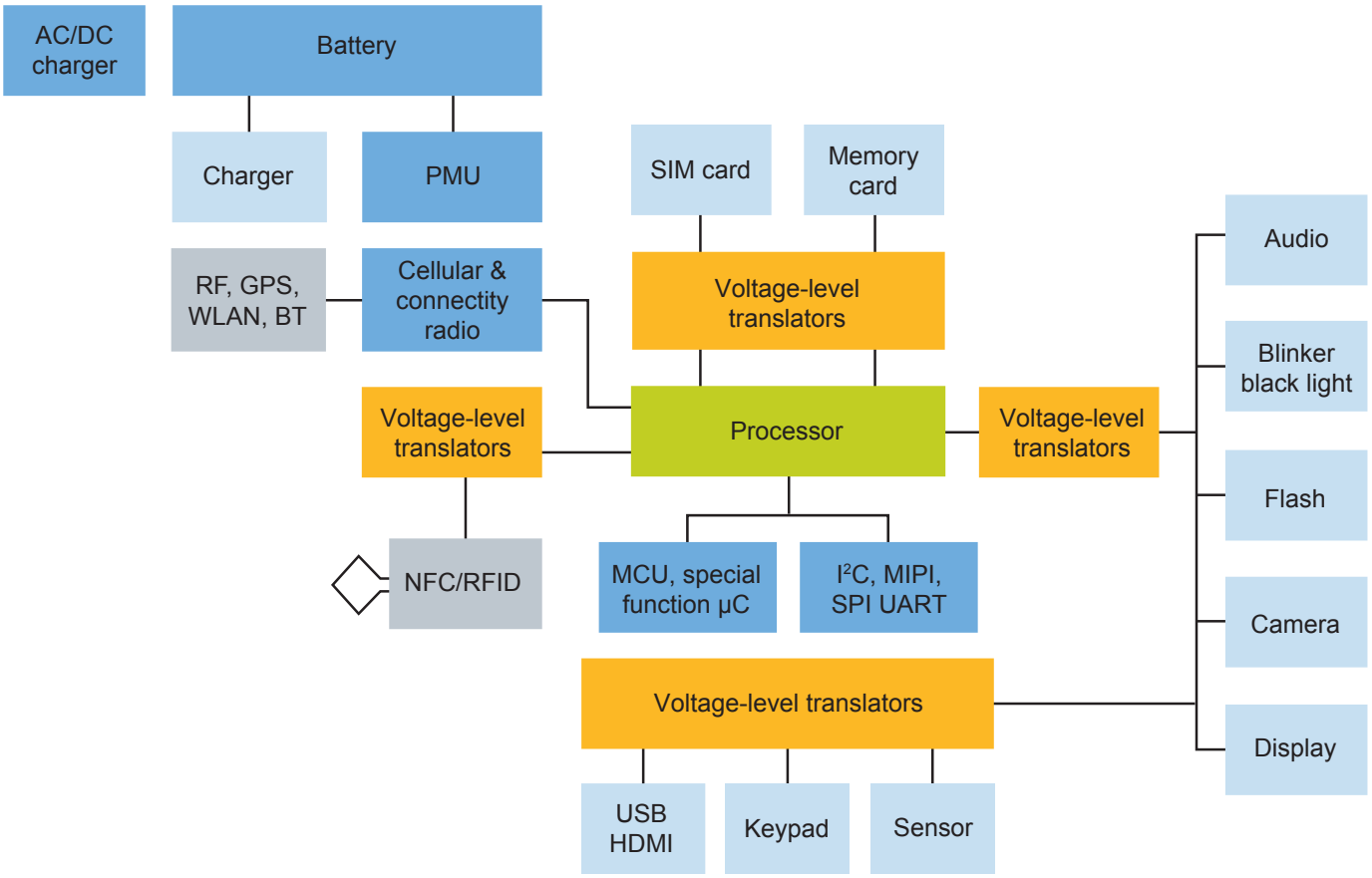


Figure 1: Typical portable application with voltage-level translators

A Quick Overview

In most mixed-voltage designs, the output voltage level of a driver device needs to be shifted up or down so that the receiver device can interpret it correctly, or vice versa **(Figure 2)**.

There are often variations in the logic switching input (VIH and VIL) and the output levels (VOH and VOL) for commonly used logic devices in the range of 3 V and 5 V **(Figure 3)**.

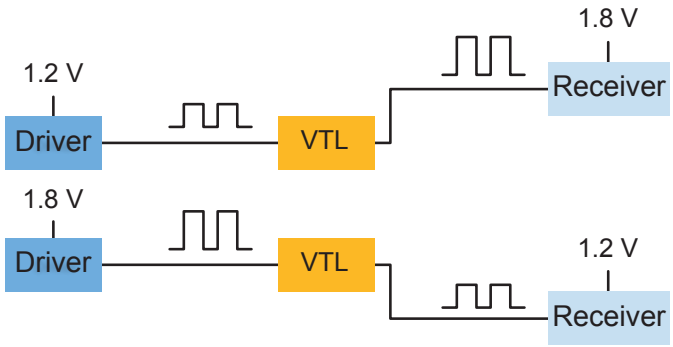


Figure 2: Shifting the output voltage level up or down

When the driver VOH is less than the receiver VIH, and/or the driver VOL is greater than the receiver VIL, system behavior becomes unpredictable **(Figure 4)**.

Configuring the system to translate voltages from high to low or from low to high, according to the recommended guidelines for the input and output voltage levels of each component, makes the system more predictable, improves overall performance and saves energy.

Bidirectional and unidirectional devices

Devices that translate voltages from low to high levels or from high to low levels also transfer data. The data transfer can work in two directions (bidirectional) or in one direction (unidirectional). **Figure 5** shows a typical application that uses the P3A1604, a bidirectional logic level translator, to translate between the processor, which uses 1.2 V signals and the memory subsystem, which uses 1.8 V signals.

Another feature, called auto direction sensing, has no DIR pin. This feature eliminates the need for a separate direction control pin since the direction of the data flow can change automatically. Auto direction sensing helps reduce the number of control pins required in the system for data flow. For example with I²C-Bus, where there is an acknowledgement every 8 bits.

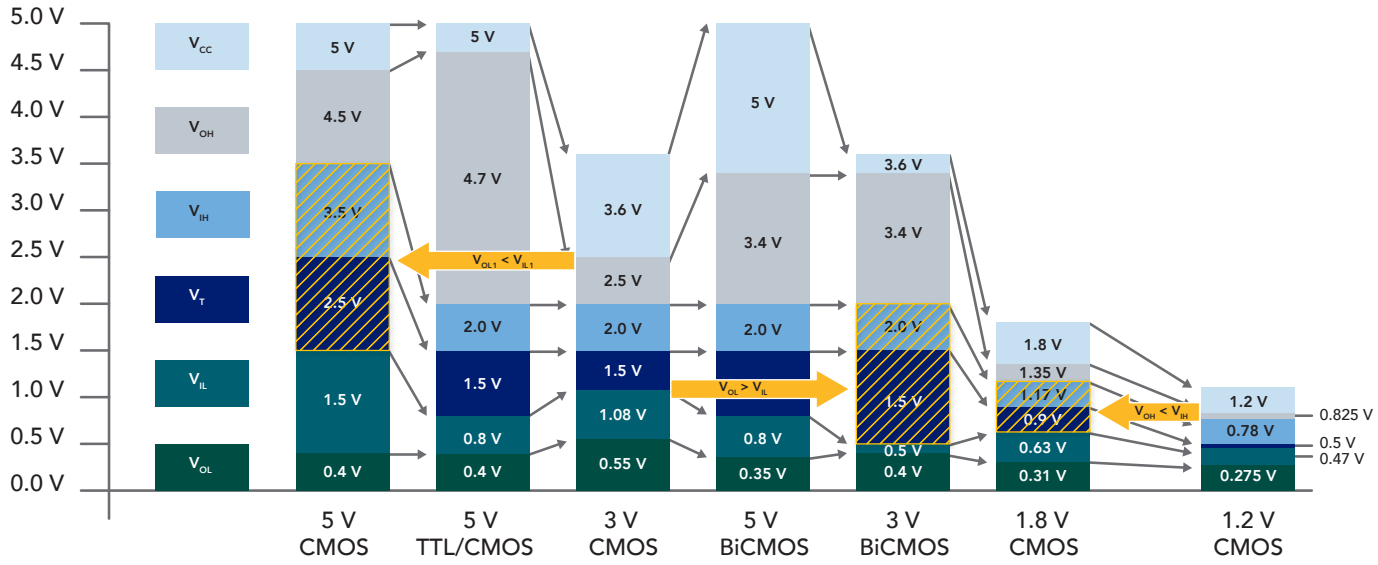


Figure 3: Incompatible voltages can cause unpredictable system behavior

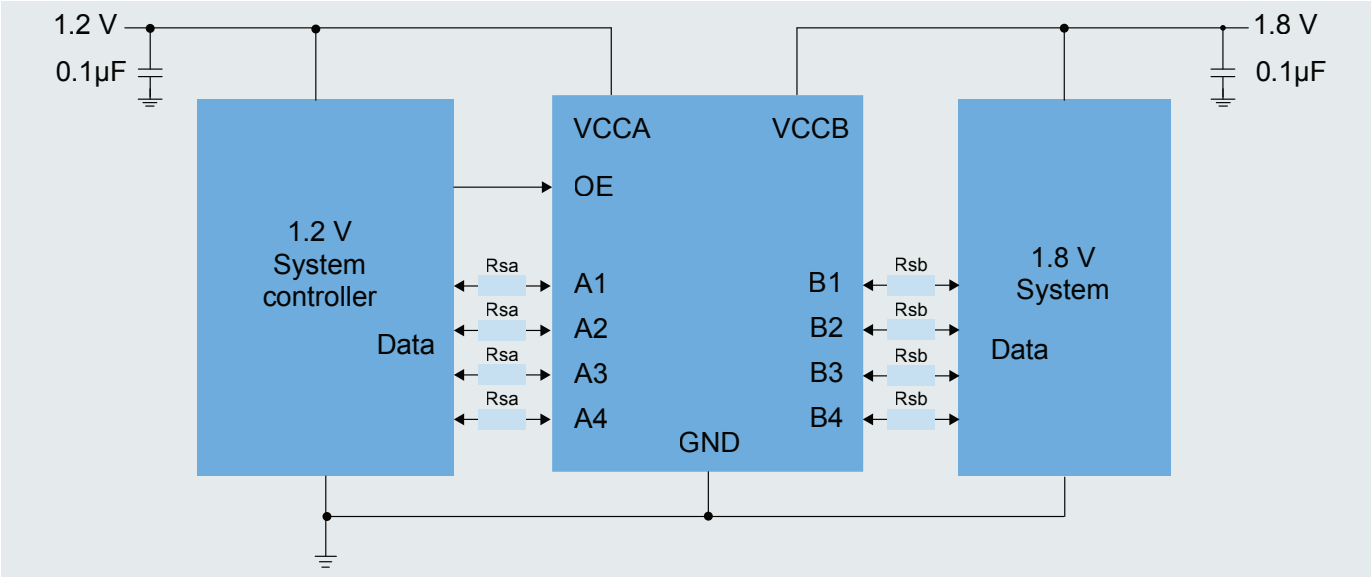


Figure 4: Typical application use case example

Find the right Translator for your design

NXP offers level translators for specific protocols and translators that work in general-purpose applications. This guide can help you find the right one for your design.

Type	NXP Families	Description
Bidirectional with auto direction sensing	P3A, NTS, NTB, NVT200x, PCA	The P3A, NTS and NTB translators integrate one-shot edge accelerators. The P3A, NTS families have integrated pull-ups, and support I3C, I^2C, SMBus, SPI, or UART interfaces. The NTB family supports buffered outputs and can be used for SPI or other push-pull interfaces.
Application specific	NVT level shifters for SIM and SD cards	The NVT SIM and SD card level shifters convert the data, RSTn and CLKn signals between a SIM card and a host microcontroller. Some NVT level shifters contain an LDO that can deliver two different voltages, from a typical mobile phone battery voltage.
Bidirectional with direction pin	GTL	This device has a direction pin that sets the direction of the data flow. GTL level translators are specially designed to support GTL logic. They convert GTL levels to LVTTL levels.

Table 1: NXP Level Translators

Bidirectional level translators with auto direction sensing

These types of translators are dual-supply and use Output Enable (OE) pins to tri-state the output. They automatically sense the direction of the data flow. This eliminates the need for an external direction pin and the associated control logic. Auto-direction sensing makes these devices especially suited for applications where the microcontroller doesn't have enough GPIOs to change the direction of the data flow, since the translators can be added to the design without external GPIO extenders or multiplexers on the PCB.

2.1 Bidirectional open-drain and push-pull VLT with one-shot

P3A level shifters

P3A level shifters **(Figure 5)** are ideal for traditional I²C-bus and SMBus applications, as well as for 12.5 MHz I3C-bus applications and higher speed SPI applications.

The architecture uses edge-rate accelerator circuitry for both the high-to-low and low-to-high, N-channel pass gate transistor and a pull-up resistor (to provide DC-bias and drive capabilities) to meet these requirements. The design is directionless and does not need a direction control signal. The implementation supports both low speed open-drain operation as well as high speed push-pull operation.

The N-channel pass device T5 will be on only during the low input cycle and will be off during the high input cycle.

When transmitting data from A-ports, during a rising edge and A port voltage = VIH, both PMOS transistor T1 and T2 are turned on by OS1 (one-shot) and OS2 (one-shot) for a short duration respectively to reduce the low to high transition time. The T1 duration is around 10 ns. The T2 duration is around 10 ns min to 30 ns maximum, which depends on the CLB (load capacitance on the B side). Similarly, during a falling edge, when transmitting data from A to B and voltage = VIL, both OS3 and OS4 one-shots turn on the N-channel transistor T3 and T4 for a short duration, which speeds up the high to low transition.

When transmitting data from B-ports, during a rising edge and B port voltage = VIH, both PMOS transistor T1 and T2 are turned on by OS1 (one-shot) and OS2 (one-shot) for a short duration respectively to reduce the low to high transition time. The T2 duration is around 10 ns. The T1 duration is around 10 ns min to 30 ns maximum, which depends on the CLA (load capacitance on the A side). Similarly, during a falling edge, when transmitting data from B to A and voltage = VIL, both OS3 and OS4 one-shots turn on the N-channel transistor T3 and T4 for a short duration, which speeds up the high to low transition.

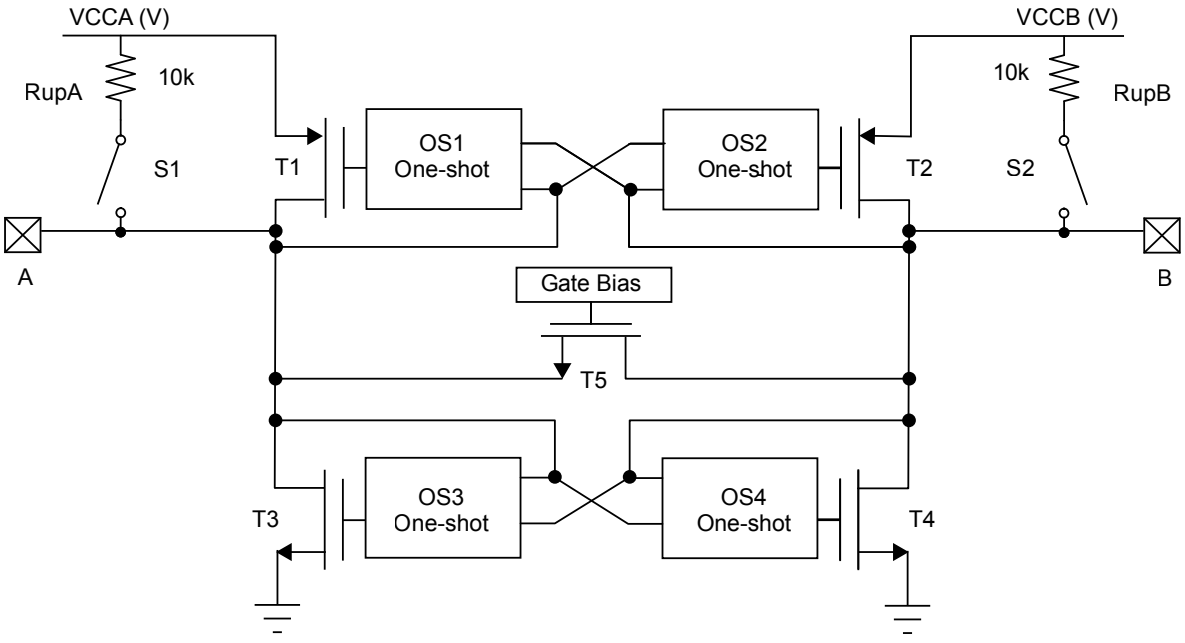


Figure 5: Architecture of P3A1604 bidirectional logic level translator

P3A are very useful in a low consumption environment because of the dynamic pull-up resistors. The internal pull-up resistor RupA and RupB have a typical value of 10 k and are controlled by switches S1 and S2 respectively. Switches S1 and S2 are controlled by their respective input signal and OE.

Pull-up resistors are connected only when the switches are closed. The switches are closed only when the input signal is high and OE enabled.

Pull-up resistors are disconnected when the switches are open. In any one of the conditions that have the switch open, the respective input signal is low or the OE input signal is low.

For push-pull application, the external pull-up resistors are not required since at least one side is driven with a clear high or low state. For open-drain application, at least one external pull-up resistor is required for pulling signal A from a low state to a high state. The external pull-up resistor can be either on A side or B side. The rising time can be estimated with Rup_ext x (CLA + CLB) + one-shot time (~10 ns). Where the Rup_ext is an external pull-up resistor, CLA is the total load capacitance on the A side. CLB is the total load capacitance on the B side.

Input driver requirements

With the P3A family as a switch-type translator, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, high-to-low output transition time (tTHL), and propagation delay (tPHL), are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters that are in the data sheet assume a driver with an output impedance below 50 Ω is used.

Output load considerations

The maximum lumped capacitive load that can be driven depends on the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output will not reach the positive rail within the one-shot pulse duration.

Type number	Description	VCCA (V)	VCCB (V)	Bandwith (MHz)	Number of bits	Tamb (°C)	Package
P3A1604UK	4-bit dual supply bidirectional I3C/ I²C-Bus, SMBus and SPI voltage-level translator	0.72 to 1.98	1.62 to 3.63	20	4	-40 to +125	WLCSP12
P3A9606	2-bit dual supply bidirectional I3C/I²C-Bus and SPI voltage-level translator	0.72 to 1.98	0.72 to 1.98	52	2	-40 to +85	X2SON8

Table 2: NXP P3A level shifters

NTS level shifters

NTS level shifters are switch-type translators suitable for open-drain drivers. They are FET-based devices that use an N-channel pass-gate transistor that ties the two ports together **(Figure 6)**, and do not need an extra input signal to change the direction of data from port A to B or from port B to A.

The combination of an N-channel pass FET, integrated 10 kΩ pull-up resistors, and edge-rate acceleration circuits makes NTS translators ideal for interfacing devices or systems operating at disparate voltage levels, while also allowing for simple interfacing with open-drain drivers, as is required in I^2C and 1-wire interfaces.

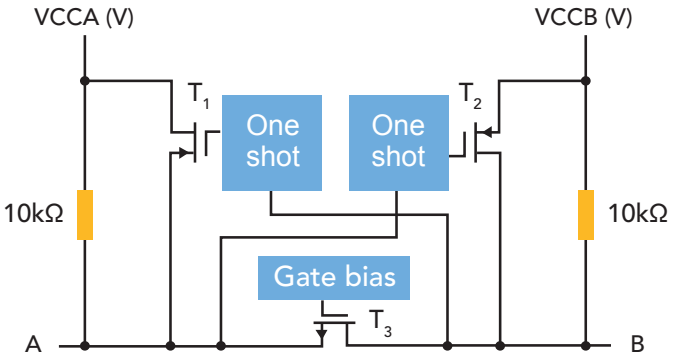


Figure 6: Architecture of single I/O channel in NTS level shifter

The N-channel pass-gate transistor is used to open and close the connection between the A and B ports. When a driver connected to A or B port is low, the opposite port is, in turn, pulled low by the N-channel pass-gate transistor. The gate bias voltage of the pass-gate transistor (T3) is set at approximately one threshold voltage above the VCC level of the low-voltage side.

During a low-to-high transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2), bypassing the 10 kQ pull-up resistors, and increasing current drive capability. The one-shot is activated once the input transition reaches approximately VCCI/2, and is deactivated approximately 50 ns after the output reaches VCCO/2. During the acceleration time, the driver output resistance is between approximately 50 and 70 Q. To avoid signal contention and minimize dynamic ICC, the user should wait for the one-shot circuit to turn off before applying a signal in the opposite direction.

The pass-gate transistor T3 is on when VGS is greater than VT. When one side of T3 is held low by an external driver, with the input to T3 at 0 V, T3 will be on and the output of T3 will be held to nearly 0 V due to the on-state resistance of T3. As the input voltage rises due to a rising edge, the output voltage of T3 tracks the input until the input voltage reaches VGATE minus VT and T3 turns off. After T3 stops conducting, the input and output ports continue to rise to their respective supply voltages due to the internal pull-up resistors. In the second case, both ports start with high levels since the integrated pull-up resistors tie the inputs to the respective supply voltages, VCC(A) and VCC(B). When the input ports are pulled low by external drivers, T3 starts to conduct when VGS is greater than VT and output starts tracking the input. The source current needed for this operation must be provided by the external driver connected to the A or B port.

To achieve faster data rates through the device, NTS translators include rising edge-rate acceleration circuitry to provide stronger AC-drive by bypassing the integrated 10 kΩ pull-up resistors through a low-impedance path during low-to-high signal transitions. A one-shot circuit with associated T1/T2 PMOS transistors is used to increase switching speeds for the rising-edge input signals. When a rising edge is detected by the one-shot circuit, the T1/T2 PMOS transistors turn on momentarily to rapidly drive the port high, effectively lowering the output impedance seen on that port and speeding up the rising-edge inputs.

Input Driver Requirements

Since NTS level shifters are switch-type level shifters, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The maximum data rate high-to-low output transition time (tTHL) and the propagation delay (tPHL) depend on the output impedance and the edge rate of the external driver. The limits provided in the data sheet for these parameters assume use of a driver with output impedance below 50 Ω.

Output load considerations

The maximum lumped capacitive load that can be driven depends on the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output will not reach the positive rail within the one-shot pulse duration. Capacitive loads up to 150 pF can be driven without any issues using NTS level shifters. **Figure 7** shows the yellow input waveform and purple output waveform for an NTS0102 driving a load of 70 pF and 50 Ω. A supply voltage of 1.8 V is used for the VCC(A) rail and a supply voltage of 3.3 V is used for the VCC(B) rail. A 1.8 V input signal with a 50 kHz frequency is used, and output swings up to approximately 3.24 V.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, it's recommended to use short trace lengths and low-capacitance connectors on NTS0102 PCB layouts. To ensure low-impedance termination, and avoid output signal oscillations and one-shot re-triggering, the length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns). The NTS030x devices are designed with longer one shot length with ability to drive larger capacitance loads but at lower maximum frequencies.

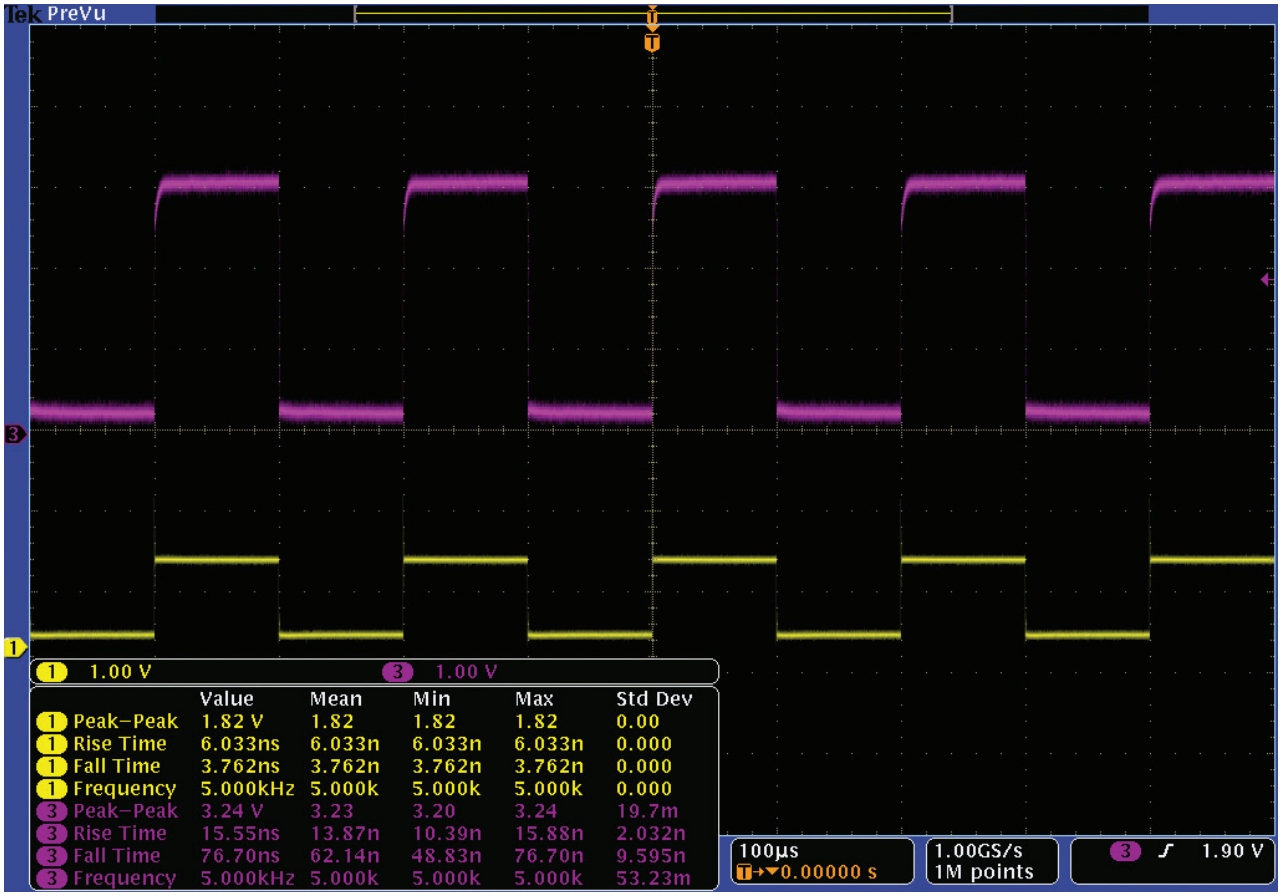


Figure 7: NTS0102 driving a load of 70 pF and 50 Ω

Power-up considerations

During operation, VCC(A) must never be higher than VCC(B). However, during power-up, having VCC(A) greater than VCC(B) does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS devices include circuitry that disables all output ports when either VCC(A) or VCC(B) is switched off.

Enable and disable operation

An OE input is used to disable the device. Setting OE to low causes all I/O to assume the high-impedance off-state. The disable time (tdis with no external load) indicates the delay from when OE goes low and when outputs actually become disabled. The enable time (ten) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken high. To ensure the high-impedance off-state during power-up or power-down, pin OE should be tied to the GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

Pull-up or pull-down resistors on I/O lines

Each A port I/O has an internal 10 kΩ pull-up resistor to VCC(A), and each B port I/O has an internal 10 kΩ pull-up resistor to VCC(B). If a smaller value of pull-up resistor is required, an external resistor must be added parallel to the internal 10 kΩ. This will affect the VOL level. When OE goes low the internal pull-ups of the NTS0102 are disabled.

NTSX level shifters are similar to NTS devices but use a modified architecture that enables use at higher capacitive loads (typically up to 600 pF). **Figure 8** gives the architecture of a single NTSX I/O channel.

There are two N-channel pass-gate transistors that tie the ports together. There is an output edge-rate accelerator that detects and accelerates rising and falling edges on the I/O pins **(Figure 9)**.

During an input transition, a one-shot accelerates the output transition by switching on the PMOS transistors (T1, T3) for a low-to-high transition. Alternatively, the one-shot switches on the NMOS transistors (T2, T4) for a high-to-low transition **(Figure 10)**. Once activated, the one-shot is deactivated after approximately 25 ns. During the acceleration time, the driver output resistance is between approximately 10 and 35 Ω. To avoid signal contention, the application must not exceed the maximum data rate or must wait for the one-shot circuit to turn off before applying a signal in the opposite direction.

NTSX level shifters: Bidirectional level translation with auto-direction sensing, open-drain outputs and dual-edge accelerators

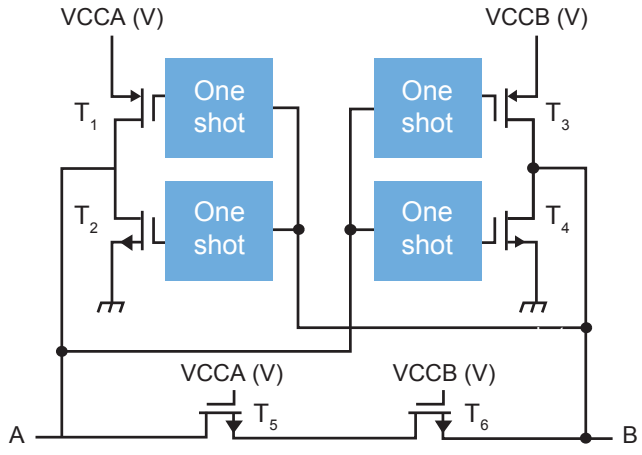


Figure 8: Architecture of NTSX2102 I/O channel

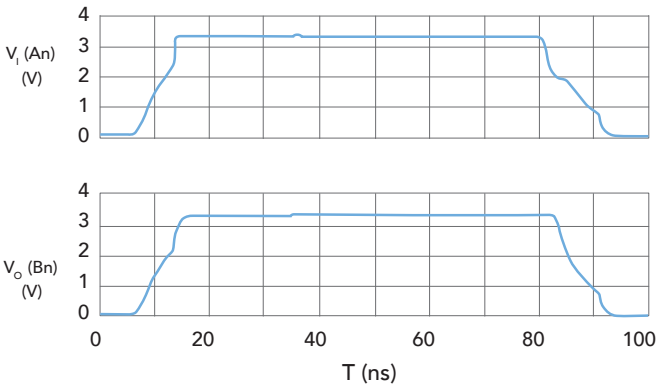


Figure 9: Input and output waveforms showing edge-rate acceleration

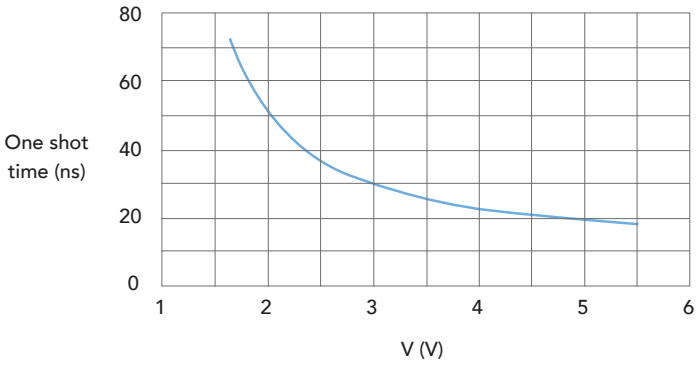


Figure 10: One-shot pulse time versus V_{CCO}

Input driver requirements

Because the NTSX2102 is a switch-type translator, properties of the input driver directly affect the output signal. The external open-drain driver applied to an I/O determines the static current sinking capability of the system. The maximum data rate, output transition times (tTHL, tTLH), and propagation delays (tPHL, tPLH) depend on the output impedance and the edge-rate of the external driver.

Output load considerations

The maximum lumped capacitive load that can be driven depends on the one-shot pulse duration and has been tuned to 600 pF. In cases with higher capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. To avoid excessive capacitive loading and ensure correct triggering of the one-shot, use short trace lengths and low-capacitance connectors on the NTSX2102 PCB layouts. The length of the PCB trace should be such that the roundtrip delay of any reflection is within the one-shot pulse duration. Such a length ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

Output enable (OE)

An OE input is used to disable the device. Setting OE to low causes all I/Os to assume the high-impedance off-state. One of the advantages of NTSX translators is that either VCC(A) or VCC(B) can be powered up first. Defining the OE pin reduces dissipation during power-up. The OE pin can be connected via a pull-down resistor to GND or, if the application allows, hardwired to VCC(A). If the OE pin is hardwired to VCC(A), either supply can be powered up or down first. If a pull-down is used, the following sequences are recommended.

For power-up

- Apply power to either supply pin
- Apply power to the other supply pin
- Enable the device by driving OE high

For power-down

- Disable the device by driving OE low
- Remove power from either supply pin
- Remove power from the other supply pin

Type number	Description	VCCA (V)	VCCB (V)	Output drive (mA)	tPD Capability (ns)	Number of bits	Tamb (°C)	Package
NTS0102	2-bit dual-supply level translator with auto-direction sensing (3-state)	1.65 to 3.6	2.3 to 5.5	-0.02	4.5	2	-40 to +125	TSSOP8, XSON8, HXSON8, X2SON8
NTS0104	4-bit dual-supply level translator with auto-direction sensing (3-state)	1.65 to 3.6	2.3 to 5.5	-0.02	4.5	4	-40 to +125	DHVQFN14, XQFN12, TSSOP14, WLCSP
NTSX2102	2-bit dual-supply level translator with auto-direction sensing (3-state)	1.65 to 3.6	2.3 to 5.5	6	2	2	-40 to +125	XSON8, XQFN8, X2SON8
NTS0302	2-bit dual-supply level translator with auto-direction sensing (3-state)	0.95 to 3.6	1.65 to 5.5	X	X	2	-40 to +125	X2SON8
NTS0304E	4-bit dual-supply level translator with auto-direction sensing (3-state)	0.95 to 3.6	1.65 to 5.5	X	X	2	-40 to +125	TSSOP14, WLCSP12
NTS0308E	8-bit dual-supply level translator with auto-direction sensing (3-state)	0.95 to 3.6	1.65 to 5.5	X	X	2	-40 to +125	TSSOP20

Table 2: Select NTS and NTSX level shifters for bidirectional translation

2.2 Bidirectional push-pull buffer VLT with one-shot

NTB level shifters

NTB level shifters **(Figure 14)** are ideal for use as push-pull or CMOS-type drivers that drive long-trace, capacitive or high-impedance loads in applications that use SPI, Secure Digital or UART interfaces.

Figure 11 shows the architecture of one I/O channel of an NTB level translator. The translator incorporates a weak buffer with one-shot circuitry to improve switching speeds for rising and falling edges. When the A port is connected to a system driver and driven high, the weak 4 kΩ buffer drives the B port high in conjunction with the upper one shot, which becomes active when it senses a rising edge. The B port is driven high by both the buffer and the T1 PMOS, which lowers the output impedance seen on the B port while the one-shot circuit is active. On the falling edge, the lower one-shot is triggered and the buffer, along with the T2 NMOS, lowers the output impedance seen on the B port while the one-shot circuit is operating and the output is driven low.

Figure 12 shows the active circuitry in the NTB I/O channel during translations from low to high and high to low. The weak buffer is shown in orange and the active one-shot circuit is in green. **Figure 13** shows the input and output waveforms with edge acceleration.

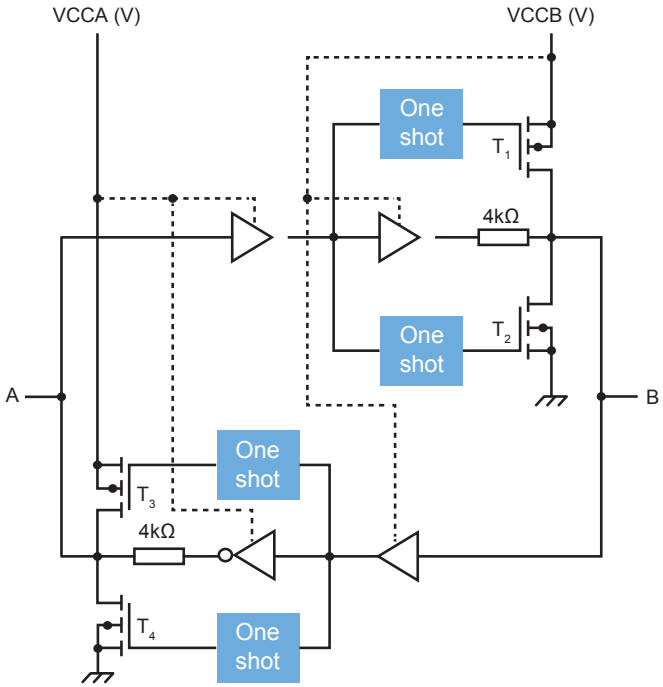


Figure 11: Architecture of single NTB I/O cell

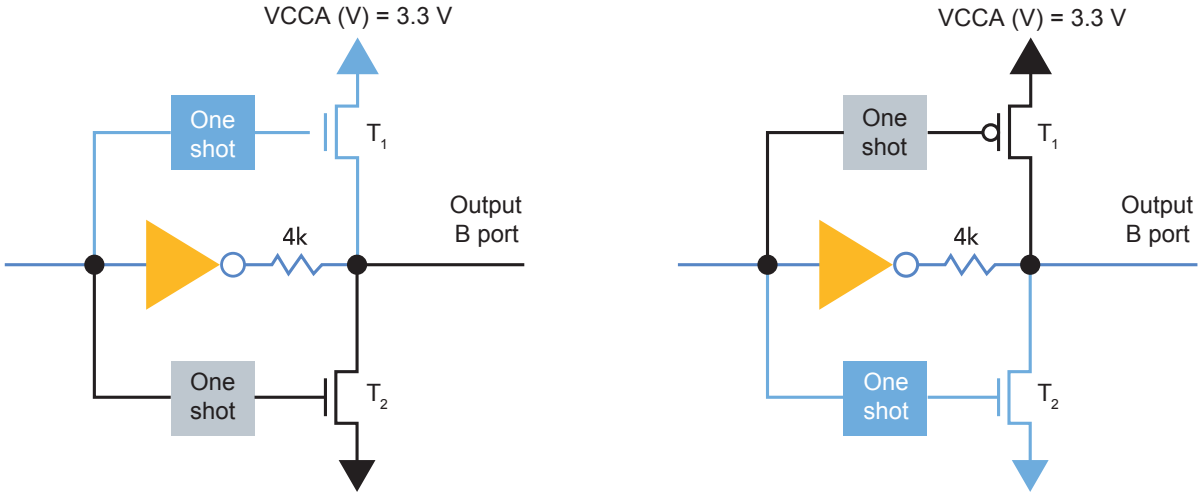


Figure 12: Active one-shot and weak buffer structures in NTB I/O channel

The one-shot circuits in NTB devices reduce the output impedance during low-to-high and high-to-low transitions so that the propagation delays can be minimized with faster edges. Once the transition is complete, the one-shot circuit times out. Port B is held high or low by the weak buffer and the integrated 4 kΩ resistor at the buffer output. NTB is a weak buffered device since the buffer is strong enough to hold the output port high or low in static state but is weak enough to be overridden by an external driver when the direction is changed.

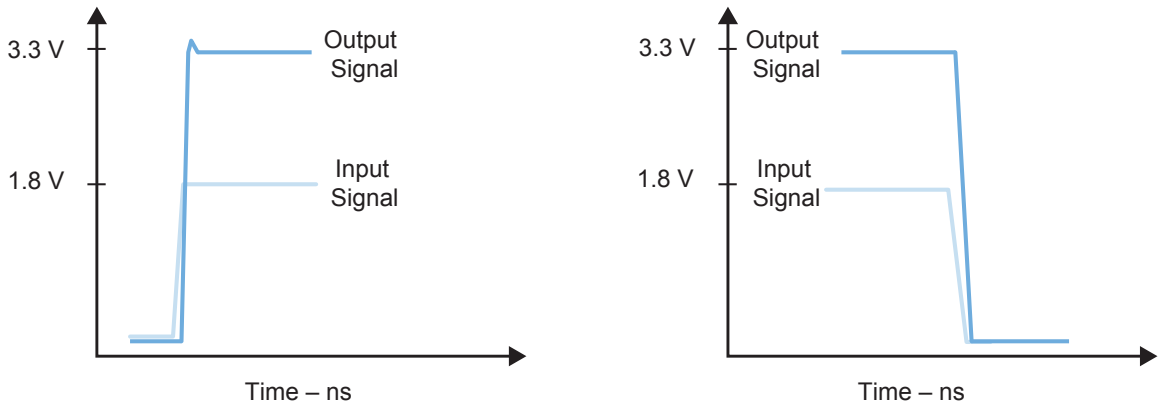


Figure 13: Input and output waveforms with edge acceleration

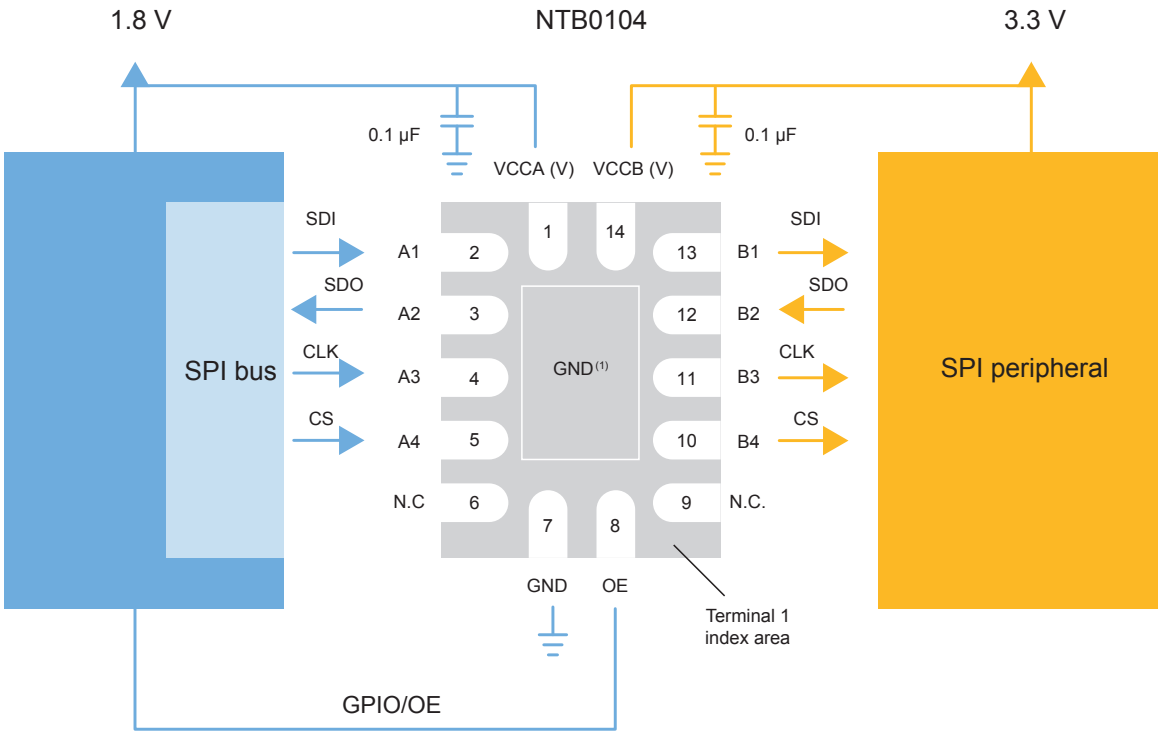
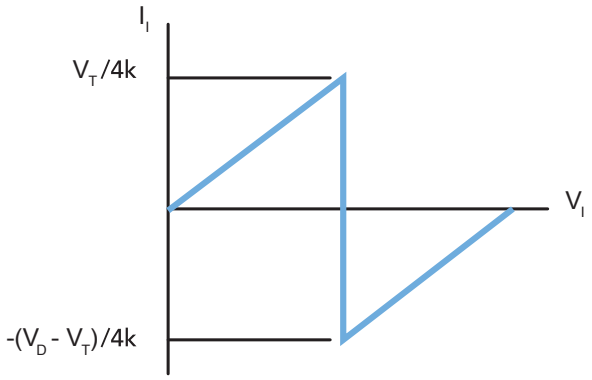


Figure 14: Four-channel NTB0104 used in SPI level-shifting application

Input driver requirements

The input driver should have at least ±2 mA drive current capability to drive the I/O of NTB devices. Input current versus input voltage for NTB devices is shown in **Figure 15**.



VT: Supply voltage of the external driver
VD: Input threshold voltage of the NTBo1o4 (typically V_{cci})

Figure 15: Typical input current versus input voltage (NTB)

Since NTB buffers are designed for driving high-impedance loads, it is important to carefully select the external pull-up or pull-down resistors if they are used in the application. For any external pull-up or pull-down resistor used with the NTB resistor, a resistor divider network is formed with a 4 kΩ buffer. The value of the external resistor should be large enough (typically greater than 50 kΩ) so that there is little change on VOH or VOL levels.

For example, the value of VOL can be determined from the following equation, when a 50 kΩ external pull-up is used:

$VOL=4k/50k + 4k \times V_{cco} = 0.075 \times V_{cco}$

During output transitions, the typical output impedance is 70 Ω at VCCO equals 1.2 to 1.8 V, 50 Ω at VCCO equals 1.8 to 3.3 V and 40 Ω at VCCO equals 3.3 to 5.0 V. When the circuits are active, a resulting high AC drive is realized by turning on T1 and the rising edge speeds up. The output port is maintained at a high signal level through this 4 kΩ internal resistor. During low-to-high transitions, one-shot circuits turn on the PMOS transistors T1 for a short time, accelerating the output edges. However, the one-shot circuits are turned off when output voltage reaches approximately 95% of the steady-state value. For high-to-low output transitions, the one-shot turns off when output voltage reaches approximately 5% of the steady-state value.

Output-enable (OE) control

NTB level translators offer a maximum power consumption of 5 µA when OE is high. When the OE is low, the NTB translator buffer will be disabled and the outputs are put into high impedance for increased power savings. The OE pin is referenced to VCC(A) voltage supply and when outputs are disabled, the one-shot and 4 kΩ buffer are also disabled for both the A and B ports. In this state, output leakage IOZ will be less than ±2 µA. If the application does not require output-enable control, the OE pin should be tied to VCC(A) supply and must never be left floating. A floating OE results in excessive quiescent current consumed by the device, which increases the total power consumption. Unwanted output oscillations may also result due to indeterminate logic level at the OE pin.

The outputs of NTB devices are tri-stated in case any of the two power supplies is 0 V. This feature, called VCC isolation, means that if VCC(B) or VCC(A) equals 0 V, the I/O of A and B ports are in high impedance. These devices are fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the output, preventing the presence of damaging backflow current when the device is powered down.

Type number	Description	VCCA (V)	VCCB (V)	Output drive (mA)	tPD Capability (ns)	Number of bits	Tamb (°C)	Package
NTB0101	1-bit dual-supply level translator with auto-direction sensing (3-state)	1.2 to 3.6	1.65 to 5.5	±0.02	3.8	1	-40 to +125	TSSOP6
NTB0102	2-bit dual-supply level translator with auto-direction sensing (3-state)	1.2 to 3.6	1.65 to 5.5	±0.02	3.8	2	-40 to +125	TSSOP8, XSON8
NTB0104	4-bit dual-supply level translator with auto-direction sensing (3-state)	1.2 to 3.6	1.65 to 5.5	±0.02	3.8	4	-40 to +125	DHVQFN14, XQFN12, WLCSP

Table 3: Select NTB Level Shifters for Bidirectional Translation

For the complete portfolio, visit **www.nxp.com/VLT.**

NVT200x Level Shifters

NVT200x level shifters perform bidirectional translation using an array of matching N-channel pass transistors with their gates tied together internally at the enable (EN) pin **(Figure 16)**.

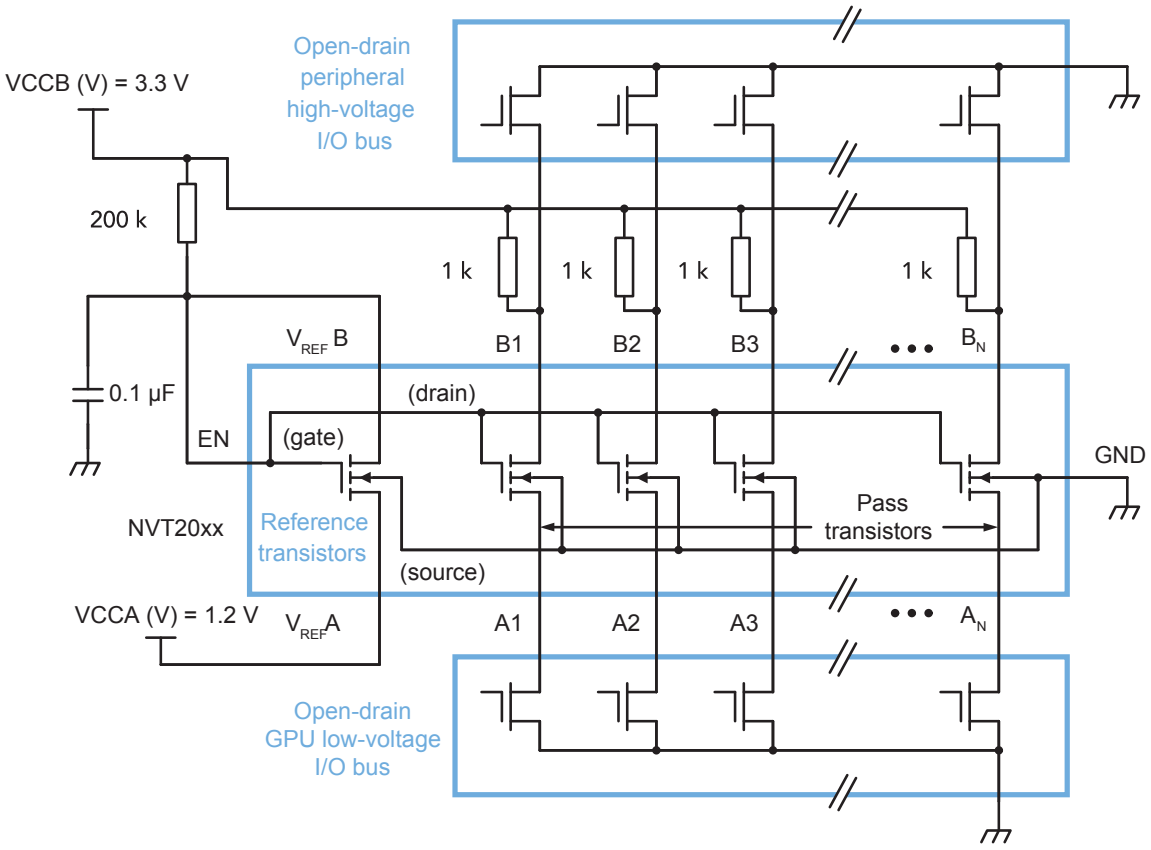


Figure 16: Typical NVT20xx device schematic

Basic operation

One of the Field-Effect Transistors (FETs) is used as a reference transistor, and the remainder as pass transistors. The low side (A1 to An) is the FET source, while the high side (B1 to Bn) is the FET drain. On the low side, the voltage of the reference transistor is the limit for the remaining pass transistors. The gate of the reference transistor should be tied to its drain to ensure that the FETs operate within the saturation region.

The reference transistor and one resistor are used to set VBIAS and the gate voltage (VG) for all the pass transistors. The gate voltage is VCC(A) plus the gate-to-source voltage (VGS). VGS can vary from 0.6 V to 1.0 V. The pass transistors on the low side are limited to VCC(A).

When either an An or Bn port is driven low, the FET is turned on and a low-resistance path exists between the An and Bn port. The low on-state resistance (RON) of the pass transistor allows connections to be made with minimal propagation delay.

When the Bn port is driven or pulled high, the voltage on the An port is limited to VCC(A). When the An port is driven or pulled high, the Bn port is pulled to VCC(B) by the pull-up resistors. VCC(A) is set equal to the I/O voltage level of the CPU. The VCC(B) is set equal to the I/O voltage level of the peripheral device. This enables seamless translation between high and low levels without the need for directional control.

When EN is connected through a 200 kΩ pull-up resistor to a high-voltage VCC(B), and the An and Bn I/O are connected, the translator switch is on, allowing bidirectional data flow between ports. When EN is pulled low, the transistor switch is off and a high-impedance or disconnect state exists between ports. In this way, these translators protect new, lower-voltage devices from the overvoltage and ESD conditions applied by older, high-voltage devices, and make easy work of translating the VIH and VOH switching levels.

Bidirectional level translation with open-drain I/O

For bidirectional level translation, with open-drain the drivers on both sides of the translator either must be open-drain outputs or must be controlled to prevent contention between a high level on an output driver on one side and a low level on the other side.

Using an open-drain device means there have to be pull-up resistors on the B side, and the resistors have to be sized so as not to overload the output drivers.

With the NVT20xx, if VCC(B) minus VCC(A) is greater than 1 V, then pull-up resistors are not required on the A side. If, however, VCC(B) minus VCC(A) is less than 1 V, then pull-up resistors must be used on the A side to bring the An outputs to VCC(A). Note that if pull-up resistors are required on both the A and B sides, then the equivalent pull-up resistor value becomes the parallel combination of the two resistors when the pass transistor is on.

Unidirectional level translation and push-pull I/O

The translators support unidirectional level translation (low to high or high to low) with push-pull or totem-pole I/O, but the I/O must be the only driver on the bus during translation. Using this configuration for bidirectional push-pull control requires a direction control bit to determine which I/O is acting on the bus and prevent bus contention. Details for unidirectional translation are given in application note AN11127.

Type number	Description	VCCA (V)	VCCB (V)	Tamb (°C)	Package
NVT2002	2-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	2	TSSOP8, X2SON8
NVT2008	8-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	8	DHVQFN20, TSSOP20
NVT2010	6-bit dual-supply level translator with auto-direction sensing	1.0 to 3.6	1.0 to 5.5	10	HVQFN24, TSSOP24

Table 4: Select NVT bidirectional translators

Application-specific level translators

This section discusses level translators that make it easier to work with SIM cards and special translators for the I²C-bus

3.1 Translators for use with SIM cards

NVT4555 WLCSP Bidirectional SIM card interface level translator and supply voltage LDO

The NVT4555 interfaces between the host processor of a smartphone or any other equipment with cellular connection and its SIM card **(Figure 17)**. Available in a tiny wafer-level chip scale package (WLCSP), it combines robust performance with the smallest available footprint. The device complies with the SIM power supply, includes EMI and ESD protection, and handles the shutdown sequence specified by the ISO 7816-3 specification.

The internal low-dropout (LDO) regulator supplies power to the SIM card using a high power supply rejection ratio (PSSR) at a very low dropout voltage (VBAT-VSIM). The NVT4555 provides two levels of fixed voltage regulation, at 1.8 V or 2.95 V, selectable using the CTRL pin.

Using the ISO 7816-3 shutdown sequence for the SIM card signals ensures the card is properly disabled — and during hot swap, the shutdown sequence helps avoid data corruption and improper writes.

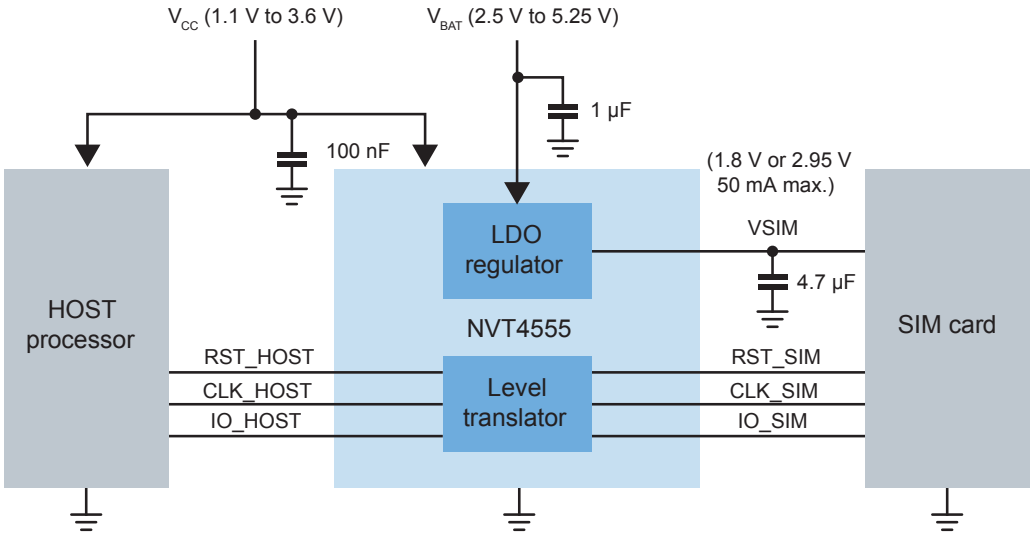


Figure 17: NVT4555 interfacing with a typical SIM card

3.2 Qualcomm Reference Design Uses Level Translators with External LDO

NVT4557 and NVT4558 SIM Card

The reference design integrates the NVT4557HK and NVT4558HK, the 10-pin package SIM-card VLT with EN pin and not the 9-pin WLCSP package NVT4557UK (without EN pin). The EN pin meets the ISO standards related to the start-up / shut-down sequence between the host and SIM card. The final decision between 10-pin and 9-pin depends on the OEMs, trading off shut-down sequence with the smaller package size that has auto shut down based on VCCB supply. The NVT4557HK is optimized for 1.8 V processor interface and the NVT4558 for 1.2 V with 0.65 x VCCA V_{IH} and 0.35 x VCCA V_{IL} HOST interface.

NVT4858 SD card

The reference design uses the 16-pin WLCSP package NVT4858UK because of its smaller size versus the lower price of the NVT4858HK (smaller die in plastic package). The final decision on the type of package will depend on the OEM, trading off board space versus component cost.

Target functions

Secure Digital (SD3.0) and SIM Voltage Level Translation CLASS B, C

End applications

Smartphones, Tablets, Digital Cameras, Wireless Modems

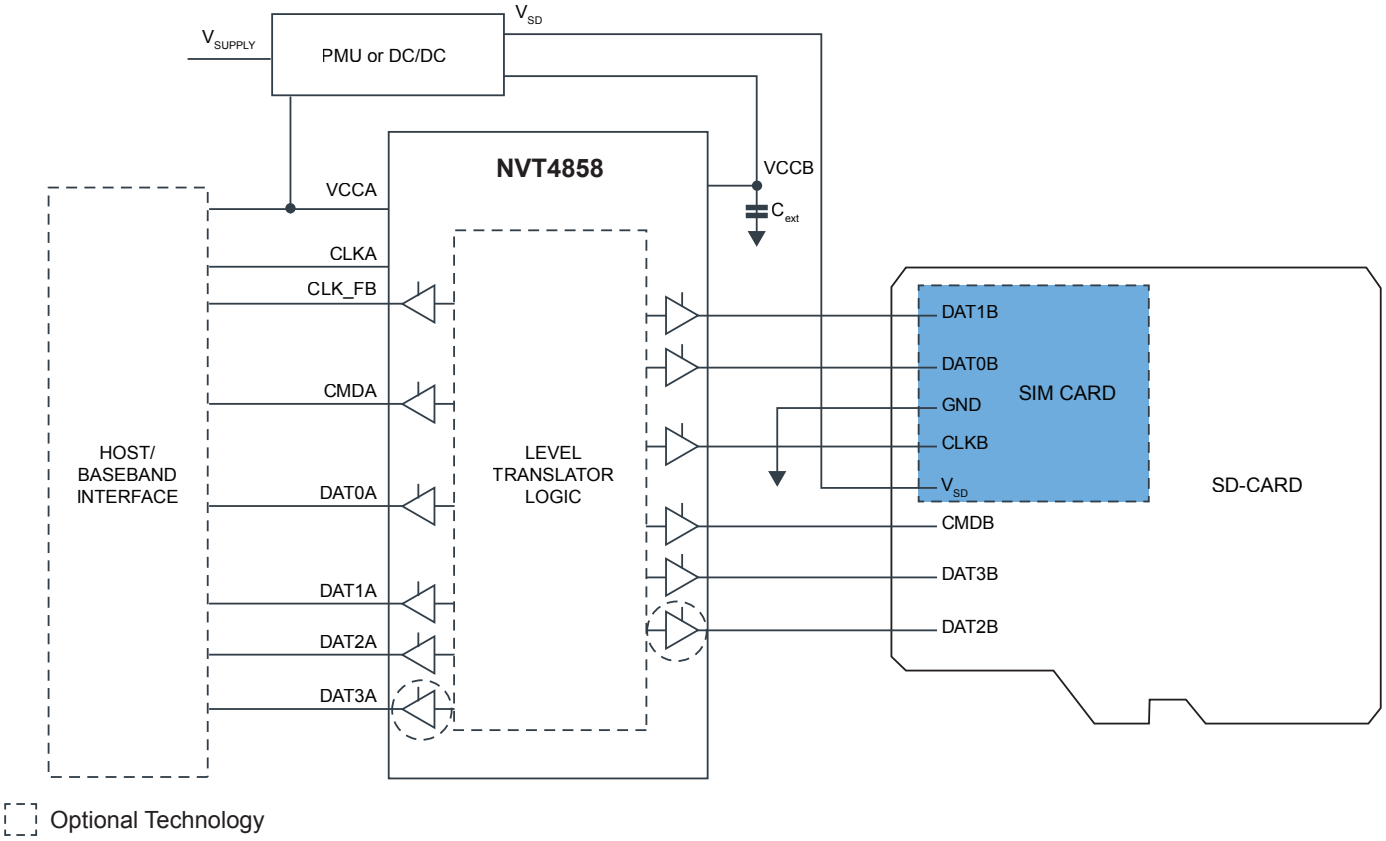


Figure 18: Typical application with external LDO

Selection information

All devices are shipped in 7” except NVT4557UK and NVT4857UK in 13” Tape and Reel with Pin 1 in Q1/T1.
All devices are temperature range of T_{amb} = -40 °C to + 85 °C and ESD HBM 2 kV and Contact 8 kV.

External LDO

Application	Part number	Package option	HOST voltage range (V)	Card voltage range (V)	LDO voltage range (V)
SIM 1.8 V Host	NVT4557	WLCSP9 and XQFN10	1.08 to 1.98	1.62 to 3.6	NA
SIM 1.2 and 1.8 V Host	NVT4558	XQFN10	1.08 to 1.98	1.62 to 3.6	NA
SD and SIM	NVT4858	WLCSP16 and XQFN16	1.08 to 1.98	1.62 to 3.6	NA

Internal LDO

Application	Part number	Package option	HOST voltage range (V)	Card voltage range (V)	LDO voltage range (V)
SIM	NVT4555	WLCSP12	1.1 to 3.6	1.8 or 2.95	2.5 to 5.25
SD and SIM	NVT4857	WLCSP20	1.1 to 2.0	1.8 or 3.0	2.9 to 3.6

Ordering information

Part number	Package	Package size (mm)	Lead/Bump pitch (mm)	Minimum order quantity	Orderable part number
NVT4555UK	WLCSP12	1.19 x 1.62 x 0.56	0.40	3000	NVT4555UKZ
NVT4557UK	WLCSP9	0.91 x 0.91 x 0.525	0.30	20000	NVT4557UKZ
NVT4557HK	XQFN10	1.4 x 1.8 x 0.5	0.40	4000	NVT4557HKX
NVT4558HK	XQFN10	1.4 x 1.8 x 0.5	0.40	4000	NVT4558HKX
NVT4857UK	WLCSP20	1.7 x 2.1 x 0.49	0.40	10000	NVT4857UKAZ
NVT4858UK	WLCSP16	2.6 x 1.8 x 0.5	0.35	3000	NVT4858UKZ
NVT4858HK	XQFN16	1.41 x 1.41 x 0.525	0.40	4000	NVT4858HKZ

Section 4

Bidirectional level translators with direction pin

Voltage translators that are equipped with two supply voltages, each supporting a different voltage range, can be used to translate from low to high or from high to low, and are typically available in versions that support either unidirectional or bidirectional level translation.

The devices in this section use the DIR pin to control the direction of translation, from the A to the B port or from the B to the A port. Integrated IOFF circuitry eliminates damaging backflow current when outputs are disabled during suspend or power-down mode. They are active translators, meaning they have a CMOS output stage with specific source and sink currents.

Bidirectional translators equipped with a direction pin are available in the NXP GTL family.

GTL-TO-LVTTL level translator and transceiver

Gunning transceiver logic (GTL) is a type of logic signaling used to drive electronic backplane buses. Defined by the JEDEC standard JESD 8-3, GTL has a voltage swing between 0.4 and 1.5 V — much lower than that used in TTL and CMOS logic — and performs symmetrical parallel resistive termination.

GTL is often found in front-side buses based on architecture designed by Intel. For GTL signals to be compatible with the rest of the system, GTL levels need to be translated to low-voltage TTL (LVTTL). NXP offers dedicated translators and transceivers for the GTL format.

Type number	Description	Operating range (V)	LVTTL 5 V tolerance	Package
GTL2012	2-bit LVTTL to GTL transceiver	3.0 to 3.6	Yes (Input only)	TSSOP8
GTL2014	4-bit LVTTL to GTL transceiver	3.0 to 3.6	Yes (Input only)	TSSOP14

Table 5: Select NXP Devices for GTL-TO-LVTTL Translation

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Document Number: VOLTLEVTRANSSG REV 3