Product Brief

SC528750PB/D
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SC528750 Integrated ColdFire® Microprocessor

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This document provides an overview of the SC528750 ColdFire® processor and general descriptions of SC528750 features and its various modules.

The SC528750 was designed as a system controller/decoder for MP3 music players, especially portable MP3 CD players. The 32-bit ColdFire core with Enhanced Multiply Accumulate (EMAC) unit provides optimum performance and code density for the combination of control code and signal processing required for MP3 decode, file management, and system control.

Low power features include a hardwired CD ROM decoder, advanced 0.18um CMOS process technology, 1.8V core power supply, and on-chip 64KByte SRAM.

The SC528750 is also an excellent general purpose system controller with over 90 Dhrystone 2.1 MIPS @ 100MHz performance at a very competitive price. The integrated peripherals and EMAC allow the SC528750 to replace both the microcontroller and the DSP in certain applications. Most peripheral pins can also be remapped as General Purpose I/O pins.

SC528750 FEATURE INTRODUCTION

The SC528750 integrated microprocessor combines a Version 2 ColdFire® processor core operating at 100MHz with the following modules.

- DMA controller with 4 DMA channels
- Integrated Enhanced Multiply-accumulate Unit (EMAC)
- 8-KByte Direct Mapped Instruction Cache
- 64-KByte SRAM (one 64K bank)
- Operates from external crystal oscillator
- Supports 16-bit wide SDRAM memories
- Serial Audio Interface which supports IIS and EIAJ audio protocols
- Digital audio transmitter and two receivers compliant with IEC958 audio protocol
- CD-ROM and CD-ROM XA block decoding and encoding function
- Two UARTS
- Queued Serial Peripheral Interface (QSPI) (Master Only)
- Two timers
- IDE and SmartMedia interfaces
- Analog/Digital Converter

- Flash Memory Card Interface
- Two I^2C modules
- System debug support
- General Purpose I/O pins shared with other functions
- 1.8V core, 3.3V I/O
- 144 pin QFP package
- -20^0 C to 70^0 C ambient operating temperature range

SC528750 BLOCK DIAGRAM

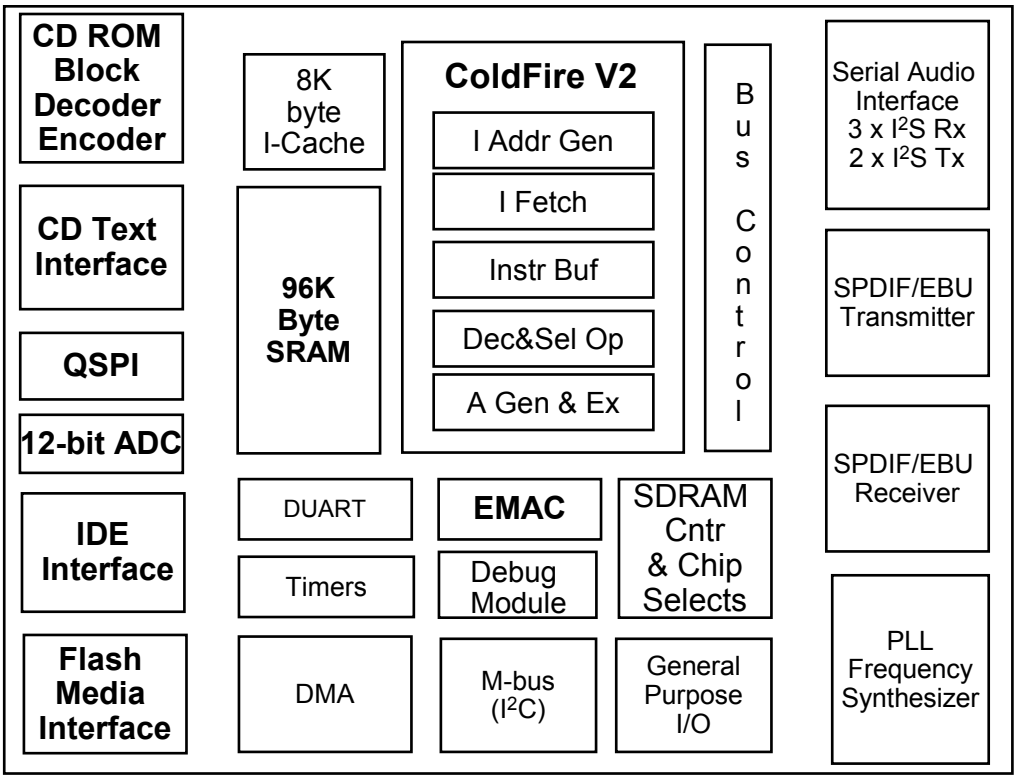

Figure 1 SC528750 Block Diagram

SC528750 FEATURE DETAILS

The primary features of the SC528750 integrated processor include the following:

- ColdFire V2 Processor Core operating at 100MHz
  - Clock-doubled Version 2 microprocessor core
  - 32-bit internal data bus, 16 bit external data bus
  - 16 user-visible, 32-bit general-purpose registers
  - Supervisor/user modes for system protection

  - Vector base register to relocate exception-vector table
  - Optimized for high-level language constructs

- DMA controller
  - Four fully programmable channels: Two dedicated to the audio interface module and two dedicated to the UART module (External requests are not supported.)
  - Supports dual- and single-address transfers with 32-bit data capability
  - Two address pointers that can increment or remain constant
  - 16-/24-bit transfer counter
  - Operand packing and unpacking support
  - Auto-alignment transfers supported for efficient block movement
  - Supports bursting and cycle stealing
  - All channels support memory to memory transfers
  - Interrupt capability
  - Provides two clock cycle internal access

- Enhanced Multiply-accumulator Unit
  - Single-cycle multiply-accumulate operations for 32 x 32 bit and 16 x 16 bit operands
  - Support for signed, unsigned, integer, and fixed-point fractional input operands
  - Four 48-bit accumulators to allow the use of a 40-bit product
  - The addition of 8 extension bits to increase the dynamic number range
  - Fast signed and unsigned integer multiplies

- 8-KByte Direct Mapped instruction cache
  - Clock-doubled to match microprocessor core speed
  - Flush capability
  - Non-blocking cache provides fast access to critical code and data

- 64-KByte SRAM
  - Provides one-cycle access to critical code and data
  - One SRAM bank - SRAM1 (64K)
  - DMA requests to/from internal SRAM1 supported

- Crystal Trim
  - The XTRIM output can be used to trim an external crystal oscillator circuit which would allow lock with an incoming IEC958 or serial audio signal

- Audio Interfaces
  - IEC958 input and output
  - Four serial Philips IIS/Sony EIAJ interfaces
    - One with input and output, one with output only, two with input only (Three inputs, two outputs)
    - Master and Slave operation

- CD Text Interface
  - Allows the interface of CD subcode (transmitter only)

- Dual Universal Synchronous/asynchronous Receiver/Transmitter (Dual UART)
  - Full duplex operation
  - Baud-rate generator
  - Modem control signals: clear-to-send (CTS) and request-to-send (RTS)
  - DMA interrupt capability
  - Processor-interrupt capability
- Queued Serial Peripheral Interface (QSPI)
  - Programmable queue to support up to 16 transfers without user intervention
  - Supports transfer sizes of 8 to 16 bits in 1-bit increments
  - Four peripheral chip-select lines for control of up to 15 devices
  - Baud rates from 273 Kbps to 12.5 Mbps at 100MHz
  - Programmable delays before and after transfers
  - Programmable clock phase and polarity
  - Supports wraparound mode for continuous transfers
  - Master mode only
- Dual 16-bit General-purpose Multimode Timers
  - Clock source selectable from external, CPU clock/2 and CPU clock/32.
  - 8-bit programmable prescaler
  - 2 timer inputs and 2 outputs
  - Processor-interrupt capability
  - 20 nS resolution with CPU clock at 100MHz
- IDE/ SmartMedia Interface
  - Allows direct connection to an IDE hard drive or other IDE peripheral
- Analog/Digital Converter
  - 12-Bit Resolution
  - 4 Muxed inputs
- Dual I^2C Interfaces
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, keypads
  - Master and slave modes, support for multiple masters
  - Automatic interrupt generation with programmable level
- System debug support
  - Real-time instruction trace for determining dynamic execution path
  - Background debug mode (BDM) for debug features while halted
  - Debug exception processing capability
  - Real-time debug support
- System Interface
  - Glueless bus interface with four chip selects and DRAMC support for interface to 16-bit for DRAM, SRAM, ROM, FLASH, and I/O devices

- Two programmable chip-select signals for static memories or peripherals, with programmable wait states and port sizes.
- One dedicated chip select for 16-bit wide DRAM /SDRAM.
- CS0 is active after reset to provide boot-up from external FLASH/ROM.
  - Programmable interrupt controller
    - Low interrupt latency
    - Eight external interrupt requests
    - Programmable autovector generator

– IEEE 1149.1 Test (JTAG) Module

- Clocking
  – Clock-multiplied PLL, programmable frequency
- 1.8V Core, 3.3V I/O
- 144 pin QFP package (qualified at 100 MHz)

SC528750 FUNCTIONAL OVERVIEW

ColdFire V2 Core

The ColdFire processor Version 2 core consists of two independent, decoupled pipeline structures to maximize performance while minimizing core size.The instruction fetch pipeline (IFP) is a two-stage pipeline for prefetching instructions. The prefetched instruction stream is then gated into the two-stage operand execution pipeline (OEP), which decodes the instruction, fetches the required operands, and then executes the required function. Because the IFP and OEP pipelines are decoupled by an instruction buffer that serves as a FIFO queue, the IFP can prefetch instructions in advance of their actual use by the OEP, which minimizes time stalled waiting for instructions. The OEP is implemented in a two-stage pipeline featuring a traditional RISC data path with a dual-read-ported register file feeding an arithmetic/logic unit (ALU).

DMA Controller

The SC528750 provides four fully programmable DMA channels for quick data transfer. Single and dual address mode is supported with the ability to program bursting and cycle stealing. Data transfer is selectable as 8, 16, 32, or 128-bits. Packing and unpacking is supported.

Two internal audio channels and the dual UART can be used with the DMA channels. All channels can perform memory to memory transfers. The DMA controller has a user-selectable, 24- or 16-bit counter and a programmable DMA exception handler.

External requests are not supported.

Enhanced Multiply and Accumulate Module (EMAC)

The integrated EMAC unit provides a common set of DSP operations and enhances the integer multiply instructions in the ColdFire architecture. The EMAC provides functionality in three related areas:

1. Faster signed and unsigned integer multiplies
2. New multiply-accumulate operations supporting signed and unsigned operands

3. New miscellaneous register operations

Multiplies of 16x16 and 32x32 with 48-bit accumulates are supported in addition to a full set of extensions for signed and unsigned integers plus signed, fixed-point fractional input operands. The EMAC has a single-clock issue for 32x32-bit multiplication instructions and implements a four-stage execution pipeline.

Instruction Cache

The instruction cache improves system performance by providing cached instructions to the execution unit in a single clock. The SC528750 processor uses a 8K-byte, direct-mapped instruction cache to achieve 90 MIPS at 100 Mhz. The cache is accessed by physical addresses, where each 16-byte line consists of an address tag and a valid bit. The instruction cache also includes a bursting interface for 16-bit and 8-bit port sizes to quickly fill cache lines.

Internal 64-KByte SRAM

The 64-KByte on-chip SRAM is available in one bank, SRAM1 (64K). It provides one clock-cycle access for the ColdFire core. This SRAM can store processor stack and critical code or data segments to maximize performance. Memory in SRAM1 can be accessed under DMA.

DRAM Controller

The SC528750 DRAM controller provides a glueless interface for one bank of DRAM up to 16MBytes. The controller supports a 16-bit data bus. A unique addressing scheme allows for increases in system memory size without rerouting address lines and rewiring boards. The controller operates in page mode, non-page mode, and burst-page mode and supports SDRAMS.

System Interface

The SC528750 provides a glueless interface to 16-bit port size SRAM, ROM, and peripheral devices with independent programmable control of the assertion and negation of chip-select and write-enable signals.

The SC528750 also supports bursting ROMs.

External Bus Interface

The bus interface controller transfers information between the ColdFire core or DMA and memory, peripherals, or other devices on the external bus. The external bus interface provides 23 bits of address bus space, a 16-bit data bus, Output Enable, and Read/Write signals. This interface implements an extended synchronous protocol that supports bursting operations.

Serial Audio Interfaces

The SC258750 digital audio interface provides four serial Philips IIS/Sony EIAJ interfaces. One interface is a 4-pin (1 bit clock, 1 word clock, 1 data in, 1 data out), the other three interfaces are 3-pin (1 bit clock, 1 word clock, 1 data in or out). The serial interfaces have no limit on minimum sampling frequency. Maximum sampling frequency is determined by maximum frequency on bit clock input. This is 1/3 the frequency of the internal system clock.

IEC958 Digital Audio Interfaces

The SC528750 has one digital audio input interface, and one digital audio output interface. The single output carries the consumer “c” channel.

Audio Bus

The audio interfaces connect to an internal bus that carries all audio data. Each receiver places its received data on the audio bus and each transmitter takes data from the audio bus for transmission. Each transmitter has a source select register.

In addition to the audio interfaces, there are six CPU accessible registers connected to the audio bus. Three of these registers allow data reads from the audio bus and allow selection of the audio source. The other three register provide a write path to the audio bus and can be selected by transmitters as the audio source. Through these registers, the CPU has access to the audio samples for processing.

Audio can be routed from a receiver to a transmitter without the data being processed by the core so the audio bus can be used as a digital audio data switch. The audio bus can also be used for audio format conversion.

CD-ROM Encoder/Decoder

The SC528750 is capable of processing CD-ROM sectors in hardware. Processing is compliant with CD-ROM and CD-ROM XA standards.

The CD-ROM decoder performs following functions in hardware:

- Sector sync recognition
- Descrambling of sectors
- Verification of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors
- Third-layer error correction is not performed

The CD-ROM encoder performs following functions in hardware:

- Sector sync recognition
- Scrambling of sectors
- Insertion of the CRC checksum for Mode 1, Mode 2 Form 1, and Mode 2 Form 2 sectors.
- Third-layer error encoding needs to be done in software. This can use approximately 5-10 Mhz of performance for single-speed.

Dual UART Module

Two full-duplex UARTs with independent receive and transmit buffers are in this module. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity, and up to 2 stop bits in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. The Dual UART module also provides several error-detection and maskable-interrupt capabilities. Modem support includes request-to-send ($\overline{\text{RTS}}$) and clear-to-send ($\overline{\text{CTS}}$) lines.

The system clock provides the clocking function from a programmable prescaler. You can select full duplex, auto-echo loopback, local loopback, and remote loopback modes. The programmable Dual UARTs can interrupt the CPU on various normal or error-condition events.

Queued Serial Peripheral Interface QSPI

The QSPI module provides a serial peripheral interface with queued transfer capability. It supports up to 16 stacked transfers at a time, making CPU intervention between transfers unnecessary. Transfers of up to 12.5 Mbits/second are possible at a CPU clock of 100 MHz. The QSPI supports master mode operation only.

Timer Module

The timer module includes two general-purpose timers, each of which contains a free-running 16-bit timer for use in any of three modes:

1. Timer Capture. This mode captures the timer value with an external event.
2. Output Capture. This mode triggers an external signal or interrupts the CPU when the timer reaches a set value
3. Event Counter. This mode counts external events.

The timer unit has an 8-bit prescaler that allows programming of the clock input frequency, which is derived from the system clock. In addition to the ÷1 and ÷16 clock derived from the bus clock (CPU clock / 2), the programmable timer-output pins either generate an active-low pulse or toggle the outputs.

IDE and SmartMedia Interfaces

The SCF5249 system bus allows connection of an IDE hard disk drive and SmartMedia flash card with a minimum of external hardware. The external hardware consists of bus buffers for address and data and are intended to reduce the load on the bus and prevent SDRAM and Flash accesses to propagate to the IDE bus. The control signals for the buffers are generated in the SC528750.

Analog/Digital Converter (ADC)

The four channel ADC is a based on the Sigma-Delta concept with 12-bit resolution. The digital portion of the ADC is provided internally. The analog voltage comparator must be provided externally as well as an external integrator circuit (resistor/capacitor) which is driven by the ADC output. A software interrupt is provided when the ADC measurement cycle is complete.

I^2C Module

The two-wire I^2C bus interface, which is compliant with the Philips I^2C bus standard, is a bidirectional serial bus that exchanges data between devices. The I^2C bus minimizes the interconnection between devices in the end system and is best suited for applications that need occasional bursts of rapid communication over short distances among several devices. Bus capacitance and the number of unique addresses limit the maximum communication length and the number of devices that can be connected.

Chip-Selects

Two programmable chip-select outputs provide signals that enable glueless connection to external memory and peripheral circuits. The base address, access permissions and automatic wait-state insertion are programmable with configuration registers. These signals also interface to 16-bit ports.

CS0 is active after reset to provide boot-up from external FLASH/ROM.

GPIO Interface

A total of 29 General Purpose inputs and 31 General Purpose outputs are available. These are multiplexed with various other signals. Seven of the GPIO inputs have edge sensitive interrupt capability.

Interrupt Controller

The interrupt controller provides user-programmable control of a total of 57 interrupts. There are 49 internal interrupt sources. In addition, there are 7 GPIOs where interrupts can be generated on the rising or falling edge of the pin. All interrupts are autovectored and interrupt levels are programmable.

JTAG

To help with system diagnostics and manufacturing testing, the SC528750 includes dedicated user-accessible test logic that complies with the IEEE 1149.1A standard for boundary scan testability, often referred to as Joint Test Action Group, or JTAG. For more information, refer to the IEEE 1149.1A standard. Motorola provides BSDL files for JTAG testing.

System Debug Interface

The ColdFire processor core debug interface supports real-time instruction trace and debug, plus background-debug mode. A background-debug mode (BDM) interface provides system debug.

In real-time instruction trace, four status lines provide information on processor activity in real time (PST pins). A four-bit wide debug data bus (DDATA) displays operand data and change-of-flow addresses, which helps track the machine's dynamic execution path.

Crystal and On-chip PLL

Typically, an external 16.92 Mhz or 33.86 Mhz clock input is used for CD R/W applications, while an 11.2896 MHz clock is more practical for Portable CD player applications. However, the on-chip programmable PLL, which generates the processor clock, allows the use of almost any low frequency external clock (5-35 Mhz).

Two clock outputs (MCLK1 and MCLK2) are provided for use as Audio Master Clock. The output frequencies of both outputs are programmable to Fxtal, Fxtal/2, Fxtal/3, and Fxtal/4. The Fxtal/3 option is only available when the 33.86 Mhz crystal is connected.

The SC528750 supports VCO operation of the oscillator by means of a 16-bit pulse density modulation output. Using this mode, it is possible to lock the oscillator to the frequency of an incoming IEC958 or IIS signal. The maximum trim depends on the type and design of the oscillator. Typically a trim of +/- 100 ppm can be achieved with a crystal oscillator and over +/- 1000 ppm with an LC oscillator.

DOCUMENTATION

Table 1 lists the documents that provide a complete description of the SC528750 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or through the Motorola DSP home page on the Internet; http://e-www.motorola.com/
(the source for the latest information).

Table 1 SC528750 Documentation

Document Name	Description	Order Number
CFPRM/D	ColdFire Family Programmer's Reference Manual	CFPRM/D
ColdFire2UM	Version 2/2M ColdFire Core Processor User's Manual	ColdFire2UM/D
ColdFire2UMAD	Version 2/2M ColdFire Core Processor User's Manual Addendum	ColdFire2UMAD/D
SCF5249UM	SCF5249 User's Manual	SCF5249UM/D

HOW TO REACH US:

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P.O. Box 5405, Denver, Colorado 80217
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