PF5400

30 A dual phase high efficiency core supply regulator with AVP and watchdog

Rev. 1.0 — 1 July 2025 **Product brief**

Document information

Information	Content
Keywords	PF5400, 30A Buck, Automotive PMIC, Industrial PMIC, NXP PMIC, High Efficiency Buck, Core Supply
Abstract	The PF5400 integrates two 15 A high-performance buck converters. These buck converters can be configured as dual phase up to 30 A capability, to power high-end automotive and industrial processors. With adaptive-voltage positioning and a high-bandwidth loop, the buck converters offer transient regulation to minimize capacitor requirements.

1 Overview

The PF5400 integrates two 15 A high-performance buck converters. These buck converters can be configured as dual phase up to 30 A capability, to power high-end automotive and industrial processors.

With adaptive-voltage positioning and a high-bandwidth loop, the buck converters offer transient regulation to minimize capacitor requirements.

The spread-spectrum feature reduces EMC issues in the system. PF5400s can operate as standalone point-of-load regulator ICs or as companion chips to a system power management IC (PMIC).

Built-in multiple-time programmable (MTP) memory stores key startup configurations, drastically reducing the number of external components. Regulator parameters are adjustable through high-speed I^2C after startup, offering flexibility for different system states.

The PF5400 has been developed to comply with the ISO 26262 automotive safety standard and the IEC61508 industrial standard. PF5400 variations include configurable feature sets to fit in or support applications with safety levels of automotive safety integrity level (ASIL) B and SIL 2.

2 Features

The PF5400 integrates two high-performance 15 A buck converters with the flexibility to be configured as dual phase, to power high-end automotive and industrial processors.

- High-performance core buck regulators
  - 15 A low RDS(on) integrated-FET high efficiency buck converters
  - 3.0 V to 5.5 V input range
  - 0.5 V to 1.2 V output range
  - High efficiency, peak efficiency > 90%
  - ±1 % output accuracy
  - FB+/FB- pin lift detection and protection
  - 2 MHz to 3 MHz switching frequency (single phase)
  - 1.1 MHz switching frequency (dual phase)
  - Dynamic voltage scaling (DVS)
  - Programmable adaptive-voltage positioning (AVP)
- 2 µA quiescent current in OFF mode
- Fast startup time (< 500 µs)
- Multiple-time programming (MTP) memory for device configuration
- Overtemperature protection
- Safety features
  - Available in SIL 2, ASIL B, and QM variations
  - Separate bandgap for Main (bg1) and FuSa (bg2) domains
  - Physically isolated digital area for safety mechanisms
  - 1 % OV/UV monitoring
  - PGOOD output
  - Analog built-in self-test (ABIST)
  - Logic built-in self-test (LBIST)
  - Watchdog timer
- AEC-Q100 qualified version available
- Rated from -40 ℃ to 150 ℃ Tj
- 6.5 mm x 5.0 mm WF-QFN package

3 Applications

QM, ASIL B, and SIL 2 applications, such as:

- Gateway
- Infotainment / cluster / driver awareness
- Telematics
- V2X
- Radar
- Vision
- ADAS
- Sensor fusion
- Machine learning

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TBD			

5 Simplified application schematic example

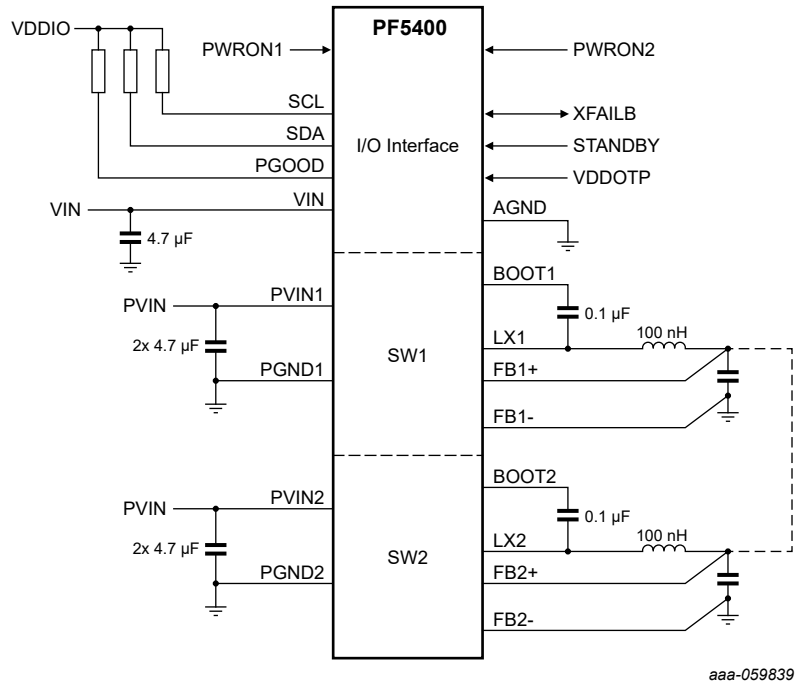

Figure 1. Simplified application schematic example

6 Device description

6.1 Functional block diagram

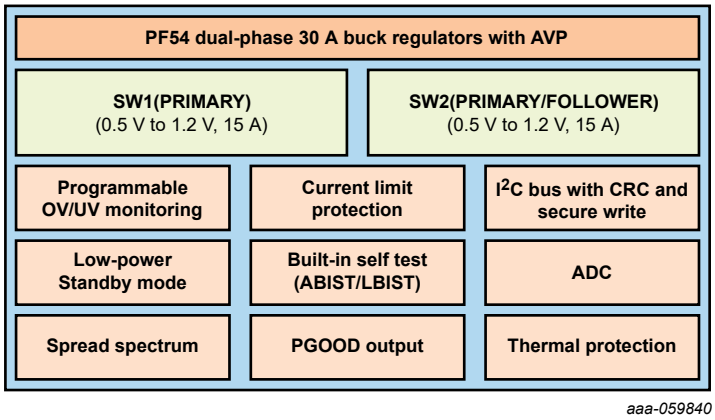

Figure 2. Functional block diagram

6.2 Pin descriptions

The PF54 will be offered in a FC QFN package. All pins are assumed to be *local* from an automotive perspective for EMI/EMC considerations.

Table 2. Pin descriptions

Pin name	Description	Absolute maximum voltage rating
FB1+	Differential amplifier positive input. Connect to positive end of SW1 output voltage.	-0.3 V to 5.5 V
FB2+	Differential amplifier positive input. Connect to positive end of SW2 output voltage.	-0.3 V to 5.5 V
FB1-	Differential amplifier negative input. Connect to negative (ground) end of SW1 output voltage.	-0.3 V to 5.5 V
FB2-	Differential amplifier negative input. Connect to negative (ground) end of SW2 output voltage.	-0.3 V to 5.5 V
LX1	Output of buck1 converter	-0.3 V to 5.5 V
LX2	Output of buck2 converter	-0.3 V to 5.5 V
BOOT1	Bootstrap pin for high-side gate drive. Connect 0.1 µF from BOOT1 to LX1 pin.	(LX1 -0.3 V) to (LX1 + 5.5 V)
BOOT2	Bootstrap pin for highside gate drive. Connect 0.1 µF from BOOT2 to LX2 pin.	(LX2 -0.3 V) to (LX2 + 5.5 V)
VIN	Gate drive power and internal digital supply input	-0.3 V to 5.5 V
PVIN1	PVIN1 input to buck1 converter	-0.3 V to 5.5 V
PVIN2	PVIN2 input to buck2 converter	-0.3 V to 5.5 V
PGND	Ground of buck1, buck2 converters	N/A
AGND	Analog ground of IC	N/A
SDA	I^2C data line. Pull up to external I/O voltage.	-0.3 V to 5.5 V

Table 2. Pin descriptions*...continued*

Pin name	Description	Absolute maximum voltage rating
SCL	I^2C clock input. Pull up to external I/O voltage.	-0.3 V to 5.5 V
STANDBY	Standby input to enter low power mode.	-0.3 V to 5.5 V
VDDOTP	VDDOTP used to program OTP memory and enter fuse emulation mode.	-0.3V to 10 V
PWRON1	PWRON1 is the hardware enable for SW1.	-0.3 V to 10 V
PWRON2	PWRON2 is the hardware enable for SW2.	-0.3 V to 5.5 V
PGOOD	Open-drain PGOOD output. Pull up to external pullup voltage via 4.7 kΩ resistor.	-0.3 V to 5.5 V
XFAILB	XFAILB pin to communicate with other NXP PF PMICs.	-0.3 V to 5.5 V

6.3 ESD rating

Table 3. ESD ratings

Symbol	Parameter	Min	Typ	Max	Unit
VESD	Human body model	—	—	± 2000	V
VESD	Charge device model - all pins	—	—	± 500	V

6.4 Thermal ratings

Table 4. Thermal ratings

Symbol	Description (Rating)	Min	Max	Unit
T_A	Ambient operating temperature range	-40	125	℃
T_J	Operating junction temperature range	-40	150	℃
θ_{JA}	Package junction to ambient thermal resistance	TBD	TBD	C/W

6.5 Device electrical specifications

Table 5. Device electrical specifications

All parameters are specified at T_A = -40 to 125 °C, PVIN1 = PVIN2 = VIN = 5V, PWRONx = high, No Load on regulator, Fsw = 2.2 MHz /1.1 MHz, typical external component values, unless otherwise noted. Typical values are specified at 25 °C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit
Quiescent current, PWRON1 = PWRON2 = 0 (ULPOFF Mode)	Iq1		2		µA
Startup time (PWRONx = 1 to PGOOD = 1)	Tst			500	µs
SW1/2 load current capability	Iload	15			A
SW1/2 nominal output voltage	Vout1/2	0.5		1.2	V
SW1/2 output voltage accuracy (0.75V ≤ Vout ≤ 1.2 V, load 0 A to 15 A, AVP disabled, PWM Mode)	Acc	-1		1	%
SW1/2 output voltage accuracy (0.5V ≤ Vout < 0.75V, load 0 A to 15 A, AVP disabled, PWM Mode)	Acc	-7.5		7.5	mV
SW1/2 output voltage accuracy (0.5 V ≤ Vout ≤ 1.2 V, load 0 A to 0.5 A, AVP disabled, PFM Mode)	Acc_PFM	-3		3	%
Voltage monitoring accuracy measured by ADC (CH1 and CH2)	Vmon_acc	-0.8		0.8	%
Buck switching frequency range (single phase)	Fsw	2	2.2	3	MHz
Buck switching frequency range (dual phase)	Fsw		1.1		MHz

7 Bill of material

Table 6. Bill of material

Block	Function	Description	Max
PF54	Silicon	FC QFN Package	PF54
Buck 1/2 converter	Inductor	100 nH, 1.5 mΩ, 15 A, each buck	HPL505028FR10MD3P
	Bootstrap	0.1 µf, 16 V, each buck	Generic, 0402
	Input capacitor	2x CAP CER 10UF 6.3V 10% X7R 0603, each buck	Generic, 0603
	Output capacitor	8x CAP CER 22UF 6.3V 20% X7R 1206 or X7T 0805 (stable to 1000 µF), each buck	Generic, 1206/0805
VIN	Gate driver and digital supply	CAP CER 4.7UF 6.3V 10% X7R 0603	Generic, 0603
SDA/SCL	I^2C Bus	2.2 kΩ, pullup resistor, 0402	Generic, 0402
PGOOD	PGOOD output	4.7 kΩ, pullup resistor, 0402	Generic, 0402
XFAILB	Interruption output	4.7 kΩ, pullup resistor, 0402	Generic, 0402

8 Revision history

Document ID	Release date	Description
PF5400_PB v. 1.0	1 July 2025	Initial release of preliminary product brief

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