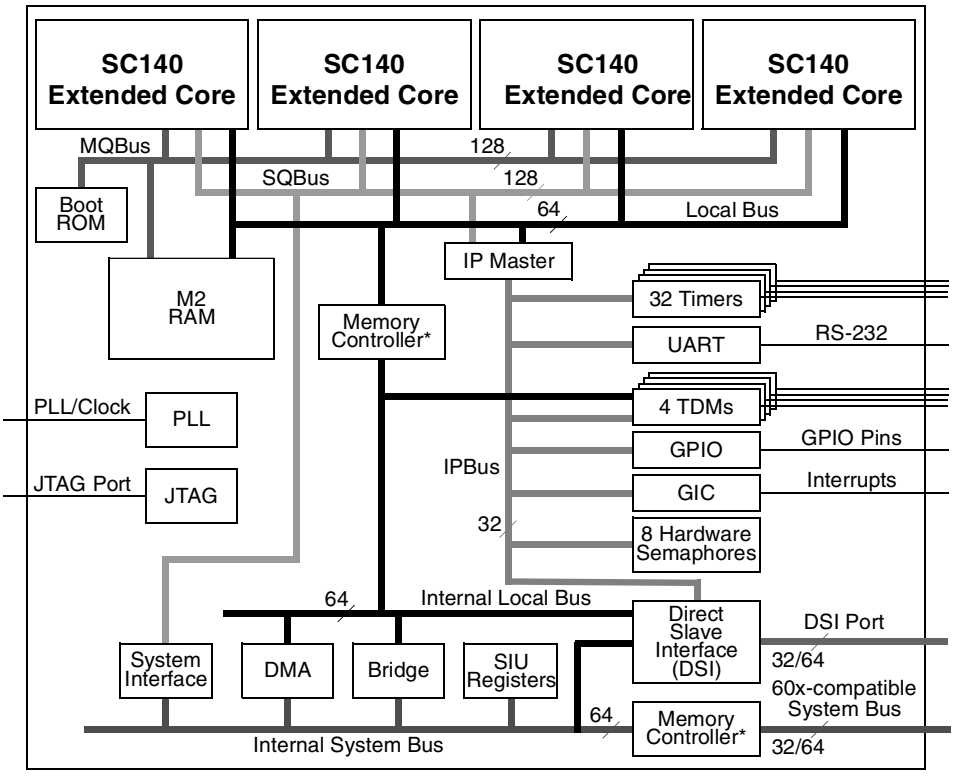
# MSC8102

## Quad Core 16-Bit Digital Signal Processor

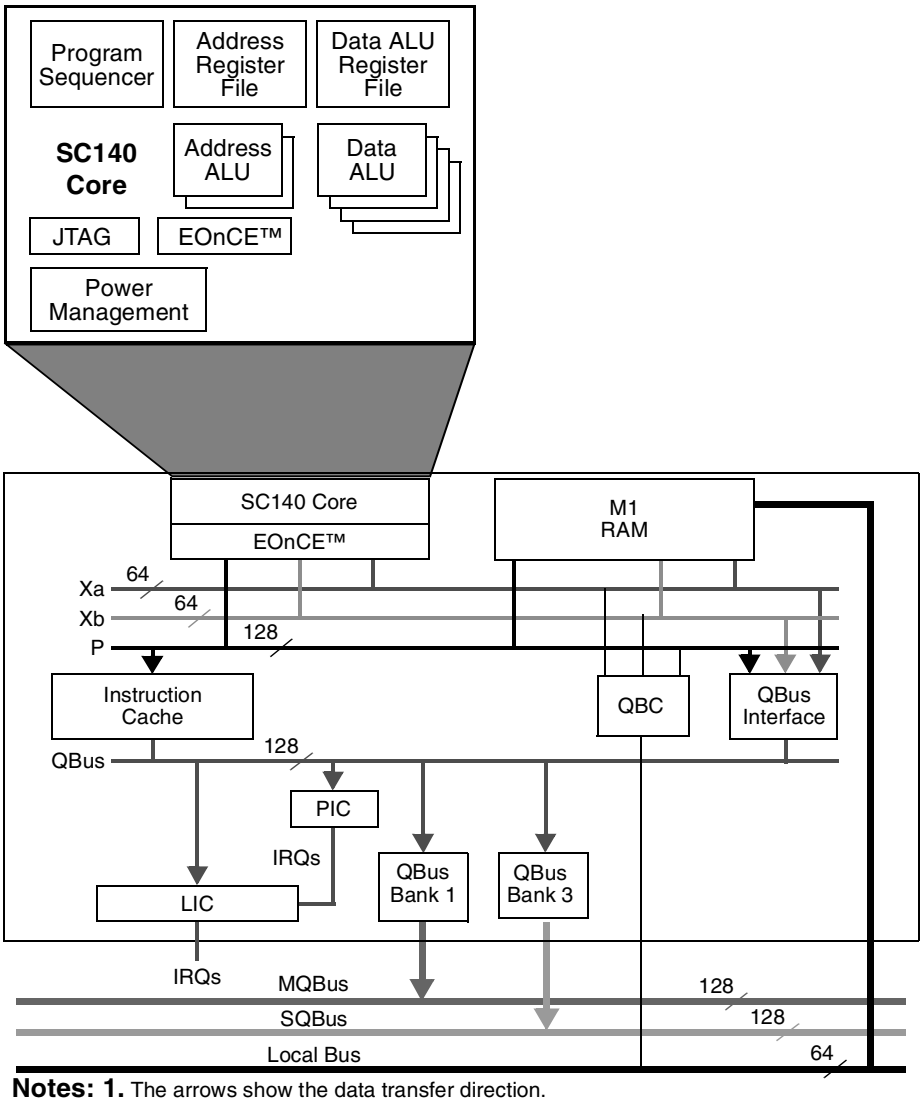



*There is a single memory controller that controls access to both the local bus and the system bus.

**Figure 1.** MSC8102 Block Diagram

*The raw processing power of this highly integrated system-on- a-chip device enables developers to create next generation networking products that offer tremendous channel densities, while maintaining system flexibility, scalability, and upgradeability. The MSC8102 is offered in two core speed levels: 250 and 275 MHz*

The MSC8102 is a highly integrated system-on- a-chip that combines four StarCore SC140 extended cores with an RS-232 serial interface, four time-division multiplexed (TDM) serial interfaces, thirty-two general-purpose timers, a flexible system interface unit (SIU), and a multi-channel DMA engine. The four extended cores can deliver a total 4400 DSP MMACS performance at 275 MHz. Each core has four arithmetic logic units (ALUs), internal memory, a write buffer, and two interrupt controllers (see **Figure 2**). The MSC8102 targets high-bandwidth highly computational DSP applications and is optimized for wireless transcoding and packet telephony as well as high-bandwidth base station applications. The MSC8102 delivers enhanced performance while maintaining low power dissipation and greatly reduces system cost.




**Notes: 1.** The arrows show the data transfer direction.

**2**. The QBus interface includes a bus switch, write buffer, fetch unit, and a control unit that defines four QBus banks. In addition, the QBC handles internal memory contentions.

**Figure 2.** SC140 Extended Core Block Diagram

# Features

The tables in this section list the features of the MSC8102 device.

**Table 1.** Extended SC140 Cores and Core Memories

| Feature | Description |
|---|---|
| **SC140 Core** | Four SC140 cores:<br>• Up to 4400 MMACS using 16 ALUs running at up to 275 MHz.<br>• A total of 1436 KB of internal SRAM (224 KB per core).<br>Each SC140 core provides the following:<br>• Up to 1100 MMACS using an internal 275 MHz clock at 1.6 V. A MAC operation includes a multiply-accumulate command with the associated data move and pointer update.<br>• 4 ALUs per SC140 core.<br>• 16 data registers, 40 bits each.<br>• 27 address registers, 32 bits each.<br>• Hardware support for fractional and integer data types.<br>• Very rich 16-bit wide orthogonal instruction set.<br>• Up to six instructions executed in a single clock cycle.<br>• Variable-length execution set (VLES) that can be optimized for code density and performance.<br>• IEEE 1149.1 JTAG port.<br>• Enhanced on-device emulation (EOnCE) with real-time debugging capabilities. |
| **Extended Core** | Each SC140 core is embedded within an extended core that provides the following:<br>• 224 KB M1 memory that is accessed by the SC140 core with zero wait states.<br>• Support for atomic accesses to the M1 memory.<br>• 16 KB instruction cache, 16 ways.<br>• A four-entry write buffer that frees the SC140 core from waiting for a write access to finish.<br>• External cache support by asserting the global signal (GBL) when predefined memory banks are accessed.<br>• Program Interrupt Controller (PIC).<br>• Local Interrupt Controller (LIC). |
| **Multi-Core Shared Memories** | • M2 memory (shared memory):<br>  • A 476 KB memory working at the core frequency.<br>  • Accessible from the local bus<br>  • Accessible from all four SC140 cores using the MQBus.<br>• 4 KB bootstrap ROM. |
| **M2-Accessible Multi-Core Bus (MQBus)** | • A QBus protocol multi-master bus connecting the four SC140 cores to the M2 memory.<br>• Data bus access of up to 128-bit read and up to 64-bit write.<br>• Operation at the SC140 core frequency.<br>• A central efficient round-robin arbiter controlling SC140 core access on the MQBus.<br>• Atomic operation control of access to M2 memory by the four SC140 cores and the local bus. |

**Table 2.** Phase-Lock Loop (PLL)

| Feature | Description |
|---|---|
| **Internal PLL** | • Generates up to 275 MHz core clock and up to 91.67 MHz bus clocks for the 60x-compatible local and system buses and other modules.<br>• PLL values are determined at reset based on configuration signal values. |

**Table 3.** Buses and Memory Controller

| Feature | Description |
|---|---|
| **Dual-Bus Architecture** | Can be configured to a 32-bit data system bus and a 64-bit data direct slave interface (DSI) or to a 64-bit data system bus and 32-bit data DSI. |
| **60x-Compatible System Bus** | • 64/32-bit data and 32-bit address 60x bus.<br>• Support for multiple-master designs.<br>• Four-beat burst transfers (eight-beat in 32-bit wide mode).<br>• Port size of 64, 32, 16, and 8 controlled by the internal memory controller.<br>• Bus can access external memory expansion or off-device peripherals, or it can enable an external host device to access internal resources.<br>• Slave support, direct access by an external host to internal resources including the M1 and M2 memories.<br>• On-device arbitration between up to four master devices. |
| **Direct Slave Interface (DSI)** | Provides a 32/64-bit wide slave host interface that operates only as a slave device under the control of an external host processor.<br>• 21 bit address, 32/64-bit data.<br>• Direct access by an external host to on-device resources, including the M1 and the M2 memories.<br>• Synchronous and asynchronous accesses, with burst capability in the synchronous mode.<br>• Dual or Single strobe modes.<br>• Write and Read buffers improves host bandwidth.<br>• Byte enable signals enables 1, 2, 4, and 8 byte write access granularity.<br>• Sliding window mode enables access with reduced number of address pins.<br>• Chip ID decoding enables using one $\overline{CS}$ signal for multiple DSPs.<br>• Broadcast $\overline{CS}$ signal enables parallel write to multiple DSPs.<br>• Big-endian, little-endian, and munged little-endian support. |
| **Memory Controller** | Flexible eight-bank memory controller:<br>• Three user-programmable machines (UPMs), general-purpose chip-select machine (GPCM), and a page-mode SDRAM machine<br>• Glueless interface to SRAM, 100 MHz page mode SDRAM, DRAM, EPROM, Flash memory, and other user-definable peripherals.<br>• Byte enables for either 64-bit or 32-bit bus width mode.<br>• Eight external memory banks (banks 0–7). Two additional memory banks (banks 9, 11) control IPBus peripherals and internal memories. Each bank has the following features:<br>  • 32-bit address decoding with programmable mask.<br>  • Variable block sizes (32 KB to 4 GB).<br>  • Selectable memory controller machine.<br>  • Two types of data errors check/correction: normal odd/even parity and read-modify-write (RMW) odd/even parity for single accesses.<br>  • Write-protection capability.<br>  • Control signal generation machine selection on a per-bank basis.<br>  • Support for internal or external masters on the 60x-compatible system bus.<br>  • Data buffer controls activated on a per-bank basis.<br>  • Atomic operation.<br>  • RMW data parity check (on 60x-compatible system bus only).<br>  • Extensive external memory-controller/bus-slave support.<br>  • Parity byte select pin, which enables a fast, glue less connection to RMW-parity devices (on 60x-compatible system bus only).<br>  • Data pipeline to reduce data set-up time for synchronous devices. |

**Table 4.** DMA Controller

| Feature | Description |
|---|---|
| **Multi-Channel DMA Controller** | • 16 time-multiplexed unidirectional channels.<br>• Services up to four external peripherals.<br>• Supports DONE or DRACK protocol on two external peripherals.<br>• Each channel group services 16 internal requests generated by eight internal FIFOs. Each FIFO generates:<br>  • a watermark request to indicate that the FIFO contains data for the DMA to empty and write to the destination<br>  • a hungry request to indicate that the FIFO can accept more data.<br>• Priority-based time-multiplexing between channels using 16 internal priority levels<br>• A flexible channel configuration:<br>  • All channels support all features.<br>  • All channels connect to the 60x-compatible system bus or local bus.<br>• Flyby transfers in which a single data access is transferred directly from the source to the destination without using a DMA FIFO. |

**Table 5.** Serial Interfaces

| Feature | Description |
|---|---|
| **Time-Division Multiplexing (TDM)** | Up to four independent TDM modules, each with the following features:<br>• Either totally independent receive and transmit, each having one data line, one clock line, and one frame sync line or four data lines, one clock and one frame sync that are shared between the transmit and receive.<br>• Glueless interface to E1/T1 framers and MVIP, SCAS, and H.110 buses.<br>• Hardware A-law/μ-law conversion<br>• Up to 50 Mbps per TDM (50 MHz bit clock if one data line is used, 25 MHz if two data lines are used, 12.5 MHz if four data lines are used).<br>• Up to 256 channels.<br>• Up to 16 MB per channel buffer (granularity 8 bytes), where A/μ law buffer size is double (granularity 16 byte)<br>• Receive buffers share one global write offset pointer that is written to the same offset relative to their start address.<br>• Transmit buffers share one global read offset pointer that is read from the same offset relative to their start address.<br>• All channels share the same word size.<br>• Two programmable receive and two programmable transmit threshold levels with interrupt generation that can be used, for example, to implement double buffering.<br>• Each channel can be programmed to be active or inactive.<br>• 2-, 4-, 8-, or 16-bit channels are stored in the internal memory as 2-, 4-, 8-, or 16-bit channels, respectively.<br>• The TDM Transmitter Sync Signal (TxTSYN) can be configured as either input or output.<br>• Frame Sync and Data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock.<br>• Frame sync can be programmed as active low or active high.<br>• Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame.<br>• MSB or LSB first support. |

**Table 5.** Serial Interfaces

| Feature | Description |
|---|---|
| **UART** | • Two signals for transmit data and receive data.<br>• No clock, asynchronous mode.<br>• Can be serviced either by the SC140 DSP cores or an external host on the 60x-compatible system bus or on the DSI.<br>• Full-duplex operation.<br>• Standard mark/space non-return-to-zero (NRZ) format.<br>• 13-bit baud rate selection.<br>• Programmable 8-bit or 9-bit data format.<br>• Separately enabled transmitter and receiver.<br>• Programmable transmitter output polarity.<br>• Two receiver walk-up methods:<br>  • Idle line walk-up.<br>  • Address mark walk-up.<br>• Separate receiver and transmitter interrupt requests.<br>• Eight flags, the first five can generate interrupt request:<br>  • Transmitter empty.<br>  • Transmission complete.<br>  • Receiver full.<br>  • Idle receiver input.<br>  • Receiver overrun.<br>  • Noise error.<br>  • Framing error.<br>  • Parity error.<br>• Receiver framing error detection.<br>• Hardware parity checking.<br>• 1/16 bit-time noise detection.<br>• Maximum bit rate 6.25 Mbps.<br>• Single-wire and loop operations. |
| **General-Purpose I/O (GPIO) port** | • 32 bidirectional signal lines that either serve the peripherals or act as programmable I/O ports.<br>• Each port can be programmed separately to serve up to two dedicated peripherals, and each port supports open-drain output mode. |

**Table 6.** Miscellaneous Modules

| Feature | Description |
|---|---|
| **Timers** | Two modules of 16 timers each. Each timer has the following features:<br>• Cyclic or one-shot.<br>• Input clock polarity control.<br>• Interrupt request when counting reaches a programmed threshold.<br>• Pulse or level interrupts.<br>• Dynamically updated programmed threshold.<br>• Read counter any time.<br>Watchdog mode for the timers that connect to the device. |
| **Hardware Semaphores** | Eight coded hardware semaphores, locked by simple write access without need for read-modify-write mechanism. |
| **Global Interrupt Controller (GIC)** | • Consolidation of chip maskable interrupt and non-maskable interrupt sources and routing to $\overline{\text{INT\_OUT}}$, $\overline{\text{NMI\_OUT}}$, and to the cores.<br>• Generation of 32 virtual interrupts (eight to each SC140 core) by a simple write access.<br>• Generation of virtual $\overline{\text{NMI}}$ (one to each SC140 core) by a simple write access. |

**Table 7.** Power and Packaging

| Feature | Description |
|---|---|
| **Reduced Power Dissipation** | • Low power CMOS design.<br>• Separate power supply for internal logic () and I/O (3.3 V).<br>• Low-power standby modes.<br>• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent). |
| **Packaging** | • 0.8 mm pitch High Temperature Coefficient for Expansion Flip-Chip Ceramic Ball-Grid Array (CBGA (HCTE)).<br>• 431-connection (ball).<br>• 20 mm × 20 mm. |

**Table 8.** Software Support

| Feature | Description |
|---|---|
| **Real-Time Operating System (RTOS)** | The Real-Time Operating System (RTOS) fully supports device architecture (multi-core, memory hierarchy, ICache, timers, DMA, interrupts, peripherals), as follows:<br>• High-performance and deterministic, delivering predictive response time.<br>• Optimized to provide low interrupt latency with high data throughput.<br>• Preemptive and priority-based multitasking.<br>• Fully interrupt/event driven.<br>• Small memory footprint.<br>• Comprehensive set of APIs.<br>• Fully supports DMA controller, interrupts, and timer schemes. |
| **Multi-Core Support** | • Enables use of one instance of kernel code all four SC140 cores.<br>• Dynamic and static memory allocation from local memory (M1) and shared memory (M2). |
| **Distributed System Support** | Enables transparent inter-task communications between tasks running inside the SC140 cores and the other tasks running in on-board devices or remote network devices:<br>• Messaging mechanism between tasks using mailboxes and semaphores.<br>• Networking support; data transfer between tasks running inside and outside the device using networking protocols.<br>• Includes integrated device drivers for such peripherals as TDM, UART, and external buses. |
| **Additional Features** | • Incorporates task debugging utilities integrated with compilers and vendors.<br>• Board support package (BSP) for the application development system (ADS).<br>• Integrated Development Environment (IDE):<br>  • C/C++ compiler with in-line assembly. Enables the developer to generate highly optimized DSP code. It translates code written in C/C++ into parallel fetch sets and maintains high code density.<br>  • Librarian. Enables the user to create libraries for modularity.<br>  • C libraries. A collection of C/C++ functions for the developer's use.<br>  • Linker. Highly efficient linker to produce executables from object code.<br>  • Debugger. Seamlessly integrated real-time, non-intrusive multi-mode debugger that enables debugging of highly optimized DSP algorithms. The developer can choose to debug in source code, assembly code, or mixed mode.<br>  • Simulator. Device simulation models, enables design and simulation before the hardware arrival.<br>  • Profiler. An analysis tool using a patented Binary Code Instrumentation (BCI) technique that enables the developer to identify program design inefficiencies.<br>  • Version control. CodeWarrior® includes plug-ins for ClearCase, Visual SourceSafe, and CVS. |
| **Boot Options** | • External memory.<br>• External host.<br>• UART.<br>• TDM. |

**Table 9.** Application Development System (ADS) Board

| Feature | Description |
|---|---|
| **MSC8102ADS** | • Host debug through single JTAG connector supports both processors.<br>• MSC8101 as the host with both devices on the board. The MSC8101 system bus connects to the DSI.<br>• Flash memory for stand-alone applications.<br>• Support for the following communications ports:<br>  • 10/100Base-T.<br>  • 155 Mbit ATM over Optical.<br>  • T1/E1 TDM interface.<br>  • H.110.<br>  • Voice codec.<br>  • RS-232.<br>  • High-density (MICTOR) logic analyzer connectors to monitor signals<br>  • 6U CompactPCI form factor.<br>• Emulates DSP farm by connecting to three other ADS boards. |

# Product Documentation

The documents listed in **Table 10** are required for a complete description of the MSC8102 and are necessary to design properly with the part. Obtain documentation from a local Freescale distributor, Freescale Semiconductor sales office, or a Freescale Literature Distribution Center. For documentation updates, visit the Freescale DSP website shown on the last page of this document.

**Table 10.** MSC8102 Documentation

| Name | Description | Order Number |
|---|---|---|
| MSC8102 *Technical Data* | MSC8102 features list and physical, electrical, timing, and package specifications | MSC8102/D |
| MSC8102 *User's Guide* | User information include system functionality, getting started tutorial, and programming topics | MSC8102UG/D |
| *MSC8102 Reference Manual* | Detailed functional description of the MSC8102 memory and peripheral configuration, operation, and register programming | MSC8102RM/D |
| *SC140 DSP Core Reference Manual* | Detailed description of the SC140 family processor core and instruction set | MNSC140CORE/D |
| *Application Notes* | Documents describing specific applications or optimized device operation including code examples | See the MSC8102 product website |

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