Freescale Semiconductor
Product Brief

Document Number: MPC8313EPB
Rev. 0, 12/2006

MPC8313E PowerQUICC™ II Pro Processor Product Brief

This document provides an overview of the MPC8313E PowerQUICC™ II Pro processor features, including a block diagram showing the major functional components. The MPC8313E is a cost-effective, low-power, highly integrated host processor that addresses the requirements of several printing and imaging, consumer, and industrial applications, including main CPUs and I/O processors in printing systems, networking switches and line cards, wireless LANs (WLANs), network access servers (NAS), VPN routers, intelligent NIC, and industrial controllers. The MPC8313E extends the PowerQUICC™ family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size. This document also supports the MPC8313 host processors but is written from the perspective of the MPC8313E.

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1 Application Examples

The features of the MPC8313E make it suitable for a wide variety of printer and network communication applications as described in this section.

1.1 Low-End Printer CPU and Interface ASIC

Figure 1 illustrates how the MPC8313E can perform the function of the CPU + interface ASIC on a low-end printer application.

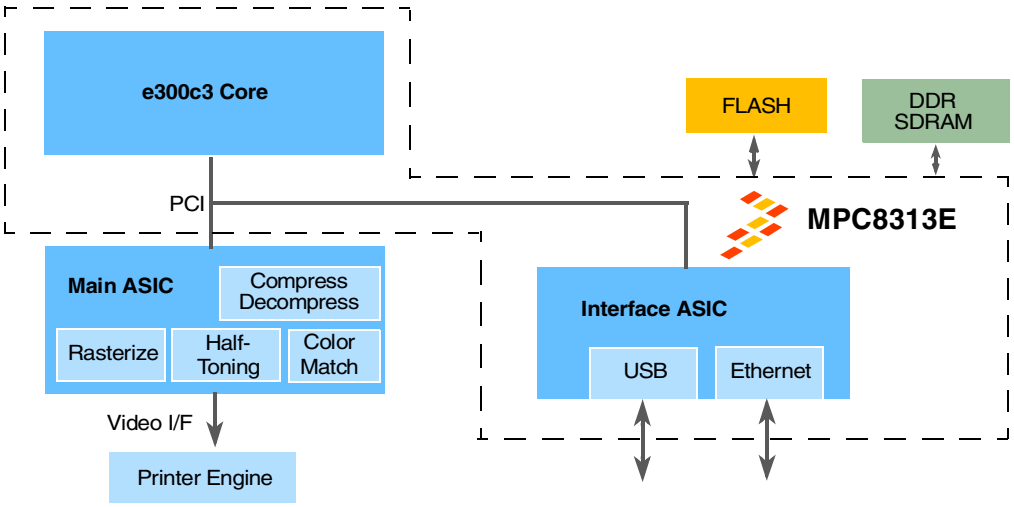

Figure 1. MPC8313E Serving as the Main CPU in a Low-End Printer Application

In this application, the CPU interfaces to the main ASIC through the high-bandwidth PCI bus. Low-end multi-function printers (MFPs) are able to share the same platform simply by adding a scanner/fax engine. The interface ASIC provides the various network interfaces that are used to access the printer.

Image data coming through the scanner or fax interface is sent to the main ASIC, which processes the image by implementing algorithms for image compression/decompression and rendering. The image data is then processed in the FPU in the CPU core at high speeds and sent to the printer engine. Likewise, image data or text data that are interfaced at the Ethernet interface on the interface ASIC are also manipulated at the main ASIC and CPU and sent to the printer engine.

Recent MFP systems require higher processor performance in order to manipulate large, high-quality images at high speeds. Required networking interfaces including USB, PCI, and Gigabit Ethernet are integrated on the MPC8313E, allowing for the CPU and interface ASIC to be consolidated in one device. As a result, an MFP application can be developed by combining the MPC8313E with the main ASIC (graphic processing ASIC) at a lower cost without the need to have separate a CPU and interface ASIC. At the same time, the system is required to consume low power. The MPC8313E provides several power management methods to reduce power consumption.

1.1.1 High-End Printer I/O Processor

The diagram in Figure 2 illustrates how an MPC8313E can function as an I/O processor in a high-end printer application.

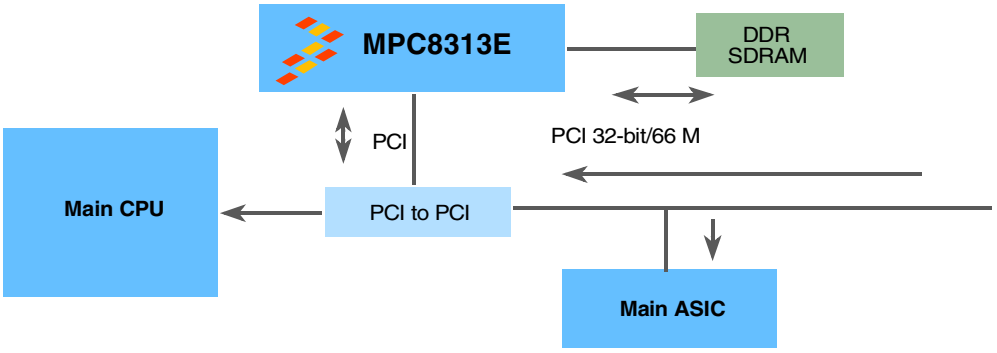

Figure 2. MPC8313E I/O Processor Implementation in a High-End Printer Application

In this example, the MPC8313E primarily functions as a controller for the main ASIC. The MPC8313E and the main ASIC connect to the main CPU through a PCI bridge.

The power consumption of high-end MFP systems is significant due to the required top-level processor performance and high-speed interfaces. In order to reduce the power consumption in stand-by mode, the MPC8313E as a secondary I/O processor shuts off the power to the main CPU and maintains the system at very low power. Once the I/O processor detects data transfer through the LAN, USB and PCI or an interrupt from the push of a button on the panel, it quickly boots up the main CPU.

1.2 IEEE Std. 1588™ in Test and Measurement and Industrial Automation

Figure 3 shows how a test and measurement application can use the IEEE Std. 1588™ precise time synchronization.

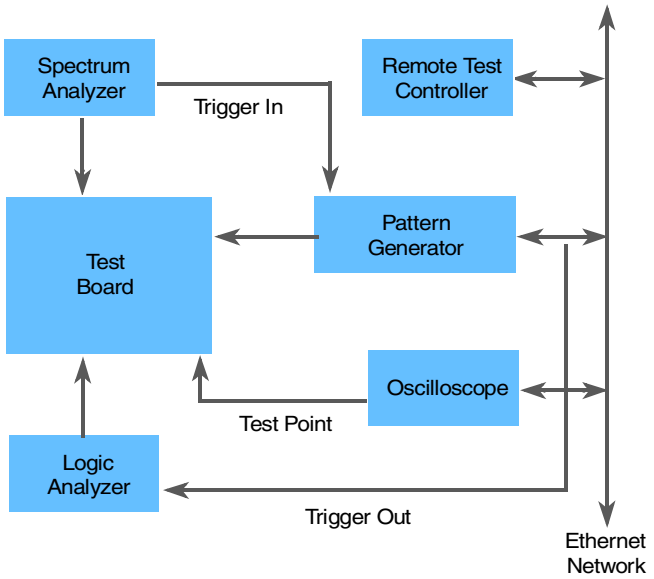

Figure 3. IEEE Std. 1588 in Test and Measurement

In this application, IEEE Std. 1588 allows coordination and control of test and measurement equipment over a distributed Ethernet network. Precise timing delivery allows test equipment to deliver patterns and

measure responses at specific times, enabling accurate timestamping of measured data and allowing coordination of input stimuli and any associated measured data. The trigger inputs and outputs enable coordination of other devices.

Figure 4 illustrates how an industrial control application is able to take advantage of the IEEE Std. 1588 precise time synchronization.

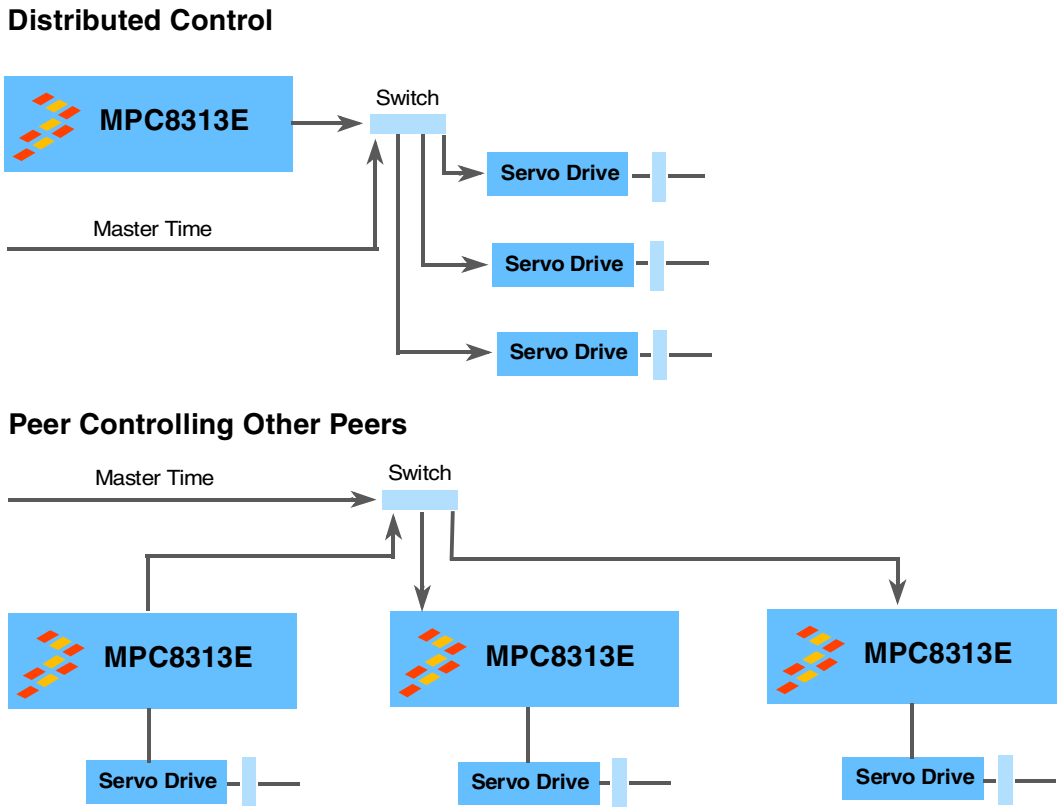

Figure 4. IEEE Std. 1588 in Industrial Control

As shown in the example on the top of the figure, IEEE Std. 1588 allows precision control over a distributed Ethernet network. Precise timing delivery allows drive units to be placed where required. Traditional mechanical control mechanisms can limit the placement of systems.

In the bottom of the figure, timing synchronization at the drive enables flexibility in system configuration. Issues due to mismatched cable lengths are minimized. Servos can be added or deleted without having to rewire other servos. Industrial control applications typically augment IEEE Std. 1588 hardware to provide trigger inputs and outputs

In summary, IEEE Std. 1588 support in the MPC8313E enables accurate synchronization of clocks with varying precision, resolution, and oscillator stability in distributed systems. IEEE Std. 1588 synchronizes individual clocks to maintain accurate distribution-wide timing. It enhances applications that need local clocks at each control node and provides sub-microsecond synchronization over long distances using standard cabling. Target applications for systems with IEEE Std. 1588 are test and measurement appliances and industrial control and automation.

1.3 IEEE Std. 802.11n WLAN Access Point

Figure 5 illustrates the MPC8313E acting as an IEEE Std. 802.11n™ WLAN access point.

Figure 5. MPC8313E as a WLAN Access Point

Current systems are being designed for IEEE Std. 802.11b and 802.11a/g™ as well as combo radios. The WiFi chipsets are on PCI in current systems. With the migration to 802.11n and the increased management features required by the IT community, the need for higher performance is growing.

These WLAN access points (WAPs) require low power and are usually powered exclusively by Power over Ethernet (POE). Each Ethernet line can power about 12 W. With the power the radios draw and the rest of the board this usually only leaves < 2.5 W for the embedded processor.

Integrated SGMII makes it possible to connect to low power Gigabit Ethernet PHYs. Power is a main consideration for WAPs deployed throughout the premise. Power is drawn from the AC outlet in the wall or power over Ethernet. Having an SGMII interface on the Gigabit Ethernet PHYs enables low overall power consumption. The MPC8313E also has superior PCI to memory performance.

1.3.1 Media Server

Figure 6 shows how the MPC8313E can be configured as a media server.

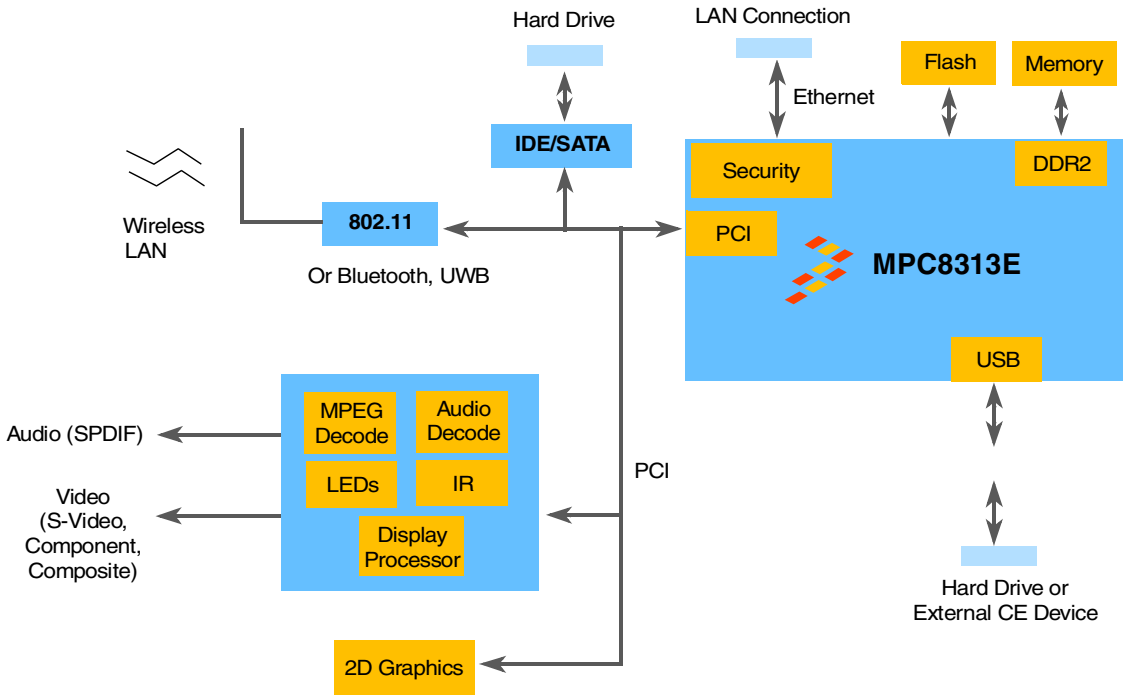

Figure 6. MPC8313E as a Media Server

Multimedia home networking emphasizes both audio and video streaming around the house. Since digital audio takes up relatively little bandwidth, just about any current home network can handle streaming, digital audio. Ultimately, it is video that is the test of a multimedia home network. Whether it's compressed MPEG 2 or MPEG 4 streams, or uncompressed, high-definition video, consumers are likely to demand some type of video streaming on a multimedia network. The trend in the industry will be more focused on providing ASSPs (MPEG processors, image processors, integrated digital TV processors, audio/video decoders).

2 Features

The MPC8313E incorporates the e300c3 core, which includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). In addition to two RGMII/RTBI/MII/RMII Ethernet interfaces, the MPC8313E offers two SGMII interfaces to dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs), a DDR-1/DDR-2 SDRAM memory controller, an enhanced local bus controller (eLBC), a 32-bit PCI-2.3 controller, a dedicated security engine, a USB 2.0 dual-role controller and an on-chip high-speed USB 2.0 PHY, a programmable interrupt controller, dual I^2C controllers, a 4-channel DMA controller, and a general-purpose I/O port.

2.1 Block Diagram

A block diagram of the MPC8313E is shown in Figure 7.

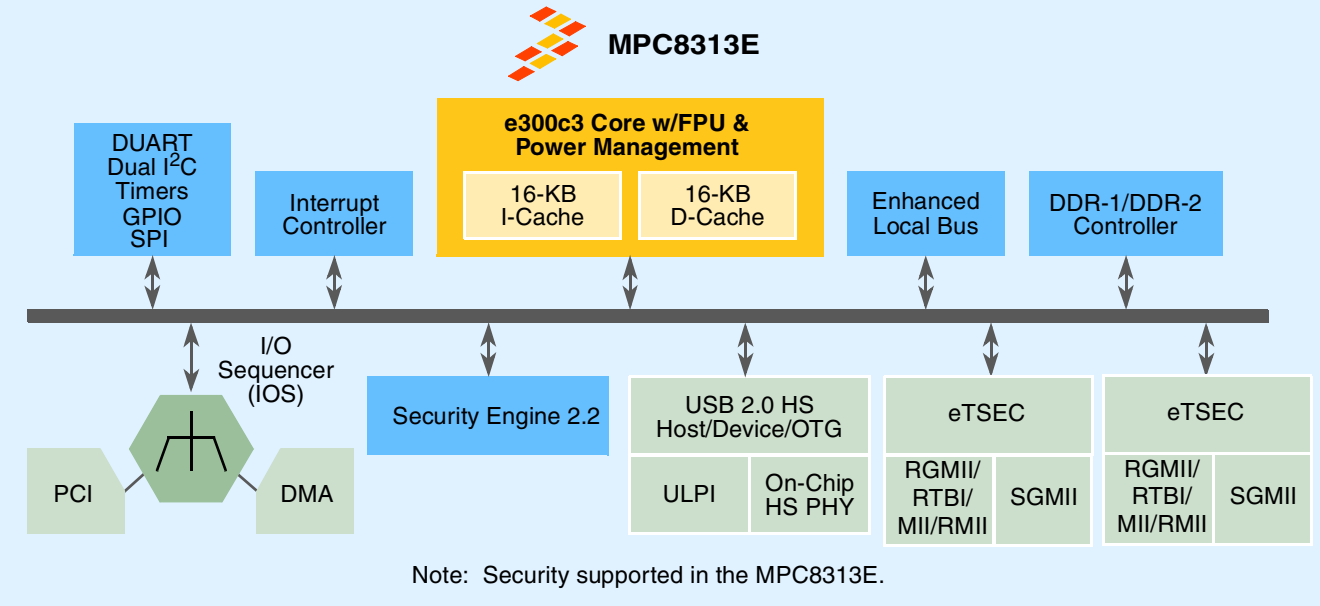

Figure 7. MPC8313E Block Diagram

The MPC8313E's security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for algorithms such as DES, 3DES, AES, SHA-1, and MD-5.

2.2 Critical Performance Parameters

Table 1 shows the clock frequency combinations supported by the MPC8313E. The DDR frequency is divided by two to calculate the CSB frequency. The CSB frequency is divided by the SPMF value to obtain the feedback reference. Note that because of divider restriction on-chip, it is not possible to run the CSB at 167 MHz when the system PLL reference frequency is 66 MHz.

Table 1. Example Clock Frequency Combinations (MHz)

				LBC				e300 Core				
Ref[1]	SPMF[2]	CSB	DDR		/4	/8	USB Ref	×1	×1.5	×2	×2.5	×3
24.0	6	144.0	288.0		36	18.0	12.0	144.0	216	288	360	
24.0	5	120.0	240.0	60	30	15.0	12.0	120.0	180	240	300	360
25.0	6	150.0	300.0		37.5	18.8	Note[3]	150.0	225	300	375	
25.0	5	125.0	250.0	62.5	31.25	15.6	Note 3	125.0	188	250	313	375
32.0	5	160.0	320.0		40	20.0	16.0	160.0	240	320		
32.0	4	128.0	256.0	64	32	16.0	16.0	128.0	192	256	320	384
33.3	5	166.5	333.0		41.625	20.8	Note 3	166.5	250	333		
33.3	4	133.2	266.4	66.6	33.3	16.7	Note 3	133.2	200	266.4	333	
48.0	3	144.0	288.0		36	18.0	48.0	144.0	216	288	360	
66.7	2	133.3	266.7	66.67	33.335	16.7	Note 3	133.3	200	266.7	333	

NOTES:
1 System reference clock (SYS_CLK_IN or PCI_CLK_IN)
2 System PLL multiplication factor between CSB clock and reference clock. Bits 4–7 of the RCWLR.
3 USB reference clock must be supplied from a separate source as it must be 12, 16, or 48 MHz

Note that the minimum frequency for DDR2 is 250 MHz, and the minimum frequency for DDR1 is 167 MHz. The system PLL VCO range is 450–750 MHz. Note also that CSB frequencies less than 133 MHz will not support Gigabit Ethernet rates.

2.3 Chip-Level Features

The following features are supported in the MPC8313E.

- High-performance, low power, and cost-effective host processor
- DDR-1/DDR-2 memory controller—one 16-/32-bit interface at up to 333 MHz
- e300c3 PowerPC core with 16-Kbyte instruction cache and 16-Kbyte data cache, a floating point unit, two integer units, and a performance monitor
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, and USB 2.0 (full/high speed) with an on-chip USB 2.0 PHY.
- Two Ethernet interfaces supporting RGMII, RTBI, MII, RMII, and SGMII.
- Security engine provides acceleration for control and data plane security protocols

- Power management controller for low-power consumption
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

2.4 Module Features

2.4.1 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, 802.11i, and iSCSI. The security engine contains one crypto-channel supporting multi-command descriptor chains, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES
- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm

2.4.2 DDR Memory Controller

The MPC8313E DDR-1/DDR-2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR-1 and DDR-2 SDRAM
- Support for up to 333-MHz data rate
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 1-Gbit devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus OR one 32-bit device or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

2.4.3 PCI Controller

The MPC8313E PCI controller includes the following features:

- PCI specification Revision 2.3 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency
- Support for PCI Power Management 1.2
- Support for PME generation (agent) and wake on PME

2.4.4 USB Dual-Role Controller

The MPC8313E USB controller includes the following features:

- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI (low-pin interface) PHY
- Complies with USB Specification, Rev. 2.0
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports ULPI (low-pin interface with host/device/OTG support) or
- UTMI with on-chip USB-2.0 full-speed/high-speed PHY (with host/device support)

2.4.5 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8313E eTSECs include the following features:

- On-chip high-speed serial interface to external SGMII PHY (MPC8313E-specific)
- Two SGMII interfaces (MPC8313E-specific), two RGMII/RTBI/MII/RMII interfaces
- Two controllers designed to comply with IEEE Stds. 802.3™, 802.3u™, 802.3x™, 802.3z™, 802.3au™, 802.3ab™, and 1588
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode

2.4.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 5 external and 34 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

2.4.7 Power Management Controller (PMC)

The MPC8313 power management controller includes the following features:

- Provides power management when the device is used in both host and agent modes
- Supports PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
- On-chip split power supply controlled through external power switch for minimum standby power
- Support for PME generation in PCI agent mode, PME detection in PCI host mode.

- Supports wake-up from Ethernet (magic packet), USB, GPIO, PCI (PME input as host), internal timer and external interrupt.
- MPC8349E backward-compatible

2.4.8 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8313E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

2.4.9 DMA Controller, Dual I^2C, DUART, Enhanced Local Bus Controller, and Timers

The MPC8313E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters).
- Supports misaligned transfers

There are two I^2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8313E provides an enhanced local bus controller (eLBC) with the following features:

- 26-bit address, 16-bit data multiplexed and non-multiplexed interface
- Four external chip select lines
- Up to 66-MHz operation
- Boot from NAND or NOR flash

The eLBC port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The NAND flash control machine (FCM) provides a glueless interface to parallel-bus NAND flash EEPROM devices. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, FCM, or UPM controller. All may exist in the same system.

The MPC8313E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

3 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support, and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e300c3 PowerPC core.

Freescale also provides an RDB board as a reference platform and programming development environment for the MPC8313E with a complete Linux board support package. The RDB board will support on-board DDR-2 SDRAM memory, Gigabit Ethernet with SGMII support, on-chip USB 2.0 PHY, one PCI interface, NAND flash memory and a debug port.

4 Document Revision History

Table 2 provides a revision history for this product brief.

Table 2. Revision History

Rev. No.	Substantive Change(s)
0	Initial revision

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Document Number: MPC8313EPB
Rev. 0
12/2006