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MCF51JG256 Product Brief

Contents

1 Introduction

1.1 MCF51JG256 Introduction

The MCF51JG256 is a member of the low-cost, low-power, high-performance Version 1 (V1) ColdFire family of 32-bit microcontroller units (MCUs). It uses the enhanced V1 Cold Fire core and is available with a variety of modules and single memory configuration. CPU clock rates on these devices can reach 50 MHz. MCF51JG256 includes 256 KB Flash, 64 KB RAM, USB 1.1 and 2.0 compliant full-speed device/Host controller, hardware encryption support (Cryptographic Acceleration Unit and Random Number Generator) and Serial Audio Interface.

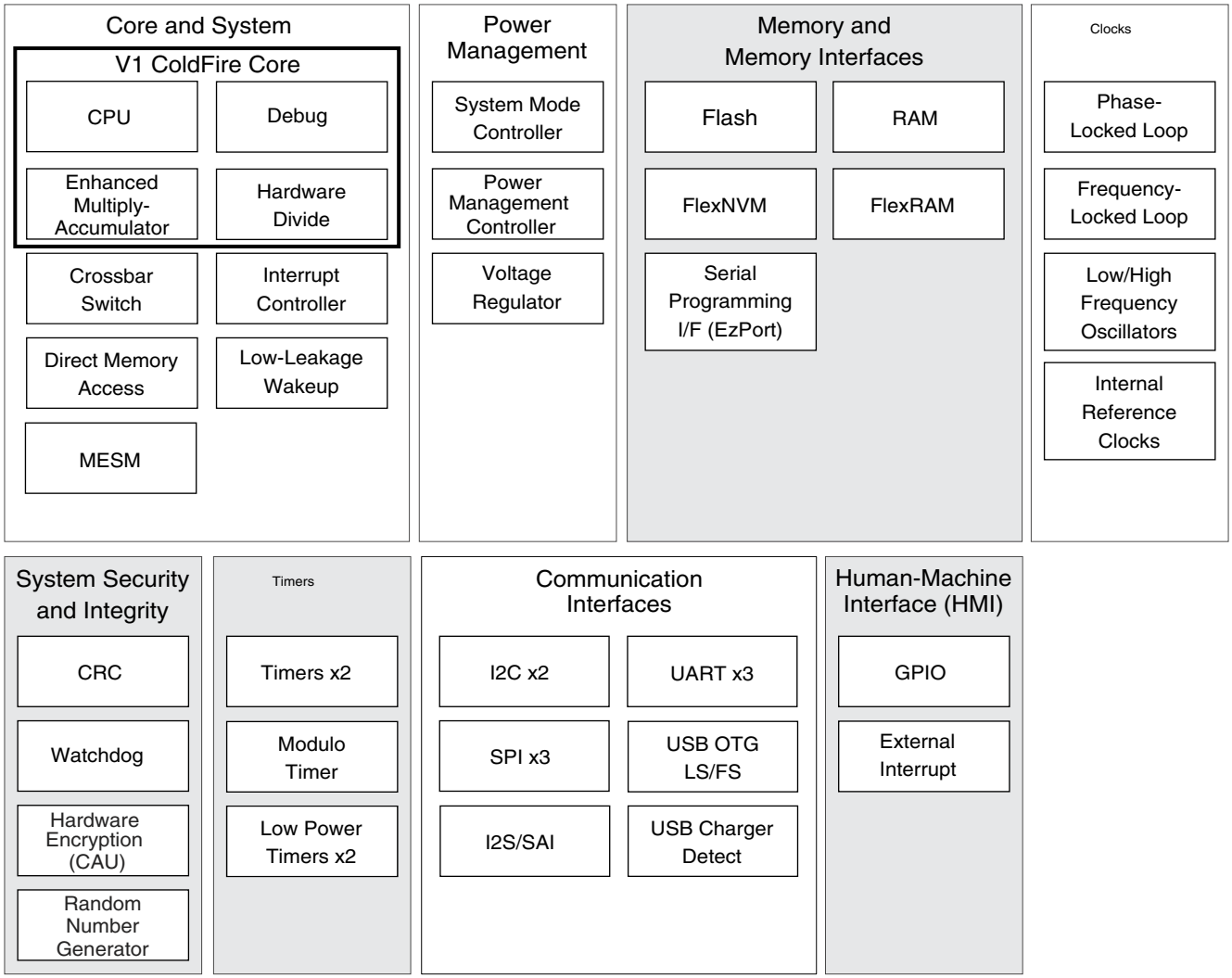

Figure 1. MCF51JG256 block diagram

2 Features

2.1 MCF51JG256 Feature Set

Devices within the entry level families have some or all the following features:

Table 1. MCF51JG256 Feature Set

Operating Characteristics	• Voltage range 1.85 V - 3.6 V • Flash write voltage 1.85 V - 3.6 V • Temperature range (T_A) -40 to 85 °C • Flexible modes of operation

Table continues on the next page...

Table 1. MCF51JG256 Feature Set (continued)

Core features	• Up to 50 MHz Version 1 (V1) ColdFire CPU
	• Provides Dhrystone 2.1 integer performance of:
	  • 1.10 DMIPS per MHz performance when running from internal RAM
	  • 0.99 DMIPS per MHz when running from flash
	• Implements instruction set revision C (ISA_C)
	• Enhanced Multiply Accumulate (EMAC) Unit and Hardware Divide Module

Clocks	• 1 MHz to 32 MHz crystal oscillator
	• 32 kHz crystal oscillator
	• Multi-purpose clock generator
	  • PLL and FLL operation
	  • Internal Reference (32 kHz or 2/4 MHz)
	  • 1 kHz internal LPO clock

System debug, protection and power management features	• Various stop, wait, and run modes to provide lower power based on application needs. • Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents • Low voltage warning and detect with selectable trip points • Illegal opcode and illegal address detection with programmable reset or processor exception response • Hardware CRC module to support fast cyclic redundancy checks (CRC) • Cryptographic Acceleration Unit (CAU) • Random Number Generator Accelerator (RNGA) • 128-bit unique chip identifier • Hardware watchdog
Debug	• Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection • Real-time debug support, with six hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into a 1- or 2-level trigger • Capture of compressed processor status and debug data into on-chip trace buffer provides program (and optional slave bus data) trace capabilities • On-chip trace buffer provides programmable start/stop recording conditions • Debug resources are accessible via single-pin BDM interface or the privileged WDEBUG • EzPort support flash In-System Programming.
DMA Controller	• Four independently programmable channels provide the capabilities to directly transfer data between system memory and I/O peripherals
Timers	• Motor control/general purpose timer (FTM) • 16-bit modulo timer (MTIM) • Low Power Timer for Pulse Counter or periodic interrupt (LPTMR0)
Real Time Clock	• Real Time Clock with Calendaring • 32 kHz operation from internal RC or external 32 kHz clock • Alarm functionality

Table continues on the next page...

Table 1. MCF51JG256 Feature Set (continued)

Communications	• Universal asynchronous receiver/transmitter (UART)/ Serial communications interface (SCI) • Serial peripheral interface (SPI) • Inter-Integrated Circuit (I2C) • USB Full Speed/Low Speed OTG/Host/Device • Serial Audio Interface (SAI) to support Full Duplex Serial Interfaces with Frame Sync I2S, TDM, AC97, CODEC
Input/Output	• 26 GPIO pins with interrupt with selectable polarity • 14 pins with programmable glitch filter • Hysteresis and configurable pull up/down device on all input pins • Configurable slew rate and drive strength on all output pins • Up to 14 rapid general purpose I/O (RGPIO) pins connected to the processor's high speed 32-bit platform bus with faster set, clear, and toggle functionality
NVM Memory/On-Chip RAM	• Flash memory read and write down to 1.85 V • FlexMemory for additional program space or EEPROM • Flash security features and block protection • Nibble parity checking on 64 KB On-chip SRAM • Ability for software to insert single-bit errors to "check the checkers"

2.2 Device Configuration

Table 2. Device Configuration

Device	MCF51JG256
General	
Maximum CPU frequency (MHz)	50
Package	44-pin MAPLGA
Dimensions (mm^2)	5 x 5 mm^2
Core and Platform	
V1 ColdFire core with EMAC and DIV	Yes
DMA	4 ch
EzPort	1
System Security and Integrity	
Cryptographic acceleration unit (CAU)	1
Random number generator accelerator (RNGA)	1
Cyclic redundancy check (CRC)	1
COP watchdog timer	1
Memory and Memory Interfaces	
Total flash memory (KB)	Up to 288
Flash (KB)	256 [Dual 128 KB Swappable Program Flash]

Table continues on the next page...

Table 2. Device Configuration (continued)

Device	MCF51JG256
Flex NVM (KB)	32
Flex RAM (KB)	2
SRAM (KB)	64
Clock Generator	
MCG	PLL, FLL + Internal OSC (32 kHz or 2 MHz)
Real Time Clock (32 kHz OSC)	1
Timer/PWM	
FlexTimer (FTM0) channel pins	2 ch
FlexTimer (FTM1) channel pins	5 ch
16-bit modulo timer (MTIM	1
Low power timer (LPTMR)	1
Communication Interfaces	
UART (SCI)	3
SPI (16-bit)	3
IIC	2
I^2S/SAI	1
USB 2.0 OTG LS/FS[1]	1
USB DCD	1
Human Machine Interface	
Total GPIO pins[2]	26
Pin Interrupts	26
RGPIO	14

1. The 3.3 V voltage regulator on this device powers the on-chip USB transceiver. The regulator input supports the 5 V supply typically provided by USB VBUS power.
2. GPIO count includes RGPIO pins.

2.3 Module-by-module feature list

2.3.1 Core Complex

2.3.1.1 32-bit Version 1 ColdFire Central Processor Unit (CPU)

- Up to 50 MHz Version 1 (V1) ColdFire CPU from 1.85 V to 3.6 V across temperature range of –40 ºC to 85 ºC
- Implements instruction set revision C (ISA_C)
- EMAC plus hardware DIV module
- Implements core microarchitecture:

- Two-stage instruction fetch pipeline (IFP) (plus optional instruction buffer stage)
- Two-stage operand execution pipeline (OEP)

- Provides Dhrystone 2.1 integer performance of:
  - 1.10 DMIPS per MHz performance when running from internal RAM
  - 0.99 DMIPS per MHz when running from flash

2.3.1.2 V1 ColdFire Interrupt Controller (CF1_INTC)

- Interrupt requests organized as a 2-dimensional matrix with 7 levels and multiple priorities within each level
- Support of up to 44 peripheral interrupt requests and seven software (one per level) interrupt requests
- Fixed association between interrupt request source and level plus priority, up to two requests can be remapped to the highest maskable level + priority
- Unique vector number for each interrupt source
- Support for service routine interrupt acknowledge (software IACK) read cycles for improved system performance

2.3.1.3 DMA Controller

- Four independently programmable DMA controller channels provide the capabilities to directly transfer data between system memory and I/O peripherals.
- DMA controller is capable of functioning in run and wait modes of operation.
- Dual-address transfers via 32-bit master connection to the system bus
- Data transfers in 8-, 16-, or 32-bit blocks
- Continuous-mode or cycle-steal transfers from software or peripheral initiation
- One programmable input selected from 16 possible peripheral requests per channel

2.3.1.4 COP - Watchdog Timer

- Independent clock source input (independent from CPU/bus clock)
- Choice between two clock sources:
  - 1 kHz LPO Oscillator
  - Bus clock

2.3.1.5 Random Number Generator Accelerator (RNGA)

- RNGA can be used along with software to attain NIST SP800-90 standards
- National Institute of Standards and Technology (NIST)-approved pseudo-random number generator
  - **csrc.nist.gov**
- Supports the key generation algorithm defined in the Digital Signature Standard
  - **itl.nist.gov/fipspubs/fip186.htm**
- Integrated entropy sources capable of providing the PRNG with entropy for its seed

2.3.1.6 Cryptographic Acceleration Unit (CAU)

- Instruction level coprocessor accessed with ColdFire coprocessor instructions
- Supports acceleration of the following cryptographic algorithms: DES, 3DES, AES {128, 192, 256}, MD5, SHA-1, and SHA-256
- Simple, flexible programming model
- Freescale-provided CAU library of C callable cryptographic functions optimized for performance

2.3.1.7 Debug

- Integrated ColdFire DEBUG_Rev_B+ interface with single wire BDM connection
- Real-time debug support with six hardware breakpoints (4 PC, 1 address pair and 1 data) that can be configured into 1- or 2-level triggers
- Capture of compressed processor status and debug data into on-chip trace buffer provides program (and optional slave bus data) trace capabilities
- On-chip trace buffer provides programmable start/stop recording conditions.
- Debug resources are accessible via single-pin BDM interface or the privileged WDEBUG instruction.

2.3.2 Power management

2.3.2.1 Power Management Controller (PMC)

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable low power modes
- No output supply decoupling capacitors required
- Wake-up from low power modes via internal modules and external inputs
- Integrated Power-on Reset (POR) providing brownout detection in all power modes
- Integrated Low Voltage Detect (LVD) with reset capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz Low Power Oscillator (LPO)

2.3.2.2 Voltage Regulator (VREG)

- 3.3 V regulated output can power MCU main power supply
- Output pin from regulator can power external board components and source up to 120 mA maximum
- Eliminates cost of external LDO
- For devices with integrated USB controller:
  - 5 V regulator input typically provided by USB VBUS power
  - 3.3 V regulated output powers on-chip USB transceiver

2.3.3 Memory

2.3.3.1 On-Chip Memory

- Up to 288 KB flash memory read/program/erase over full operating voltage and temperature
  - Up to 256 KB standard flash array
    - Dual 128 KB program flash space which can be swapped to switch between firmware upgrades
  - Protection scheme prevents accidental program or erase of stored data in 8 KB blocks.
  - 32 KB FlexMemory for additional data/program space or up to 2 KB enhanced EEPROM
  - Program and erase across complete MCU voltage range, 1.85 V to 3.6 V
  - Separate block protection for standard flash array and FlexMemory (including data and enhanced EEPROM)
- Up to 64 KB random access memory (RAM)

- Separate 2 KB RAM associated with enhanced EEPROM can be used as normal RAM if enhanced EEPROM not used
- Supports nibble parity checking on on-chip RAM
  - Mixed [Even/Odd] parity scheme to maximize fault coverage
  - User programmable enable/disable parity check on 8 KB granularity. Does not affect writes to RAM.
  - Parity check disabled on reset and needs to be enabled by startup software
  - Provides faulting address, attributes and a bit field that indicates the specific nibbles with errors as a part of programmable error reporting (interrupt or bus error exception)
  - Programmable mechanism to inject single-bit errors under software control to "check the checkers"
- Security circuitry to prevent unauthorized access to RAM and flash contents

2.3.3.2 Programmable Cyclic Redundancy Check (CRC32)

- Hardware CRC generator circuit using 16-bit or 32-bit (programmable) shift register
- Programmable initial seed value and Polynomial
- Error detection for all single, double, odd, and most multi-bit errors
- Programmable initial seed value
- Optional feature to transpose input data and CRC result via transpose register, required for certain standards
- Final XOR of the output. Some CRCs have final XOR of their CRC checksum with 0xFFFFFFFF or 0xFFFF in their protocol.

2.3.4 System Clocks

- Frequency-locked loop (FLL)
  - Digitally-controlled oscillator (DCO)
  - DCO frequency range is programmable
  - Option to program DCO frequency for a 32,768 Hz external reference clock source
  - Internal or external reference clock can be used to control the FLL.
  - 0.2% resolution using 32 kHz internal reference clock
  - 2% deviation over voltage and temperature range using internal 32 kHz internal reference clock, 1% deviation with limited temperature range (0°C to 70°C)
- Phase-locked loop (PLL)
  - Voltage-controlled oscillator (VCO)
  - External reference clock is used to control the PLL
  - Modulo VCO frequency divider Phase/Frequency detector
  - Integrated loop filter
- Internal reference clock generator
  - Slow clock with nine trim bits for accuracy
  - Fast clock with three trim bits
  - Factory provided trim values for both slow and fast internal reference clocks
  - Can be used to control the FLL
  - Either the slow or the fast clock can be selected as the clock source for the MCU.
  - Can be used as a clock source for other on-chip peripherals
- External clock from the Crystal Oscillator (XOSC)
  - Can be used to control the FLL and/or the PLL
  - Can be selected as the clock source for the MCU
- External clock monitor with reset request capability
- Lock detector with interrupt request capability for use with the PLL
- Auto Trim Machine (ATM) for trimming both the slow and fast internal reference clocks
- Reference dividers for both the FLL and PLL are provided.
- Clock source selected can be divided down by 1, 2, 4, 8 or 16
- MCGPLLSCLK is provided as a clock source from either the FLL or PLL for other on-chip peripherals.
- MCGFFCLK is provided as a clock source for other on-chip peripherals.

2.3.5 Timers

2.3.5.1 FlexTimers (FTM)

- Selectable FTM source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Input capture and output compare modes
- Operation of FTM channels as pairs with equal outputs, pairs with complimentary outputs, or independent channels with independent outputs
- Deadtime insertion is available for each complementary pair.
- Generation of hardware triggers
- Software control of PWM outputs
- Configurable channel polarity
- Programmable interrupt on input capture, reference compare, overflowed counter, or detected fault condition

2.3.5.2 Modulo Timer (MTIM)

- 16-bit up-counter
  - Free-running or 16-bit modulo
  - Software controllable interrupt on overflow
  - Counter reset bit (TRST)
  - Counter stop bit (TSTP)
- Four software selectable clock sources for input to prescaler:
  - System bus clock — rising edge
  - Fixed frequency clock (XCLK) — rising edge
  - External clock source on the TCLK pin — rising edge
  - External clock source on the TCLK pin — falling edge
- Nine selectable clock prescale values:
  - Clock source divided by 1, 2, 4, 8, 16, 32, 64, 128, or 256

2.3.5.3 Low Power Timer (LPTMR)

- Operates as timer or pulse counter
- Selectable clock for prescaler/glitch filter
  - 1 kHz internal LPO
  - External low power crystal oscillator
  - Internal reference clock (not available in low leakage power modes)
- Configurable glitch filter or prescaler with 15-bit counter
- Interrupt generated on timer compare
- Hardware trigger generated on timer compare (not available in low leakage power modes)

2.3.5.4 Real-Time Clock (RTC)

- Independent Power Supply, POR and 32 kHz Crystal Oscillator
- 32-bit Seconds Counter with 32-bit Alarm
- 16-bit Prescaler with Compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register Write Protection

  - Hard Lock requires SRTC POR to enable write access.
  - Soft Lock requires System Reset to enable write/read access.
- Chip Configuration Register

2.3.6 Communication interfaces

2.3.6.1 USB On-the-Go Controller

- USB 1.1 and 2.0 compliant full-speed device/Host controller
- On-the-Go protocol logic
- 16 bidirectional endpoints
- DMA or FIFO data stream interfaces
- Low-power consumption

2.3.6.2 USB Device Charge Detect (DCD)

- Compliant with the latest industry standard specification, USB Battery Charging Specification, Revision 1.1
- Compatible with systems powered from:
  - Rechargeable battery
  - Nonrechargeable battery
  - External 3.3 V LDO regulator powered from USB or directly from USB using internal regulator
- Programmable event timers for flexibility and better compatibility with future udpates to the standards
- Minimal configuration required:
  - Set the clock frequency and enable the module
  - Preprogrammed default values ensure compatibility with the USB Battery Charging Specification, Revision 1.1

2.3.6.3 Inter-IC Sound (I2S) / Synchronous Audio Interface (SAI)

- Support for full-duplex serial interfaces with frame synchronization such as I^2S, AC97, and CODEC/DSP interfaces
- Two independent bit clock / frame sync pairs
- Four software configurable transmit or receive channels that can be software allocated to any bit clock / frame sync pair
- Independent 16 word x 32-bit FIFO per channel
- Graceful restart after FIFO Error
- Operation in stop modes

2.3.6.4 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Programmable 8- or 16-bit data transmission length
- Receive data buffer hardware match feature
- 64-bit FIFO mode for high speed/large amounts of data transfers (SPI0 only)
- Support transfer of both transmit and receive data by DMA

2.3.6.5 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard and SMBus version 2 features
- Up to 100 kbit/s with maximum bus loading
- Multi-master operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt driven or DMA support for byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when processor is in low power modes

2.3.6.6 Serial Communication Interface (SCI)

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths (SCI0 only)
- 13-bit baud rate selection with fractional divide of 32
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity
- Programmable receive input polarity
- 13-bit break character option
- 11-bit break character detection option
- Parameterizable buffer support for one dataword for each transmit and receive
- Independent FIFO structure for transmit and receive(only SCI0)
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be first bit on wire
- Hardware flow control support for request to send (RTS) and clear to send (CTS) signals
- Interrupt-driven operation with 11 flags:
  - Transmitter data buffer at or below watermark
  - Transmission complete
  - Receiver data buffer at or above watermark
  - Idle receiver input
  - Receiver overrun
  - Receiver data buffer underflow
  - Noise error
  - Framing error
  - Parity error
  - Active edge on receive pin
  - LIN Break detect
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection
- 5 channel DMA requests

2.3.7 Human-machine interface

2.3.7.1 Enhanced General Purpose Input/Output (EGPIO)

- 26 eGPIO pins (PTA, PTB, PTC and PTD)
- Progammable glitch filter and interrupt with selectable polarity on two GPIO Ports (14 pins)
- Hysteresis and configurable pull up/down device on all input pins
- Configurable slew rate and drive strength on all output pins
- Independent pin value register to read logic level on digital pin

2.3.7.2 Rapid General Purpose Input/Output (RGPIO)

- 14 bits of high-speed GPIO functionality connected to the processor's high-speed 32-bit bus
- Memory-mapped device
  - Support for all access sizes: byte, word, and longword
  - All reads and writes complete in a single data phase cycle for zero wait-state response
- Data bits can be accessed directly or via alternate addresses to provide set, clear, and toggle functions.
  - Alternate addresses allow set, clear, toggle functions using simple store operations without the need for read-modify-write references.

- Unique data direction and pin enable control registers
- Package pin toggle rates typically 1.5–3.5x faster than comparable GPIO pin mapped onto peripheral bus

3 Family Pin-Out

3.1 Signal Multiplexing and Pin Assignments

44 MAPLGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	EZPORT
1	VDD	VDD	VDD						
2	VREGIN	VREGIN	VREGIN						
3	VOUT33	VOUT33	VOUT33						
4	USB_DM	USB_DM	USB_DM						
5	USB_DP	USB_DP	USB_DP						
6	BKGD/ MS/ PTD4	BKGD/ MS	Disabled	PTD4	BKGD	MS			
7	EXTAL32	EXTAL32	EXTAL32						
8	XTAL32	XTAL32	XTAL32						
9	PTA1/ FTM1_CH0/ IIC1_SCL/ RGPIO1	Disabled	Disabled	PTA1	FTM1_CH0		IIC1_SCL	RGPIO1	

44 MAPLGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	EZPORT
10	PTA2/ FTM1_CH1/ IIC1_SDA/ RGPIO2	Disabled	Disabled	PTA2	FTM1_CH1		IIC1_SDA	RGPIO2	
11	VDD	VDD	VDD						
12	VSS	VSS	VSS						
13	PTA3/ FTM1_CH2/ CLKOUT/ SAI0_RX_BCLK/ RGPIO3	Disabled	Disabled	PTA3	FTM1_CH2	CLKOUT	SAI0_RX_BCLK	RGPIO3	
14	PTA5/ SCI2_CTS_b/ FTM1_CH4/ SAI0_RXD/ RGPIO5	Disabled	Disabled	PTA5	SCI2_CTS_b	FTM1_CH4	SAI0_RXD	RGPIO5	
15	PTA6/ SAI0_RX_FS/ RGPIO6/ EZP_DO	Disabled	Disabled	PTA6			SAI0_RX_FS	RGPIO6	EZP_DO
16	PTA7/ LPT_ALT0/ RGPIO7/ EZP_DI	Disabled	Disabled	PTA7	LPT_ALT0			RGPIO7	EZP_DI
17	PTB0/ RGPIO8/ EZP_CLK	Disabled	Disabled	PTB0				RGPIO8	EZP_CLK
18	IRQ0/ PTB1/ EZP_MS_b/ RGPIO9/ EZP_CS_b	IRQ0	IRQ0	PTB1	EZP_MS_b			RGPIO9	EZP_CS_b
19	PTB2/ SCI0_RTS_b/ FTM0_CH1/ IIC0_SCL/ RGPIO10	Disabled	Disabled	PTB2	SCI0_RTS_b	FTM0_CH1	IIC0_SCL	RGPIO10	
20	PTB3/ SCI0_CTS_b/ FTM0_CH0/ IIC0_SDA/ RGPIO11	Disabled	Disabled	PTB3	SCI0_CTS_b	FTM0_CH0	IIC0_SDA	RGPIO11	
21	PTB4/ SCI2_TX/ SPI2_MOSI/ RGPIO12	Disabled	Disabled	PTB4	SCI2_TX	SPI2_MOSI		RGPIO12	
22	VSS	VSS	VSS						
23	VDD	VDD	VDD						
24	PTB5/ SCI2_RX/	Disabled	Disabled	PTB5	SCI2_RX	SPI2_MISO		RGPIO13	

44 MAPLGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	EZPORT
	SPI2_MISO/ RGPIO13								
25	PTB6/ SPI2_CLK/ RGPIO14	Disabled	Disabled	PTB6		SPI2_CLK		RGPIO14	
26	PTB7/ SCI1_TX/ SPI1_MOSI/ RGPIO15	Disabled	Disabled	PTB7	SCI1_TX	SPI1_MOSI		RGPIO15	
27	PTC0/ SPI2_SS/ USBCLKIN	Disabled	Disabled	PTC0		SPI2_SS		USBCLKIN	
28	IRQ3/ PTC1/ FTM1_CH5/ CLKOUT	IRQ3	IRQ3	PTC1	FTM1_CH5	CLKOUT			
29	PTC2/ SCI1_RX/ SPI1_MISO	Disabled	Disabled	PTC2	SCI1_RX	SPI1_MISO			
30	PTC3/ SPI1_CLK/	Disabled	Disabled	PTC3		SPI1_CLK			
31	IRQ1/ PTC4/ SCI1_RTS_b	IRQ1	IRQ1	PTC4	SCI1_RTS_b				
32	IRQ2/ PTC5/ SCI1_CTS_b/ TMR_CLKIN0	IRQ2	IRQ2	PTC5	SCI1_CTS_b	TMR_CLKIN0			
33	VDD	VDD	VDD						
34	VSS	VSS	VSS						
35	ENABLE_USB_ REG	ENABLE_USB_ REG	ENABLE_USB_ REG						
36	RESET_B	RESET_B	RESET_B						
37	EXTAL	EXTAL	EXTAL						
38	XTAL	XTAL	XTAL						
39	PTC7/ SPI1_SS	Disabled	Disabled	PTC7		SPI1_SS			
40	PTD0/ SPI0_SS/ SAI0_TX_FS	Disabled	Disabled	PTD0	SPI0_SS		SAI0_TX_FS		
41	PTD1/ SCI0_TX/ SPI0_MOSI/ SAI0_TXD	Disabled	Disabled	PTD1	SCI0_TX	SPI0_MOSI	SAI0_TXD		
42	PTD2/ SCI0_RX/ SPI0_MISO/ SAI0_TX_BCLK	Disabled	Disabled	PTD2	SCI0_RX	SPI0_MISO	SAI0_TX_BCLK		

44 MAPLGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	EZPORT
43	PTD3/ SPI0_CLK/ SAI0_MCLK/ SAI0_CLKIN	Disabled	Disabled	PTD3		SPI0_CLK	SAI0_MCLK/ SAI0_CLKIN		
44	VSS	VSS	VSS						

3.2 Pinout Diagram

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin.

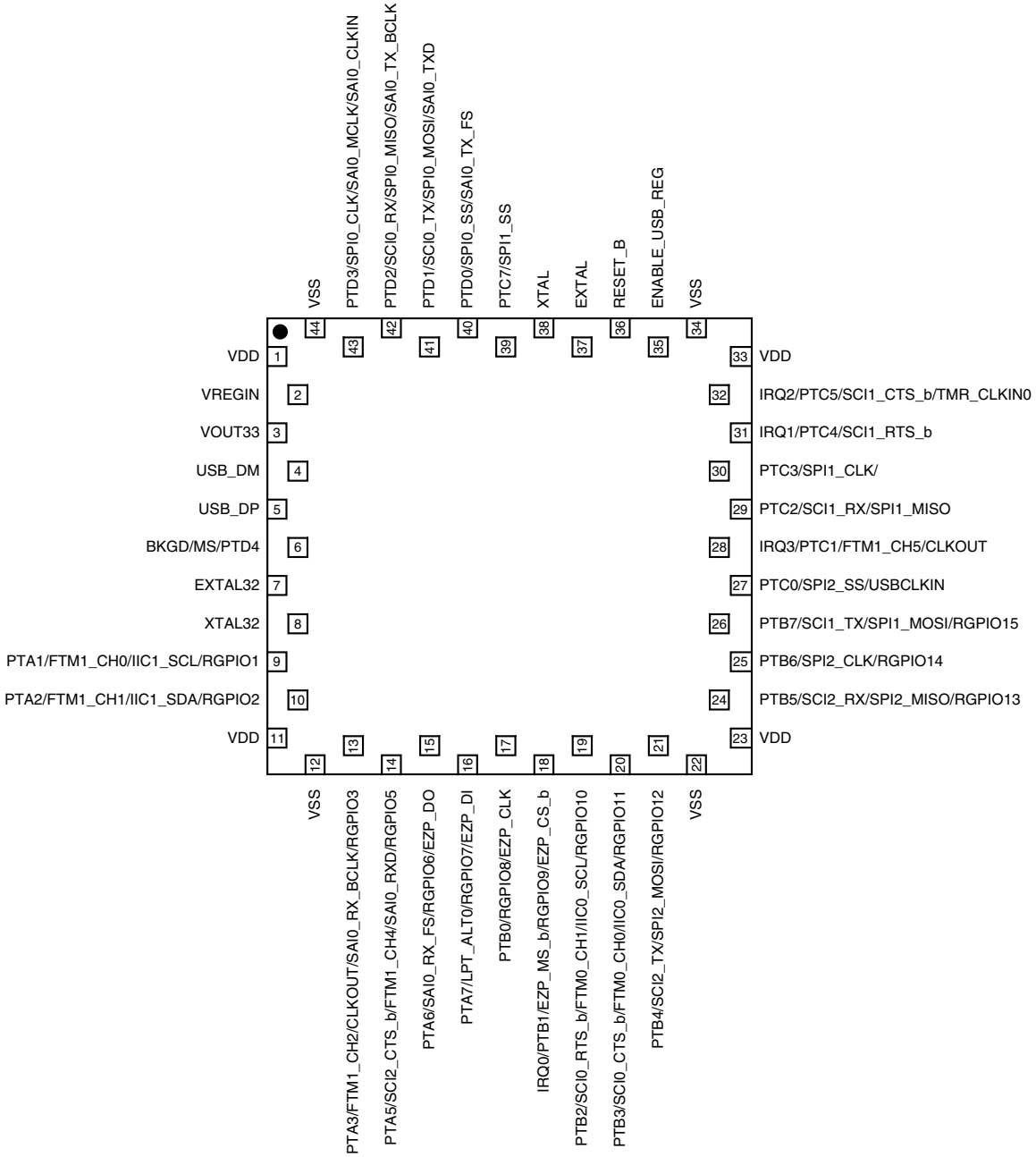

Figure 2. MCF51JG256 44-pin MAPLGA Pinout Diagram

NOTE

PTD4 is adjacent to EXTAL32 and may inject coupling noise on EXTAL32 when both PTD4 as well as EXTAL32 is being used. So it is highly recommended that PTD4 be only used for the cases where EXTAL32 is not used at all and system relies on internal RC clock or external EXTAL clock.

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