S12XHZ512PB
Rev. 4.1, 4-Jan-2007

MC9S12XHZ512

Also covers MC9S12XHZ384 and MC9S12XHZ256

16-bit S12X Microcontroller with LCD and Stepper Motor Drivers

Introduction

Targeted at automotive instrumentation applications, the MC9S12XHZ512 microcontroller unit (MCU) is a fully pin-compatible extension to the existing MC9S12HZ-Family of microcontrollers. It offers not only a larger memory than the existing S12-based family but also incorporates all the architectural benefits of the new S12X-based family to deliver significantly higher performance. The MC9S12XHZ512 retains the low cost, power consumption, EMC and code-size efficiency advantages currently associated with the MC9S12HZ-Family products.

Based around S12X core, the MC9S12XHZ512 runs 16-bit wide accesses without wait states for all peripherals and memories. The MC9S12XHZ512 also features a new flexible interrupt handler, which allows multilevel nested interrupts.

The MC9S12XHZ512 features the performance boosting XGATE co-processor. The XGATE is programmable in “C” language and runs at twice the bus frequency of the S12. Its instruction set is optimized for data movement, logic and bit manipulation instructions. Any peripheral module can be serviced by the XGATE.

The MC9S12XHZ512 contains 512K bytes of Freescale Semiconductor’s industry leading, full automotive qualified Split-Gate Flash memory, with 4K bytes of additional integrated data EEPROM and 32K bytes of static RAM.

freescale semiconductor

The MC9S12XHZ512 features a 32x4 liquid crystal display (LCD) controller/driver and a motor pulse width modulator (MC) consisting of up to 24 high current outputs suited to drive six stepper motors with stall detectors (SSD) to simultaneously calibrate the pointer reset position of each motor. It also features two MSCAN modules, each with a FIFO receiver buffer arrangement, and input filters optimized for Gateway applications handling numerous message identifiers.

In addition, the MC9S12XHZ512 is composed of standard on-chip peripherals including two asynchronous serial communications interfaces (SCI0 and SCI1), one serial peripheral interface (SPI), two IIC-bus interface (IIC0 and IIC1), an 8-channel 16-bit enhanced capture timer (ECT), a 16-channel, 10-bit analog-to-digital converter (ADC), and one 8-channel pulse width modulator (PWM).

The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. The new fast-exit from STOP mode feature can further improve system power consumption. In addition to the I/O ports available in each module, 8 general purpose I/O ports are available with interrupt capability allowing wake-up from STOP or WAIT mode.

The MC9S12XHZ512 is available in 112-pin LQFP and 144-pin LQFP packages. The 144-pin LQFP package option provides a full 16-bit wide non-multiplexed external bus interface.

Features

Features of the MC9S12XHZ512 are listed here. Please see Table 1 for the features that are available on the different family members.

16-Bit CPU12X	• Upward compatible with MC9S12 instruction set • Enhanced indexed addressing • Additional (superset) instructions to improve 32-bit calculations and semaphore handling • Access large data segments independent of PPAGE
Enhanced Interrupt Module	• Eight levels of nested interrupt • Flexible assignment of interrupt sources to each interrupt level • One non-maskable high priority interrupt (XIRQ) • Wakeup interrupt inputs (IRQ and XIRQ)
XGATE	• Programmable, high performance I/O co-processor - up to 80 MIPS RISC performance • Transfers data to or from all peripherals and RAM without CPU intervention or CPU wait states • Performs simple logical, shifts, arithmetic, and bit operations on data • Enables FullCAN capability when used in conjunction with MSCAN • Full LIN master or slave capability when used in conjunction with SCI. • Triggers from any hardware module as well as from the CPU

Memory Options	• 512K, 384K, 256K byte FLASH – Erase sector size 1024 bytes – Automated program and erase algorithm – Fast sector erase and word program operation – 2-stage command pipeline for faster multi-word program times – Sector erase abort feature for critical interrupt response – Protection scheme to prevent accidental program or erase – Security option to prevent unauthorized access – Code integrity check using built-in data compression – Sense-amp margin level setting for reads • 4K byte EEPROM – Small erase sector 4 bytes – Automated program and erase algorithm – Fast sector erase and word program operation – 2-stage command pipeline for faster multi-word program times – Sector erase abort feature for critical interrupt response – Protection scheme to prevent accidental program or erase • 32K, 28K, 16K byte RAM
Oscillator (OSC_LCP)	• Loop Control Pierce oscillator utilizing a 0.5Mhz to 16Mhz crystal • Option for full-swing Pierce without internal feedback resistor utilizing a 0.5Mhz to 40Mhz crystal • Current gain control on amplitude output – Signal with low harmonic distortion – Low power – Good noise immunity – Eliminates need for external current limiting resistor • Transconductance sized for optimum start-up margin for typical crystals • Clock monitor
Clock and Reset Generator (CRG)	• Phase-locked-loop clock frequency multiplier – Reference divider – Automatic bandwidth control mode for low-jitter operation – Automatic frequency lock detector • Fast wake up from STOP in self clock mode for power saving and immediate program execution • Computer Operating Properly (COP) watchdog with optional safety window to initialize time-out counter • Real Time Interrupt for task scheduling purposes or cyclic wake-up from low power modes • System reset generation

Liquid Crystal Display (LCD)	• 32 frontplanes and 4 backplanes • 5 modes of operation allow for different display sizes to meet application requirements • Programmable frame clock generator and bias voltage level
Motor Controller (MC)	• 24 high current drivers suited for PWM motor control • Each PWM channel switchable between two drivers in an H-bridge configuration • Support for sine and cosine drive • 11-bit resolution with selectable dithering function • Left, right or center aligned outputs • Slew rate control
Stepper Stall Detector (SSD0, SSD1, SSD2, SSD3, SSD4, SSD5)	• Flexible full step and polarity set up to return the pointer to its reset position in clockwise or counter clockwise direction. • Integrator/Sigma Delta converter circuit to measure the induced voltage by the back EMF of non-powered coil during full step (only one of the two motor coils is powered) operation. • 16-Bit Down Counter to monitor blanking and integration time to support stepper motors with different gear ratios. • 16-Bit accumulator register to read integration value, compare to a threshold at the end of integration time, and decide if the motor is stalled under this value or moving above this value.
Analog-to-Digital Converter (ADC)	• 8-bit or 10-bit resolution • Multiplexer for 16 analog input channels • 7μs, 10-bit single conversion time • Programmable sample time • Left/right, signed/unsigned result data • Continuous conversion mode • Multiple channel scans • External and internal conversion trigger capability
Enhanced Capture Timer (ECT)	• Eight 16-bit channels for input capture or output compare • One 16-bit free-running counter with 8-bit precision prescaler • One 16-bit modulus down counter with 8-bit precision prescaler • Four 8-bit or two 16-bit pulse accumulators • Four channels have enhanced input capture capabilities: – Delay counter for noise immunity – 16-bit capture buffer – 8-bit pulse accumulator buffer

Periodic Interrupt Timer (PIT)	• Four channel x 24-bit modulus down-count timers – Timeout interrupt – Timeout peripheral trigger • Start of timers can be aligned
Pulse Width Modulator (PWM)	• Eight 8-bit or four 16-bit independent channels • Programmable period and duty cycle per channel • Center-aligned or left-aligned outputs • Programmable clock select and with a wide frequency range
Multi-scalable Controller Area Networks (MSCAN0, MSCAN1)	• CAN 2.0 A, B software compatible – Standard and extended data frames – 0 - 8 bytes data length – Programmable bit rate up to 1 Mbps • Five receive buffers with FIFO storage scheme • Three transmit buffers with internal prioritization • Flexible identifier acceptance filter programmable as: – 2 x 32-bit – 4 x 16-bit – 8 x 8-bit • Wake-up with integrated low pass filter option • Loop back for self test • Listen-only mode to monitor CAN bus • Bus-off recovery by software intervention or automatically • 16-bit time stamp of transmitted/received messages • FullCAN capability when used in conjuntion with XGATE
Serial Communication Interfaces (SCI0, SCI1)	• Full-duplex or single wire operation • Standard mark/space non-return-to-zero (NRZ) format • Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths • 13-bit baud rate selection • Programmable character length • Programmable polarity for transmitter and receiver • Receive wakeup on active edge • Break detect and transmit collision detect supporting LIN

Serial Peripheral Interface (SPI)	• Full-duplex or single-wire bidirectional • Double-buffered transmit and receive • Master or Slave mode • MSB-first or LSB-first shifting • Serial clock phase and polarity options
Inter-IC Bus (IIC0, IIC1)	• Compatible with I2C Bus standard • Supports 400 kbps • Multi-master operation • Software programmable for one of 256 different serial clock frequencies • Software selectable acknowledge bit • Interrupt driven byte-by-byte data transfer • Arbitration lost interrupt with automatic switch from master to slave mode • 7-bit or 10-bit calling address identication interrupt • Bus busy detection • Supports General Call address
Background Debug (BDM)	• Background debug controller (BDC) with single-wire interface – Non-intrusive memory access commands – Supports in-circuit programming of on-chip non-volatile memory – Supports security
Debugger (XDBG)	• Four comparators A, B, C and D – Each can monitor CPU or XGATE busses – A and C compares 23-bit address bus and 16-bit data bus with mask register – B and D compares 23-bit address bus only – Three modes: simple address/data match, inside address range or outside address range • 64 x 64-bit circular trace buffer to capture change-of-flow addresses or address and data of every access • Tag-type or force-type hardware breakpoint requests
System Protection	• Power-on reset (POR) • Illegal opcode and illegal address detection with reset • Low-voltage detection with interrupt or reset

Input/Output	• 115 general-purpose input/output (I/O) pins and 2 input-only pins • Hysteresis and configurable pull up/pull down device on all input pins • Configurable drive strength on all output pins • Eight interrupt pins with digital filtering and rising or falling edge trigger
Package Options	• 144-pin low-profile quad flat-pack (LQFP) • 112-pin low-profile quad flat-pack (LQFP)
Operating Conditions	• Ambient temperature range –40 to 125°C • Temperature options: – –40 to 85°C – –40 to 105°C – –40 to 125°C • Supply voltage 4.5 to 5.5 V • 40 MHz maximum CPU bus frequency in single chip mode • 80 Mhz maximum XGATE bus frequency

Table 1 Options of MC9S12XHZ-Family

Device	Package	Flash	RAM	EEPROM	XGATE	CAN	SCI	SPI	IIC	A/D	ECT	LCD	PWM	Motor	SSD	KWU	EBI	I/O
9S12XHZ512	144 LQFP	512K	32K	4K	yes	2	2	1	2	16	8	32x4	8	24/6	6	8	Yes	117
	112 LQFP												6	16/4	4		No	85
9S12XHZ384	144 LQFP	384K	28K	4K	yes	2	2	1	2	16	8	32x4	8	24/6	6	8	Yes	117
	112 LQFP												6	16/4	4		No	85
9S12XHZ256	144 LQFP	256K	16K	4K	yes	2	2	1	2	16	8	32x4	8	24/6	6	8	Yes	117
	112 LQFP												6	16/4	4		No	85

- **Pin out explanations:**
  - A/D is the number of A/D channels.
  - PWM is the number of PWM channels.
  - ECT is the number of ECT channels.
  - LCD denotes the number of front planes times the number of back planes.
  - Motor denotes the number of high current drive pins / number of stepper motors which can be driven
  - SSD denotes whether this device features a Stepper Stall Detection Circuit
  - Versions with one SCI will use SCI0
  - Versions with one CAN will use CAN0
  - Versions with one IIC will use IIC0
  - I/O is the sum of ports capable to act as digital input or output.

Block Diagram

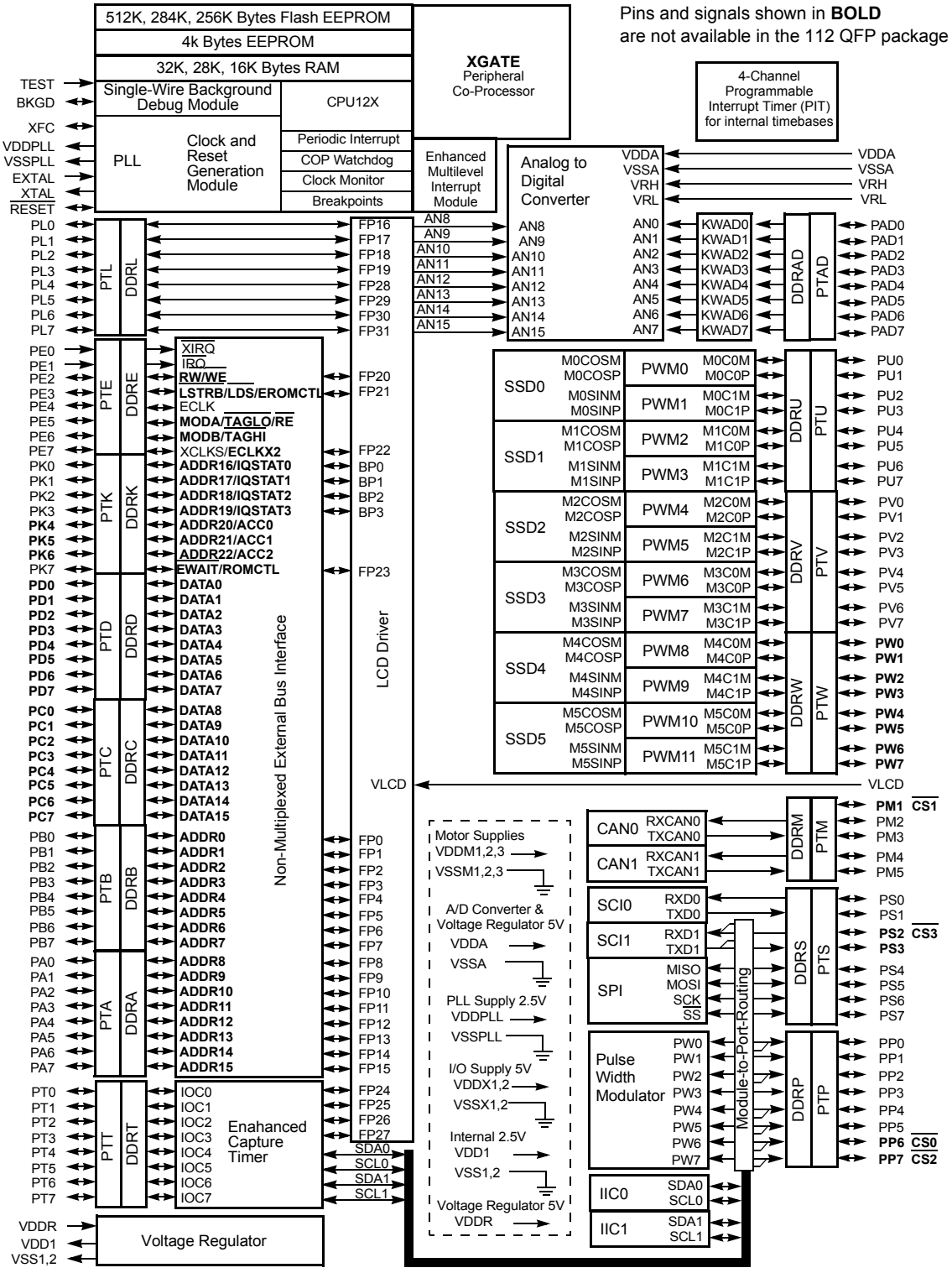


Figure 1. MC9S12XHZ512 Block Diagram

Pin Assignments

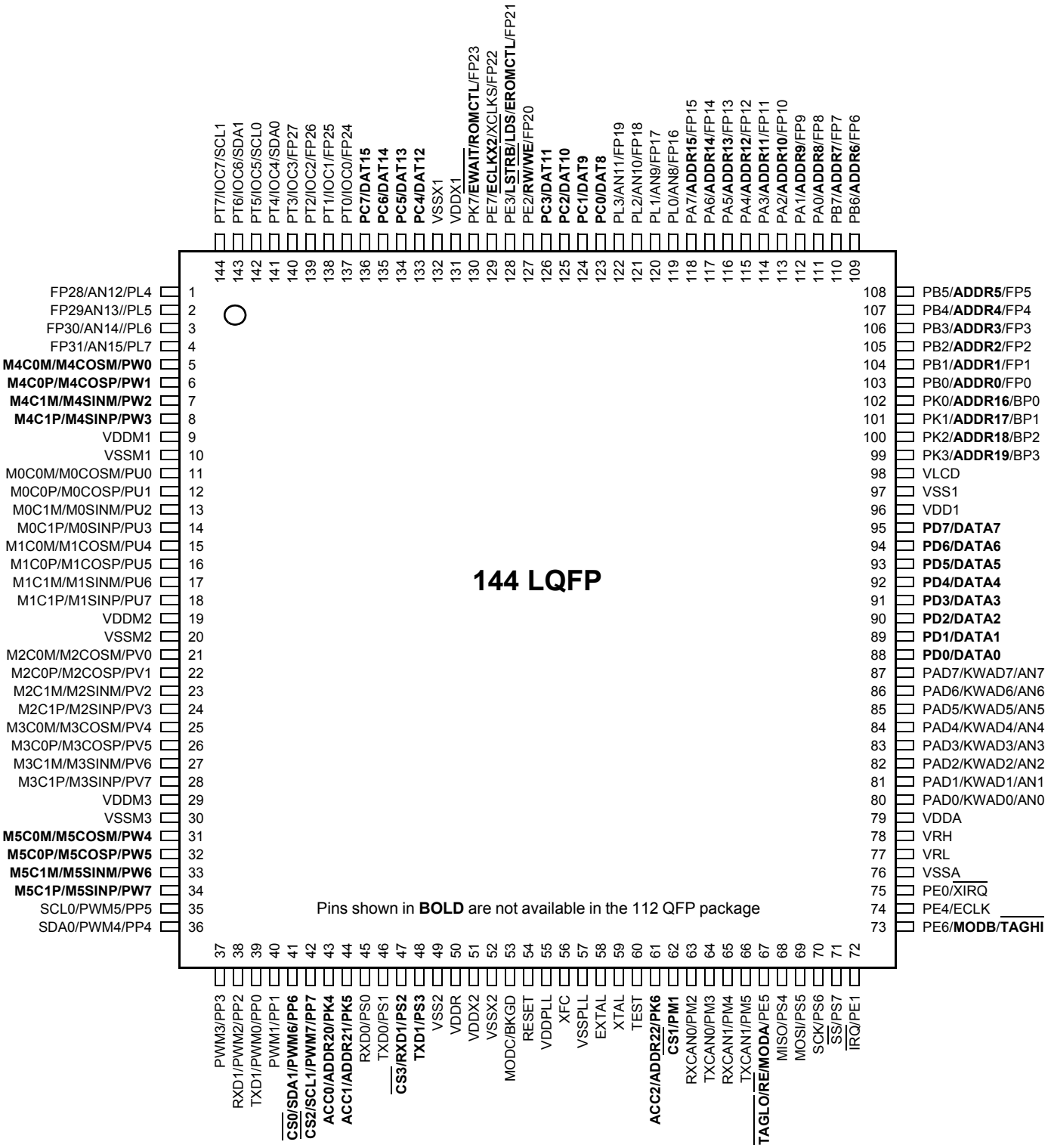


Figure 2. 144-Pin Package Signal Assignments

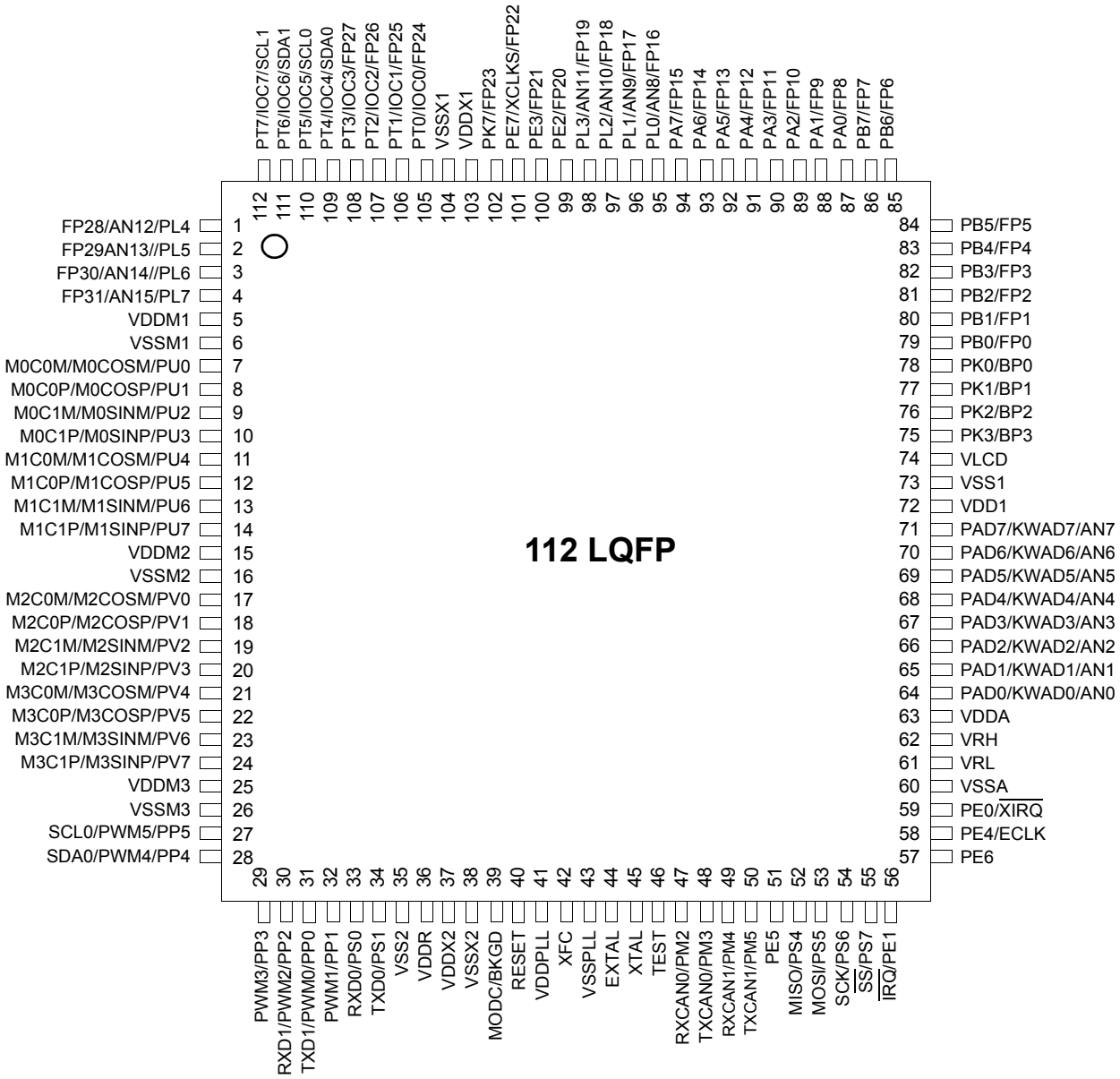


Figure 3. 112-Pin Package Signal Assignments

Table 2. Port and Peripheral Availability by Package Option

Port	144 LQFP	112 LQFP
Port AD pins	8	8
Port A pins	8	8
Port B pins	8	8
Port C pins	8	0
Port D pins	8	0
Port E pins incl. IRQ/XIRQ input only	8	8
Port K pins	5	5
Port L pins	8	8
Port M pins	8	4
Port P pins	8	6
Port S pins	8	6
Port T pins	8	8
Port U pins	8	8
Port V pins	8	8
Port W pins	8	0
Sum of Ports	**117**	**85**

Table 3. Peripheral–Port Cross Reference[1]

	CAN0	CAN1	SCI0	SCI1	SPI	IIC0	IIC1
PM3:2	X						
PM5:4		X					
PS1:0			X				
PP0,PP2				X			
PP5:4						X	
PP7:6							X
PS3:2				O			
PS7:4					X		
PT5:4						O	
PT7:6							O

NOTES:
1. X denotes the reset condition and O denotes a possible rerouting under software control

Memory Maps

Figure 4 shows the CPU & BDM local address translation to the global memory map. It indicates also the location of the internal resources in the memory map.

Table 4 Device Internal Resources

Device	RAMSIZE / RAM_LOW	EEPROMSIZE / EEPROM_LOW	FLASHSIZE0 / FLASH_LOW	FLASHSIZE1 / FLASH_HIGH
MC9S12XHZ512	32K / 0x0F_8000	4K / 0x13_F000	256K / 0x7B_FFFF	256K / 0x7C_0000
MC9S12XHZ384	28K / 0x0F_9000	4K / 0x13_F000	128K / 0x79_FFFF	256K / 0x7C_0000
MC9S12XHZ256	16K / 0x0F_C000	4K / 0x13_F000	128K / 0x79_FFFF	128K / 0x7E_0000

Figure 5 shows XGATE local address translation to the global memory map. It indicates also the location of used internal resources in the memory map.

Table 5 XGATE Resources

Device	XGRAMSIZE / XGRAM_LOW	XGFLASHSIZE / XGFLASH_HIGH
MC9S12XHZ512	32K / 0x0F_8000	30K / 0x78_7FFF
MC9S12XHZ384	28K / 0x0F_9000	
MC9S12XHZ256	16K / 0x0F_C000	

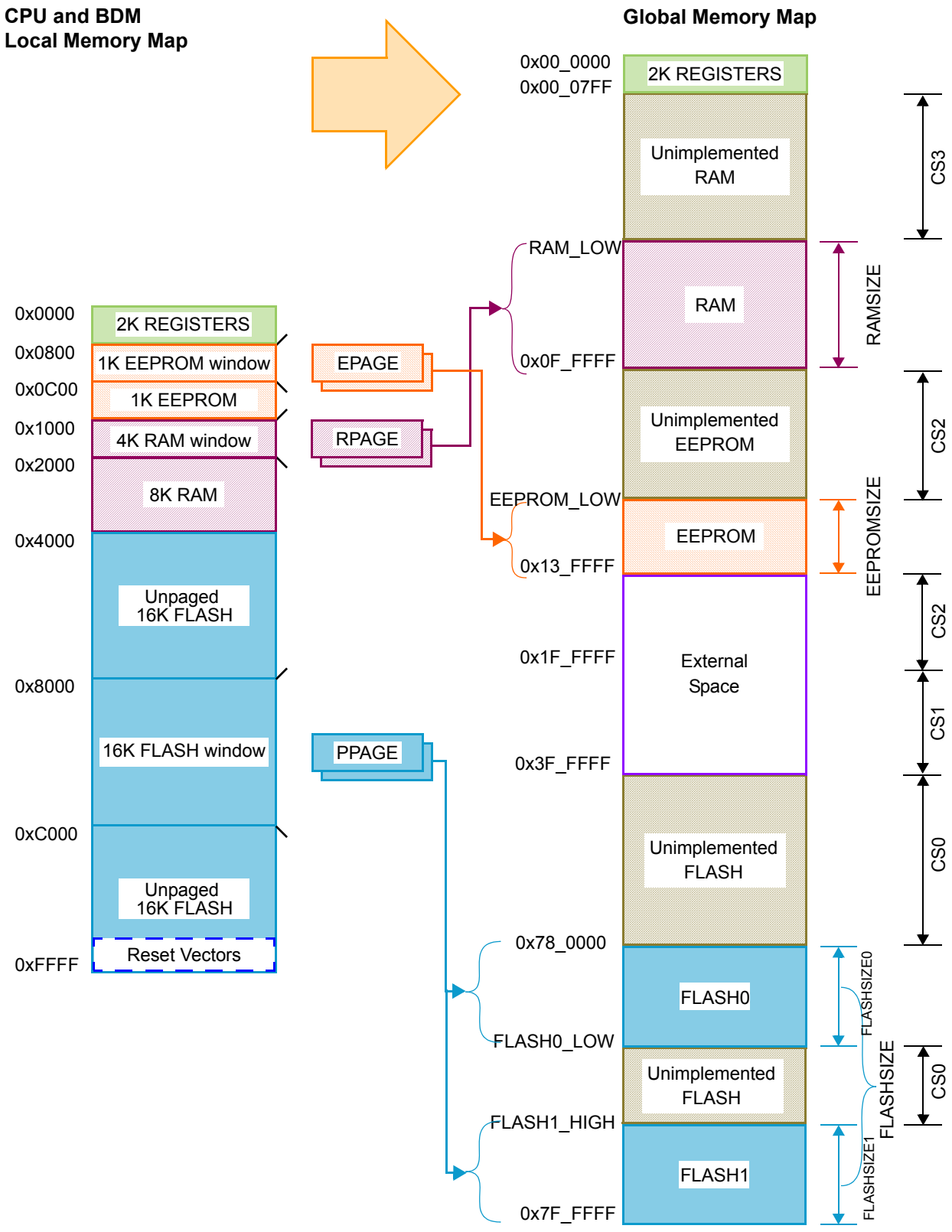


Figure 4. S12X CPU & BDM Global Address Mapping

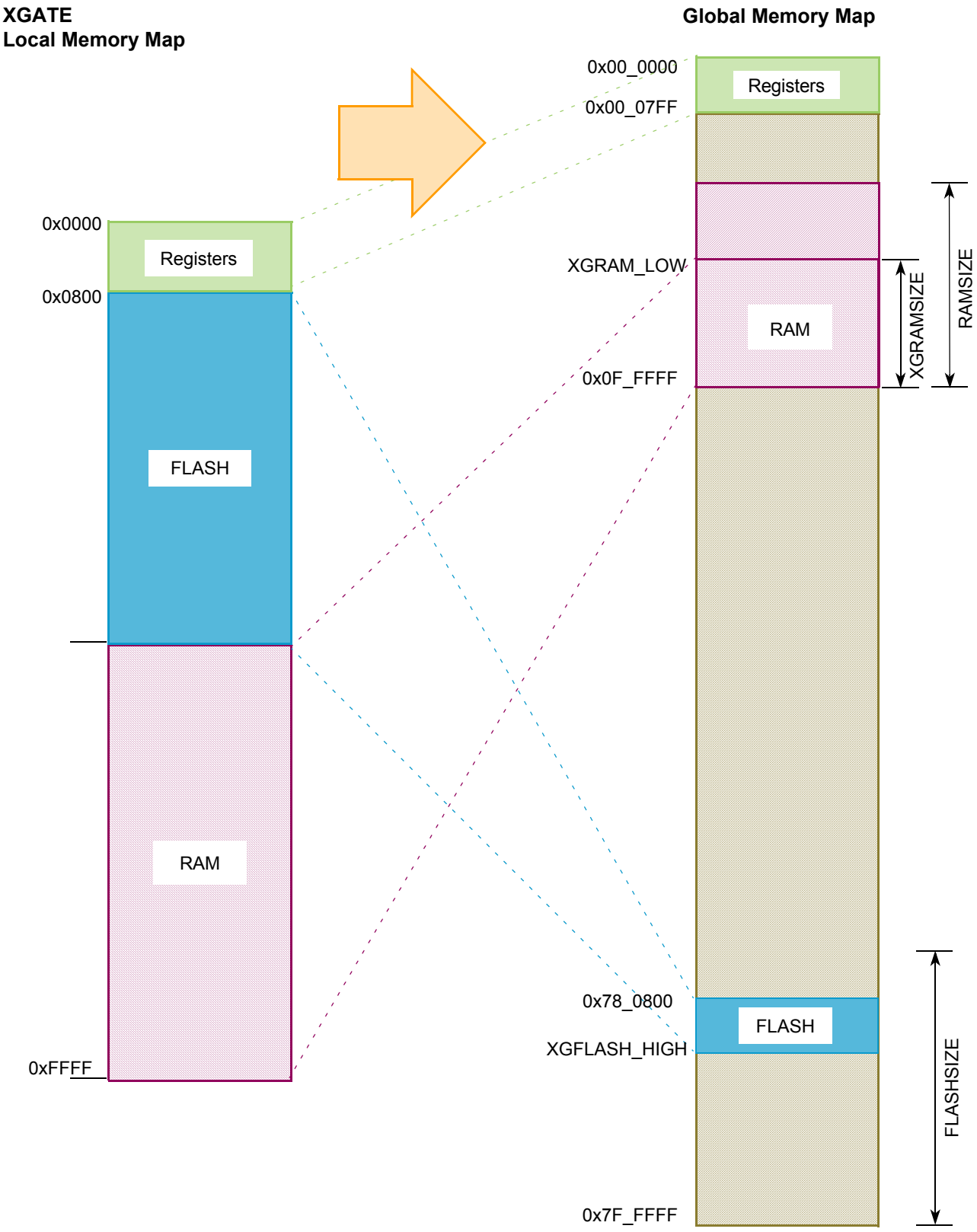
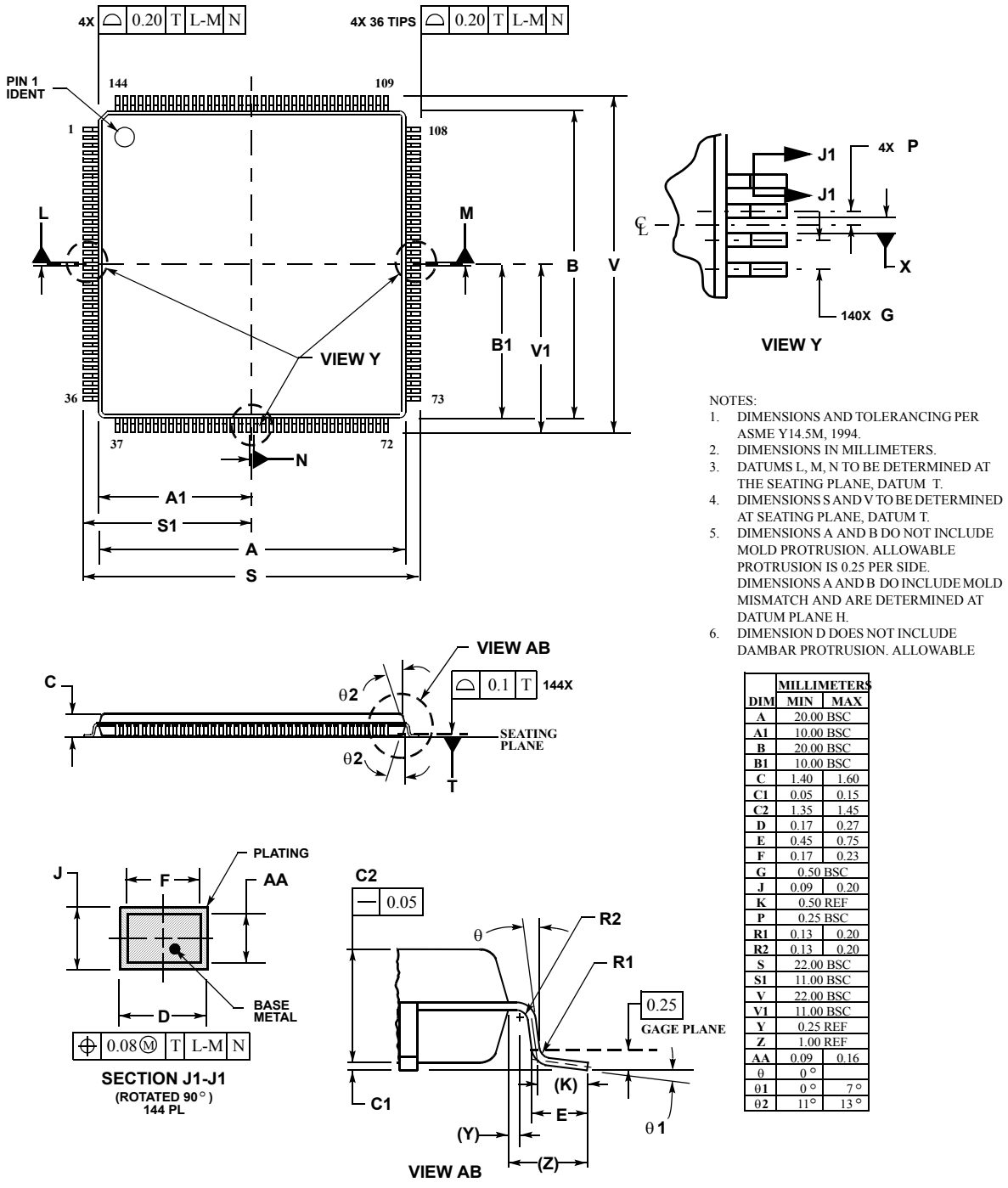


Figure 5. XGATE Global Address Mapping

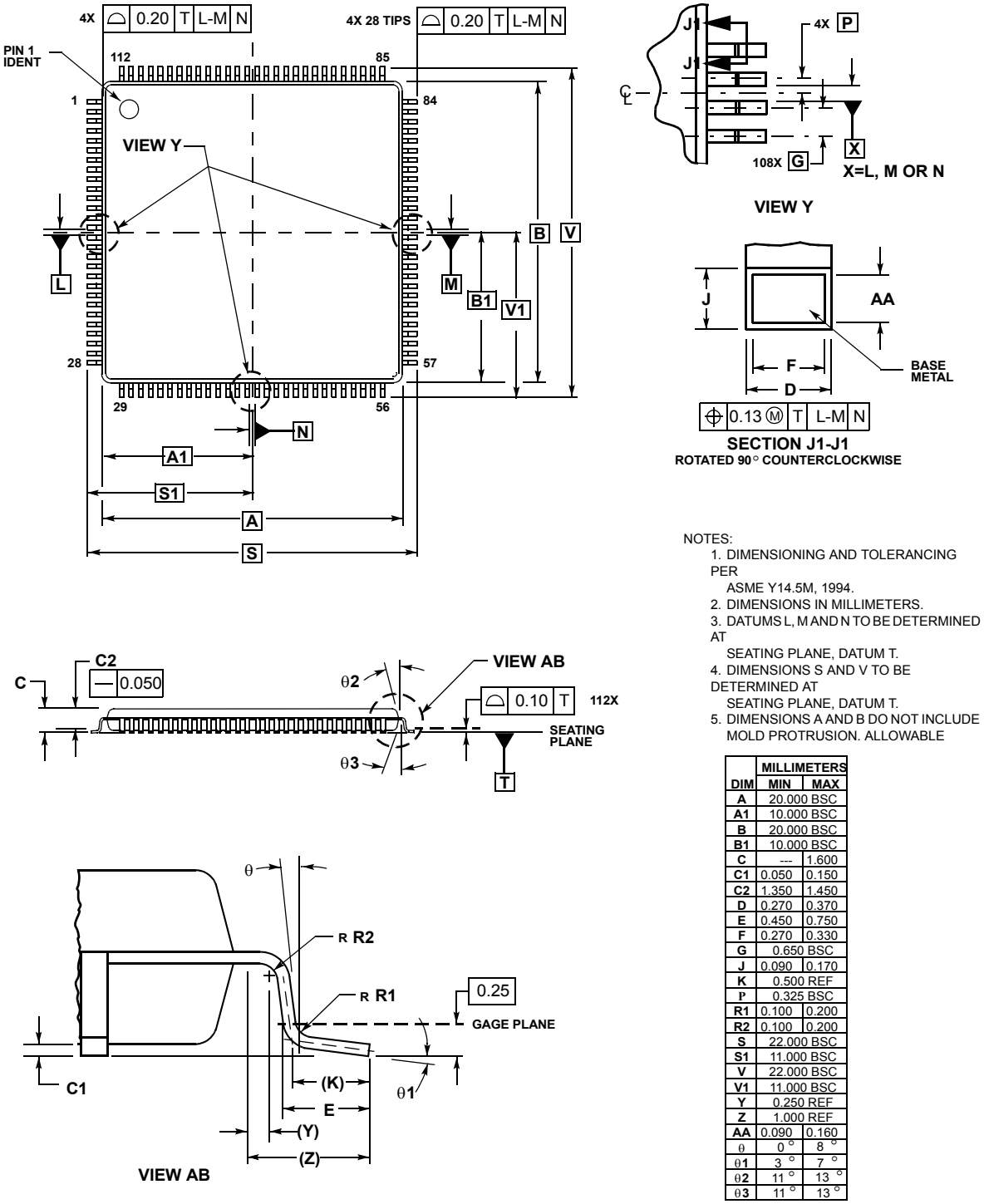
Mechanical Package Dimensions



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M, N TO BE DETERMINED AT THE SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE

	MILLIMETERS	
DIM	MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	
θ1	0°	7°
θ2	11°	13°

Figure 6. 144-pin LQFP Mechanical Dimensions (case no. 918-03)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 7. 112-pin LQFP Mechanical Dimensions (case no. 987)

How to Reach Us:

USA/Europe/Locations not listed:
Freescale Semiconductor Literature Distribution
P.O. Box 5405, Denver, Colorado 80217
1-800-521-6274 or 480-768-2130

Japan:
Freescale Semiconductor Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu
Minato-ku
Tokyo 106-8573, Japan
81-3-3440-3569

Asia/Pacific:
Freescale Semiconductor H.K. Ltd.
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T. Hong Kong
852-26668334

Learn More:
For more information about Freescale Semiconductor products, please visit
http://www.freescale.com

S12XHZ512PB
Rev. 4.1, 4-Jan-2007

freescale™
semiconductor