MC9S12XB Family

16-bit Microcontroller Family (covers MC9S12XB128 through MC9S12XB256)

1 Introduction

Targeted at general automotive body applications, the MC9S12XB-Family is a fully compatible subset of the popular MC9S12XD-Family. Relative to the MC9S12XD-Family, it has some functionality removed and its speed reduced in order to deliver a significant cost saving. Like the MC9S12XD-Family, the MC9S12XB-Family is designed to retain the low cost, low power consumption, excellent EMC performance, and code-size efficiency advantages associated with all 16-bit MCUs from Freescale.

The MC9S12XB-Family features the performance boosting XGATE co-processor. The XGATE, which is programmable in “C” language, has an instruction set optimized for data movement, logic, and bit manipulation instructions. It runs at twice the bus frequency of the S12X and off-loads the CPU by providing high speed data transfer (and data processing) between any peripheral module, RAM, and I/O ports.

Memory options are 128 Kbytes or 256 Kbytes of Freescale's industry-leading, full automotive spec Split-Gate-Flash with additional integrated EEPROM.

The MC9S12XB-Family has full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. System power consumption is further improved with the new “fast exit from STOP mode” feature and an ultra low power wakeup timer.

In addition to the I/O ports available in each module, up to 20 further I/O ports are available with interrupt capability allowing wakeup from STOP or WAIT mode.

The MC9S12XB-Family will be available in 112-pin LQFP, and 80-pin QFP package options and will run at 33 MHz bus speed.

2 Features

NOTE

Not all features listed here are available in all configurations.

Features of the MC9S12XB-Family are listed here. See Table 1 for memory options and Table 2 for the peripheral features that are available on the different family members.

16-bit CPU12X	• Upward compatible with MC9S12 instruction set • Enhanced index register operation • Additional (superset) instructions to improve 32-bit calculations and semaphore handling • Access large data segments independent of PPAGE
Enhanced Interrupt Module	• Eight levels of nested interrupt • Flexible assignment of interrupt sources to each interrupt level. • One non-maskable high priority interrupt (XIRQ) • Wakeup interrupt inputs — IRQ and non-maskable XIRQ
XGATE	• Programmable, high performance I/O co-processor module — up to 66 MIPS RISC performance • Transfers data to or from all peripherals and RAM without CPU intervention or CPU wait states • Performs logical, shifts, arithmetic, and bit operations on data • Enables FullCAN capability when used in conjunction with MSCAN module • Full LIN master or slave capability when used in conjunction with the two integrated LIN SCI modules • Can interrupt the HCS12X CPU signalling transfer completion • Triggers from any hardware module, as well as from the CPU, are possible

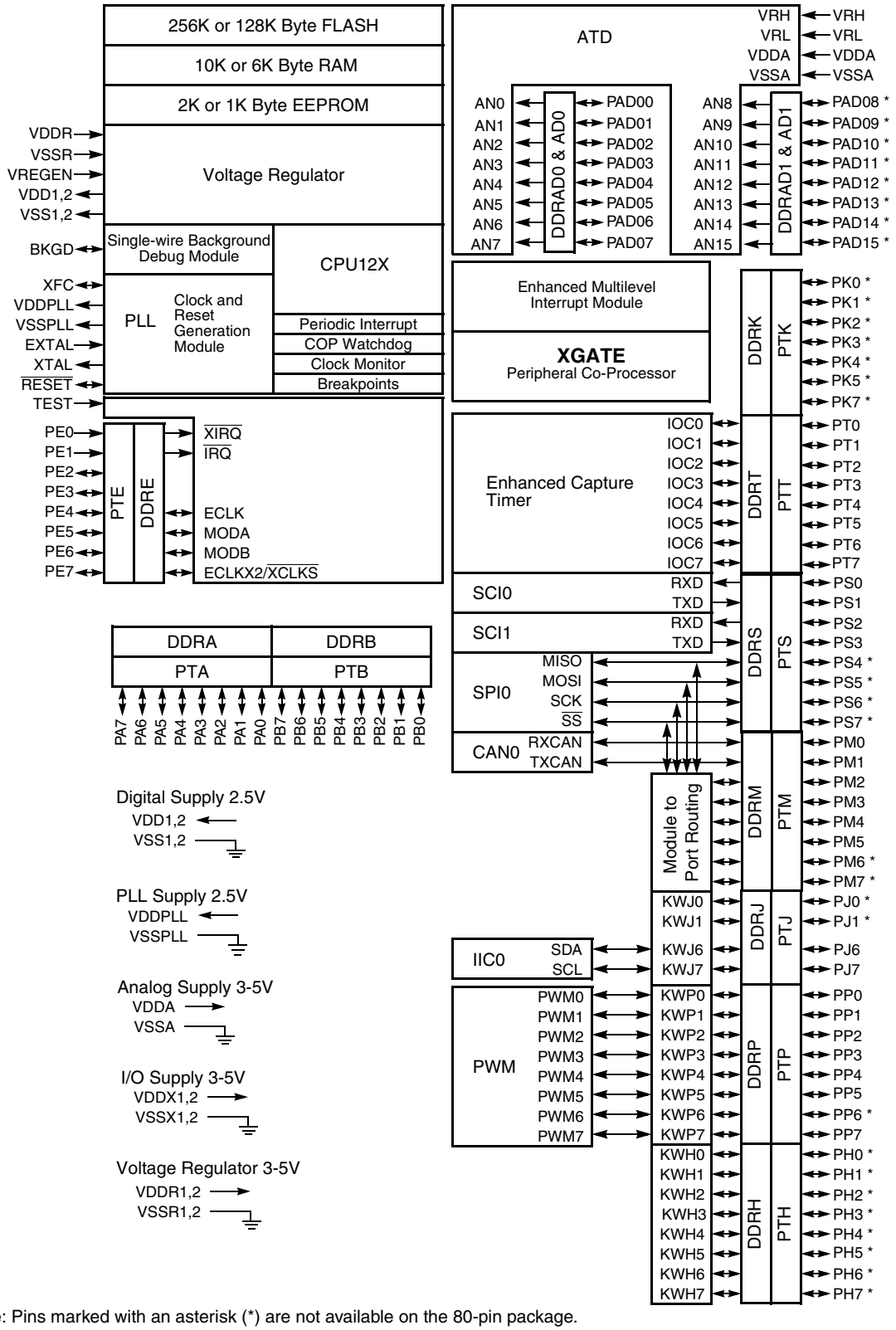
Memory Options	• 128K or 256K byte Flash • Flash General Features — Erase sector size 1024 bytes — Automated program and erase algorithm — Fast sector erase and word program operation — Two-stage command pipeline for faster multi-word program times — Sector erase abort feature for critical interrupt response — Protection scheme to prevent accidental program or erase — Security option to prevent unauthorized access — Code integrity check using built-in data compression — Sense-amp margin level setting for reads • 1K or 2K byte EEPROM — Small erase sector (four bytes) — Automated program and erase algorithm — Fast sector erase and word program operation — Two-stage command pipeline for faster multi-word program times — Sector erase abort feature for critical interrupt response — Protection scheme to prevent accidental program or erase • 6K or 10K byte RAM
Oscillator (OSC_LCP)	• Loop control Pierce oscillator using a 4 MHz to 16 MHz crystal • Option for full-swing Pierce without internal feedback resistor using a 2 MHz to 40 MHz crystal • Current gain control on amplitude output — Signal with low harmonic distortion — Low power — Good noise immunity — Eliminates the requirement for external current limiting resistor • Transconductance sized for optimum start-up margin for typical crystals • Clock monitor

Clock and Reset Generator (CRG)	• Phase-locked-loop clock frequency multiplier — Reference divider — Automatic bandwidth control mode for low-jitter operation — Automatic frequency lock detector • Fast wakeup from STOP in self-clock mode for power saving and immediate program execution • Computer operating properly (COP) watchdog with optional safety window to initialize timeout counter • Real-time interrupt for task scheduling, or cyclic wakeup from low power modes • System reset generation
Analog-to-Digital Converter (ATD)	• Sixteen channels for 112-pin package, eight channels for 80-pin package. (see Table 2) • 8-bit or 10-bit resolution • Multiplexer for sixteen analog input channels • 7 µs, 10-bit single conversion time • Programmable sample time • Left/right, signed/unsigned result data • Continuous conversion mode • Multiple channel scans • External and internal conversion trigger capability • Pins can also be used as digital I/O
Enhanced Capture Timer (ECT)	• Eight 16-bit channels for input capture or output compare • One 16-bit free-running counter with 8-bit precision prescaler • One 16-bit modulus down counter with 8-bit precision prescaler • Four 8-bit or two 16-bit pulse accumulators • Four channels have enhanced input capture capabilities: — Delay counter for noise immunity — 16-bit capture buffer — 8-bit pulse accumulator buffer
Pulse Width Modulator (PWM)	• 8-channel x 8-bit or 4-channel x 16-bit pulse width modulator • Programmable period and duty cycle per channel • Center-aligned or left-aligned outputs • Programmable clock select logic with a wide range of frequencies

Multi-scalable Controller Area Networks (MSCAN)	• CAN 2.0 A, B software compatible — Standard and extended data frames — 0–8 bytes data length — Programmable bit rate up to 1 Mbps • Five receive buffers with FIFO storage scheme • Three transmit buffers with internal prioritization • Flexible identifier acceptance filter programmable as: — 2 x 32-bit — 4 x 16-bit — 8 x 8-bit • Wakeup with integrated low-pass filter option • Loop-back for self test • Listen-only mode to monitor CAN bus • Bus-off recovery by software intervention or automatically • 16-bit time stamp of transmitted/received messages • FullCAN capability when used in conjunction with XGATE
Serial Peripheral Interface (SPI)	• Full-duplex or single-wire bidirectional • Double-buffered transmit and receive • Master or slave mode • MSB-first or LSB-first shifting • Serial clock phase and polarity options
Serial Communication Interfaces (SCI)	• Two SCI modules • Full-duplex or single wire operation • Standard mark/space non-return-to-zero (NRZ) format • Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths • 13-bit baud rate selection • Programmable character length • Programmable polarity for transmitter and receiver • Receive wakeup on active edge • Break detect and transmit collision detect supporting LIN

Inter IC Module (IIC)	• Compatible with I2C Bus standard • Multi-master operation • Software programmable for one of 256 serial clock frequencies • Software selectable acknowledge bit • Interrupt driven byte-by-byte data transfer • Arbitration lost interrupt with automatic mode switching from master to slave • Calling address identification interrupt • Start and stop signal generation/detection • Repeated start signal generation • Acknowledge bit generation/detection • Bus busy detection • supports 400 kbps
Background Debug (BDM)	• Background debug controller (BDM) with single-wire interface — Non-intrusive memory access commands — Supports in-circuit programming of on-chip non-volatile memory — Supports security
Debug Module (XDBG)	• Four comparators A, B, C and D: — Each can monitor CPU or XGATE buses — A and C compare 23-bit address bus and 16-bit data bus with mask register — B and D compare 23-bit address bus only — Three modes: – simple address/data match, – inside address range – outside address range • 64 x 64-bit circular trace buffer to capture change-of-flow addresses or address and data of every access • Tag-type or force-type hardware breakpoint requests
System Protection	• Power-on reset (POR) • Illegal address Detection with reset • Low-Voltage Detection with interrupt or reset

Input/Output	• Up to 91 general purpose input/output (I/O) pins, depending on the package option, and two input-only pins • Hysteresis and configurable pullup/pulldown device on all input pins • Configurable drive strength on all output pins
Package Options	• 112-pin low-profile quad flat-pack (LQFP) • 80-pin quad flat-pack (QFP)
Operating Conditions	• Ambient temperature range -40°C to 125°C • Temperature options: — -40°C to 85°C — -40°C to 105°C — -40°C to 125°C • Supply voltage 3.15V to 5.5V • Internal voltage regulator providing 2.5 V logic supply — 33 MHz maximum CPU bus frequency in single chip mode — 66 MHz maximum XGATE bus frequency



Note: Pins marked with an asterisk (*) are not available on the 80-pin package.

Figure 1. MC9S12XB Family Block Diagram

Table 1. Package and Memory Options of MC9S12XB-Family Members

Device	Package	Flash	RAM	EEPROM
9S12XB256	112LQFP	256K	10K	2K
	80QFP			
9S12XB128	112LQFP	128K	6K	1K
	80QFP			

Table 2. Peripheral Options of MC9S12XB-Family Members

Device	Flash	RAM	EEPROM	Package	XGATE	CAN	SCI	SPI	IIC	ECT	A/D	I/O
9S12XB256	256k	10k	2k	112LQFP	yes	1	2	1	1	8	1/16	91
				80QFP		1	2	1	1	8	1/8	59
9S12XB128	128k	6k	1k	112LQFP		1	2	1	1	8	1/16	91
				80QFP		1	2	1	1	8	1/8	59

Pinout Explanations

- A/D is the number of modules/total number of A/D channels.
- I/O is the number of ports capable of acting as digital inputs or outputs:
  - 112-pin Packages:
    Port A = 8, B = 8, E = 6 + 2 input only, H = 8, J = 4, K = 7, M = 8, P = 8, S = 8, T = 8, PAD = 16
    22 inputs provide interrupt capability (H =8, P= 8, J = 4, IRQ, XIRQ)
  - 80-pin Packages:
    Port A = 8, B = 8, E = 6 + 2 input only, J = 2, M = 6, P = 7, S = 4, T = 8, PAD = 8
    11 inputs provide interrupt capability (P= 7, J = 2, IRQ, XIRQ)
- CAN0 can be routed under software control from PM[1:0].
- SPI0 can be routed to pins PS[7:4] or PM[5:2].

3 Pin Assignments

Table 3. Port and Peripheral Availability by Package Option

Port	112LQFP	80QFP
Port AD/ADC Channels	16/16	8/8
Port A pins	8	8
Port B pins	8	8
Port E pins including IRQ and XIRQ (input only)	8	8
Port H pins	8	0
Port J pins	4	2
Port K pins	7	0
Port M pins	8	6
Port P pins	8	7
Port S pins	8	4
Port T pins	8	8
Total Number of Ports	**91**	**59**
VDDX/VSSX	3/3	2/2

Table 4. Pin Function Summary

Pin Number		Function			
112LQFP	80QFP	1st	2nd	3rd	4th
1	1	PP3	KWP3	PWM3	
2	2	PP2	KWP2	PWM2	
3	3	PP1	KWP1	PWM1	
4	4	PP0	KWP0	PWM0	
5	—	PK3			
6	—	PK2			
7	—	PK1			
8	—	PK0			
9	5	PT0	IOC0		
10	6	PT1	IOC1		
11	7	PT2	IOC2		
12	8	PT3	IOC3		
13	9	VDD1			
14	10	VSS1			
15	11	PT4	IOC4		
16	12	PT5	IOC5		
17	13	PT6	IOC6		
18	14	PT7	IOC7		
19	—	PK5			
20	—	PK4			
21	—	PJ1	KWJ1		
22	—	PJ0	KWJ0		
23	15	BKGD	MODC		
24	16	PB0			
25	17	PB1			
26	18	PB2			
27	19	PB3			
28	20	PB4			

Table 4. Pin Function Summary (continued)

Pin Number		Function			
112LQFP	80QFP	1st	2nd	3rd	4th
29	21	PB5			
30	22	PB6			
31	23	PB7			
32	—	PH7	KWH7		
33	—	PH6	KWH6		
34	—	PH5	KWH5		
35	—	PH4	KWH4		
36	24	PE7	$\overline{\text{XCLKS}}$	ECLKX2	
37	25	PE6	MODB		
38	26	PE5	MODA		
39	27	PE4	ECLK		
40	28	VSSR			
41	29	VDDR			
42	30	$\overline{\text{RESET}}$			
43	31	VDDPLL			
44	32	XFC			
45	33	VSSPLL			
46	34	EXTAL			
47	35	XTAL			
48	36	TEST			
49	—	PH3	KWH3		
50	—	PH2	KWH2		
51	—	PH1	KWH1		
52	—	PH0	KWH0		
53	37	PE3			
54	38	PE2			
55	39	PE1	$\overline{\text{IRQ}}$		
56	40	PE0	$\overline{\text{XIRQ}}$		

Table 4. Pin Function Summary (continued)

Pin Number		Function			
112LQFP	80QFP	1st	2nd	3rd	4th
57	41	PA0			
58	42	PA1			
59	43	PA2			
60	44	PA3			
61	45	PA4			
62	46	PA5			
63	47	PA6			
64	48	PA7			
65	49	VDD2			
66	50	VSS2			
67	51	PAD00	AN0		
68	—	PAD08	AN8		
69	52	PAD01	AN1		
70	—	PAD09	AN9		
71	53	PAD02	AN2		
72	—	PAD10	AN8		
73	54	PAD03	AN3		
74	—	PAD11	AN11		
75	55	PAD04	AN4		
76	—	PAD12	AN12		
77	56	PAD05	AN5		
78	—	PAD13	AN13		
79	57	PAD06	AN6		
80	—	PAD14	AN14		
81	58	PAD07	AN7		
82	—	PAD15	AN15		
83	59	VDDA			
84	60	VRH			

Table 4. Pin Function Summary (continued)

Pin Number		Function			
112LQFP	80QFP	1st	2nd	3rd	4th
85	61	VRL			
86	62	VSSA			
87	—	PM7			
88	—	PM6			
89	63	PS0	RXD0		
90	64	PS1	TXD0		
91	65	PS2	RXD1		
92	66	PS3	TXD1		
93	—	PS4	MISO0		
94	—	PS5	MOSI0		
95	—	PS6	SCK0		
96	—	PS7	SS0		
97	67	VREGEN			
98	68	PJ7	KWJ7	SCL0	TXCAN0
99	69	PJ6	KWJ6	SDA0	RXCAN0
100	70	PM5	TXCAN0		
101	71	PM4	RXCAN0		
102	72	PM3	TXCAN0		
103	73	PM2	RXCAN0		
104	74	PM1	TXCAN0		
105	75	PM0	RXCAN0		
106	76	VSSX1			
107	77	VDDX1			
108	—	PK7	ROMCTL		
109	78	PP7	KWP7	PWM7	
110	—	PP6	KWP6	PWM6	
111	79	PP5	KWP5	PWM5	
112	80	PP4	KWP4	PWM4	

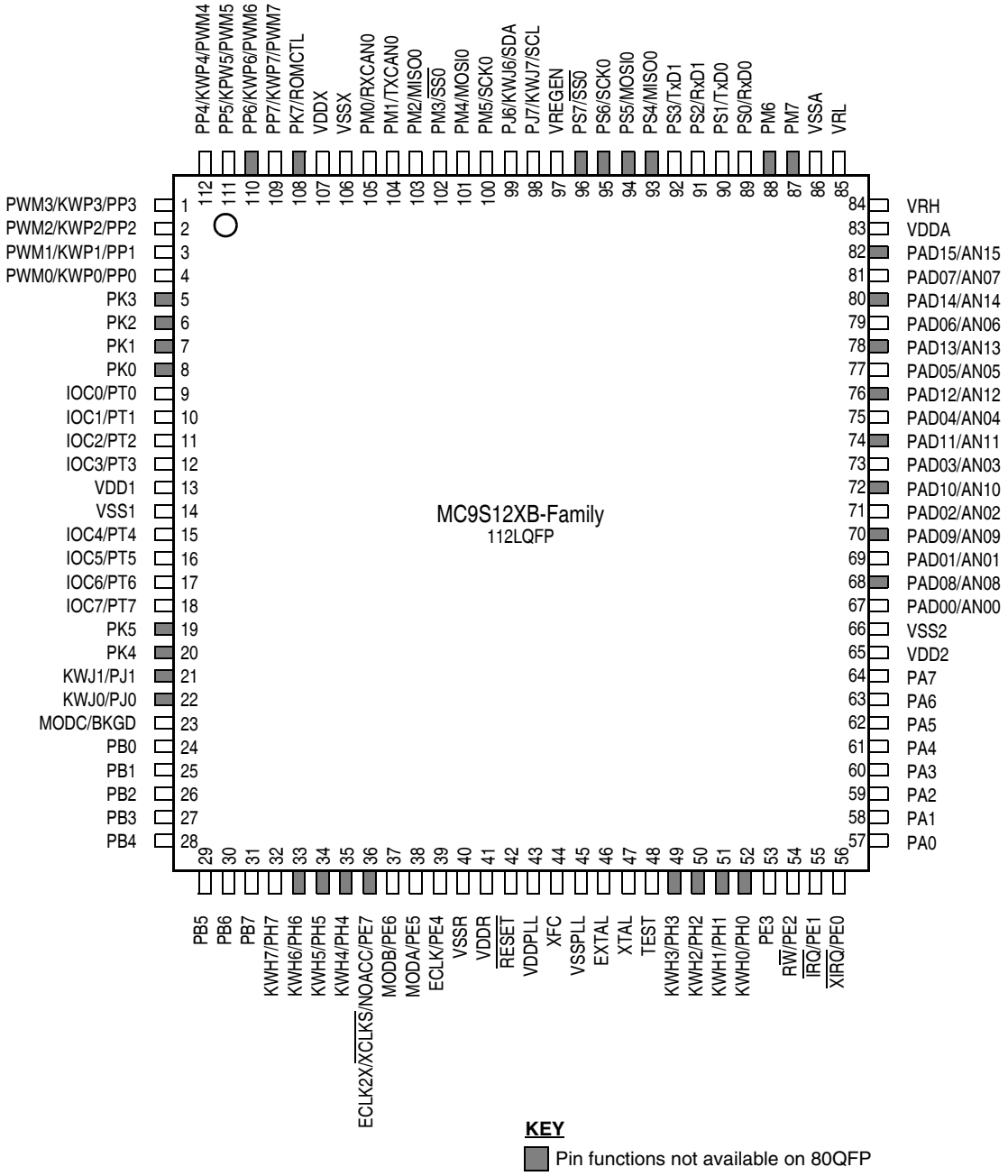


Figure 2. Pin assignments 112LQFP for MC9S12XB-Family

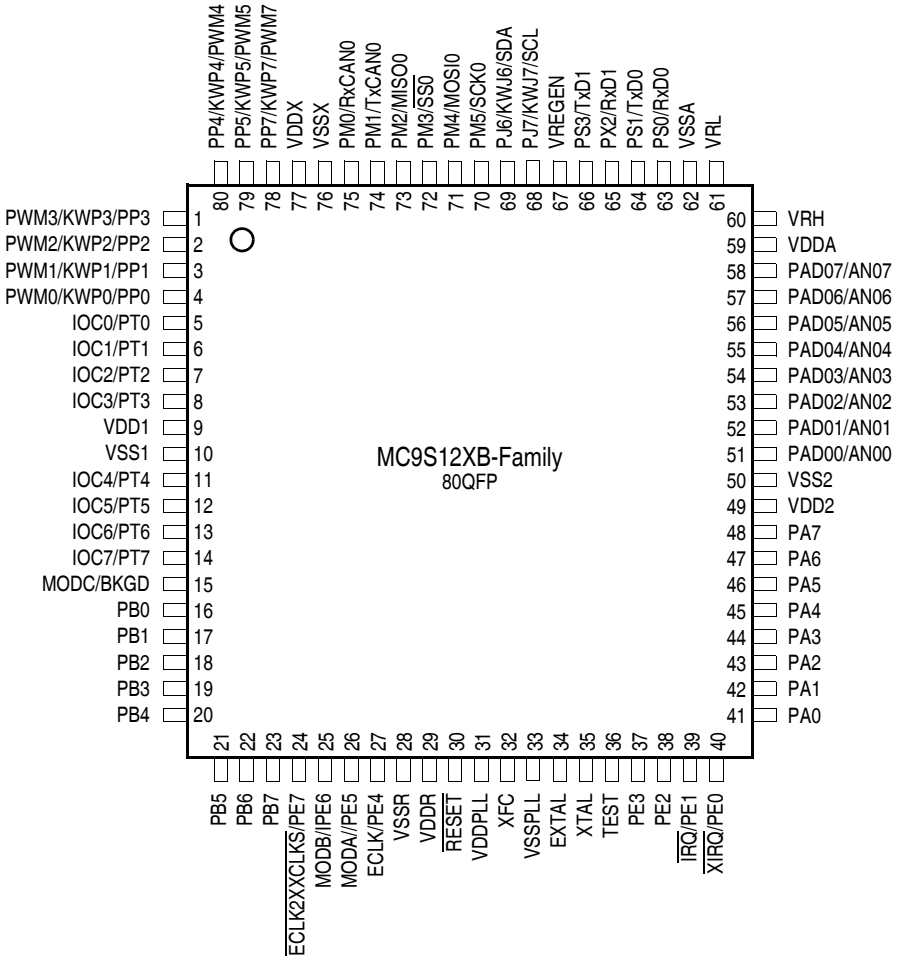
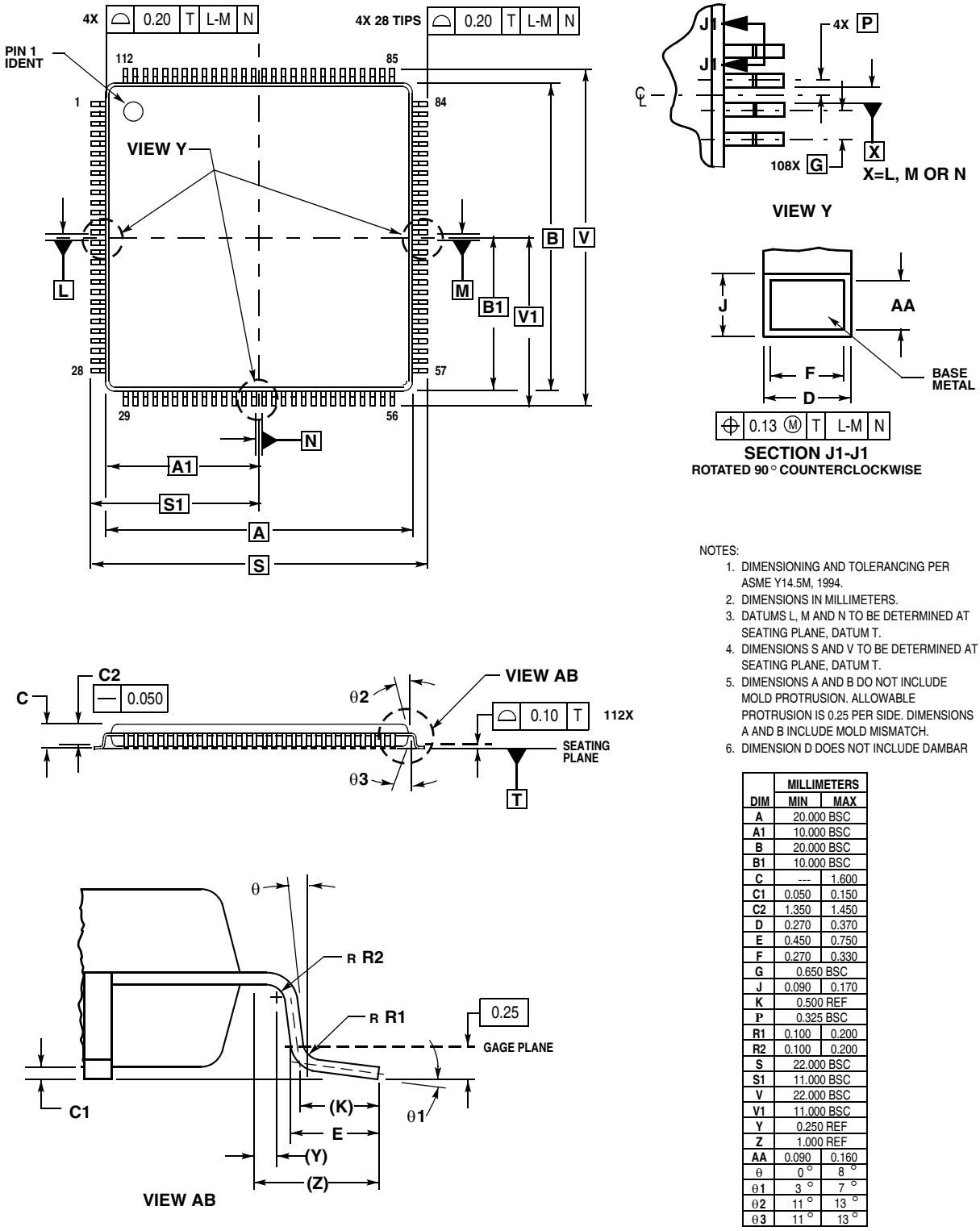


Figure 3. Pin Assignments in 80QFP for MC9S12XB-Family

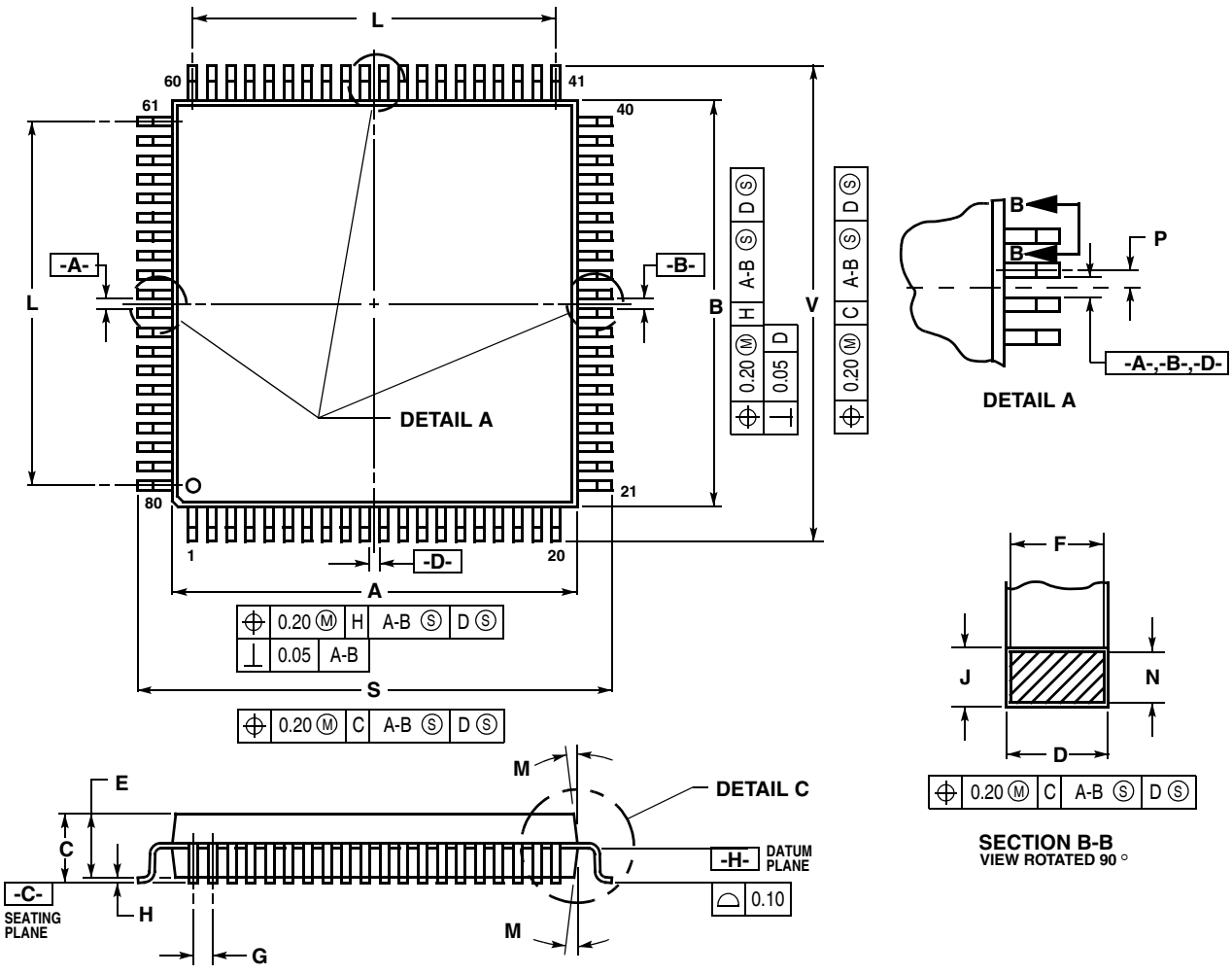


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure 4. 112-pin LQFP Mechanical Dimensions (case no. 987)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5°	10°
N	0.13	0.17
P	0.325 BSC	
Q	0°	7°
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0°	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure 5. 80-pin QFP Mechanical Dimensions (case no. 841B)

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
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