

MC68VZ328

MC68VZ328 (DragonBall™ VZ) Integrated Portable System Processor Product Brief

The MC68VZ328 (DragonBall VZ) microprocessor, the third generation of the DragonBall™ family of products, is designed to save time, power, and cost in the design and operation of new products. DragonBall VZ requires less board space and allows for reduced pin count and fewer programming steps in designing your product. The major differences between previous versions of DragonBall processors and the new VZ product are system-speed improvement and SDRAM support.

All these features combine to make the MC68VZ328 the microprocessor of choice among many system designers. Its functionality and glue logic are all optimally connected, timed with the same clock, fully tested, and uniformly documented. Also, only the essential signals are brought out to the pins. The MC68VZ328's primary package consists of TQFP and MBGA, designed to occupy the smallest possible footprint on your board.

Although the DragonBall VZ is the integrated processor of choice for some of the most popular PDA designs, it can be used in a wide variety of applications including exercise monitors, navigation systems, and smart phones. Figure 1 on page 2 shows a simplified block diagram of the MC68VZ328.

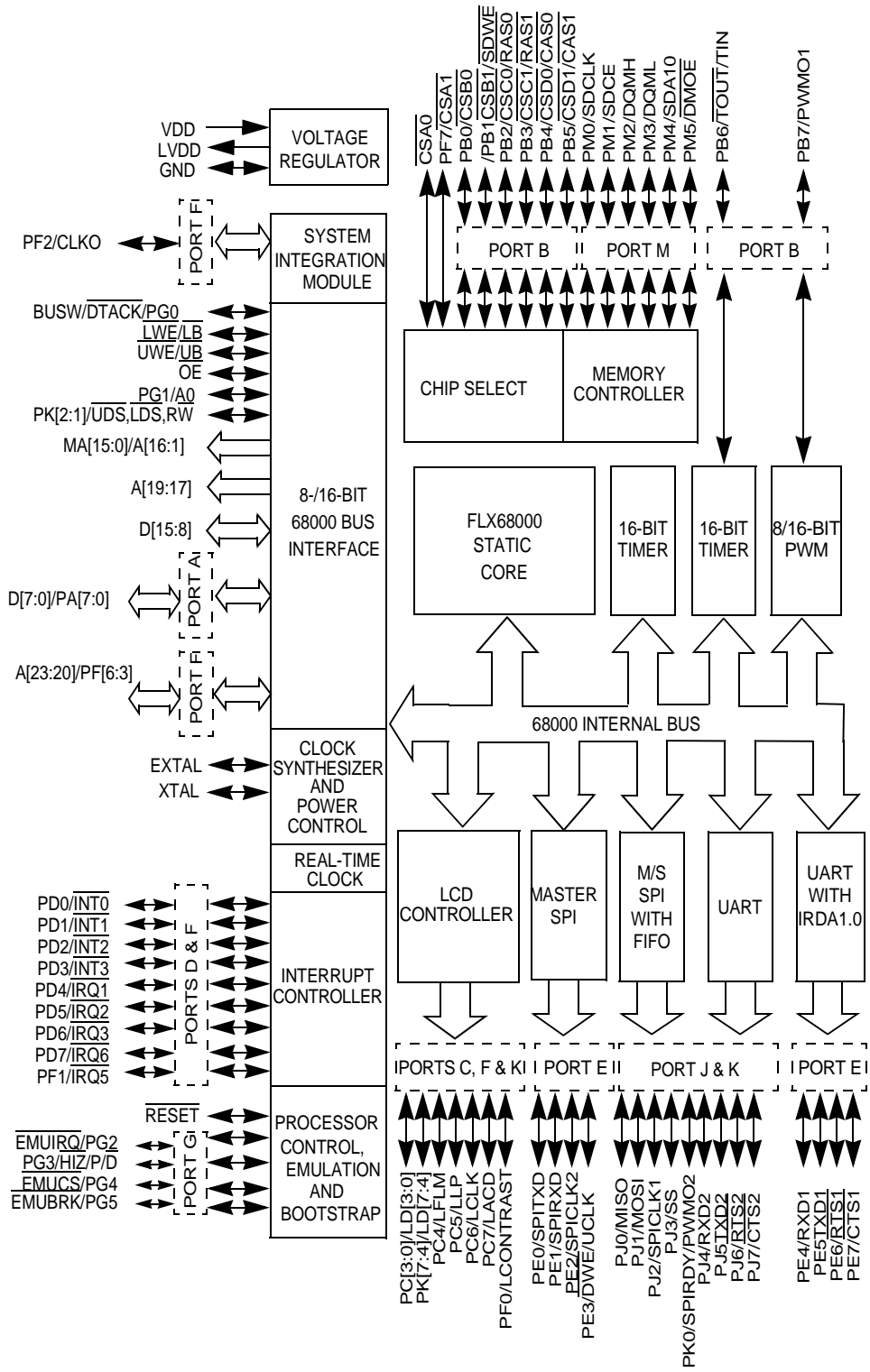


Figure 1. MC68VZ328 Simplified Block Diagram

1 Features

The features of the DragonBall VZ include the following:

- Static FLX68000 CPU—identical to MC68EC000 microprocessor
 - Full compatibility with MC68000 and MC68EC000
 - 32-bit internal address bus
 - Static design that allows processor clock to be stopped to provide power savings
 - 5.4 MIPS performance at 33 MHz processor clock
 - External M68000 bus interface with selectable bus sizing for 8-bit and 16-bit data ports
- System Integration Module (SIM) incorporating many functions typically related to external array logic, reducing parts counts in design, with functions that include the following:
 - System configuration and programmable address mapping
 - Glueless interface to SRAM, DRAM, SDRAM, EPROM, and FLASH memory
 - Eight programmable chip selects with wait state generation logic
 - Four programmable interrupt I/Os, with keyboard interrupt capability
 - Five general-purpose, programmable edge/level/polarity interrupt IRQs
 - Other programmable I/O, multiplexed with peripheral functions of up to 47 parallel I/O lines
 - Programmable interrupt vector response for on-chip peripheral modules
 - Low-power mode control
- Synchronous DRAM controller
 - Support for CAS-before-RAS refresh cycles and self-refresh mode DRAM
 - Support for 8-bit / 16-bit port DRAM
 - EDO or Automatic Fast Page Mode for LCDC access
 - Programmable refresh rate
 - Support for up to two banks of DRAM / EDO DRAM
 - Programmable column address size
- 76 general-purpose ports
- Two UART ports
- Two Serial Peripheral Interface (SPI) ports
- Two 16-bit general-purpose counters/timers
 - Automatic interrupt generation
 - 30 ns resolution at 33 MHz system clock
 - Timer input/output pin
- Real-time clock / sampling timer
 - Separate power supply for the RTC
 - One programmable alarm
 - Capability of counting up to 512 days

- Sampling timer with selectable frequency (4 Hz, 8 Hz, 16 Hz, 32 Hz, 64 Hz, 128 Hz, 256 Hz, 512 Hz)
- Interrupt generation for digitizer sampling or keyboard debouncing
- LCD controller
 - Software-programmable screen size (up to 640 x 480) to support single (non-split) monochrome panels
 - Capability of directly driving popular LCD drivers/modules from Motorola, Sharp, Hitachi, Toshiba, and numerous other manufacturers
 - Support for up to 16 gray levels out of 16 palettes
 - Utilization of system memory as display memory
 - LCD contrast control using 8-bit PWM
- Two Pulse Width Modulation (PWM) modules
 - Audio-effects support
 - 16- and 8-bit resolution
 - 5-byte FIFO that provides more flexibility on performance
 - Sound and melody generation
- Built-in emulation function
 - Dedicated memory space for emulator debug monitor with chip select
 - Dedicated interrupt (interrupt level 7) for ICE
 - One address-signal comparator and one control-signal comparator, with masking to support single or multiple hardware execution
 - Breakpoint
 - One breakpoint instruction insertion unit
- Boot Strap mode function
 - Allows user to initialize system and download program/data to system memory through UART
 - Accepts execution command to run program stored in system memory
 - Provides an 8-byte-long instruction buffer for 68000 instruction storage and execution
- Power management
 - Fully static HCMOS technology
 - Programmable clock synthesizer using 32.768 kHz / 38.4 kHz crystal for full frequency control
 - Low-power stop capabilities
 - Modules that can be individually shut down
 - Operation from DC to 33 MHz (processor clock)
 - Operating voltage of $(3.0 \pm 10\%)$ V
 - Compact 144-lead Thin Quad Flat Pack (TQFP) and MAP BGA

2 DragonBall Series

The DragonBall VZ marks the third generation in the DragonBall series. Table 1 compares the new processor with previous versions.

Table 1. DragonBall Series Comparison

Feature	DragonBall	DragonBall EZ	DragonBall VZ
CPU	68EC000	68EC000	Synthesizable 68000
Chip Selects	16	8	8
LCD Controller	4 gray levels	16 gray levels	16 gray levels
LCD Resolution	Up to 1024 * 512	Up to 640 * 512	Up to 640 * 480
Timer	2 * 16-bit	1 * 16-bit	2 * 16-bit
SPI	Master and Slave	Master	Master and Config. Master/Slave
PWM	16-bit	8-bit with FIFO	16-bit, 8-bit with FIFO
UART	UART 1	UART 1	UART 1 UART 2
RTC	Yes	512 day count	512 day count
PCMCIA 1.0	Yes	No	No
DRAM Controller	No	EDO/Fast Page DRAM	EDO/Fast Page DRAM
GPIO	Up to 78	Up to 54	Up to 76
Boot Strap Mode	No	Yes	Yes
Speed	16 MHz	16/20 MHz	33 MHz
Voltage	3.3 V ± 10%	3.3 V ± 10%	3.0 V ± 10%
Package	144 TQFP	100 TQFP, 144 MAP BGA	144 TQFP, 144 MAP BGA

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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado, 80217.
1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku,
Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd., Silicon Harbour Centre, 2 Dai King Street,
Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

Technical Information Center: 1-800-521-6274

HOME PAGE: <http://www.motorola.com/semiconductors/>

