Freescale Semiconductor
56858 Product Brief

The 56858 offers a rich feature set and on-chip memory interface. It includes external memory expansion with up to 2M words of program or up to 8M words of data addressing space, and is available in both 144 LQFP and 144 MBGA packages. The 56858 includes 40K words of on-chip rogram SRAM and 24K words of on-chip data SRAM. With two enhanced serial synchronous serial interfaces (ESSIs), this device can provide outputs for 5.1-channel surround sound. The 56858 is ideal for client-side telecom/datacom applications requiring up to four channels, including IP phones. This device can be designed into multi-processor systems to provide internet audio and speech processing functionalities and can provide a stand-alone device for internet audio.

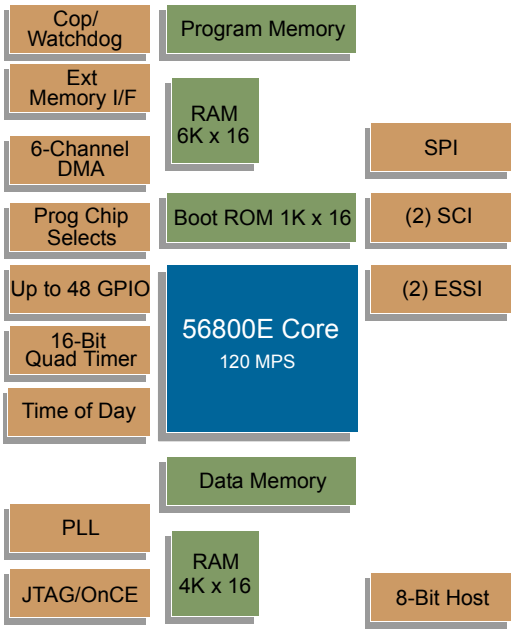
BENEFITS

- Easy to program with flexible application development tools
- Supports multiple processor connections
- 16-bit quad timer module (with four external pins) that allows capture/compare functionality, and can be cascaded
- Quad timer module can also be used for simple digital-to-analog conversion functionality
- Enhanced synchronous serial interface with enhanced network and audio modes
- Time of Day for applications requiring clock display
- Flexible 6-Channel Direct Memory Access (DMA) allows both internal and external memory transfers with almost no CPU interruption
- Serial peripheral interface with master and slave mode supporting connection to other processors or serial memory devices
- Two enhanced synchronous serial interfaces with three transmitters per module provide support for 5.1 channel surround sound for audio applications

FEATURES

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers, enabling rapid development of optimized control applications. Features of the 56800E core include:

- Efficient 16-bit controller engine with dual Harvard architecture
- 120 Million Instructions Per Second (MIPS) at 120MHz core frequency
- Single-cycle 16 x 16-bit parallel Multiplier-Accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Four hardware interrupt levels
- Five software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/Enhanced OnCE debug programming interface



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MEMORY FEATURES

- Harvard architecture permits up to three simultaneous accesses to program and data memory
- On-Chip Memory
  - 40K x 16-bit Program RAM
  - 24K x 16-bit Data RAM
  - 1K x 16-bit Boot ROM
- Off-Chip Memory Expansion (EMI)
  - Access up to 2M words of program or up to 8M data memory (using chip selects)
  - Chip Select Logic for glueless interface to ROM and SRAM

AWARD-WINNING DEVELOPMENT ENVIRONMENT

- Processor Expert™ (PE) provides a Rapid Application Design (RAD) tool that combines easy-to-use component-based software application creation with an expert knowledge system.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigation, compiling, and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE, CodeWarrior and EVMs create a complete, scalable tools solution for easy, fast, and efficient development.

EXAMPLE APPLICATIONS

- Full duplex feature phones
- IP phones
- Client-side IP applications
- IADs
- Voice and audio processing
- Voice recognition and command
- General purpose devices

56858 PERIPHERAL CIRCUIT FEATURES

- General Purpose 16-bit Quad Timer*
- Two Serial Communication Interfaces (SCI)*
- Serial Peripheral Interface (SPI) Port*
- Two Enhanced Synchronous Serial Interface (ESSI) modules*
- Computer Operating Properly (COP)/Watchdog Timer
- JTAG/Enhanced On-Chip Emulation (OnCE) for unobtrusive, real-time debugging
- Six independent channels of DMA
- 8-bit parallel Host Interface*
- Time of Day (TOD)
- 144-pin LQFP and 144 MBGA packages
- Up to 48 GPIO

** Each peripheral I/O can be used alternately as a General Purpose I/O*

PRODUCT DOCUMENTATION

56800E Reference Manual	Detailed description of the 56800E architecture, 16-bit core processor and the instruction set Order Number: DSP56800ERM
5685x User Manual	Detailed description of memory, peripherals, and interfaces of the 56853, 56854, 56855, 56857, 56858 Order Number: DSP5685xUM
56858 Technical Data Sheet	Electrical and timing specifications, pin descriptions, and package descriptions Order Number: DSP56F858

ORDERING INFORMATION

PART	***DSP56858***
PACKAGE	***144 MBGA or LQFP***
ORDER NUMBER	***DSP56852V120 (LQFP)*** ***DSP56852VF120 (MBGA)***
SUPPLY VOLTAGE	***1.8V, 3.3 V***

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