



Product Brief

DSP56366

24-BIT AUDIO DIGITAL SIGNAL PROCESSOR

The DSP56366 processor is a new audio digital signal processor based on the 24-bit DSP56300 architecture. The DSP56366 utilizes the single-instruction-per-clock-cycle DSP56300 core, while retaining code compatibility with the DSP56000 core family. The DSP56366 is targeted to applications that require digital audio compression/decompression, sound field processing, acoustic equalization and other digital audio algorithms. The DSP56366, Figure 1, is a member of the 56300 Motorola Symphony™ DSP Family.

Freescale Semiconductor, Inc.

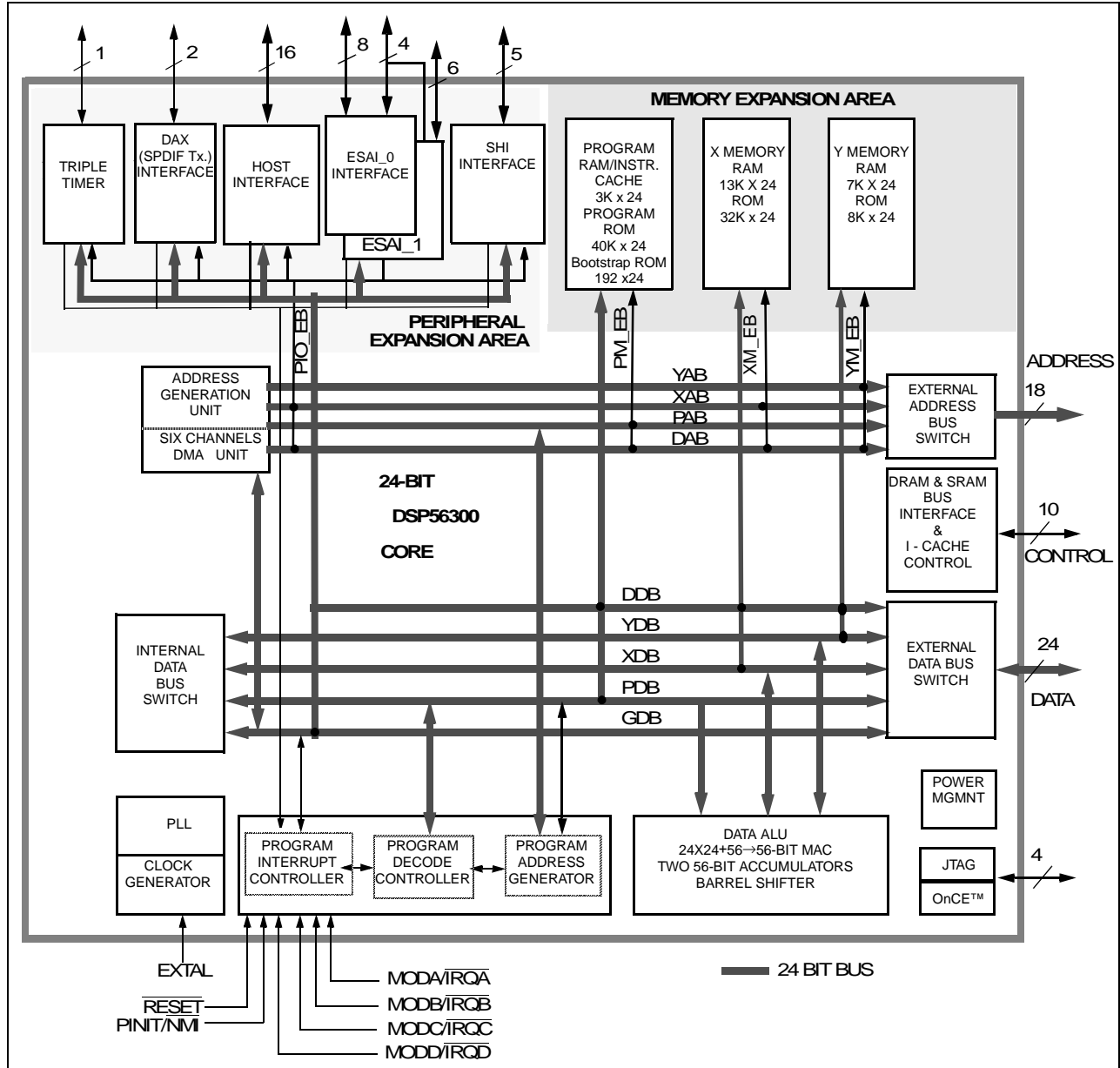


Figure 1 DSP56366 Block Diagram

This document contains information on a new product. Specifications and information herein are subject to change without notice.

DSP56366 Product Brief



FEATURES

- DSP56300 modular chassis
 - 100/120 Million Instructions Per Second (MIPS) with an 100/120 MHz clock at 3.3V.
 - Object Code Compatible with the 56K core.
 - Data ALU with a 24 x 24 bit multiplier-accumulator and a 56-bit barrel shifter. 16-bit arithmetic support.
 - Program Control with position independent code support and instruction cache support.
 - Six-channel DMA controller.
 - PLL based clocking with a wide range of frequency multiplications (1 to 4096), predivider factors (1 to 16) and power saving clock divider (2^i : $i=0$ to 7). Reduces clock noise.
 - Internal address tracing support and OnCE™ for Hardware/Software debugging.
 - JTAG port.
 - Very low-power CMOS design, fully static design with operating frequencies down to DC.
 - STOP and WAIT low-power standby modes.
- On-chip Memory Configuration
 - 7Kx24 Bit Y-Data RAM and 8Kx24 Bit Y-Data ROM.
 - 13Kx24 Bit X-Data RAM and 32Kx24 Bit X-Data ROM.
 - 40Kx24 Bit Program ROM.
 - 3Kx24 Bit Program RAM and 192x24 Bit Bootstrap ROM. 1K of Program RAM may be used as Instruction Cache or for Program ROM patching.
 - 2Kx24 Bit from Y Data RAM and 5Kx24 Bit from X Data RAM can be switched to Program RAM resulting in up to 10Kx24 Bit of Program RAM.
- Off-chip memory expansion
 - External Memory Expansion Port.
 - Off-chip expansion up to two 16M x 24-bit word of Data memory.
 - Off-chip expansion up to 16M x 24-bit word of Program memory.
 - Simultaneous glueless interface to SRAM and DRAM.
- Peripheral modules
 - Enhanced Serial Audio Interface (ESAI_0): up to 4 receivers and up to 6 transmitters, master or slave. I²S, Sony, AC97, network and other programmable protocols.
 - Enhanced Serial Audio Interface I(ESAI_1): up to 4 receivers and up to 6 transmitters, master or slave. I²S, Sony, AC97, network and other programmable protocols
The ESAI_1 shares four of the data pins with ESAI_0, and ESAI_1 does NOT support HCKR and HCKT (high speed clocks)
 - Serial Host Interface (SHI): SPI and I²C protocols, 10-word receive FIFO, support for 8, 16 and 24-bit words.
 - Byte-wide parallel Host Interface (HDI08) with DMA support.
 - Triple Timer module.
 - Digital Audio Transmitter (DAX): 1 serial transmitter capable of supporting the SPDIF, IEC958, CP-340 and AES/EBU digital audio formats.
 - Pins of unused peripherals (except SHI) may be programmed as GPIO lines.

PACKAGE

- 144-pin plastic Thin Quad Flat Pack (TQFP) surface-mount package

DOCUMENTATION

Table 1 lists the documents that provide a complete description of the DSP56362 and are required to design properly with the part. Documentation is available from a local Motorola distributor, a Motorola semiconductor sales office, a Motorola Literature Distribution Center, or (for the latest information) through the Motorola DSP home page on the Internet.

Table 1 DSP56366 Chip Documentation

Topic	Description	Order Number
DSP56300 Family Manual	Detailed description of the DSP56300 family architecture and the 24-bit core processor and instruction set	DSP56300FM/AD
DSP56366 User's Manual	Detailed description of memory, peripherals, and interfaces	DSP56366UM/AD
DSP56366 Technical Data Sheet	Electrical and timing specifications and pin and package descriptions	DSP56366/D

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