SOT650-3(DD)

HVSON10, thermal enhanced very thin small outline; no leads, 10 terminals, 0.5 mm pitch, $3 \text{ mm} \times 3 \text{ mm} \times 0.85 \text{ mm}$ body

13 November 2025 Package information



1 Package summary

Terminal position code D (double)

Package type descriptive code HVSON10

Package style descriptive code HVSON (thermal enhanced very thin small outline; no leads)

Package body material type P (plastic)

Mounting method type S (surface mount)

Issue date 04-11-2025

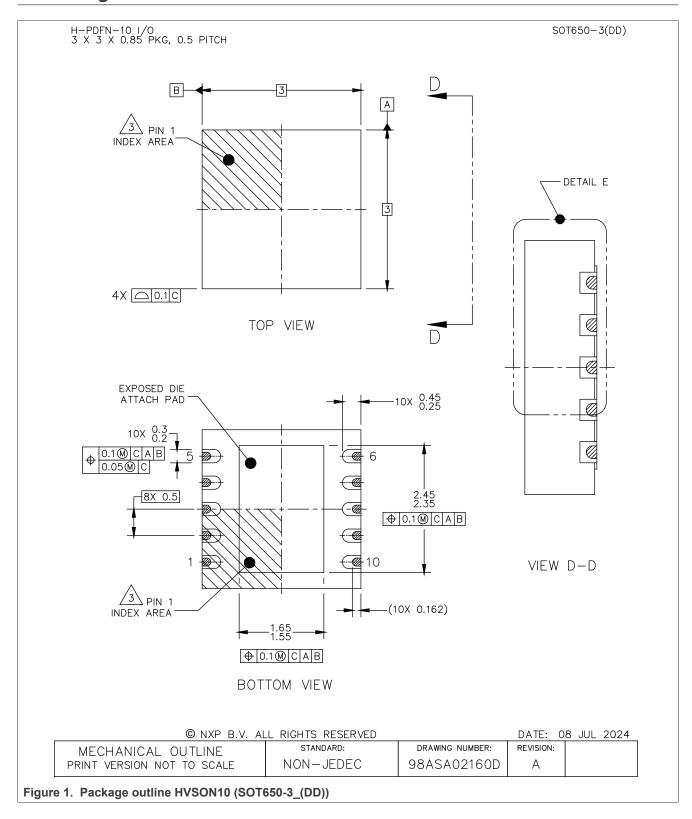
Manufacturer package code 98ASA02160D

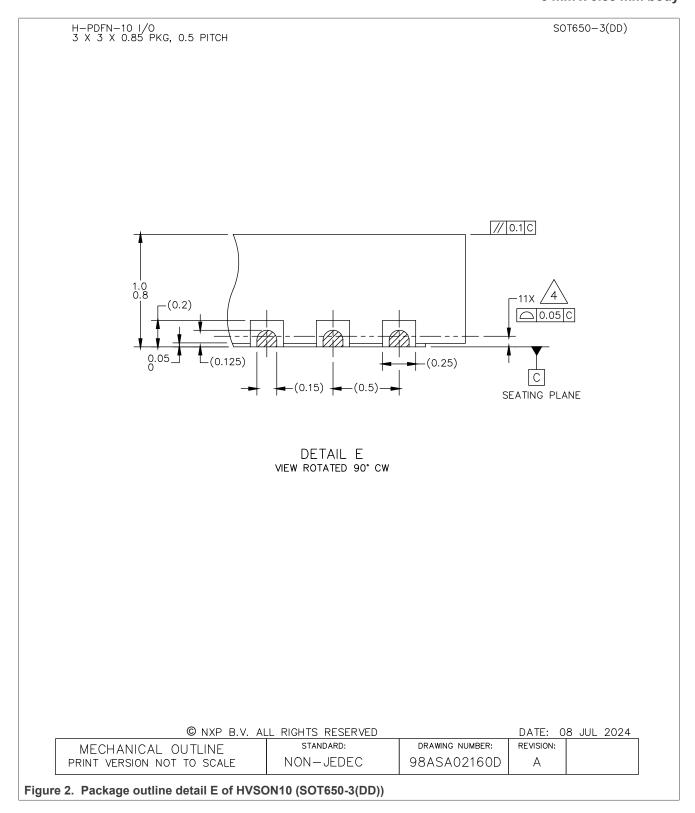
Table 1. Package summary

Table II I dottage callinary				
Parameter	Min	Nom	Max	Unit
package length	2.9	3	3.1	mm
package width	2.9	3	3.1	mm
package height	0.8	0.85	1	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	10	-	

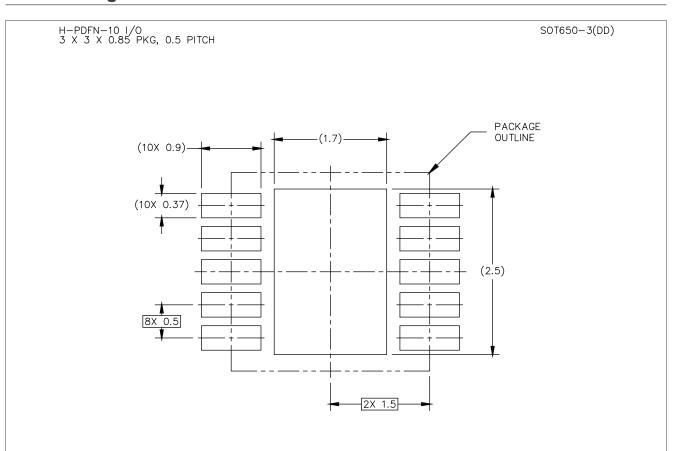


2 Package outline





3 Soldering

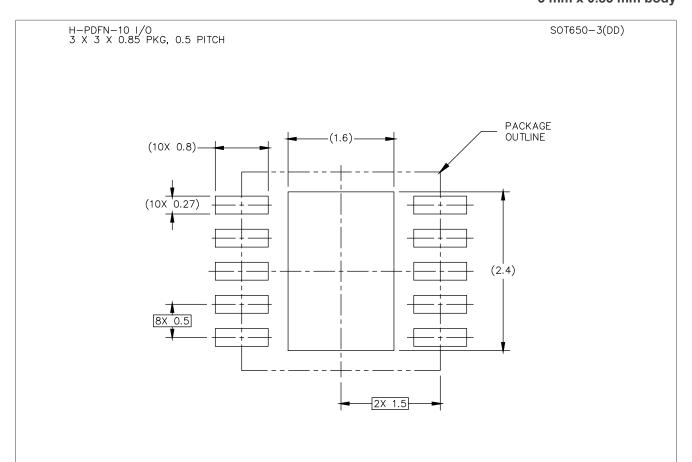


PCB DESIGN GUIDELINES RECOMMENDED SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. AL	L RIGHTS RESERVED		DATE: 0	8 JUL 2024
MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON-JEDEC	98ASA02160D	А	

Figure 3. Reflow soldering footprint part1 for HVSON10 (SOT650-3(DD))

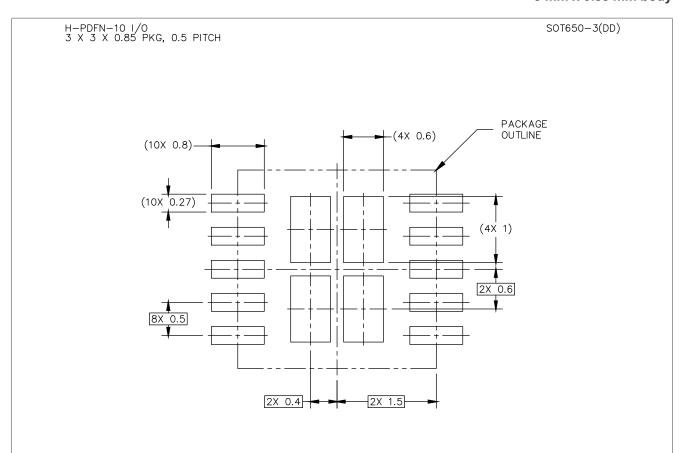


PCB DESIGN GUIDELINES RECOMMENDED I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. AL	L RIGHTS RESERVED		DATE: 0	8 JUL 2024
MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON-JEDEC	98ASA02160D	А	

Figure 4. Reflow soldering footprint part2 for HVSON10 (SOT650-3(DD))



RECOMMENDED STENCIL THICKNESS 0.100

PCB DESIGN GUIDELINES - RECOMMENDED SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

	© NXP B.V. AL	L RIGHTS RESERVED		DATE: 0	8 JUL 2024
ſ	MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
	PRINT VERSION NOT TO SCALE	NON-JEDEC	98ASA02160D	А	

Figure 5. Reflow soldering footprint part3 for HVSON10 (SOT650-3(DD))

H-PDFN-10 I/O 3 X 3 X 0.85 PKG, 0.5 PITCH SOT650-3(DD) NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994. $\sqrt{3}$. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY. 4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG. 5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM. © NXP B.V. ALL RIGHTS RESERVED DATE: 08 JUL 2024 STANDARD: DRAWING NUMBER: REVISION: MECHANICAL OUTLINE NON-JEDEC 98ASA02160D Α PRINT VERSION NOT TO SCALE

Figure 6. Package outline note HVSON10 (SOT650-3(DD))

SOT650-3(DD)

HVSON10, thermal enhanced very thin small outline; no leads, 10 terminals, 0.5 mm pitch, 3 mm x 3 mm x 0.85 mm body

4 Legal information

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

NXP Semiconductors

SOT650-3(DD)

HVSON10, thermal enhanced very thin small outline; no leads, 10 terminals, 0.5 mm pitch, 3 mm x 3 mm x 0.85 mm body

Tables

Tab. 1. Package summary 1

NXP Semiconductors

SOT650-3(DD)

HVSON10, thermal enhanced very thin small outline; no leads, 10 terminals, 0.5 mm pitch, 3 mm x 3 mm x 0.85 mm body

Figures

Fig. 1. Fig. 2.	Package outline HVSON10 (SOT650-3_ (DD))2 Package outline detail E of HVSON10	Fig. 4. 2 Fig. 5.	Reflow soldering footprint part2 for HVSON10 (SOT650-3(DD))	•••••
Fig. 3.	(SOT650-3(DD))	Fig. 6.	HVSON10 (SOT650-3(DD)) Package outline note HVSON10 (SOT650-3(DD))	

NXP Semiconductors

SOT650-3(DD)

HVSON10, thermal enhanced very thin small outline; no leads, 10 terminals, 0.5 mm pitch, 3 mm x 3 mm x 0.85 mm body

Contents

1	Package summary	1
2	Package outline	2
3	Soldering	4
4	Legal information	8