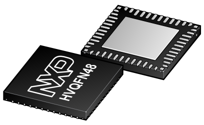


SOT619-26(SC)

plastic thermal enhanced very thin quad flat package; no leads; step-cut, wettable flank, 48 terminals; 7 mm x 7 mm x 0.85 mm body

19 December 2018 Package information

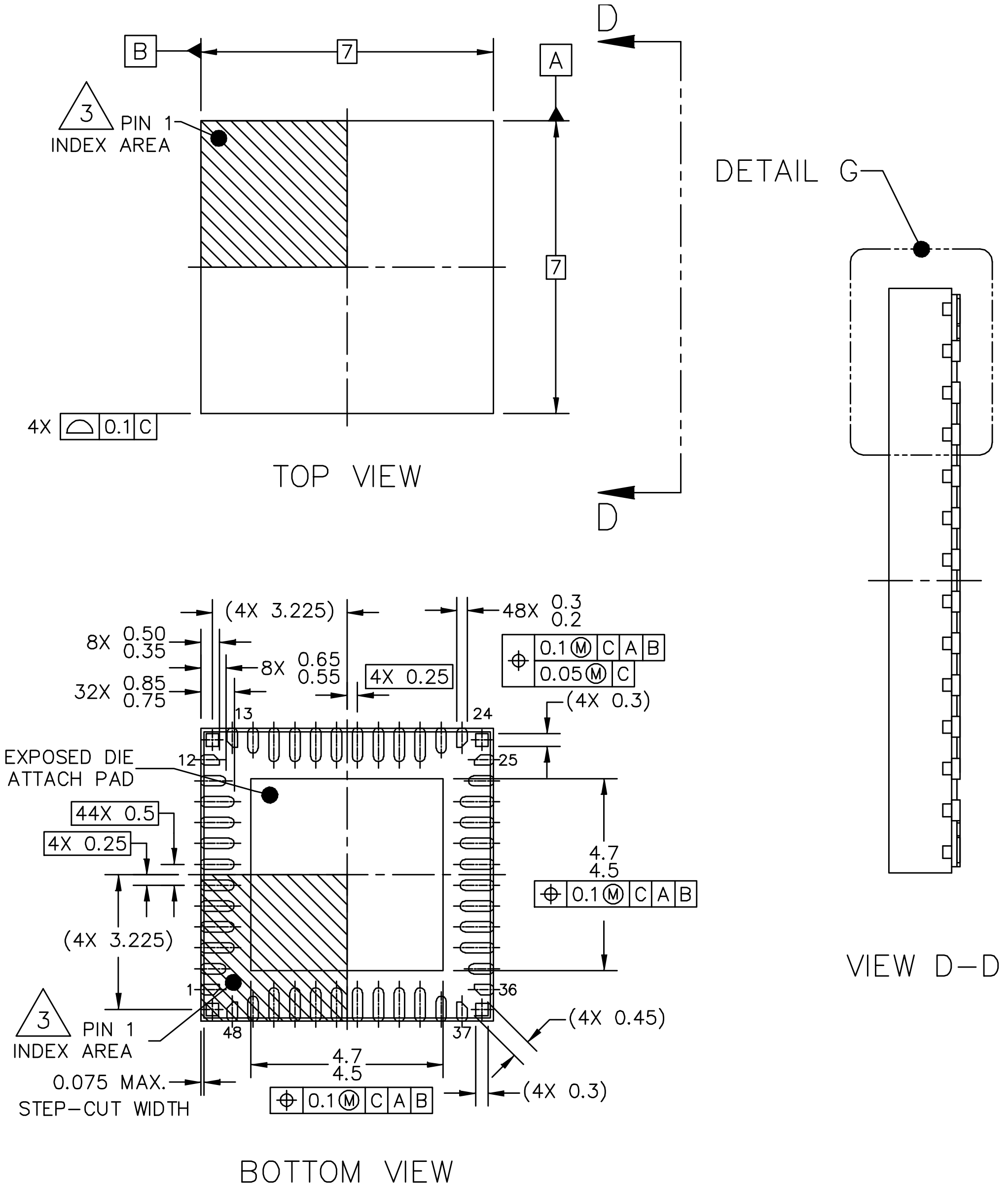
1 Package summary

Terminal position code	Q (quad)
Package type descriptive code	HVQFN48
Package style descriptive code	HVQFN (thermal enhanced very thin quad flatpack; no leads)
Package body material type	P (plastic)
Mounting method type	S (surface mount)
Issue date	04-12-2018
Manufacturer package code	98ASA01344D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	-	7	-	mm
package width	-	7	-	mm
package height	-	0.85	-	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	48	-	

2 Package outline



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DATE: 05 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01344D	REVISION: 0	

Figure 1. Package outline HVQFN48 (SOT619-26(SC))

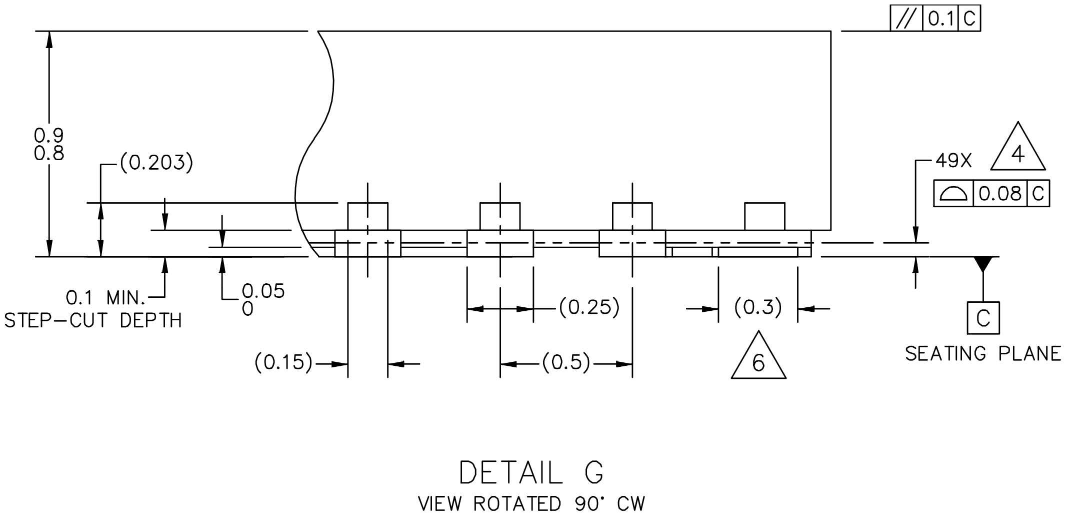

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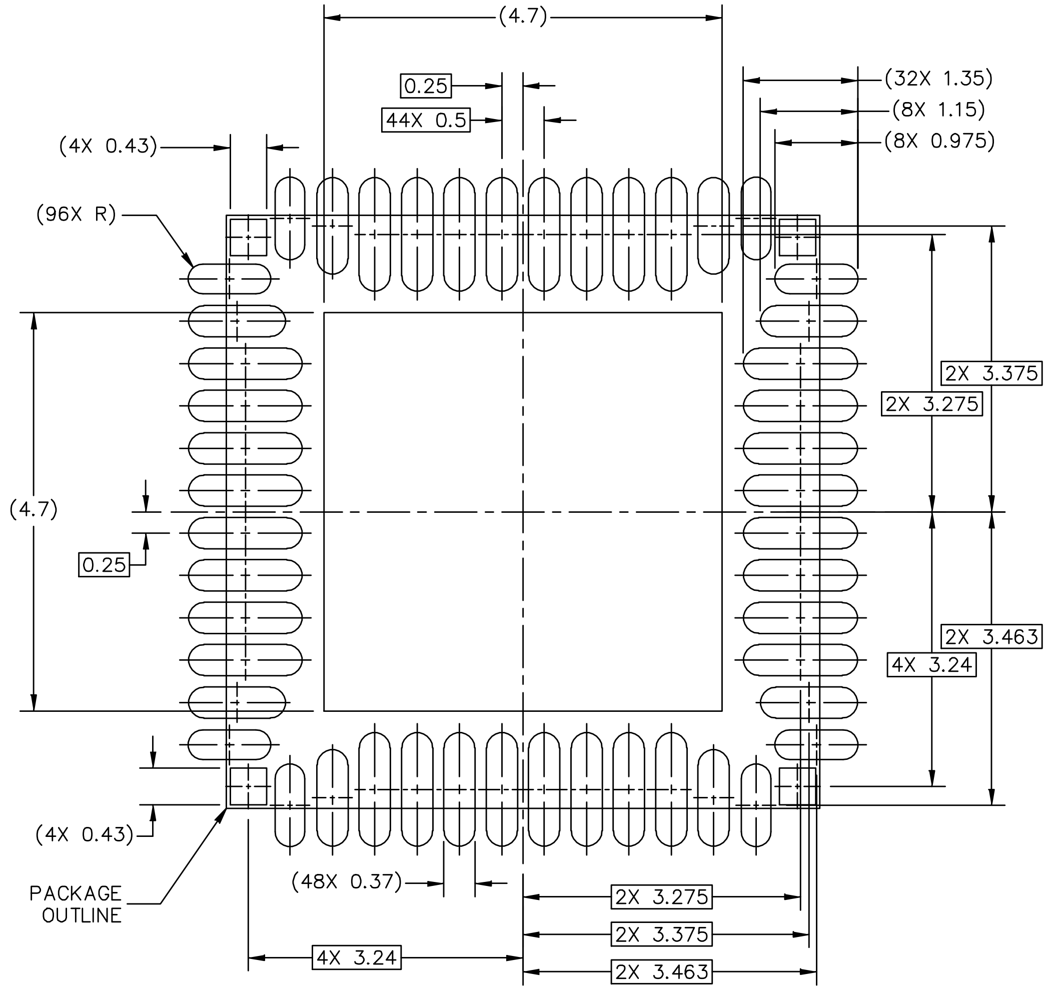
Figure 2. Package outline detail HVQFN48 (SOT619-26(SC))

3 Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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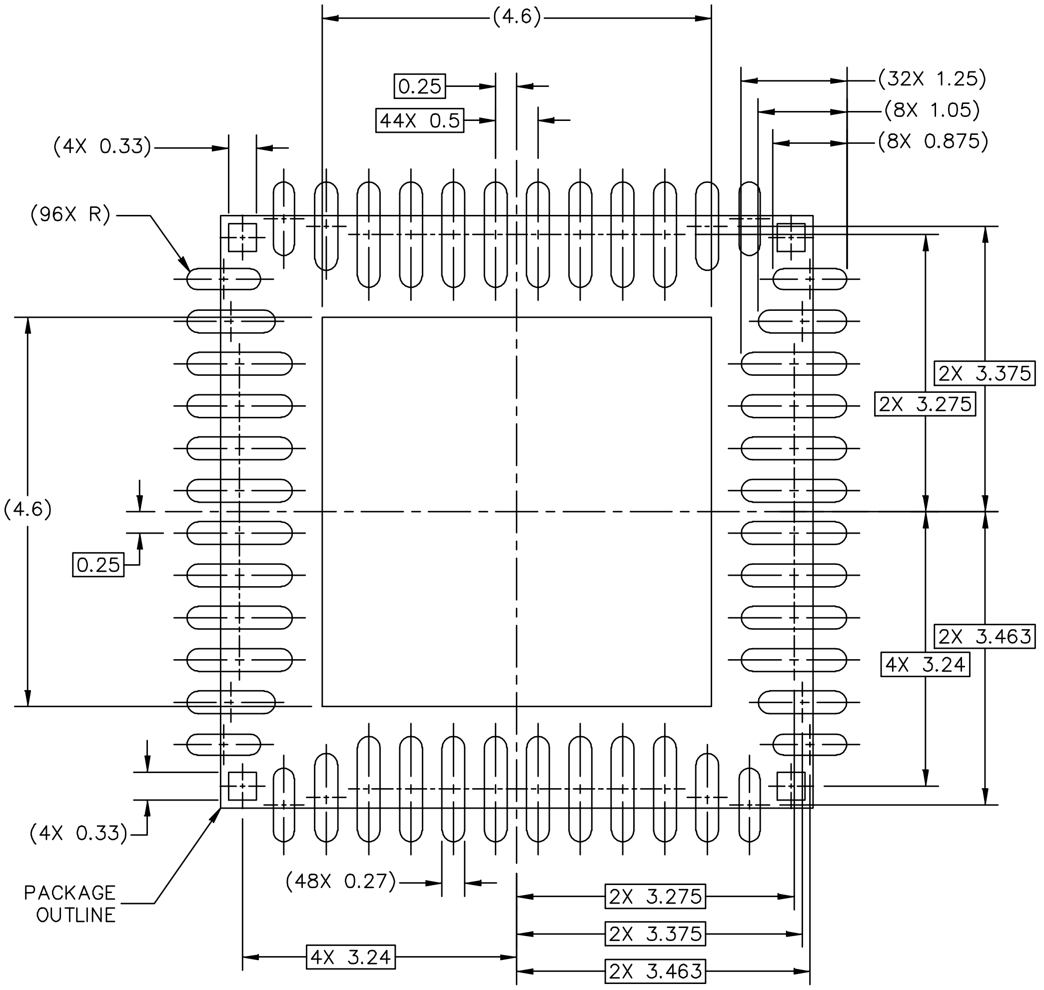
Figure 3. Reflow soldering footprint part1 for HVQFN48 (SOT619-26(SC))



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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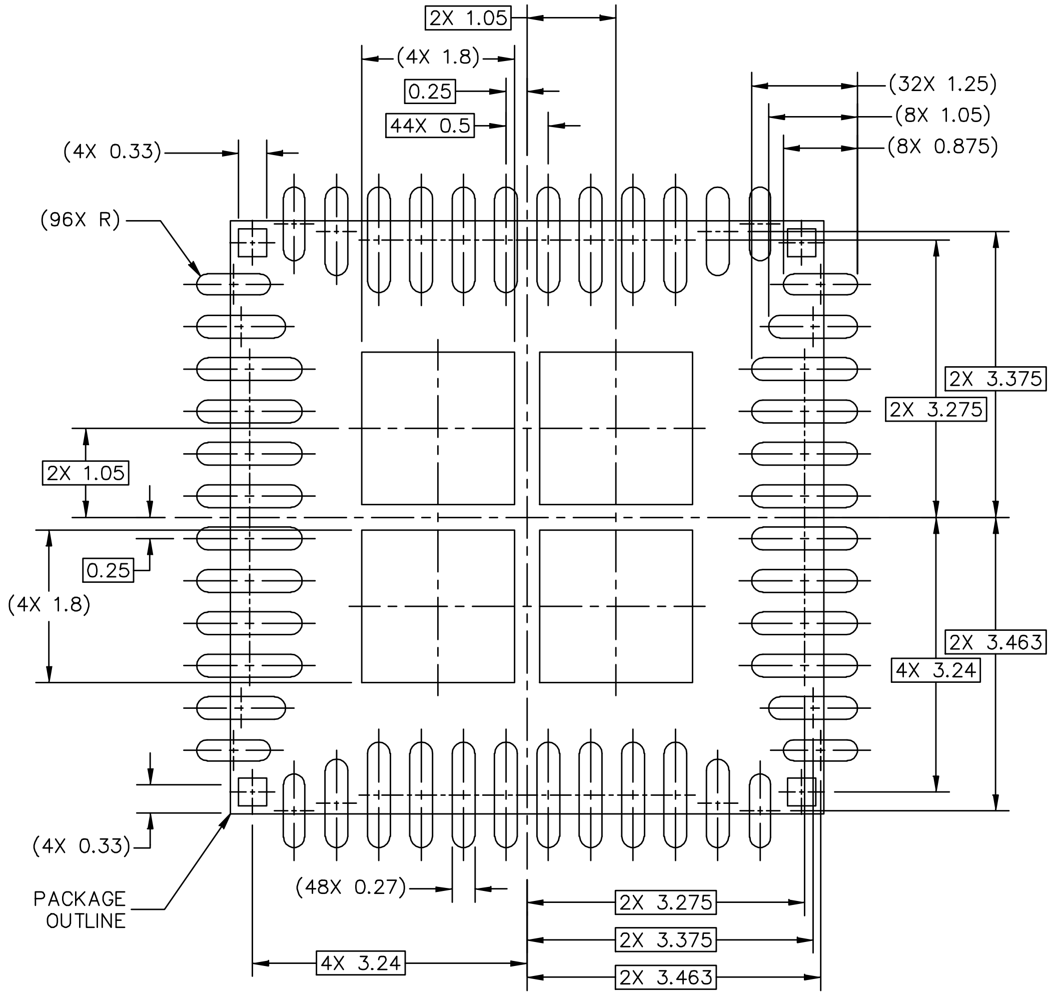
DATE: 05 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01344D	REVISION: 0	

Figure 4. Reflow soldering footprint part2 for HVQFN48 (SOT619-26(SC))



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 05 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01344D	REVISION: 0	

Figure 5. Reflow soldering footprint part3 for HVQFN48 (SOT619-26(SC))

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN ONE CONFIGURATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.
5. MIN. METAL GAP SHOULD BE 0.25 MM.
6. ANCHORING PADS.

DATE: 05 DEC 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01344D	REVISION: O	

Figure 6. Package outline note HVQFN48 (SOT619-26(SC))

4 Legal information

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Date of release: 19 December 2018