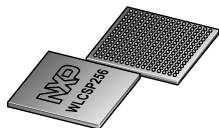


SOT2213-1

WLCSP256, wafer level chip-size package, 256 terminals, 0.35 mm pitch, 6.02 mm x 6.065 mm x 0.49 mm body

29 August 2025

Package information



1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP256
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	S (silicon)
Mounting method type	S (surface mount)
Manufacturer package code	98ASA01940D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	5.99	6.02	6.05	mm
package width	6.035	6.065	6.095	mm
seated height	-	0.49	0.525	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	256	-	



WLCSP256, wafer level chip-size package, 256 terminals, 0.35 mm pitch, 6.02 mm x 6.065 mm x 0.49 mm body

2 Package outline

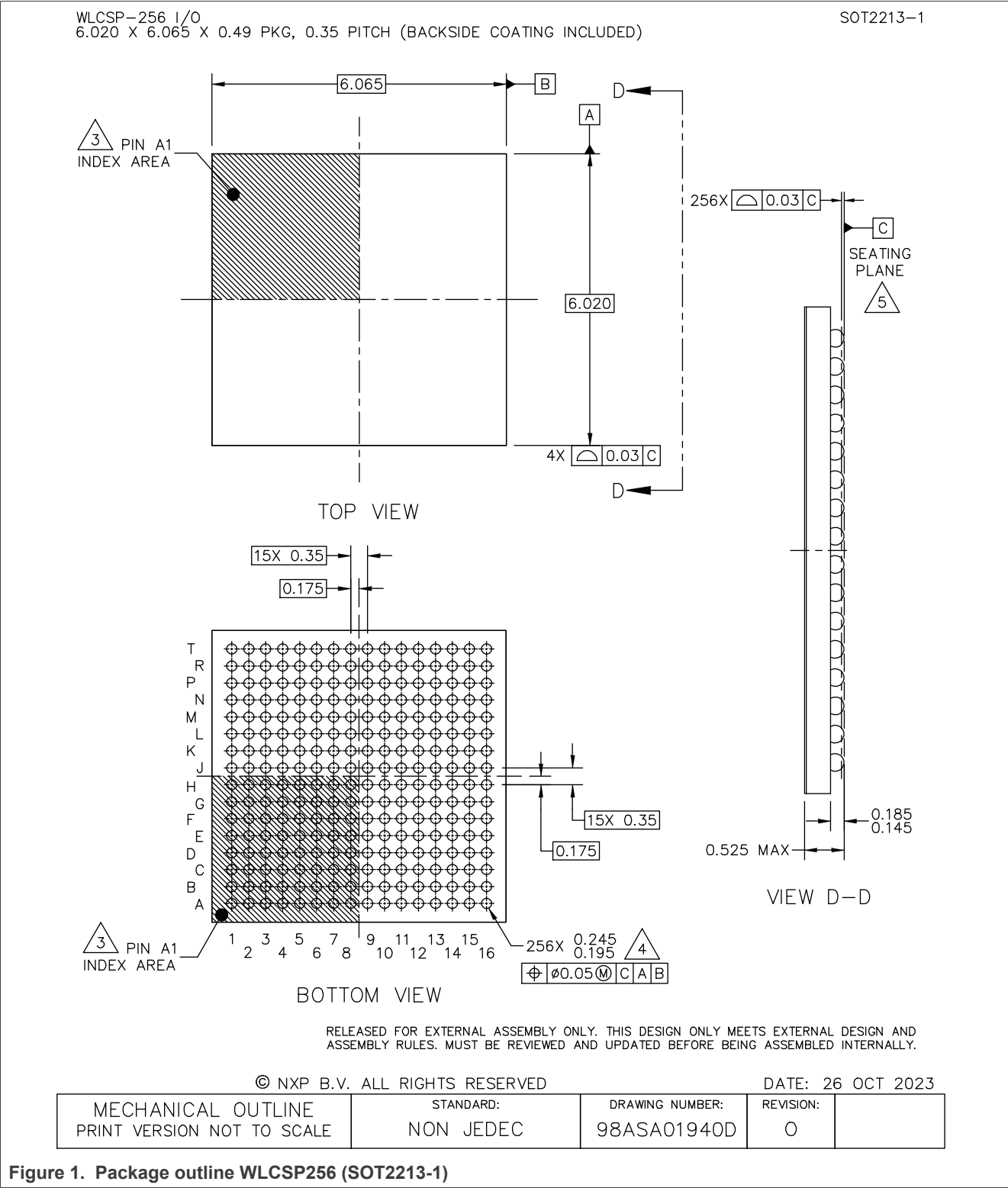
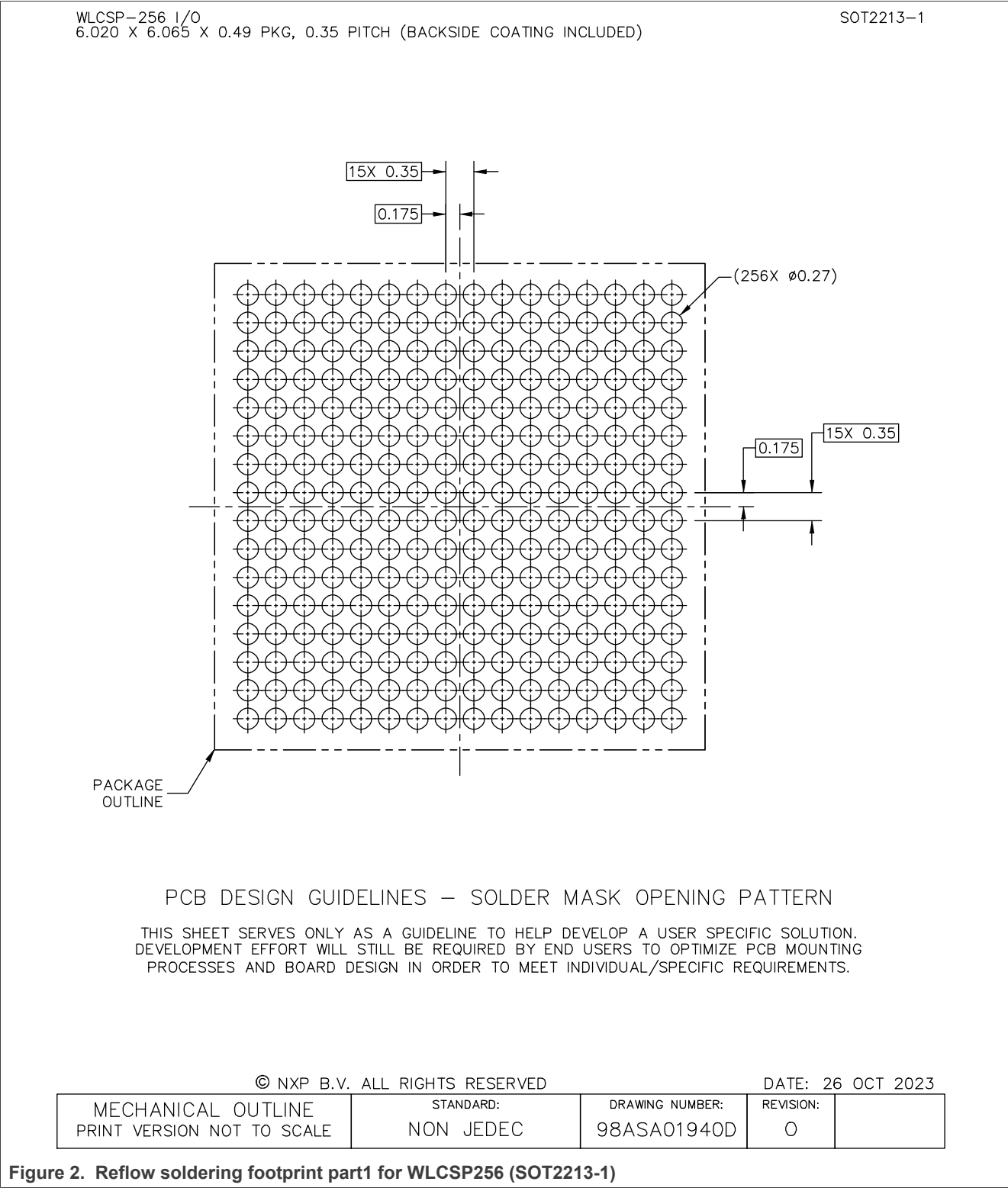


Figure 1. Package outline WLCSP256 (SOT2213-1)

WLCSP256, wafer level chip-size package, 256 terminals, 0.35 mm pitch, 6.02 mm x 6.065 mm x 0.49 mm body

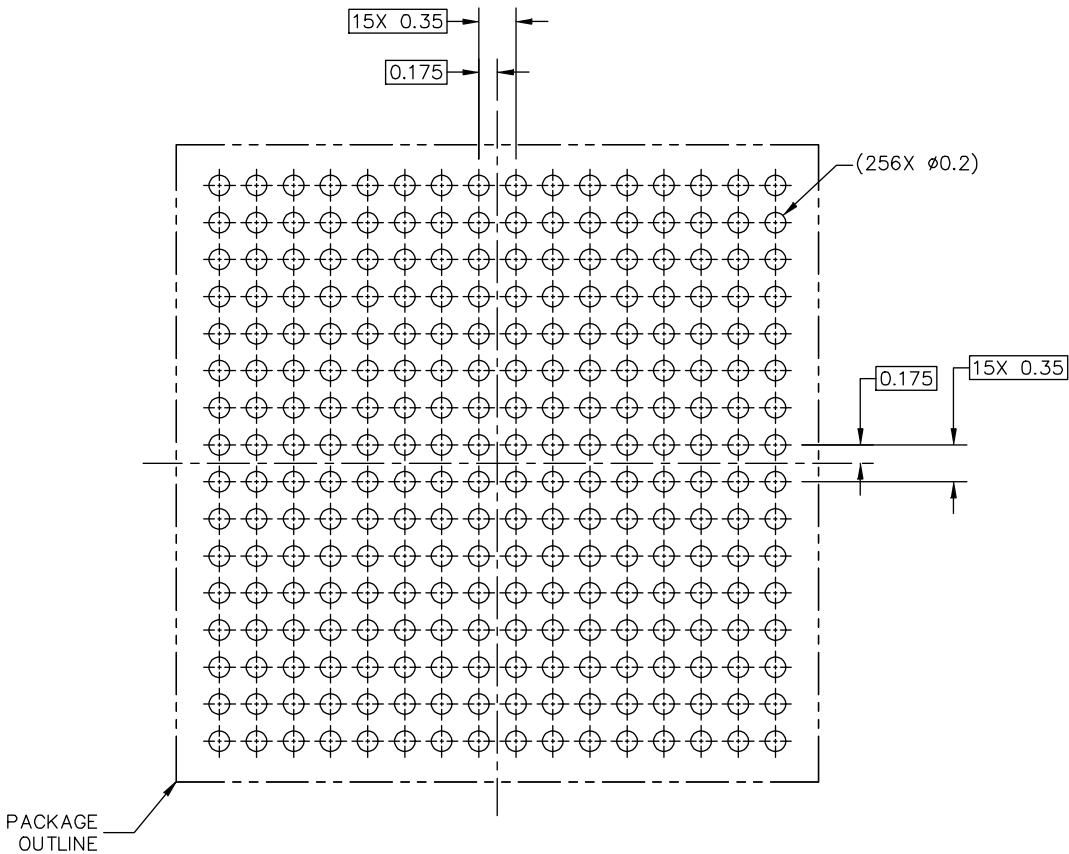
3 Soldering



WLCSP256, wafer level chip-size package, 256 terminals, 0.35 mm pitch, 6.02 mm x 6.065 mm x 0.49 mm body

WLCSP-256 I/O
6.020 X 6.065 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2213-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 26 OCT 2023

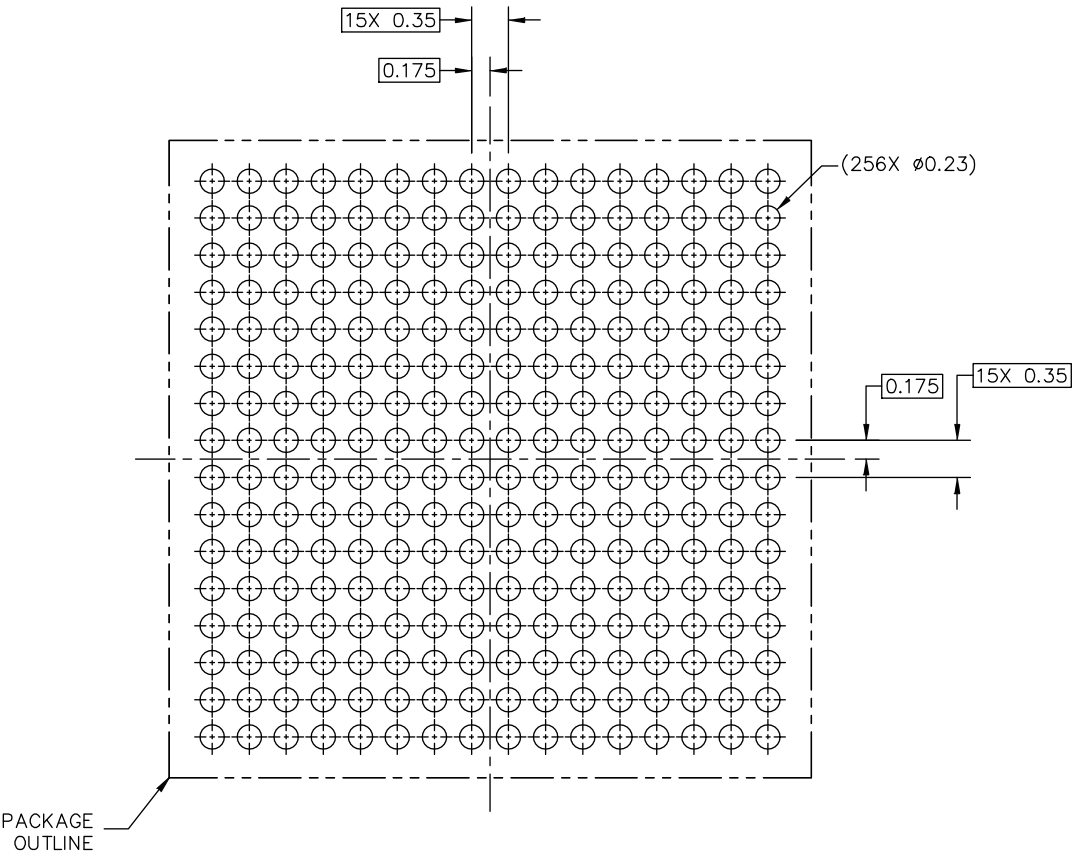
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01940D	REVISION: O	
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Figure 3. Reflow soldering footprint part2 for WLCSP256 (SOT2213-1)

WLCSP256, wafer level chip-size package, 256 terminals, 0.35 mm pitch, 6.02 mm x 6.065 mm x 0.49 mm body

WLCSP-256 I/O
6.020 X 6.065 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2213-1



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP256 (SOT2213-1)

WLCSP256, wafer level chip-size package, 256 terminals, 0.35 mm pitch, 6.02 mm x 6.065 mm x 0.49 mm body

WLCSP-256 I/O
6.020 X 6.065 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2213-1

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP256 (SOT2213-1)

4 Legal information

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WLCSP256, wafer level chip-size package, 256 terminals, 0.35 mm pitch, 6.02 mm x 6.065 mm x 0.49 mm body

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