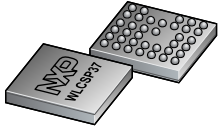


# SOT2173-1

WLCSP37, wafer level chip-size package; 37 terminals; 0.35 mm pitch; 2.63 mm x 2.495 mm x 0.49 mm body

16 April 2025

Package information



## 1 Package summary

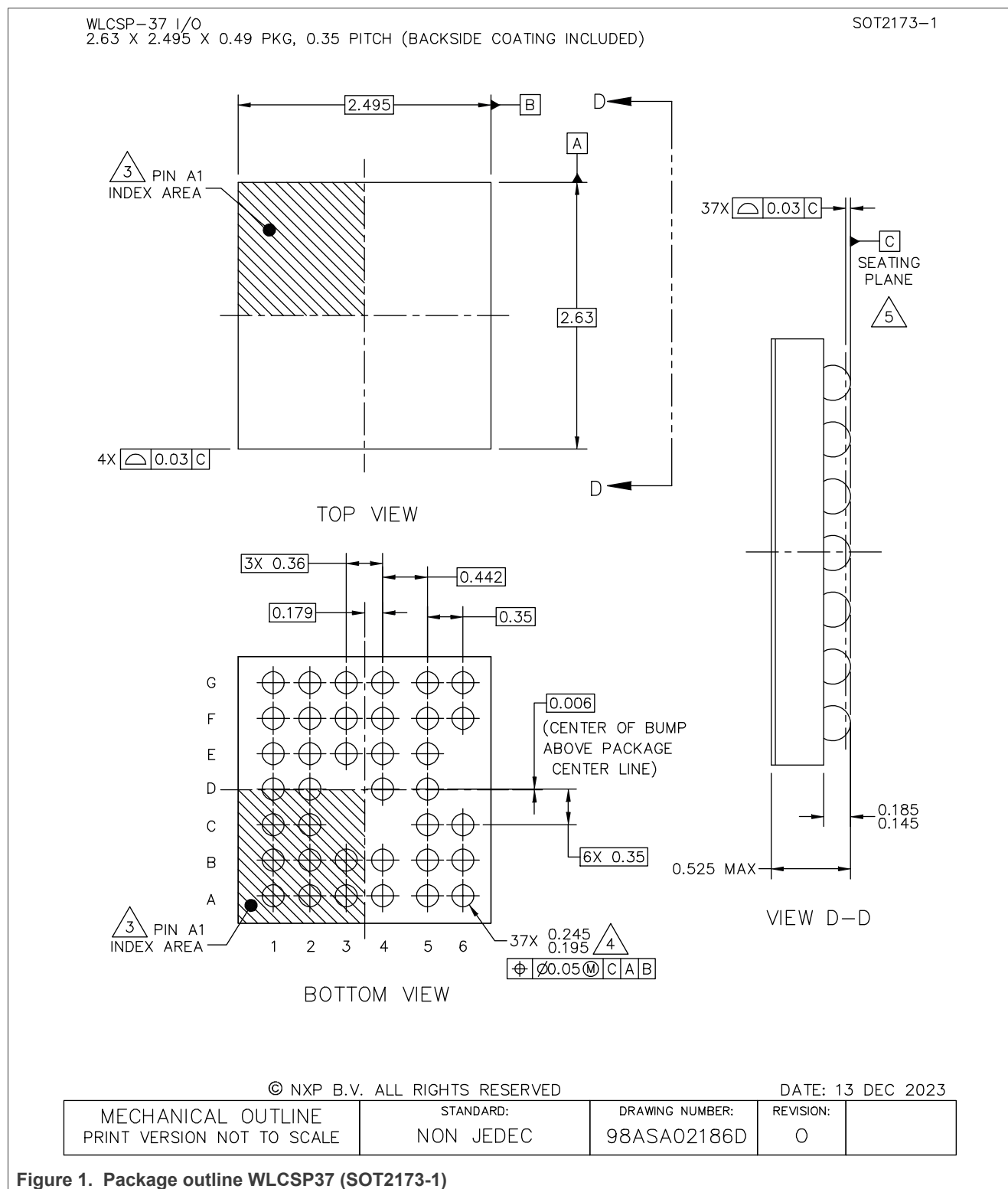
Package type descriptive code	WLCSP37
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	S (silicon)
Manufacturer package code	98ASA02186D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.6	2.63	2.66	mm
package width	2.915	2.945	2.975	mm
seated height	0.455	0.49	0.525	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	37	-	

**WLCSP37, wafer level chip-size package; 37 terminals; 0.35 mm pitch; 2.63 mm x 2.495 mm x 0.49 mm body**

## 2 Package outline



WLCSP37, wafer level chip-size package; 37 terminals; 0.35 mm pitch; 2.63 mm x 2.495 mm x 0.49 mm body

3 Soldering

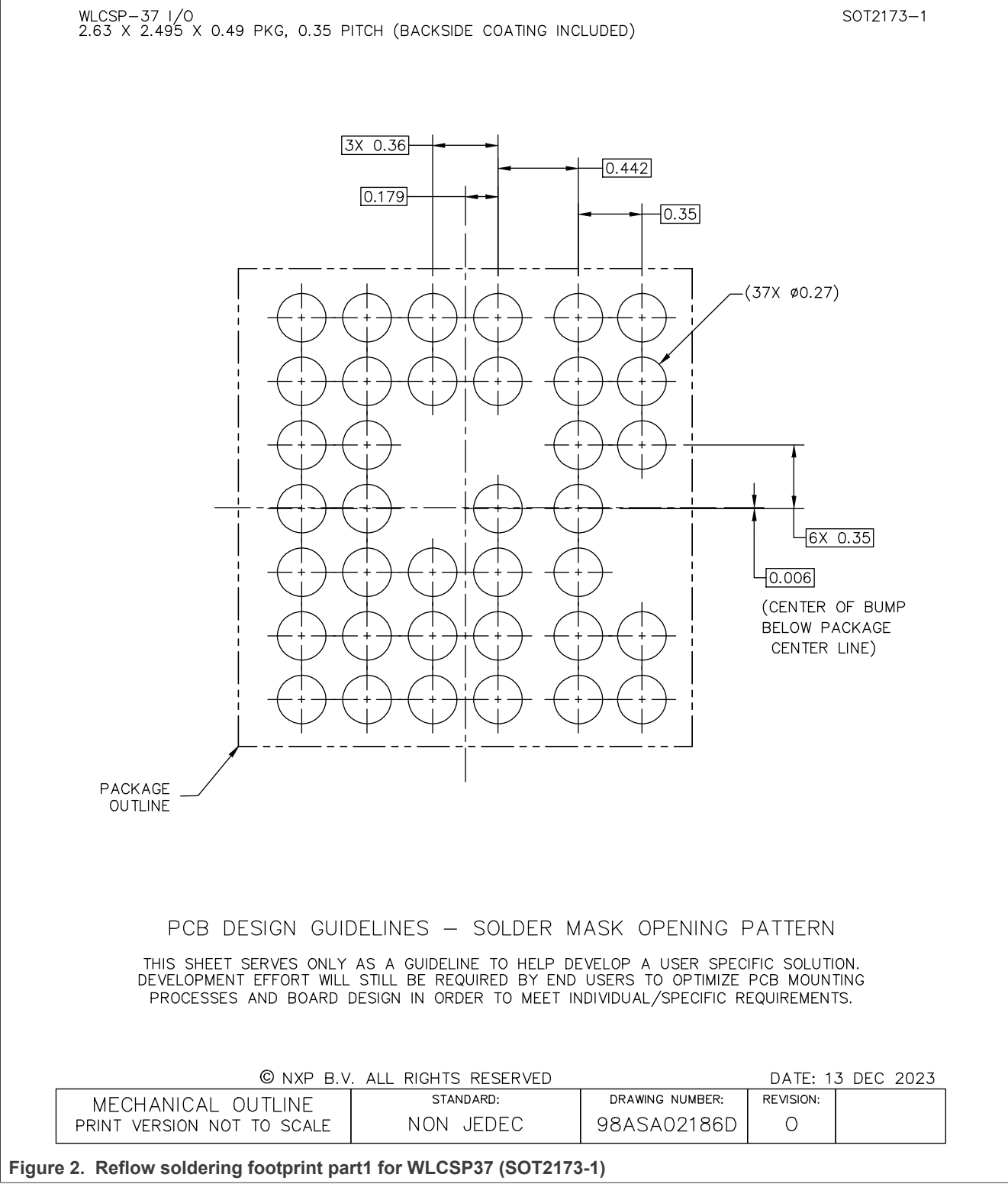
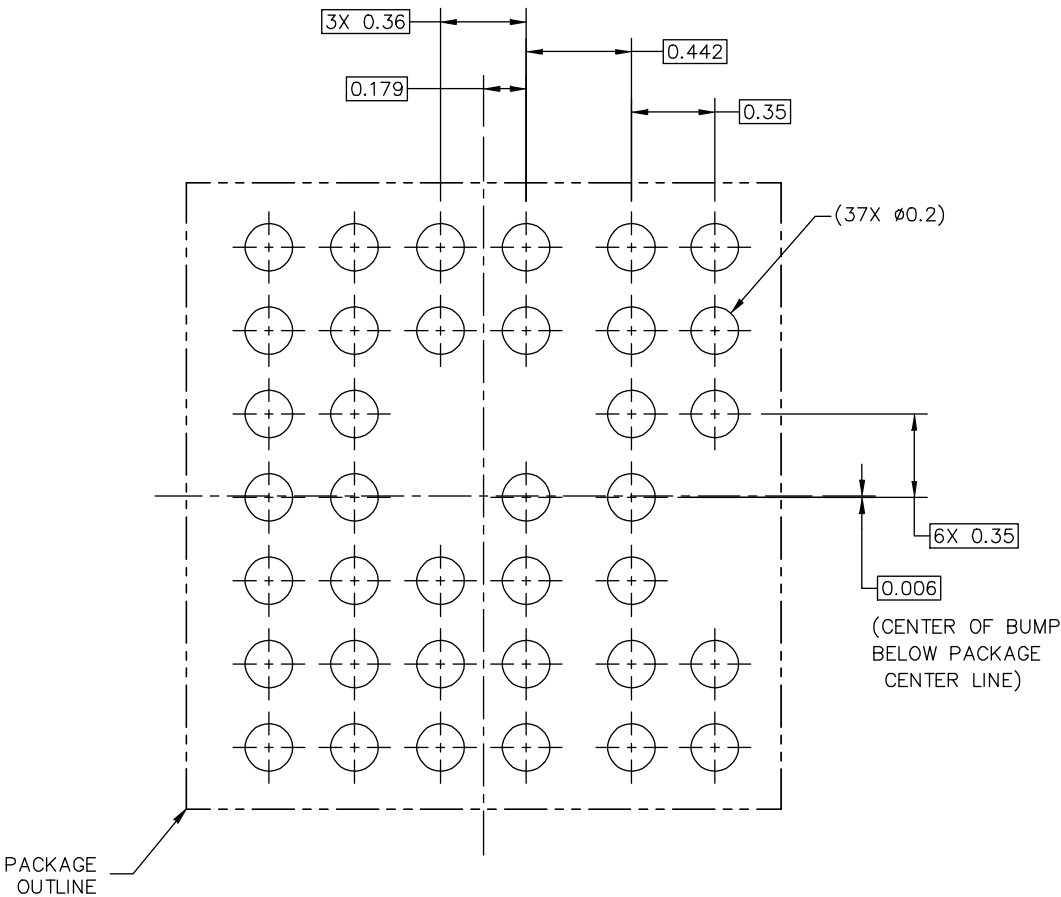


Figure 2. Reflow soldering footprint part1 for WLCSP37 (SOT2173-1)

WLCSP37, wafer level chip-size package; 37 terminals; 0.35 mm pitch; 2.63 mm x 2.495 mm x 0.49 mm body

WLCSP-37 I/O  
2.63 X 2.495 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2173-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 13 DEC 2023

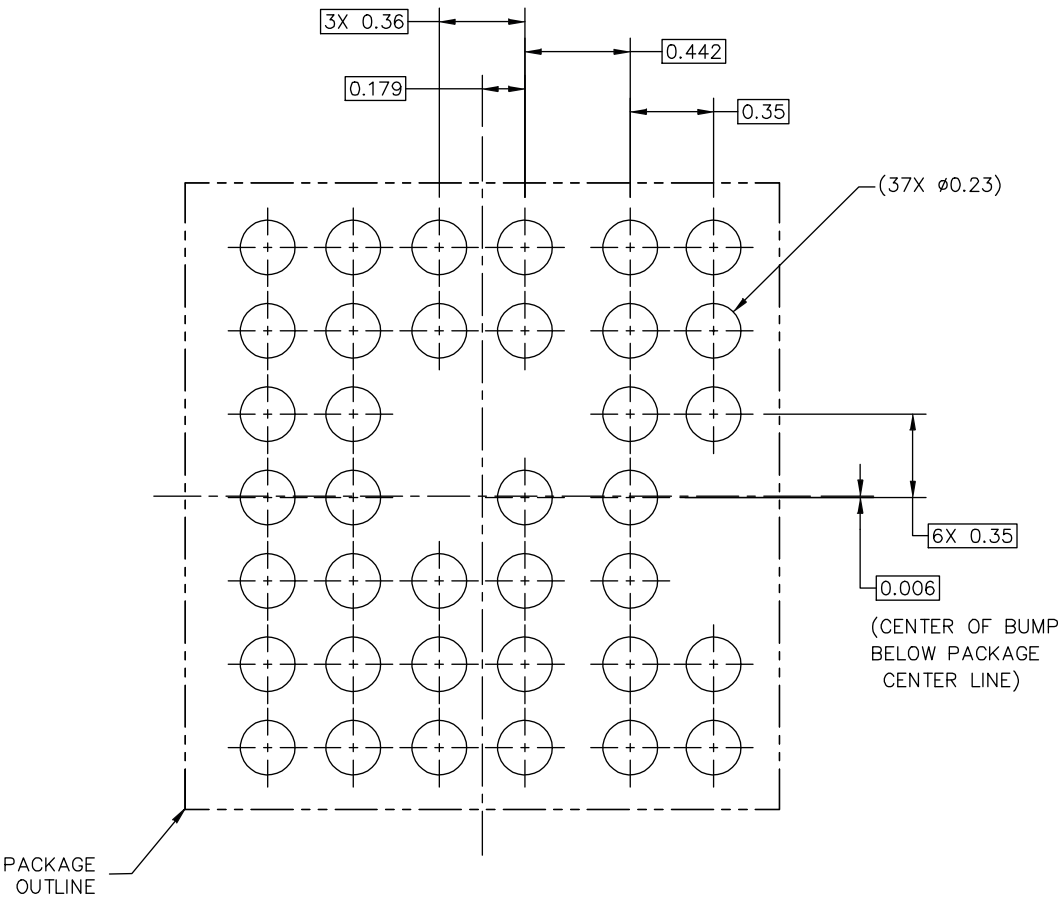
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02186D	REVISION: 0	
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Figure 3. Reflow soldering footprint part2 for WLCSP37 (SOT2173-1)

WLCSP37, wafer level chip-size package; 37 terminals; 0.35 mm pitch; 2.63 mm x 2.495 mm x 0.49 mm body

WLCSP-37 I/O  
2.63 X 2.495 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2173-1



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02186D	REVISION: 0	
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Figure 4. Reflow soldering footprint part3 for WLCSP37 (SOT2173-1)

WLCSP37, wafer level chip-size package; 37 terminals; 0.35 mm pitch; 2.63 mm x 2.495 mm x 0.49 mm body

WLCSP-37 I/O  
2.63 X 2.495 X 0.49 PKG, 0.35 PITCH (BACKSIDE COATING INCLUDED)

SOT2173-1

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 13 DEC 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA02186D	REVISION: 0	
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Figure 5. Package outline note WLCSP37 (SOT2173-1)

## 4 Legal information

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WLCSP37, wafer level chip-size package; 37 terminals; 0.35 mm pitch; 2.63 mm x 2.495 mm x 0.49 mm body

Contents

1	Package summary .....	1
2	Package outline .....	2
3	Soldering .....	3
4	Legal information .....	7