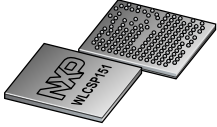


SOT2152-1

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

29 November 2024

Package information



1 Package summary

Terminal position code	P (perpendicular)
Package type descriptive code	WLCSP151
Package style descriptive code	WLCSP (wafer level chip-size package)
Package body material type	S (silicon)
Mounting method type	S (surface mount)
Issue date	04-05-2023
Manufacturer package code	98ASA01782D

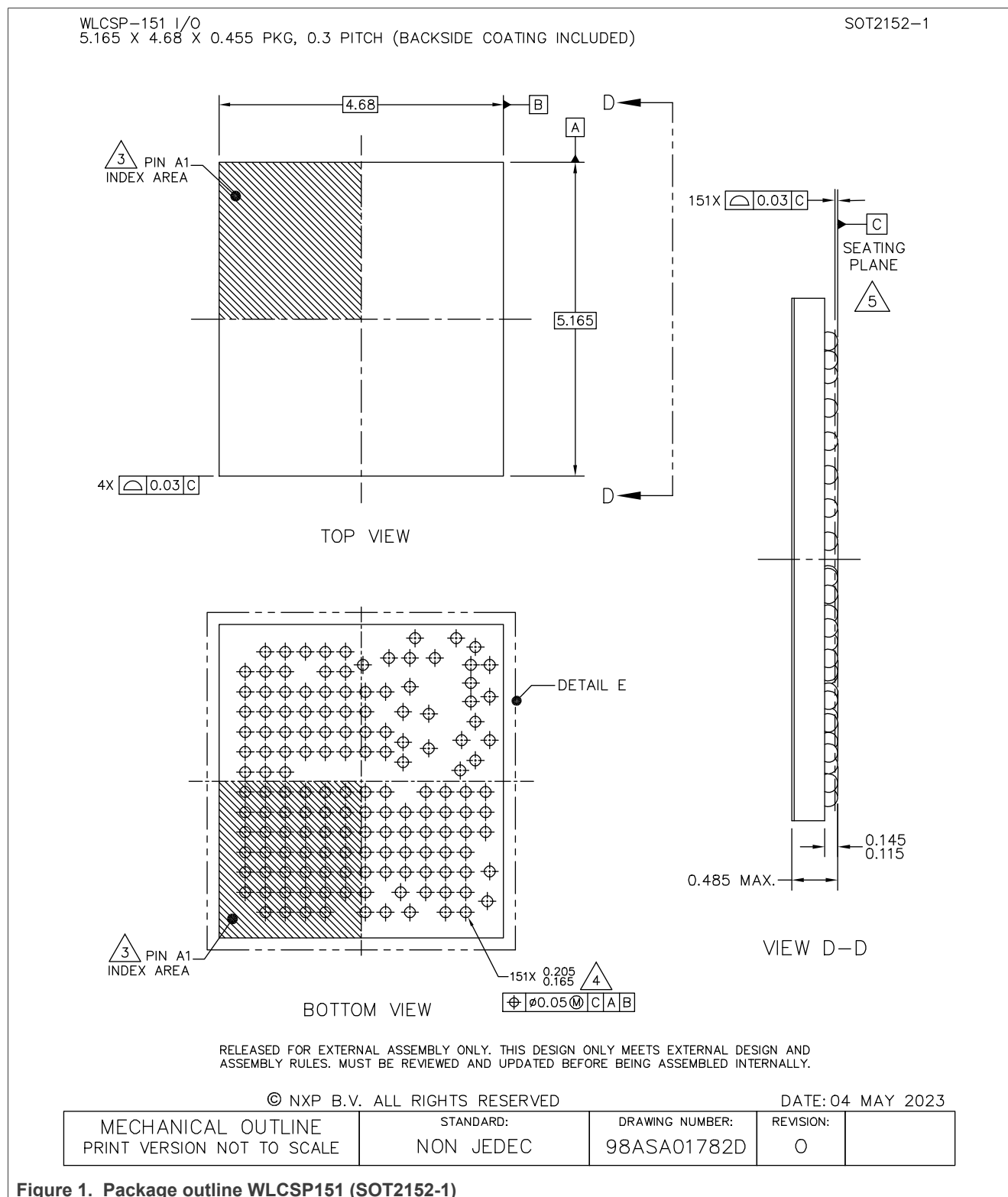
Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	5.135	5.165	5.195	mm
package width	4.65	4.68	4.71	mm
package height	0.425	0.455	0.485	mm
nominal pitch	-	0.3	-	mm



WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

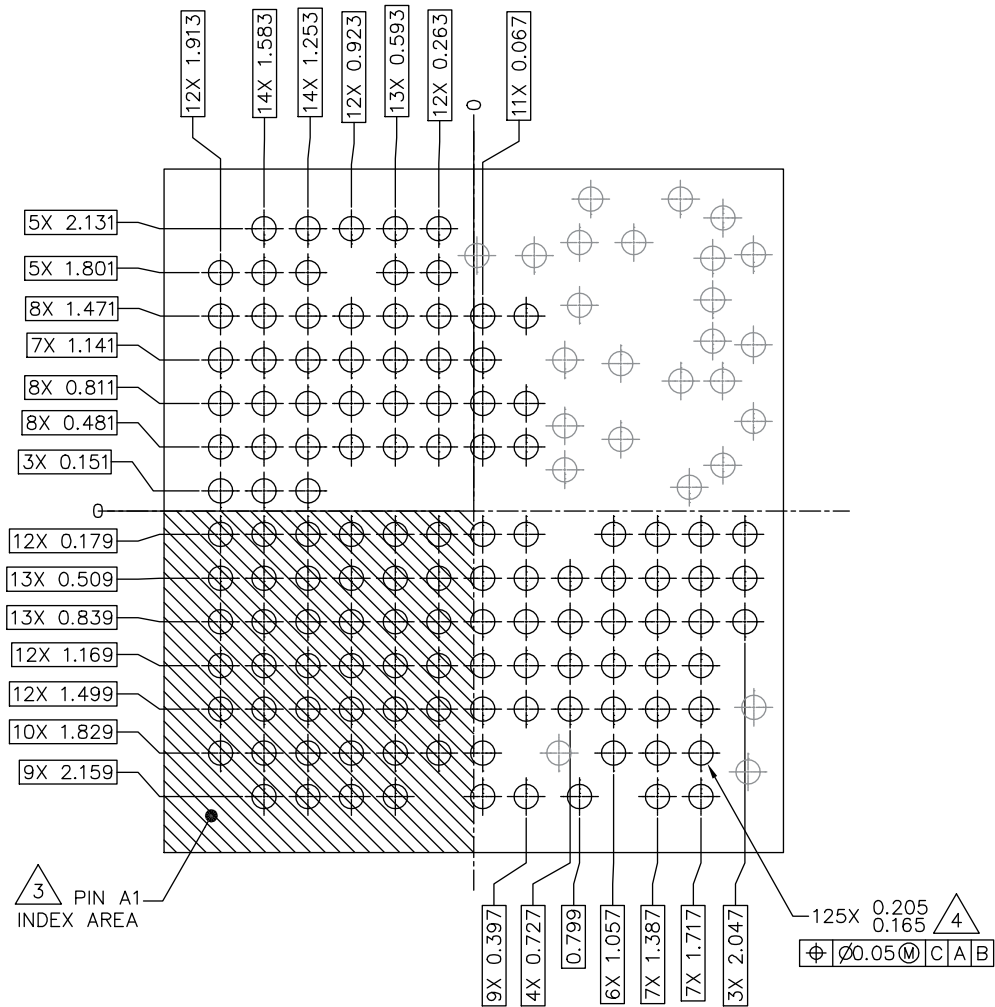
2 Package outline



WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1



DETAIL E (I)
(ARRAY BUMPS (125X))

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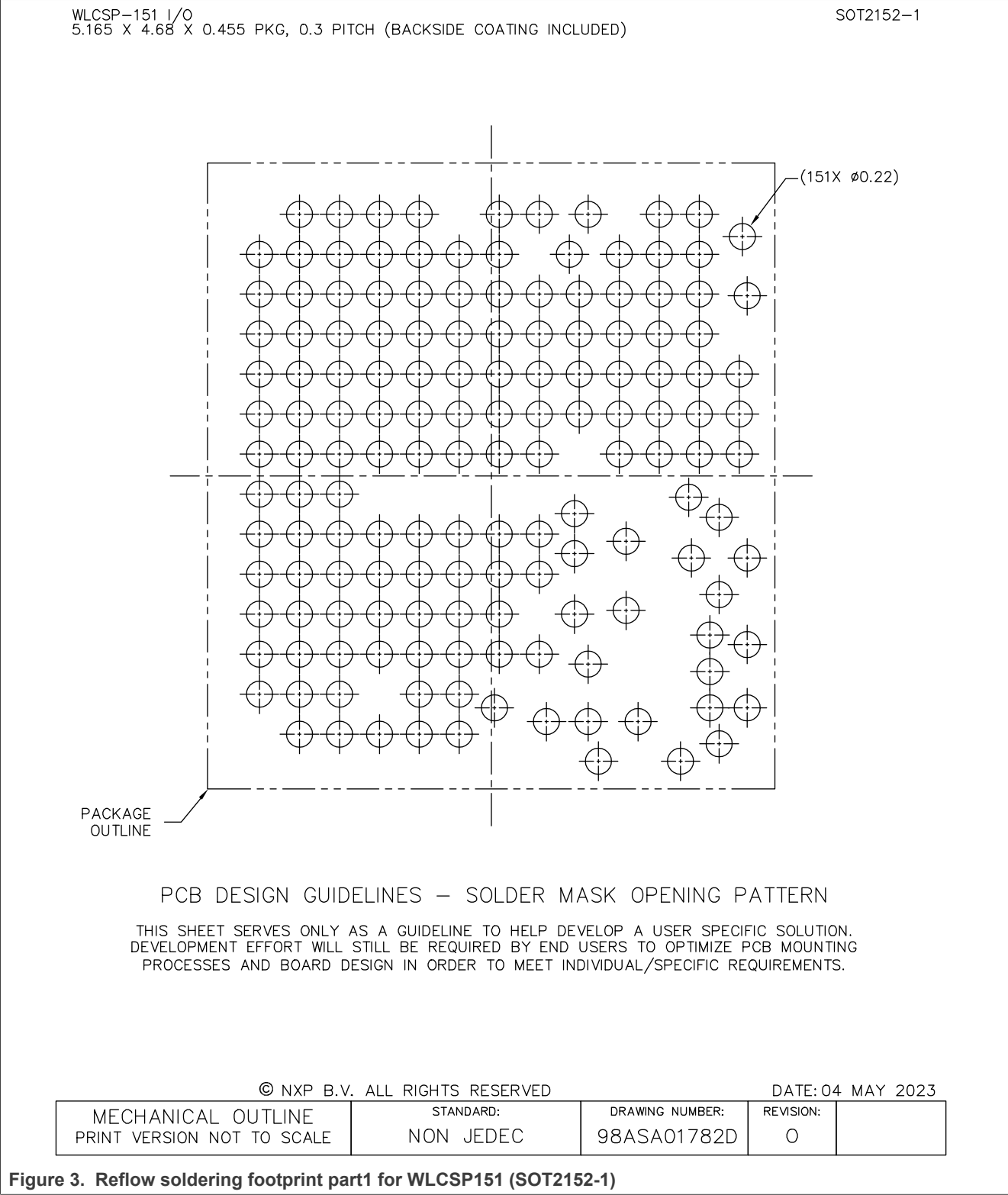
DATE: 04 MAY 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: 0	
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Figure 2. Package outline detail E of WLCSP151 (SOT2152-1)

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

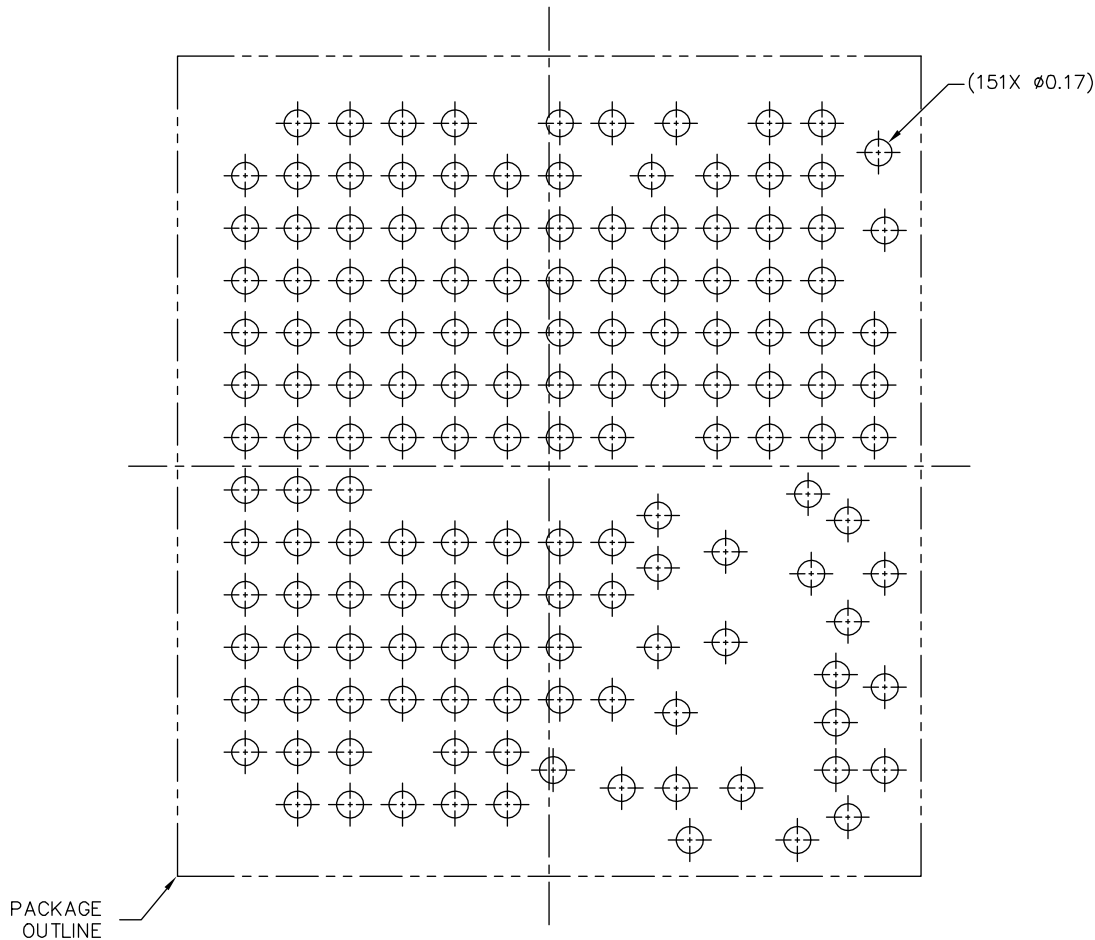
3 Soldering



WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 04 MAY 2023

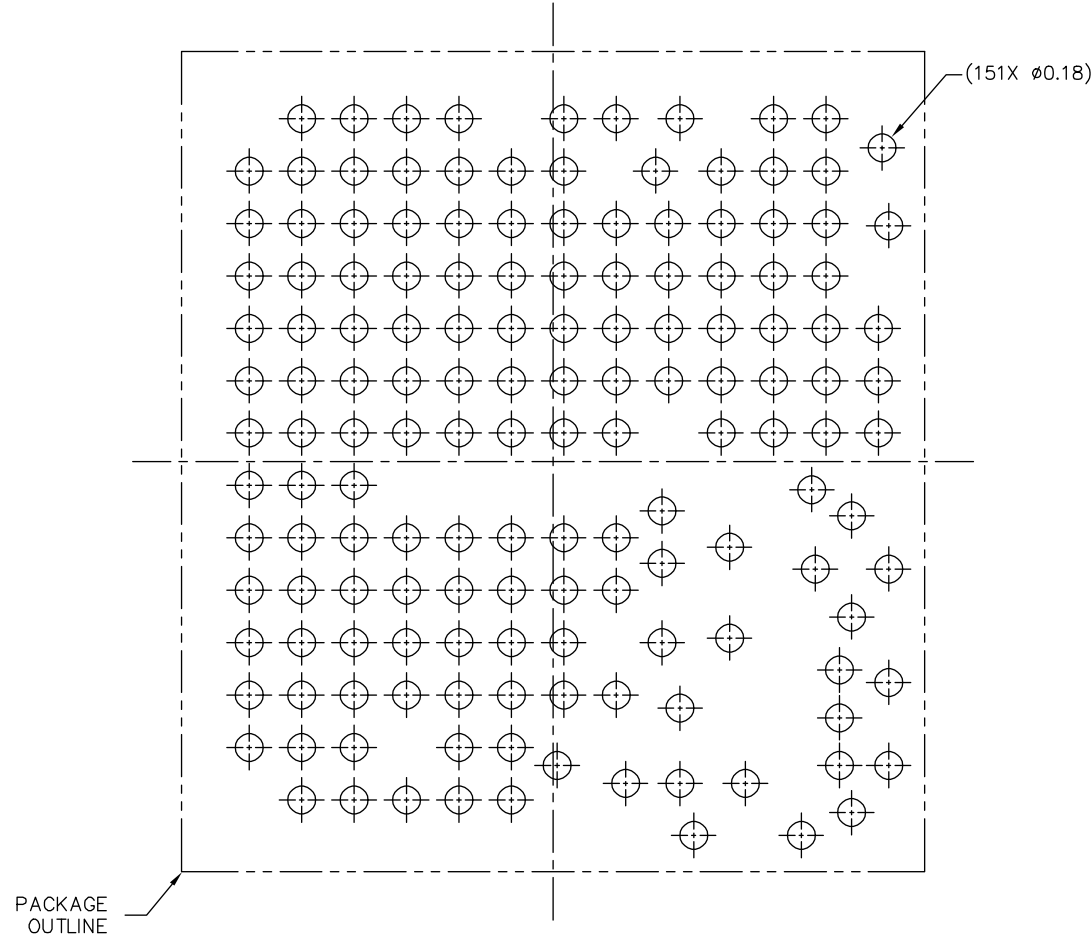
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: 0	
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Figure 4. Reflow soldering footprint part2 for WLCSP151 (SOT2152-1)

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1



RECOMMENDED STENCIL THICKNESS 0.08

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 5. Reflow soldering footprint part3 for WLCSP151 (SOT2152-1)

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

WLCSP-151 I/O
5.165 X 4.68 X 0.455 PKG, 0.3 PITCH (BACKSIDE COATING INCLUDED)

SOT2152-1

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
- 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
- 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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DATE: 04 MAY 2023

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01782D	REVISION: 0	
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Figure 6. Package outline note WLCSP151 (SOT2152-1)

WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

4 Legal information

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WLCSP151 wafer level chip-size package, 151 terminals, 0.3 mm pitch, 5.165 mm x 4.68 mm x 0.455 mm body (backside coating included)

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