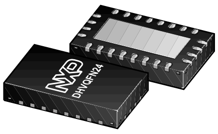


SOT2066-1

DHVQFN24, DIL-compatible thermal enhanced very thin quad flat package, no leads, 24 terminals, 0.5 mm pitch, 3 mm x 5 mm x 0.85 mm body

23 November 2020 Package information

1 Package summary

Terminal position code	Q (quad)
Package type descriptive code	DHVQFN24
Package style descriptive code	DHVQFN (DIL-compatible thermal enhanced very thin quad flatpack; no leads)
Mounting method type	S (surface mount)
Issue date	27-10-2020
Manufacturer package code	98ASA01638D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.9	3	3.1	mm
package width	4.9	5	5.1	mm
package height	-	0.85	1	mm
nominal pitch	-	0.5	-	mm
actual quantity of termination	-	24	-	

2 Package outline

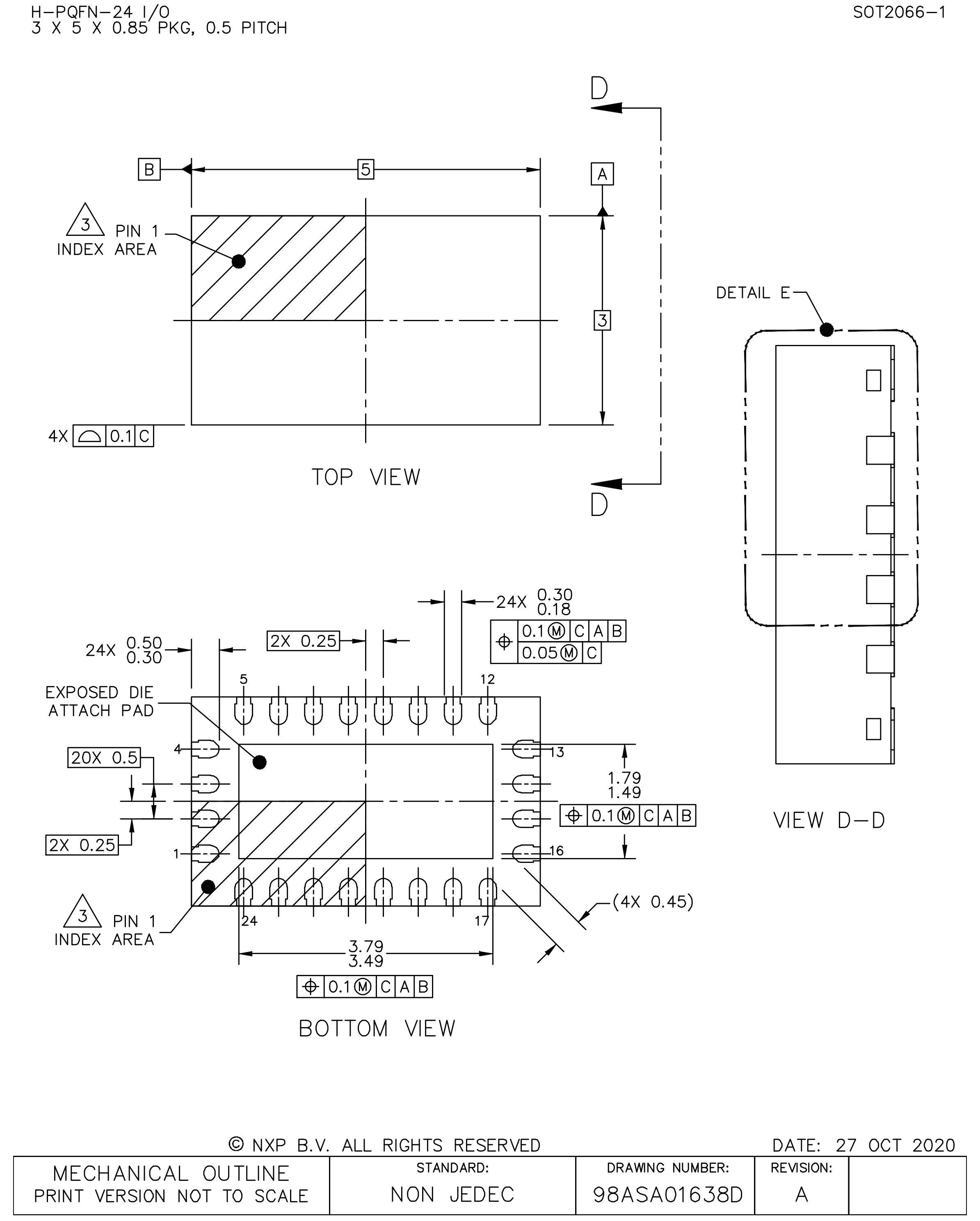
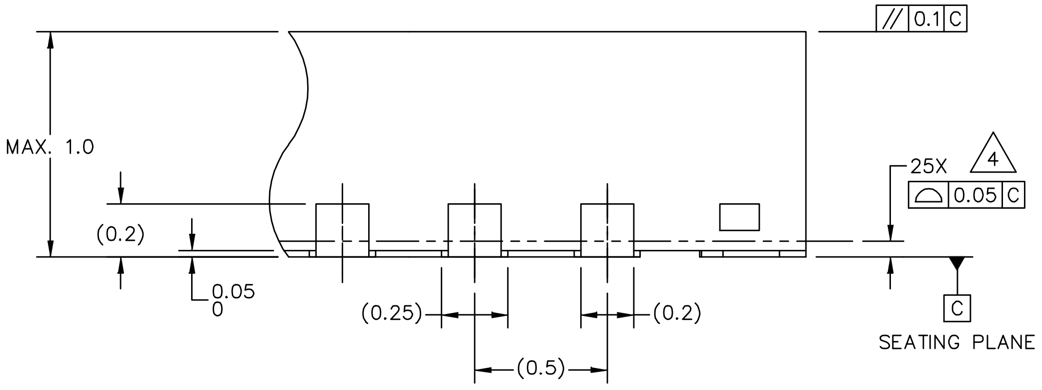


Figure 1. Package outline DHVQFN24 (SOT2066-1)

H-PQFN-24 I/O
3 X 5 X 0.85 PKG, 0.5 PITCH

SOT2066-1



DETAIL E
VIEW ROTATED 90° CW

DATE: 27 OCT 2020

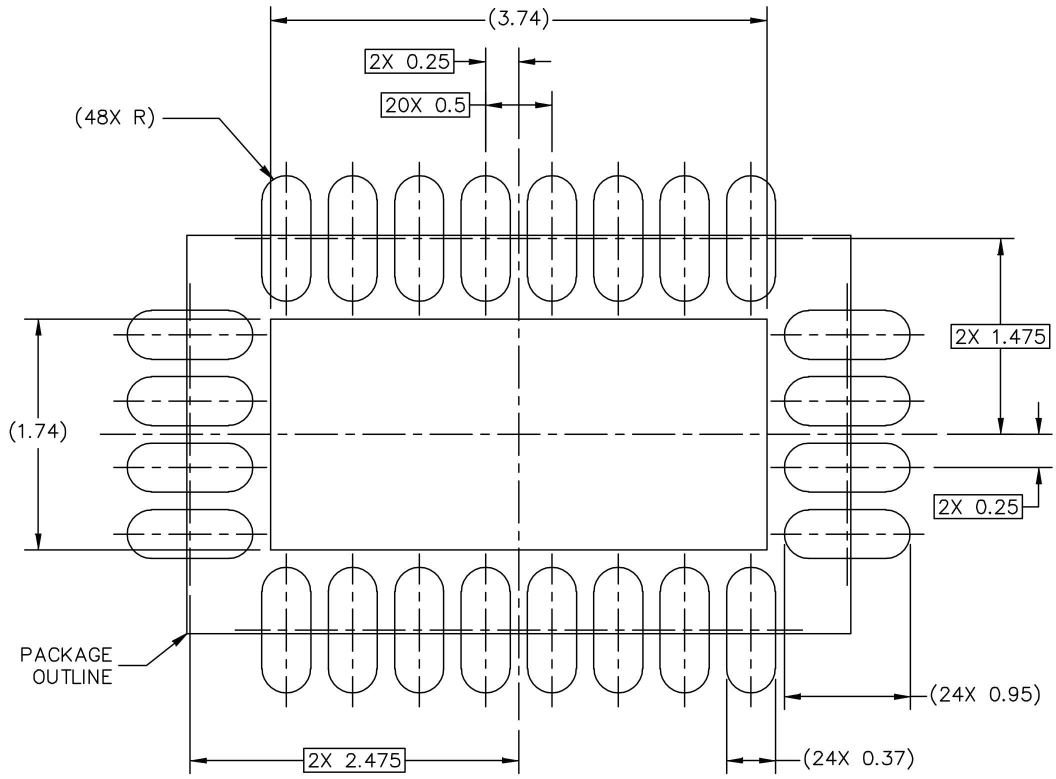
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01638D	REVISION: A	

Figure 2. Package outline detail of DHVQFN24 (SOT2066-1)

3 Soldering

H-PQFN-24 I/O
3 X 5 X 0.85 PKG, 0.5 PITCH

SOT2066-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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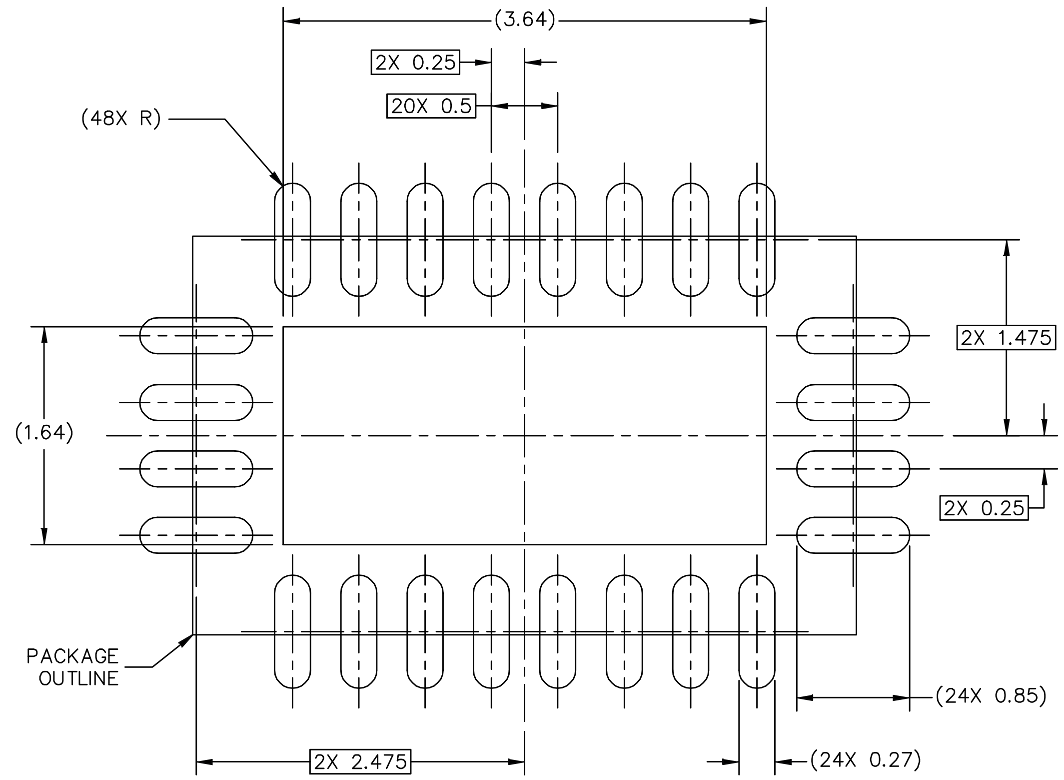
DATE: 27 OCT 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01638D	REVISION: A	

Figure 3. Reflow soldering footprint part1 for DHVQFN24 (SOT2066-1)

H-PQFN-24 I/O
3 X 5 X 0.85 PKG, 0.5 PITCH

SOT2066-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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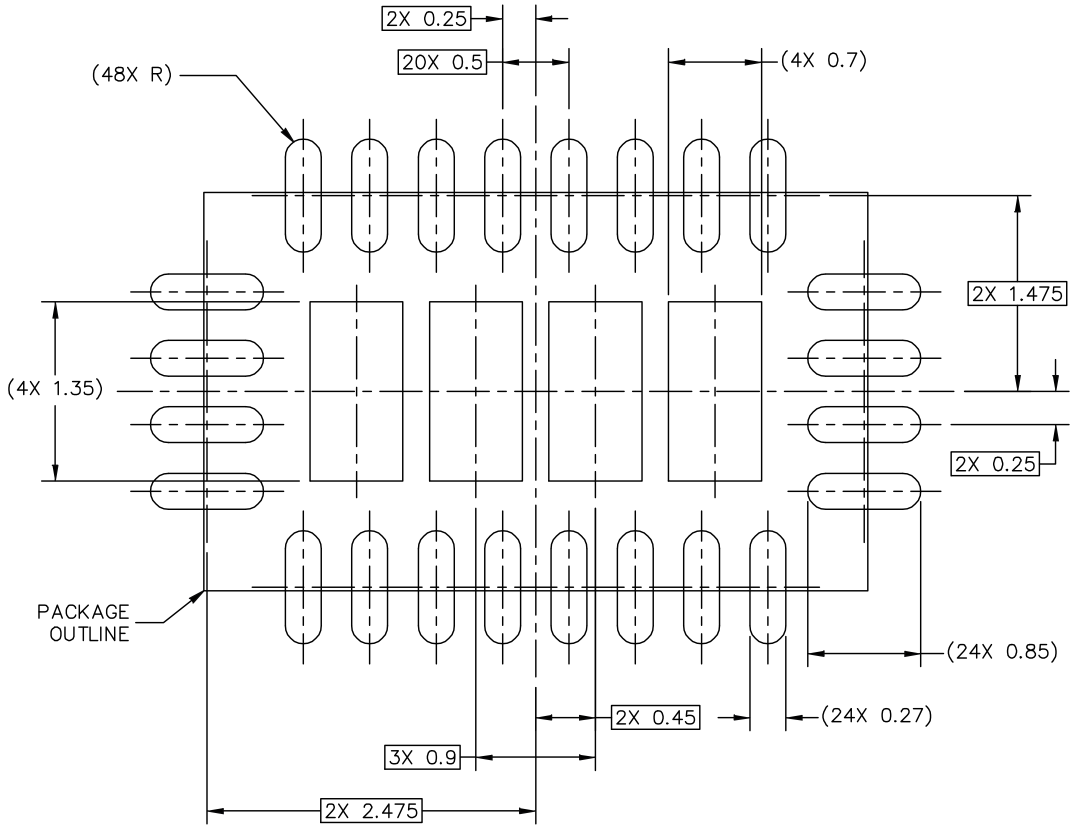
DATE: 27 OCT 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01638D	REVISION: A	

Figure 4. Reflow soldering footprint part2 for DHVQFN24 (SOT2066-1)

H-PQFN-24 I/O
3 X 5 X 0.85 PKG, 0.5 PITCH

SOT2066-1



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 27 OCT 2020

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01638D	REVISION: A	

Figure 5. Reflow soldering footprint part3 for DHVQFN24 (SOT2066-1)

H–PQFN–24 I/O
3 X 5 X 0.85 PKG, 0.5 PITCH

SOT2066–1

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

△3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

△4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.

5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

DATE: 27 OCT 2020

MECHANICAL OUTLINE	STANDARD:	DRAWING NUMBER:	REVISION:	
PRINT VERSION NOT TO SCALE	NON JEDEC	98ASA01638D	A	

Figure 6. Package outline note DHVQFN24 (SOT2066-1)

4 Legal information

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