

SOT1917-5

WLCSP72, wafer level chip-scale package; 72 bumps; 3.54 mm x 2.99 mm x 0.365 mm body (backside coating included)

15 August 2019

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP72
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	04-07-2019
Manufacturer package code	98ASA01472D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	3.51	3.54	3.57	mm
package width	2.95	2.99	3.02	mm
seated height	0.33	0.365	0.4	mm
nominal pitch	-	0.35	-	mm
actual quantity of termination	-	72	-	



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2 Package outline

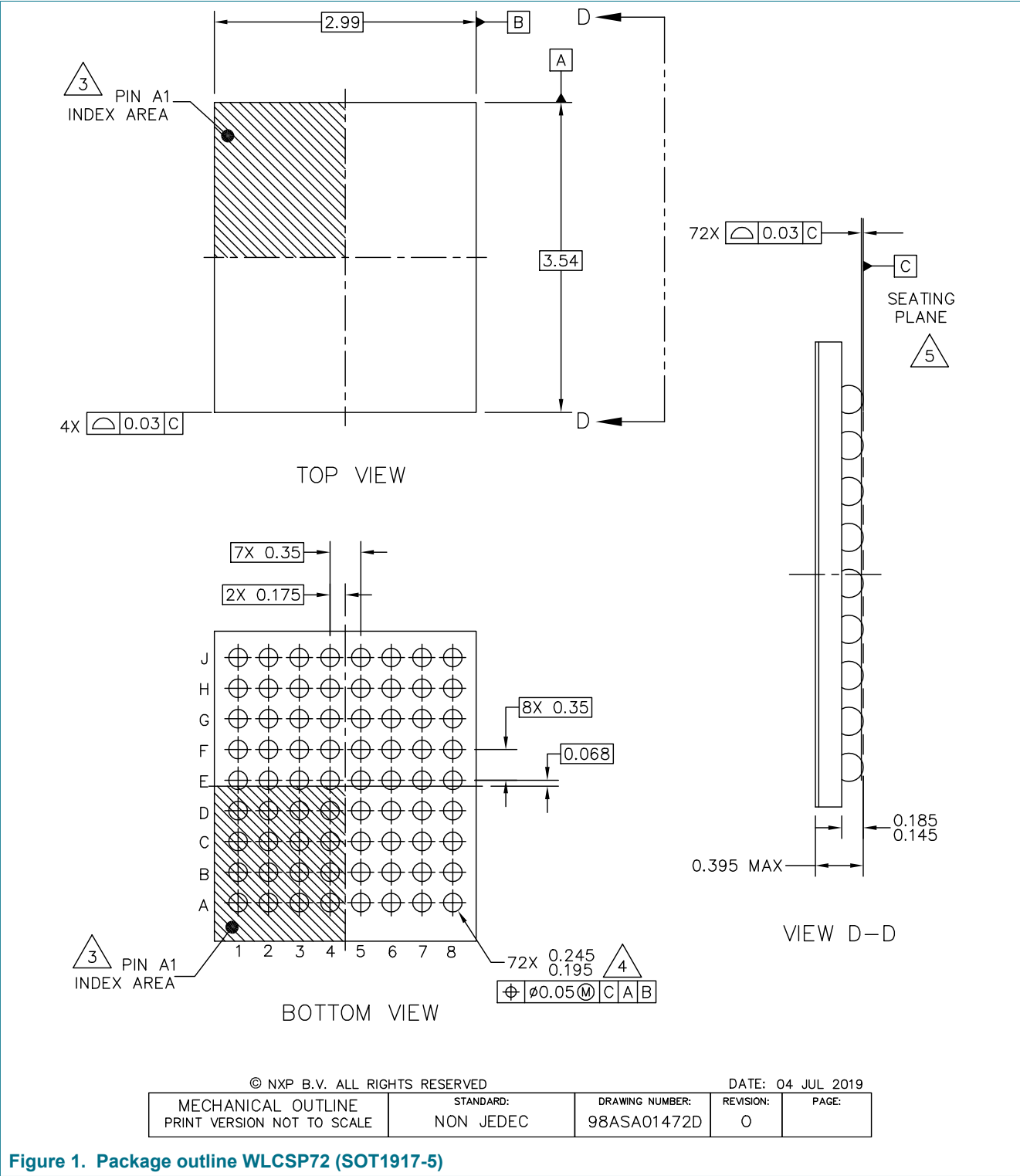


Figure 1. Package outline WLCSP72 (SOT1917-5)

WLCSP72, wafer level chip-scale package; 72 bumps; 3.54 mm x 2.99 mm x 0.365 mm body (backside coating included)

3 Soldering

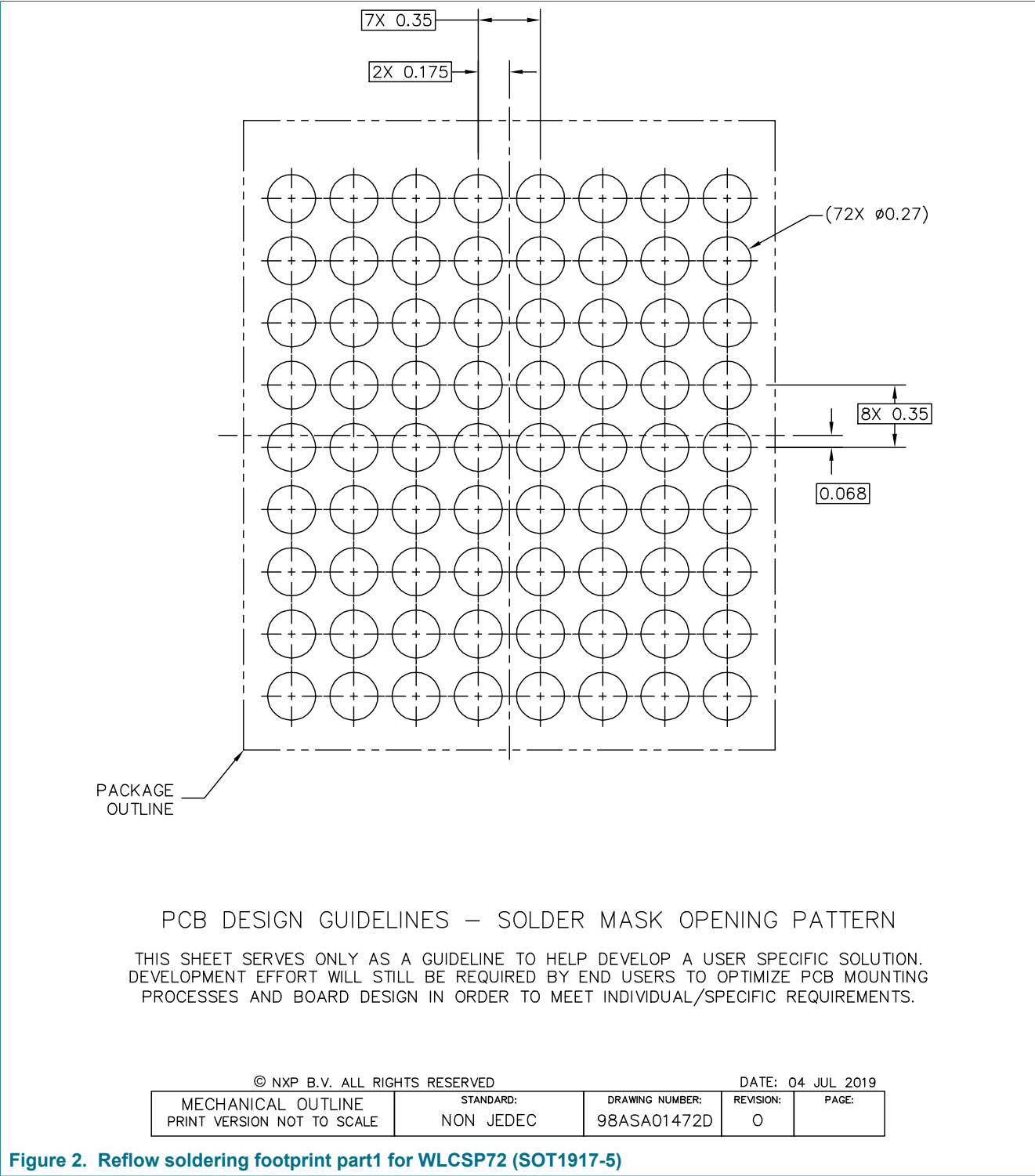


Figure 2. Reflow soldering footprint part1 for WLCSP72 (SOT1917-5)

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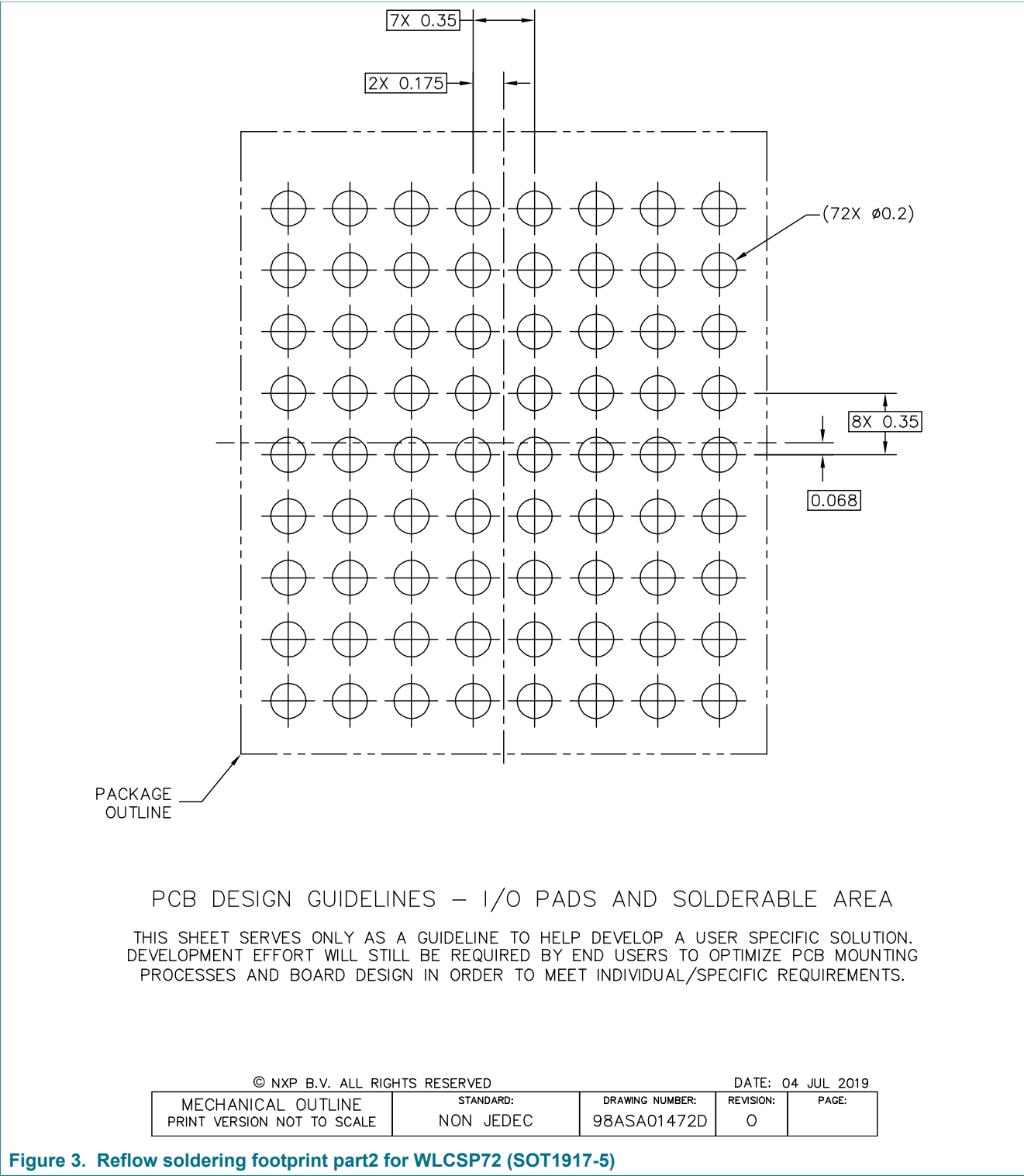


Figure 3. Reflow soldering footprint part2 for WLCSP72 (SOT1917-5)

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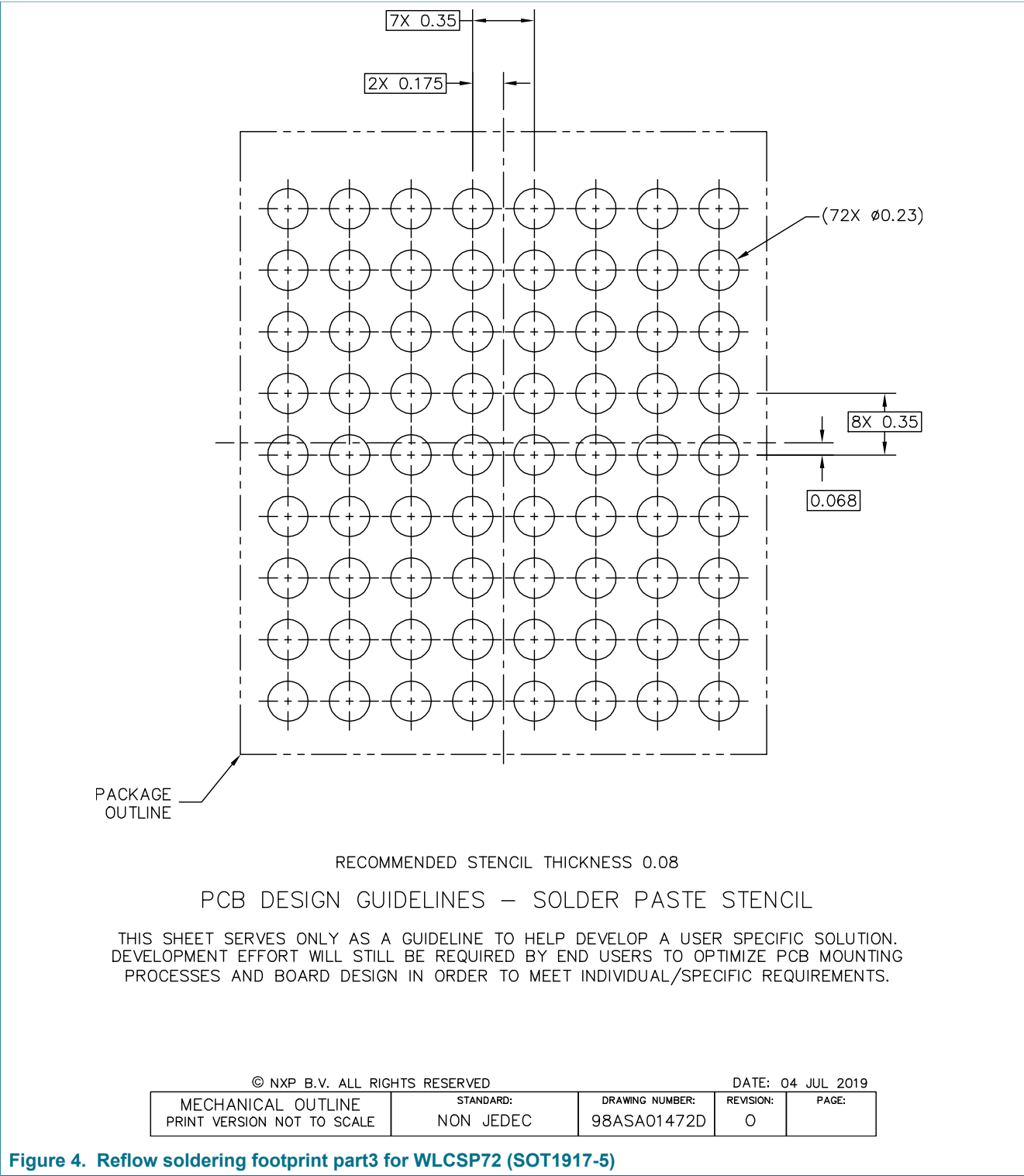


Figure 4. Reflow soldering footprint part3 for WLCSP72 (SOT1917-5)

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- NOTES:
- 1. ALL DIMENSIONS IN MILLIMETERS.
 - 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
 - 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
 - 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
 - 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 - 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01472D	REVISION: O	PAGE:

Figure 5. Package outline note WLCSP72 (SOT1917-5)

4 Legal information

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Contents

1	Package summary	1
2	Package outline	2
3	Soldering	3
4	Legal information	7