

SOT1780-6

WLCSP36, wafer level chip-scale package; 36 bumps; 0.4 mm pitch, 2.62 mm x 2.51 mm x 0.5 mm body

4 October 2017

Package information

1. Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP36
Package type industry code	WLCSP36
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	18-9-2017
Manufacturer package code	SOT1780-6

Table 1. Package summary

Symbol	Parameter		Min	Typ	Nom	Max	Unit
D	package length		-	-	2.62	-	mm
E	package width		-	-	2.51	-	mm
A	seated height		-	-	0.5	-	mm
e	nominal pitch		-	-	0.4	-	mm
n ₂	actual quantity of termination		-	-	36	-	A/A



2. Package outline

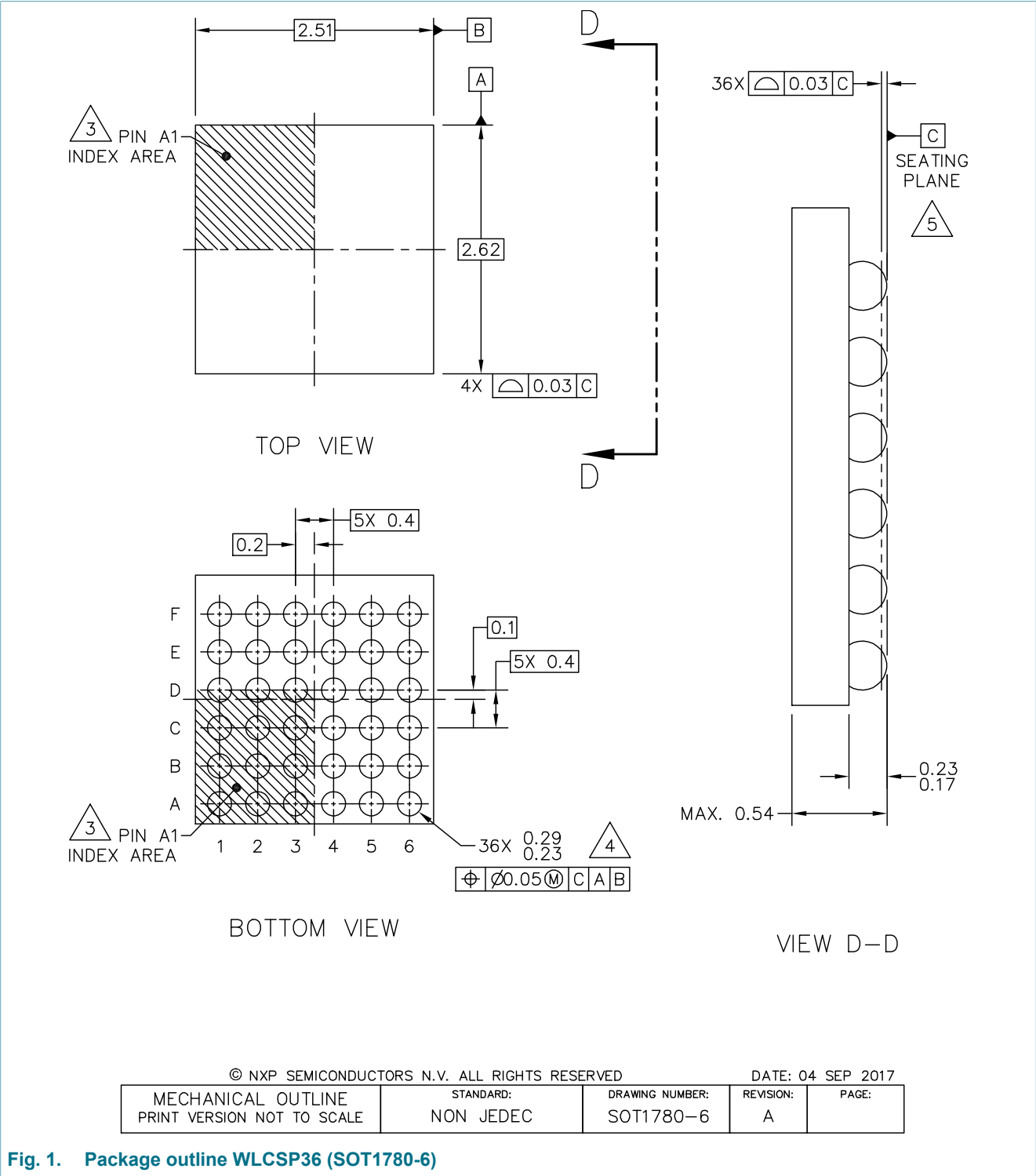


Fig. 1. Package outline WLCSP36 (SOT1780-6)

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NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.

5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

Fig. 2. Package outline note WLCSP36 (SOT1780-6)

3. Soldering

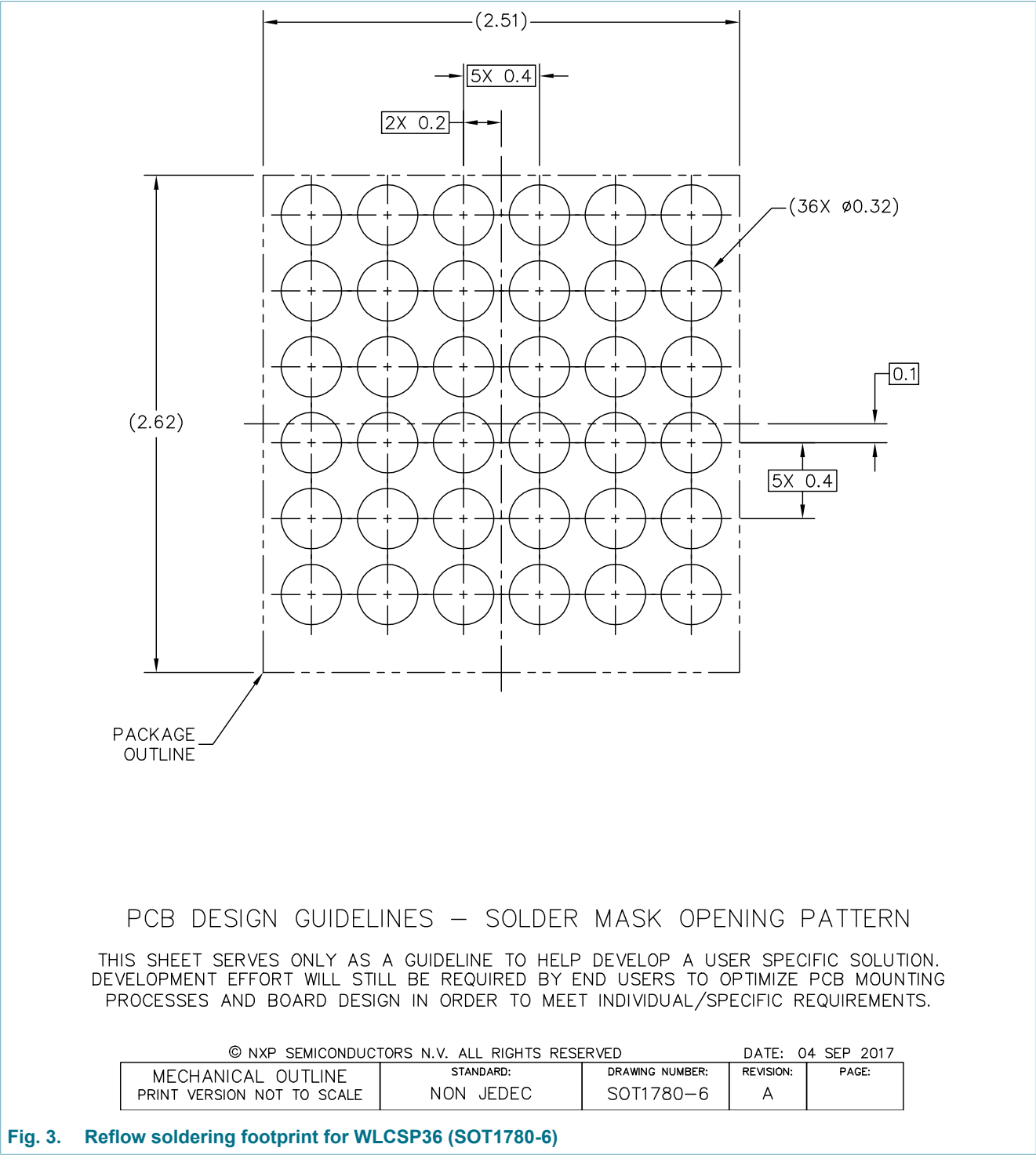
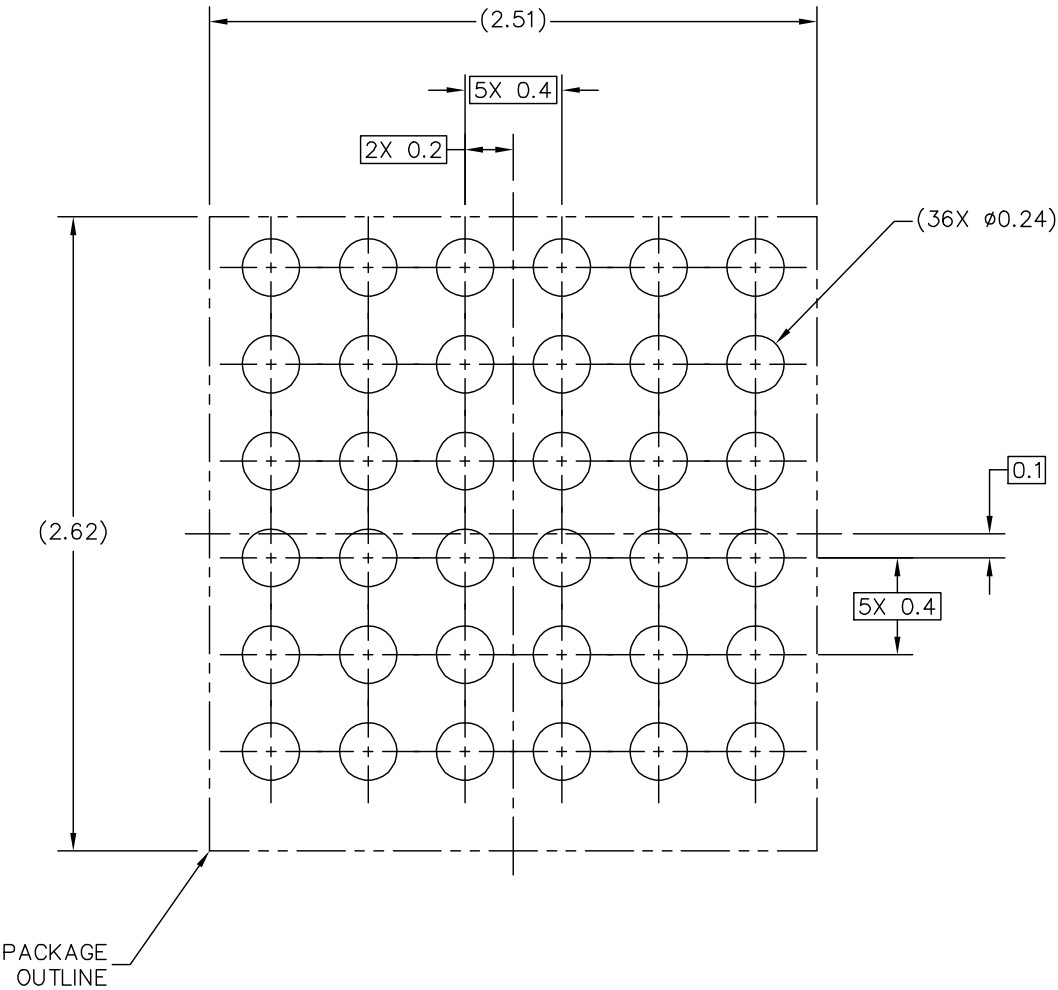


Fig. 3. Reflow soldering footprint for WLCSP36 (SOT1780-6)



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: SOT1780-6	REVISION: A	PAGE:

Fig. 4. Reflow soldering footprint part2 for WLCSP36 (SOT1780-6)

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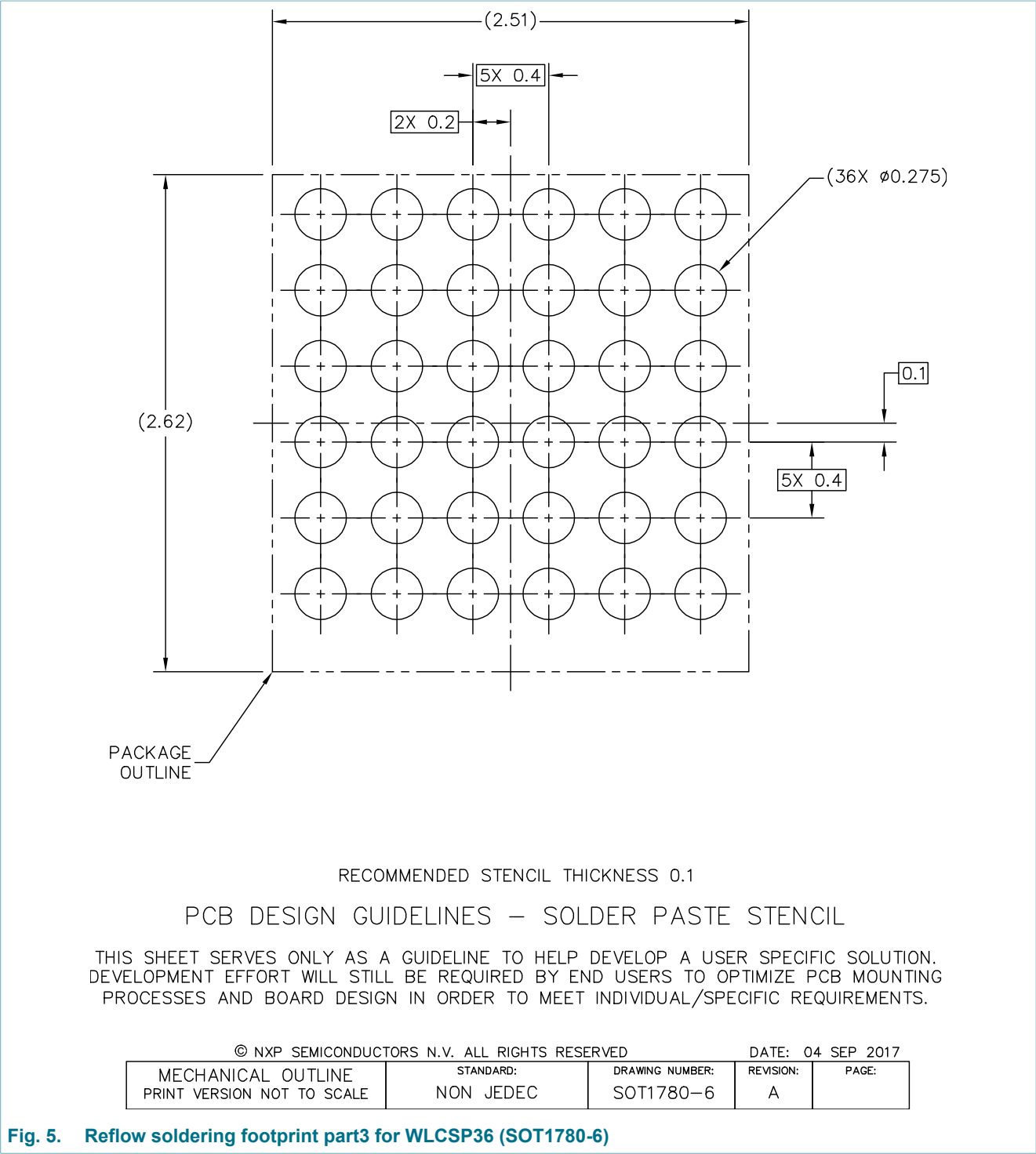


Fig. 5. Reflow soldering footprint part3 for WLCSP36 (SOT1780-6)

4. Legal information

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