

SOT1459-8

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm body (backside coating included)

11 December 2020

Package information

1 Package summary

Terminal position code	B (bottom)
Package type descriptive code	WLCSP42
Package style descriptive code	WLCSP (wafer level chip-size package)
Mounting method type	S (surface mount)
Issue date	03-12-2020
Manufacturer package code	98ASA01726D

Table 1. Package summary

Parameter	Min	Nom	Max	Unit
package length	2.69	2.72	2.75	mm
package width	2.99	3.02	3.05	mm
package height	-	0.525	0.565	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	42	-	



WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm
body (backside coating included)

2 Package outline

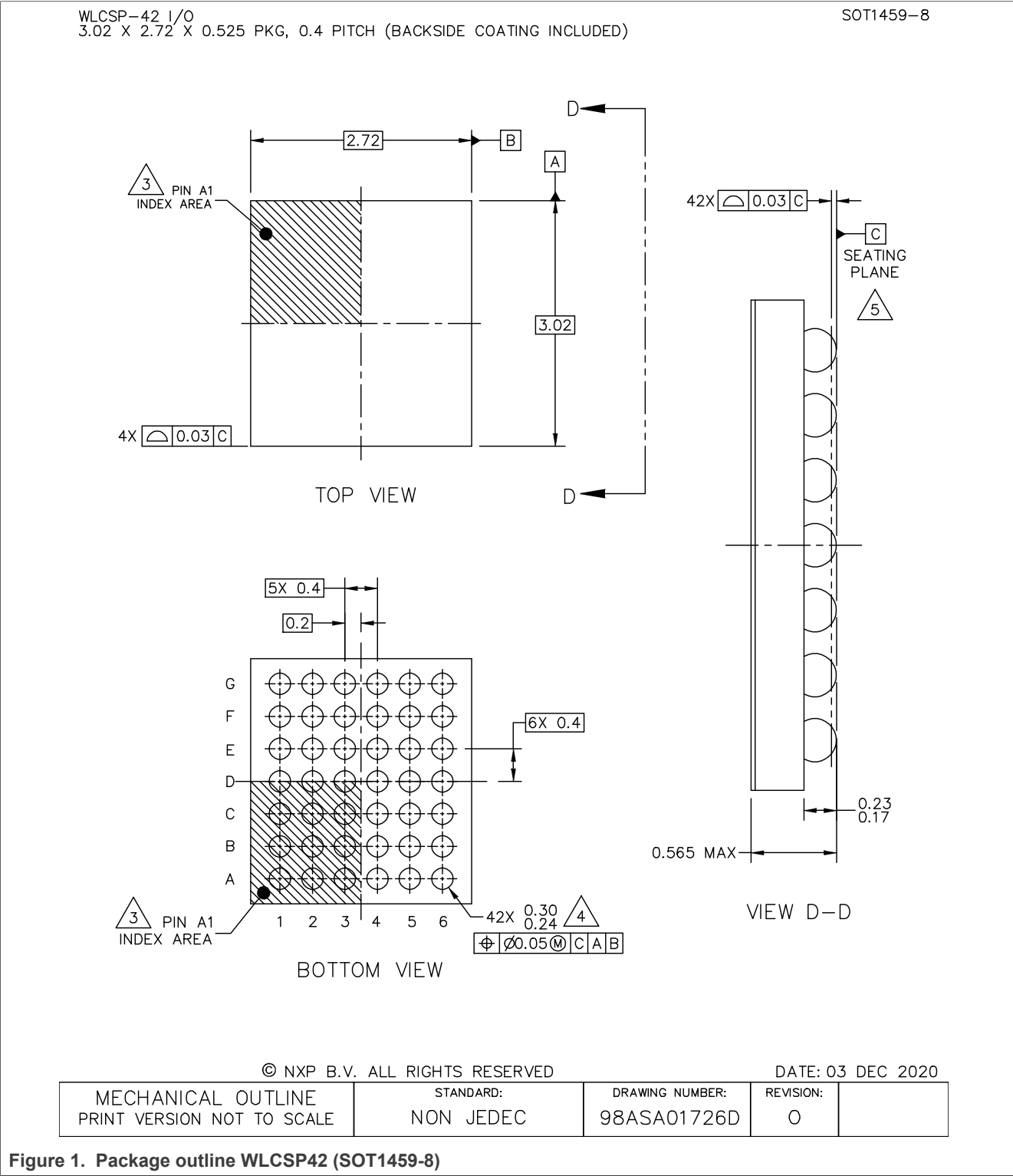
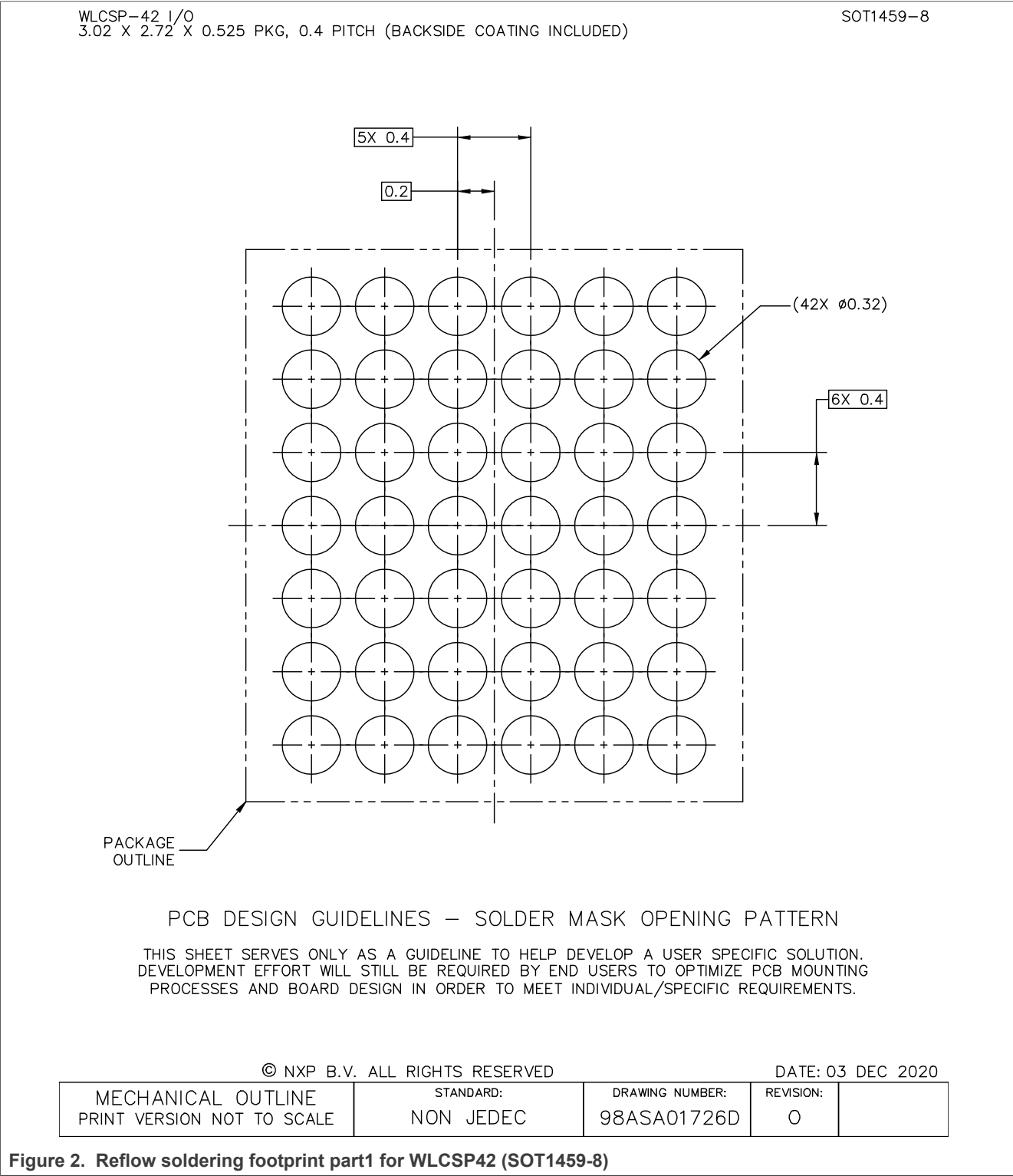


Figure 1. Package outline WLCSP42 (SOT1459-8)

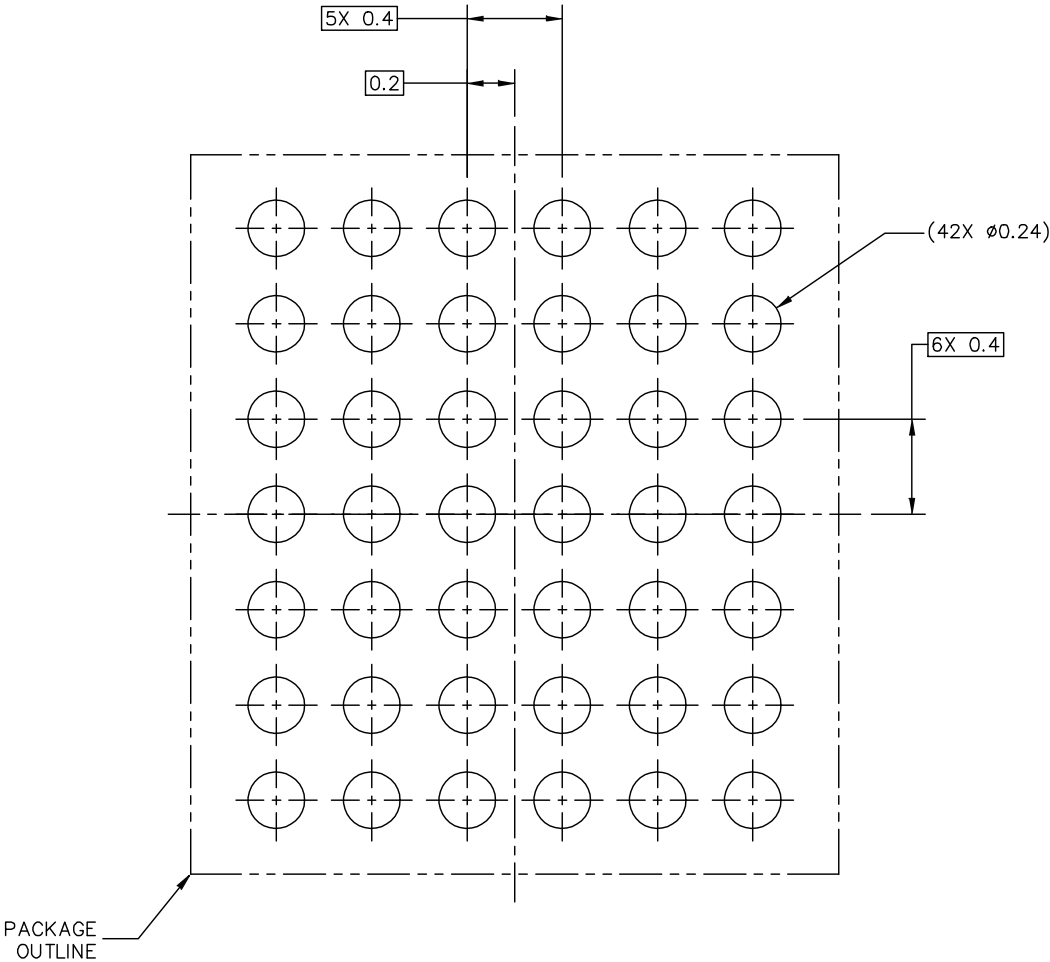
WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm
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3 Soldering



WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm
body (backside coating included)

WLCSP-42 I/O
3.02 X 2.72 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED) SOT1459-8



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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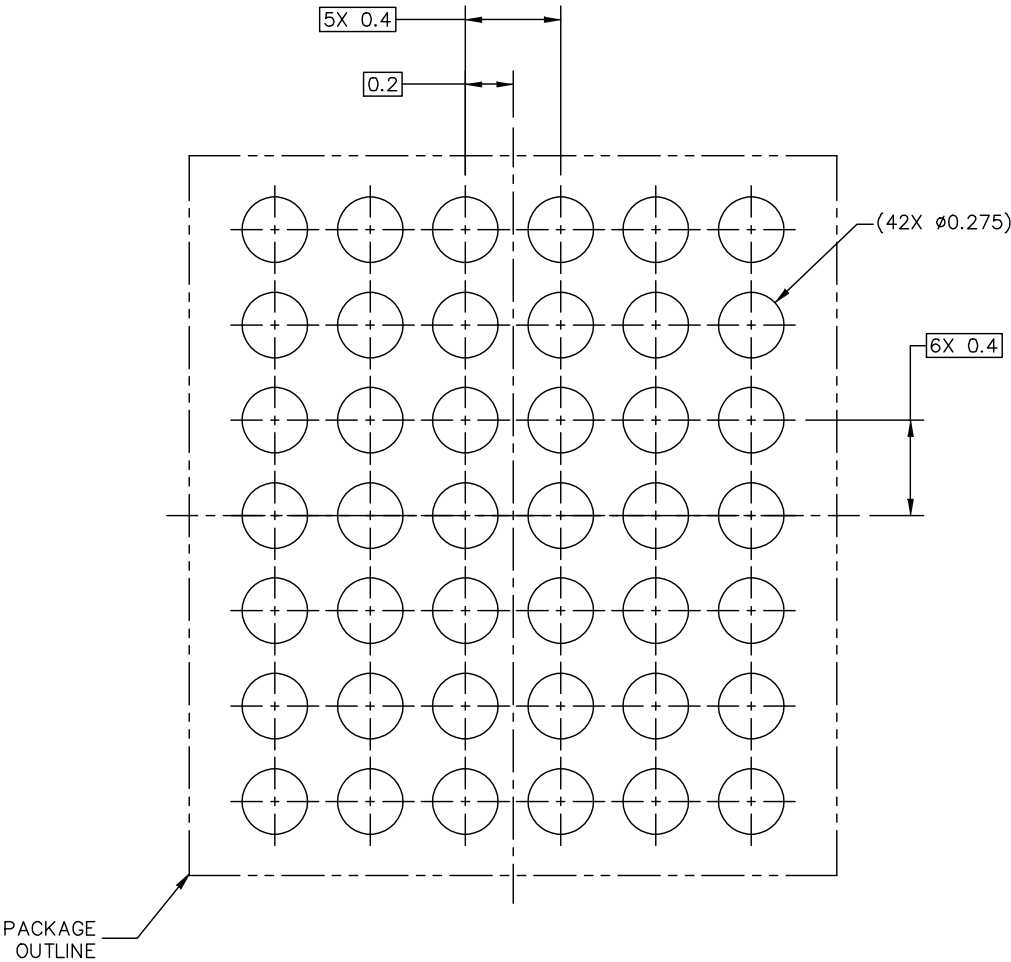
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01726D	REVISION: O	
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Figure 3. Reflow soldering footprint part2 for WLCSP42 (SOT1459-8)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm
body (backside coating included)

WLCSP-42 I/O
3.02 X 2.72 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459-8



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Figure 4. Reflow soldering footprint part3 for WLCSP42 (SOT1459-8)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm
body (backside coating included)

WLCSP-42 I/O
3.02 X 2.72 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459-8

- NOTES:
- 1. ALL DIMENSIONS IN MILLIMETERS.
 - 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - 3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
 - 4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
 - 5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 - 6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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Figure 5. Package outline note WLCSP42 (SOT1459-8)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm body (backside coating included)

WLCSP-42 I/O
3.02 X 2.72 X 0.525 PKG, 0.4 PITCH (BACKSIDE COATING INCLUDED)

SOT1459-8

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Figure 6. Package outline note WLCSP42 (SOT1459-8)

WLCSP42, wafer level chip scale package, 42 terminals, 0.4 mm pitch, 3.02 mm x 2.72 mm x 0.525 mm
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