

WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 2.915 mm x 3.142 mm x 0.564 mm body

28 May 2018

Package information

# 1. Package summary

Terminal position code B (bottom)

Package type descriptive code WLCSP49

Package style descriptive code WLCSP (wafer level chip-size package)

Mounting method type S (surface mount)

Issue date20-4-2018Manufacturer package code98ASA00718D

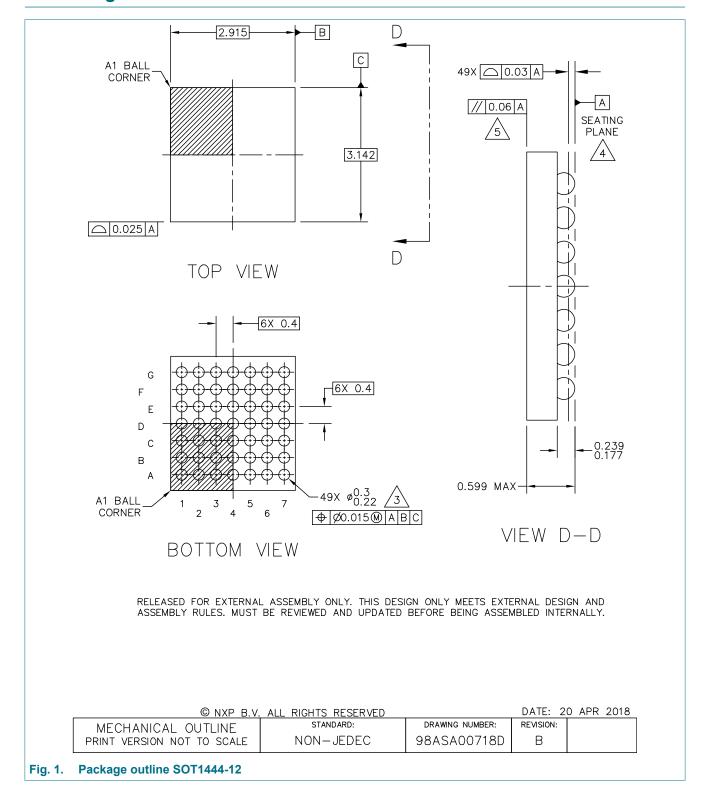
#### **Table 1. Package summary**

Parameter	Min	Nom	Max	Unit
package length	-	3.142	-	mm
package width	-	2.915	-	mm
seated height	-	0.564	-	mm
nominal pitch	-	0.4	-	mm
actual quantity of termination	-	49	-	A/A



WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 2.915 mm x 3.142 mm x 0.564 mm body

# 2. Package outline



WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 2.915 mm x 3.142 mm x 0.564 mm body

### NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5-2009.

<u>/3.\</u>

MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.

<u>/ 4.\</u>

DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5.

PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

© NXP B.V. ALL RIGHTS RESERVED

MECHANICAL OUTLINE STANDARD: DRAWING NUMBER: REVISION: PRINT VERSION NOT TO SCALE NON-JEDEC 98ASA00718D B

Fig. 2. Package outline note WLCSP49 (SOT1444-12)

WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 2.915 mm x 3.142 mm x 0.564 mm

## 3. Legal information

#### **Disclaimers**

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

WLCSP49, wafer level chip-scale package, 49 terminals, 0.4 mm pitch, 2.915 mm x 3.142 mm x 0.564 mm body

## 4. Contents

1.	Package summary	1
2.	Package outline	2
3.	Legal information	4
© N	NXP B.V. 2018. All rights reserved	
For	more information, please visit: http://www.nxp.com sales office addresses, please send an email to: salesaddresses@nxp.com te of release: 28 May 2018	