AN11878

TEA19362T GreenChip SMPS control IC

Rev. 1 — 5 October 2017

Application note

Table 1. Revision history

Rev	Date	Description
v.1	20171005	first issue

1   Introduction

This application note describes the implementation of TEA19362T functions in practical applications. Information is provided on a practical converter design.

The TEA19362T only operates in Fixed Frequency (FF) DCM mode. It is intended for mobile applications using touch screens requiring high spectral purity from the supply to prevent disturbance of the touchscreen operation.

Additional family members are TEA19361T, TEA19363T, TEA19363LT, and TEA1938T.

The TEA19361T operates in DCM mode and QR mode with valley switching for optimal efficiency. The burst mode is optimized for minimal audible noise. It is suited for applications using touch screens with standard Common Mode Noise requirements.

The TEA19363 operation can be compared with the TEA19361T operation, but it also includes active X-capacitor discharge. Furthermore, the TEA19363 comes in a latched (TEA19363LT) and a non-latched version (TEA19363T). When an OVP or OTP exception occurs, the latched version halts operation. The non-latched version initially halts and then resumes operation via a safe restart strategy. The higher Common Mode Noise due to the X-capacitor discharge function makes it less suitable for applications with touchscreen.

The TEA1938T is comparable to the TEA19361T. It contains a different burst mode, which is optimized for minimum ripple. The HV pin and VCCH pin have an ESD rating of 2 kV (for the TEA1936x, the level is 1 kV). It is suited for applications using touchscreens with standard Common Mode Noise requirements.

Each section can be read as a standalone description with few cross-references to other parts of the application note or the data sheet. Unless stated otherwise, typical values are given to enhance the readability.

2   Features and applications

2.1   General features

- Switched-Mode Power Supply (SMPS) controller IC supporting smart-charging applications and multiple-output-voltage applications
- Wide output range (5 V to 20 V in Constant Voltage (CV) mode, 3 V to 20 V in Constant Current (CC) mode, and 3 V to 6.5 V for direct charging)
- FF DCM mode operation at all power levels, including burst mode. Suited for mobile charger applications that require low CMN and high spectral purity (touchscreens)
- Small SO10 package
- Adaptive dual supply for highest efficiency over the entire output voltage range
- Integrated high-voltage start-up
- Continuous VCC regulation during start-up and protection via the HV pin, allowing minimum values for the buffer capacitors that are connected to the VCCL and VCCH pins
- Reduced optocoupler current enabling low no-load power (20 mW at 5 V output)
- Fast transient response from zero to full load
- Minimal output voltage ripple in all operating modes
- Integrated soft start

2.2 Green features

Enables high efficiency operation over a wide power range via:

- Low supply current during normal operation (0.6 mA without load)
- Low supply current during non-switching state in burst mode (0.2 mA)
- Demagnetization switching to minimize switching losses
- DCM controller can be used in combination with NXP Semiconductors Synchronous Rectification (SR) controllers for optimal efficiency performance

2.3 Protection features

- Mains voltage compensated OverPower Protection (OPP)
- OverTemperature Protection (OTP)
- Integrated overpower timeout
- Integrated restart timer for system fault conditions
- Continuous mode protection using demagnetization detection
- Accurate OverVoltage Protection (OVP)
- General-purpose input for safe restart protection; used with system OverTemperature Protection (OTP)
- Driver maximum on-time protection
- Brownin and brownout protection
- The TEA19362T OVP and OTP protections are safe restart protections

2.4 Applications

- Supports multiple-output-voltage applications
- Easy implementation of a USB-PD (type C) application together with the NXP Semiconductors TEA1903 or TEA1905 secondary side controllers
- Allows easy implementation of a direct charge application using Constant Voltage (CV) and Constant Current (CC) mode
- Touchscreen applications, like mobile phones, tablets, netbooks, and notebook adapters and chargers.

3 Functional description

This section describes the functional behavior of the TEA19362T IC on the primary side of an SMPS application. The TEA19362T can operate with various implementations of the secondary side of the SMPS:

- Single fixed voltage SMPS, e.g. a single 19.5 V output voltage (for notebooks)
- Multiple fixed voltages SMPS, e.g. simultaneous 12 V and 5 V output voltages
- Single variable voltages SMPS, e.g. 5 V, 9 V, 12 V, or 19.5 V switchable or autoswitchable output voltage (for USB-PD) that typically uses a TEA1903 or TEA1905 secondary controller

3.1 Application - primary side

The general behavior of the primary side of the applications that use the TEA19362T is explained using the elementary circuit diagram shown in Figure 1.

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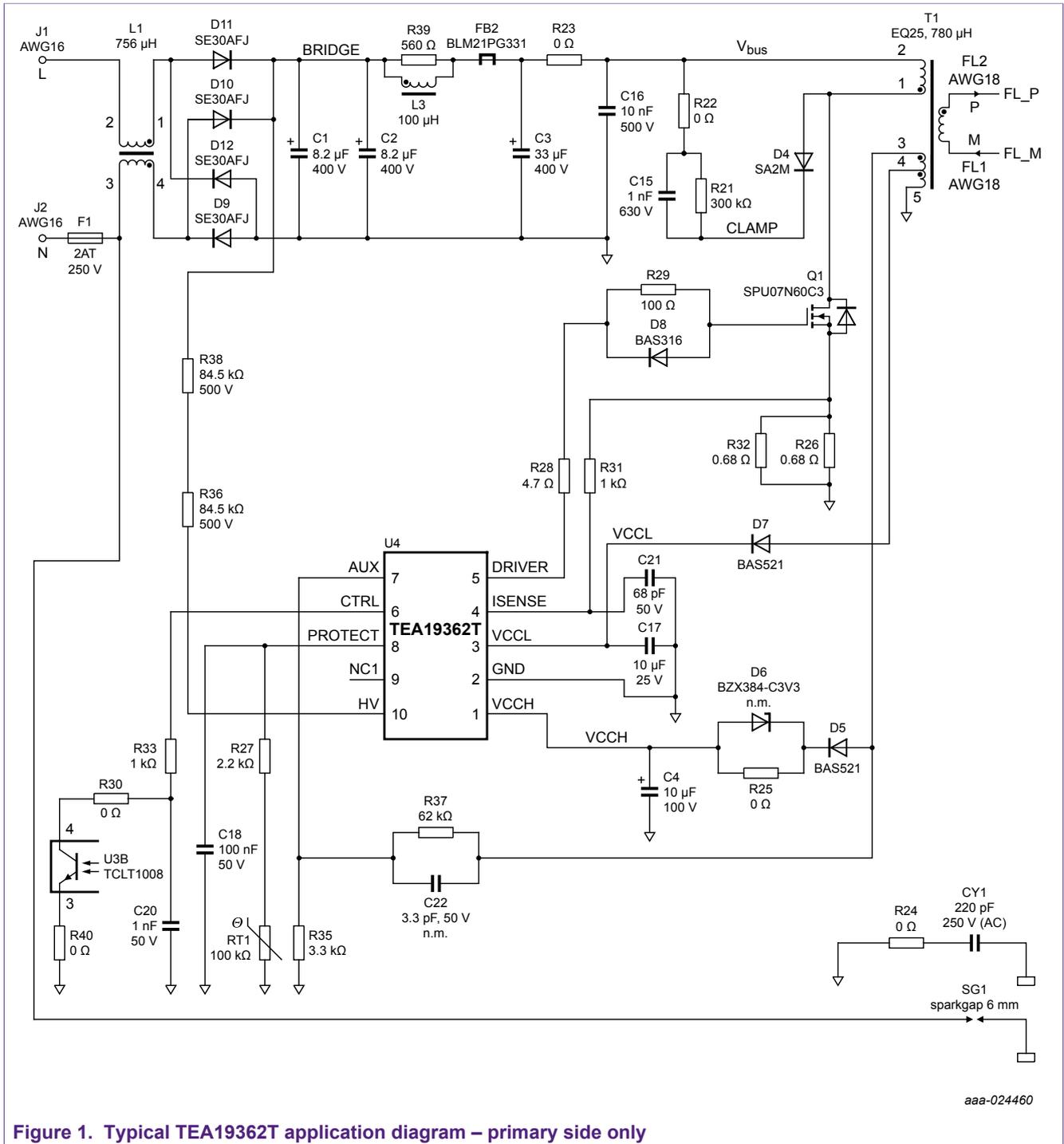
Figure 1. Typical TEA19362T application diagram – primary side only

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3.2 Pinning

3.2.1 Pin configuration
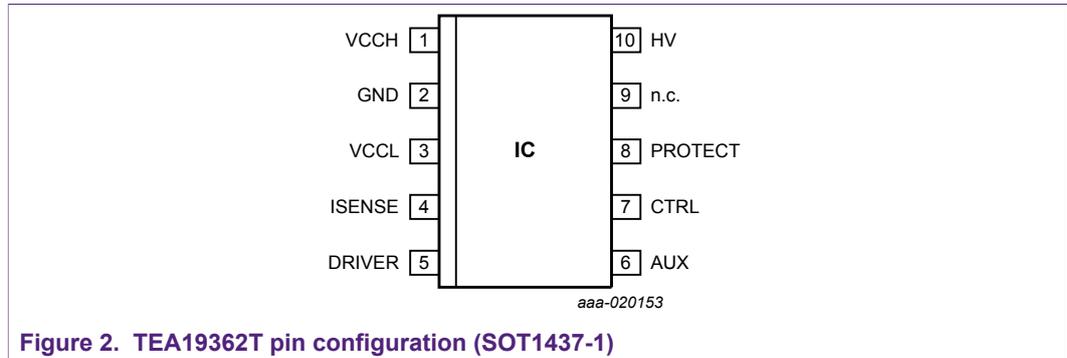
Figure 2. TEA19362T pin configuration (SOT1437-1)

3.2.2 Pin descriptions

Table 2. Pin descriptions

Pin	Pin name	Functional description summary
1	VCCH	High IC supply voltage input
		When used, the VCCH pin is supplied from an auxiliary winding of the flyback transformer with a higher voltage than the auxiliary winding uses for the VCCL pin.
		When the voltage on pin VCCL is lower than 12.5 V, the (higher) voltage on the VCCH pin provides the supply current via an internal regulator to the VCCL pin. It makes the TEA19362T operate on the VCCH voltage.
		When the voltage on pin VCCL exceeds 12.5 V, the internal regulator between VCCH and VCCL is switched off. The supply current is taken from the VCCL voltage.
		The combination of the VCCH and the VCCL pins ensures that for the supply the lowest voltage exceeding 12.5 V is selected for the IC supply. It enables building supplies with a wide output voltage range without supplying the IC from an excessively high voltage. The latter causes unnecessary power loss.
2	GND	Ground connection; reference for other pins
3	VCCL	Low IC supply voltage input and source for the internal HV start-up output
		All internal circuits, except the high-voltage circuit, are supplied from this pin.
		The buffer capacitor on the VCCL pin can be charged in several ways:
		• Internal High-Voltage (HV) start-up source (start-up and protection). The capacitance on the VCCH pin is also charged via an internal diode between the VCCH and VCCL pins. It can be used as energy reservoir during start-up before the auxiliary supply takes over.
		• Auxiliary winding from the flyback transformer (when switching)
		• External DC supply
		When the voltage on the VCCL pin reaches 14.9 V, IC operation is enabled. In burst mode, when the voltage on the VCCL drops to below 11 V, additional switching cycles are generated. The switching cycles prevent that the VCCL voltage drops to below the stop operation level. This voltage drop can occur when no energy is required on the secondary side for a prolonged time after a load step from maximum to no load. When the voltage on the VCCL pin drops to below 9.9 V, the IC halts operation. Shutdown reset is activated at 8.65 V.

| Pin	Pin name	Functional description summary
4	ISENSE	Current sense input This pin senses the primary current through the MOSFET switch via an external resistor. • Soft start A soft-start procedure is used to limit stress and audible noise during start-up. The I_{pk} level, measured over the sense resistor, is gradually increased to the regulated level in 15 steps. The soft-start time constant is 4 ms. • Burst mode In this mode, the peak current is kept constant. When a fixed level of 145 mV is reached on the ISENSE pin, the drive switches off. Controlling the number of strokes per burst cycle regulates the output voltage and output power. The switching frequency in the burst cycle is fixed. It is the same as in DCM mode. • DCM mode In this mode, the switching frequency is kept constant. The increase or decrease of the peak current regulates the output voltage and output power. The voltage level for switch-off is regulated from 145 mV upward to 510 mV • Leading-edge blanking During the first 325 ns of each switching cycle, the ISENSE input is internally blanked. The blanking of the ISENSE input prevents that the spike caused by parasitic capacitance triggers the peak current comparator prematurely. • Propagation delay There is a delay between the moment the ISENSE comparator is triggered and the MOSFET is switched off. During this time, the primary current continues to increase. How much it increases, depends on the dI/dt slope, and so, on the mains voltage. So, the resulting peak current not only depends on the level set by control, but also on the mains voltage. • Overpower protection counter When the voltage on the ISENSE pin exceeds the overpower protection level (510 mV), the overpower counter is started. When the overpower timer reaches 200 ms (40 ms during start-up), a safe restart is initiated. • Overpower compensation for mains voltage by AUX sensing current To compensate the output power level for dependency on the input voltage, an overpower compensation circuit regulates protection level based on the input voltage sensed on the AUX pin.
5	DRIVER	MOSFET gate driver output

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Pin	Pin name	Functional description summary
6	AUX	Auxiliary winding input A resistor divider on the AUX pin applies the voltage from an auxiliary winding of the flyback transformer. The voltage on this pin is used for three functions in three different time slots: • Demagnetization detection When the AUX voltage drops to below 40 mV, demagnetization is detected. Only when demagnetization is detected, the driver can be switched on to start the next power conversion cycle. So, switch-on is only allowed in the lower half of the ringing. Depending on the operating condition, the MOSFET switches on the first lower half of the ringing or in one of the lower halfs of the subsequent ringing cycles. • Input voltage sensing for OPP compensation When the external MOSFET is switched on, the voltage at the auxiliary winding reflects the input voltage. During this period, the AUX pin is clamped to −0.7 V. The measured input current is used to calculate the maximum allowed voltage on the ISENSE pin. Changing the value of the series resistor between the auxiliary winding and the AUX pin adjusts the measured current. • Output voltage sensing for OVP The resistor for input voltage sensing and a resistor from the AUX pin to ground make up a voltage divider. During secondary stroke, the divider voltage reflects the output voltage. The internal level for OVP detection is 3 V. The divider must be dimensioned for a 3 V level during secondary stroke at the desired OVP level on the secondary side.
7	CTRL	Control input In DCM, the control current flowing out of the CTRL pin is regulated to an 80 µA fixed value for all modes. The regulation of the control current is achieved by generating an internal offset which regulates the power level via the internal control curve. In burst mode, the control current level varies between 100 µA and 200 µA. The internal voltage of the CTRL pin is 3 V with a 1.5 kΩ series resistance to the pin.
8	PROTECT	Protection When the voltage level on the PROTECT pin drops to below 0.5 V, a safe restart is initiated after 2 ms to 4 ms. When the pin voltage is lower than 1.45 V, an internal current source delivers −74 µA out of the pin. When the pin voltage reaches 1.45 V, the internal current source is automatically pinched off. Connecting a suitable NTC from the PROTECT pin to GND can realize an external OTP for the system.
9	n.c.	Not connected This pin has no internal connection. It is used as high-voltage spacer.

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Pin	Pin name	Functional description summary
10	HV	High-voltage start-up The HV pin combines two functions: • High-voltage current source At start-up, the 1.1 mA HV current source is used to charge the VCCL capacitor (and via a diode also the VCCH capacitor). In this way, IC operation can start. Until VCCL reaches the start-up level (14.9 V), the IC current consumption is limited to 40 µA. When all conditions (VCCL start-up level, PROTECT pin level, and CTRL pin level) are met, start-up commences. • Mains voltage sensing Sampling the HV input current value every 1 ms senses the mains voltage during operation. Pulling the HV input to 2.9 V for 20 µs measures the HV input current. The series resistance of the HV pin to the bulk electrolytic capacitor determines this current value. It reflects the mains voltage value. The value of the external series resistors between bulk electrolytic capacitor and HV pin can set the start and stop levels. When the current exceeds 663 µA, start-up is enabled (brownin). When the current drops to below 587 µA for more than 30 ms, the operation is stopped (brownout). The 30 ms period is required to avoid that the system stops switching due to the zero crossings of the mains or during a short mains interruption. During operation, conditional sensing control reduces the sampling frequency. When a mains voltage is detected, mains voltage sensing is halted for 6.7 ms (101 ms during burst mode) to improve efficiency.

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3.3 Operating modes

This chapter describes the flyback converter operation modes that are implemented in the TEA19362T. In all operating modes, the TEA19362T works in Discontinuous Conduction Mode (DCM). In short, the flyback transformer in the TEA19362T application is fully demagnetized at the end of every power conversion cycle. One benefit for DCM operation is that it easily cooperates with Synchronous Rectification (SR) controllers on the secondary side of the SMPS. This cooperation enables optimal efficiency.

Figure 3 shows the elementary circuit diagram of a flyback converter. It also shows the typical voltage and current waveforms when the converter operates in DCM.

a. Basic circuit diagram

b. Waveforms

Figure 3. Flyback converter in DCM

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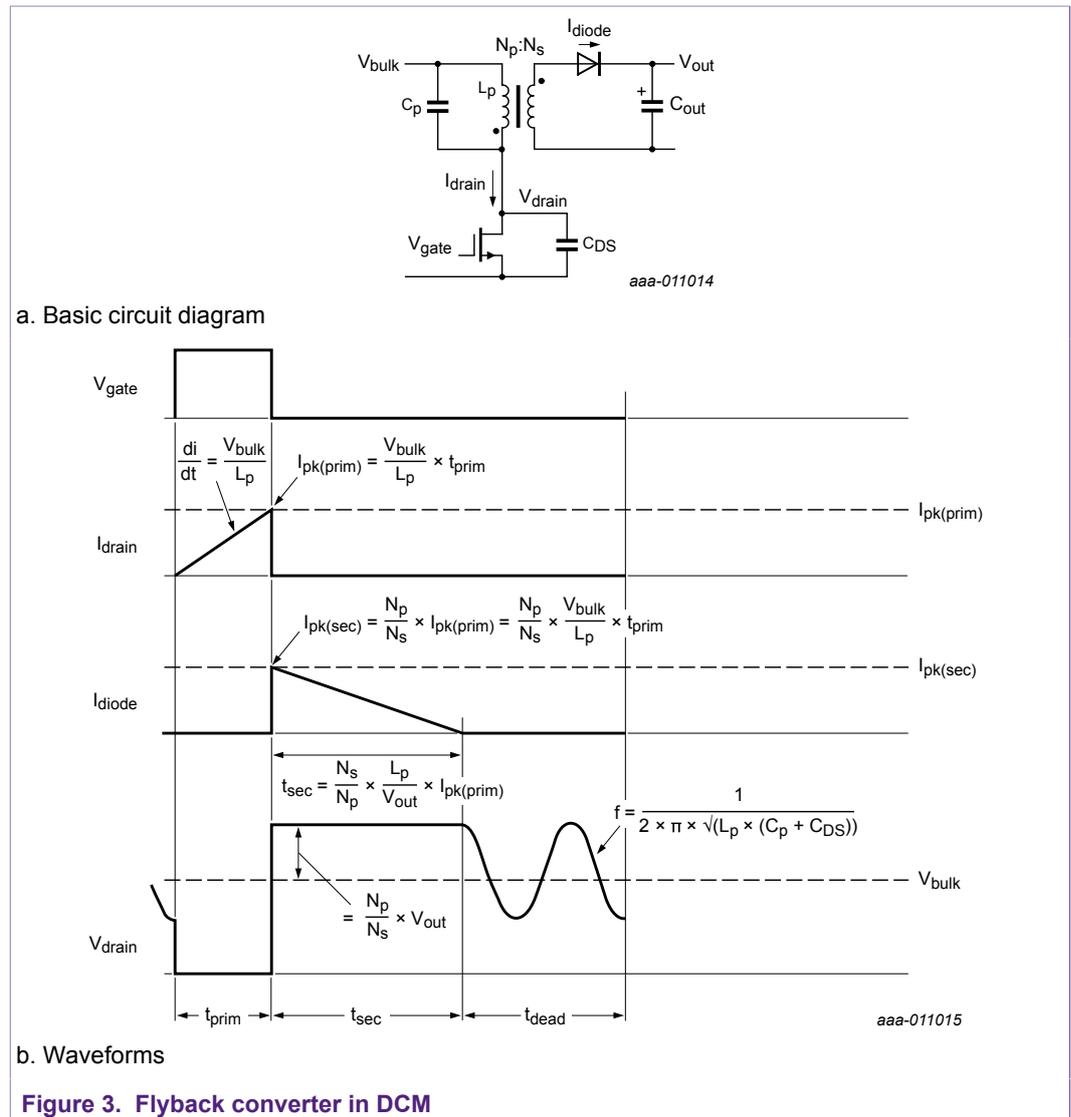
During t_{prim}, the MOSFET is switched on. The current flows through the primary winding of the transformer and the MOSFET. The transformer is magnetized. When the MOSFET is switched off, the drain voltage increases to the sum of the input voltage and the reflected output voltage (output voltage multiplied by the transformer turns ratio). The voltage at the secondary winding increases and the output diode conducts current to the output. The transformer is demagnetized during t_{sec}. After demagnetization, the voltage on the drain initiates a resonance in the primary inductance and the total capacitance at the MOSFET drain node during t_{dead}. The next cycle can then start.

There is some deviation from the basic waveforms because of parasitic elements in the components. Figure 4 shows the main deviations. A very important design aspect of the flyback transformer is to keep the leakage inductance and parasitic capacitances as low as possible. The remaining leakage leads to unwanted effects that do not contribute to the basic power conversion.
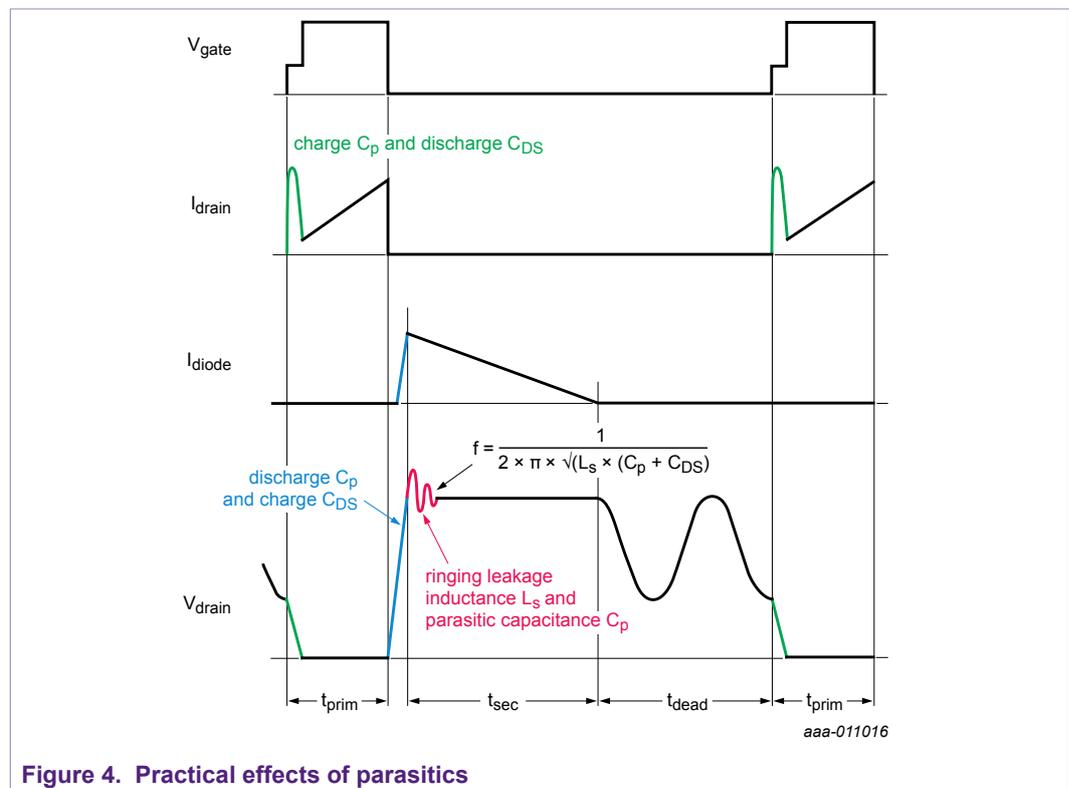
Figure 4. Practical effects of parasitics

Within DCM operation, two operating modes can be discriminated:

• Discontinuous Conduction Mode (DCM) with fixed frequency (medium and high power level)
• Burst mode (low power level)

Depending on the required output power, the system switches between operating modes. For spectral purity (touchscreens), the switching frequency is kept constant in DCM and in burst mode.

To maintain the spectral purity, the flyback converter must operate in DCM for all powers, including maximum power.

When the power is increased to exceed the level where DCM with fixed switching frequency is possible, the system enters Quasi-Resonant (QR) Mode. The switching

frequency is not fixed anymore then. It drops with the increased output power. To prevent spoiling the spectral purity and CMN performance, decreasing of the switching frequency must be avoided in normal operation.

Figure 5. TEA19362T flyback operating modes

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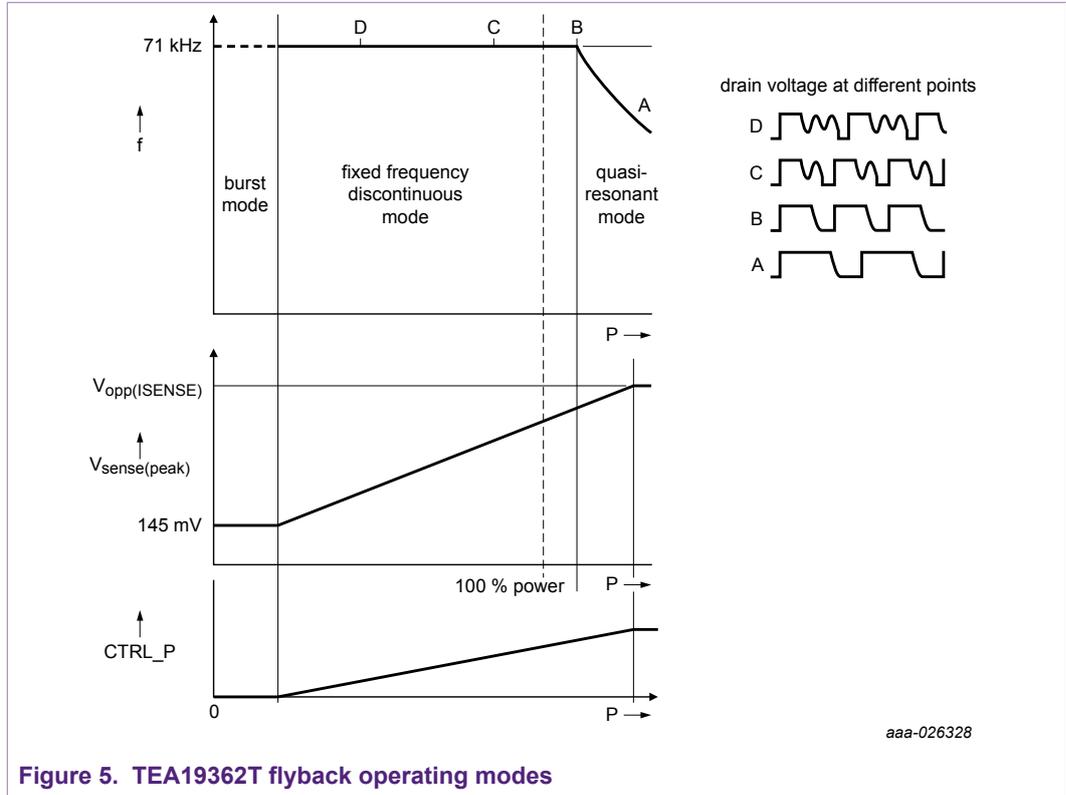
3.3.1 Flyback operating modes control

The operating modes are controlled via the CTRL pin. The TEA19362T incorporates a current mode control. Figure 6 shows the principle.
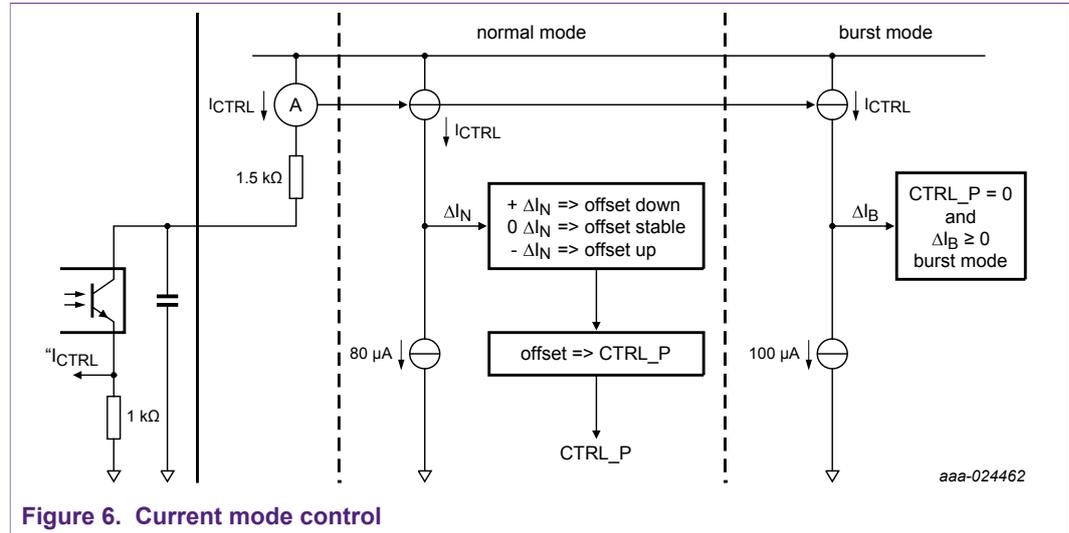
Figure 6. Current mode control

3.3.1.1 CTRL pin during FF DCM

In FF DCM, the current flowing out of the CTRL pin is kept at constant 80 µA. The current I_{CTRL}, pulled from the CTRL pin by the optocoupler is mirrored for the FF DCM mode and for burst mode. In FF DCM, I_{CTRL} is compared with an 80 µA reference current. If I_{CTRL} is not 80 µA, the difference is integrated using a slow time constant. The integrated difference increases or decreases an internal offset. This offset is converted to a proportional signal CTRL_P, which directly controls the power the IC converts (see Figure 5, flyback operating modes). For $\Delta I_N > 0$, CTRL_P is decreased, which lowers the converted power. As a consequence, V_{out} decreases and so the optocoupler current drops until I_{CTRL} becomes 80 µA again. For $\Delta I_N < 0$, CTRL_P is increased. So, V_{out} increases and so the optocoupler current increases until I_{CTRL} becomes 80 µA again. So, I_{CTRL} is always regulated to 80 µA. The regulation does not depend on the converted power, which ensures stable operation at all output power levels.

3.3.1.2 CTRL pin during burst mode

When $I_{CTRL} > 80$ µA for a longer period and CTRL_P is lowered to zero (IC is switching at 71 kHz at minimal I_{pk}, see Figure 5), CTRL_P cannot be lowered anymore. As a consequence, I_{CTRL} increases to exceed 80 µA. When it reaches 100 µA, the IC enters burst mode. The burst mode and related I_{CTRL} waveforms are discussed in Section 3.3.3. In burst mode, when $I_{CTRL} < 80$ µA for a longer period, the IC enters normal mode again.

3.3.1.3 CTRL pin provisions load steps

To achieve minimum undershoot and overshoot for load steps, various additional provisions are built in. These additional provisions shorten the reaction time for fast changing load conditions:

- When the burst-on time is longer than 1.5 times the minimum burst period (150 µs) during a burst period, the IC changes to normal mode immediately.
- In burst mode, when I_{CTRL} remains below 100 µA due to increased load, the IC keeps on switching at 71 kHz with a minimum I_{pk} level (145 mV).
- When I_{CTRL} drops to below 60 µA due to increased load, the gain is increased and the time constant is reduced. To counteract the voltage drop at the output, the IC moves quickly to maximum power.
- When the load suddenly decreases to very low values and I_{CTRL} increases to exceed 200 µA, switching stops immediately to prevent a high output voltage overshoot.

3.3.2 Fixed-Frequency Discontinuous Conduction Mode (FF DCM)

In DCM, a certain dead time always exists between the ending of the secondary stroke and the next switch-on moment of the MOSFET. The dead time enables control of the switching frequency. The system is only allowed to switch on the MOSFET in the bottom half of the ringing (demagnetizing switching), balancing the switching frequency deviation against switch-on losses. Figure 7 shows the switching behavior.

a. Switch-on immediately allowed

b. Switch-on blocked until lower half ringing

c. Signal on AUX pin and demagnetization signal
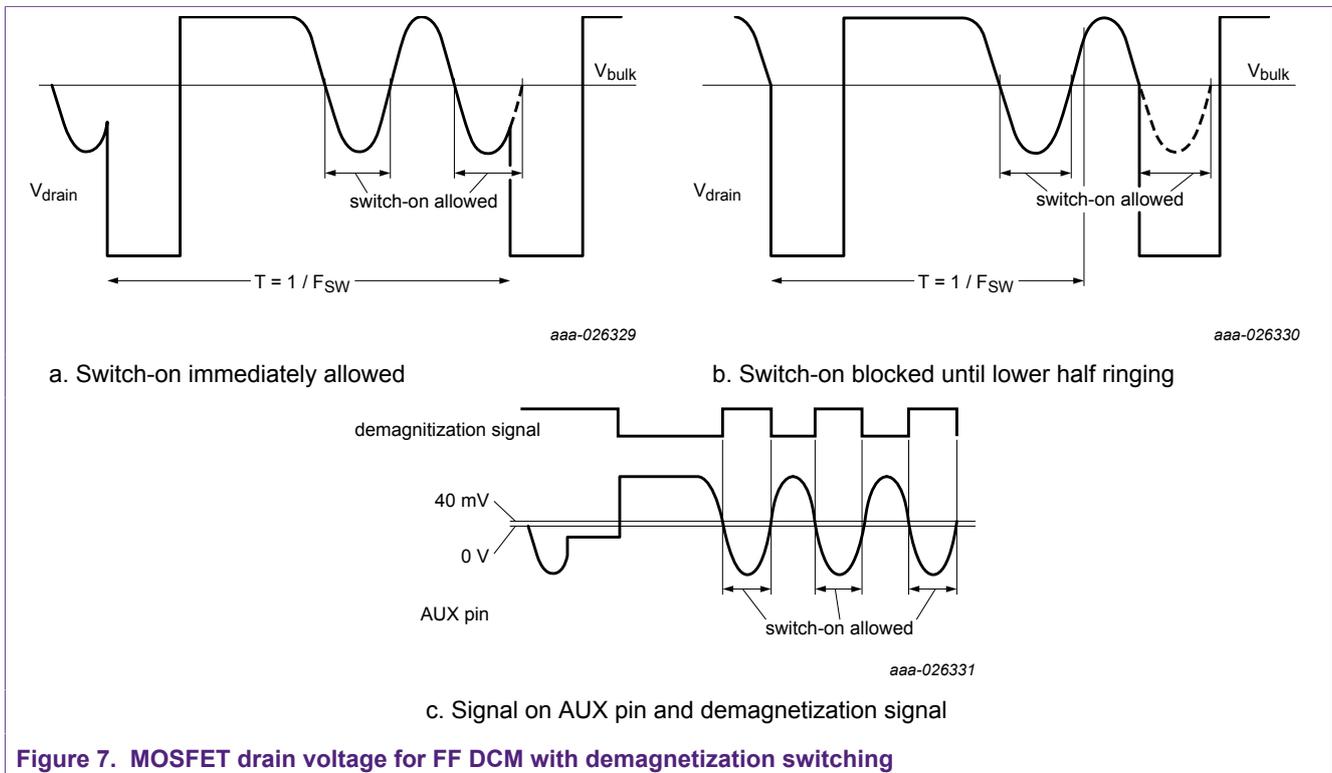
Figure 7. MOSFET drain voltage for FF DCM with demagnetization switching

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When the secondary stroke has ended, the drain voltage starts ringing. When the fixed frequency switch-on timing occurs during the bottom half of the ringing, the MOSFET is switched on immediately (Figure 7a). When the switch-on timing occurs during the upper half of the ringing, the switch-on is delayed until the lower half of the ringing is reached (Figure 7b). The time slots where switch-on is allowed are derived from the demagnetization signal generated on the AUX pin (Figure 7c). Via a resistive divider the signal of the AUX supply winding is fed to the AUX pin. Each time the signal drops below 40 mV, the demagnetization signal becomes high and switch-on is enabled. The demagnetization signal is also used to prevent switch-on during secondary stroke.

The switch-on losses are related to the voltage on the drain at switch-on and are equal to:

$$Switching\ loss\ per\ cycle = 0.5 \times \left(C_p + C_{DS} \right) \times \left(V_{DRAIN} \right)^2 \tag{1}$$

Where:

- C_p the parasitic transformer capacitance
- C_{DS} the drain-source capacitance of the MOSFET (see Figure 7a)

The efficiency gain at higher input voltages by not switching in the top of the ringing is around 1 %.

The switch-on timing deviation, caused by only allowing switching during the bottom half of the ringing, is maximally equal to half the period time of the ringing. With a typical ringing frequency of 750 kHz, the timing deviation becomes 0.67 µs. The frequency deviation at 71 kHz is 4.8 %. This deviation is small enough to safeguard the spectral purity.

During DCM, the current flowing out of the CTRL pin is regulated to a fixed value of 80 µA. To regulate that current, an offset is generated internally, which controls the operation mode curve (see Section 3.3.1). The internal offset regulates the output power. It increases I_{pk} by controlling the level of the ISENSE pin for switch-off from 145 mV to 510 mV.

To maintain the spectral purity, the flyback converter must operate in DCM for all powers, including maximum power. When the power is increased to exceed the level where DCM with fixed switching frequency is possible, the system enters the Quasi-Resonant (QR) mode. The switching frequency is not fixed anymore then. It drops with the increased output power. To prevent spoiling the spectral purity and CMN performance, the switching frequency decreasing must be avoided in normal operation.

3.3.3 Burst mode

Burst mode operation is used to minimize power loss during low output power conditions. The goal is to generate the required output power with bursts of variable lengths, while switching operation is turned off for shorter or longer periods. When the converter is not switching, conversion losses are zero.

During the intervals that switching is off, it is also important to minimize the current flowing into various circuits of the power converter. Minimizing this current reduces the power consumption. In modern control ICs like the TEA19362T, several internal circuits are switched off during the non-switching period. It minimizes the supply current to less than half the nominal supply current during switching.

Burst mode operation usually results in a higher output voltage ripple than in normal (DCM) mode (see Figure 8).
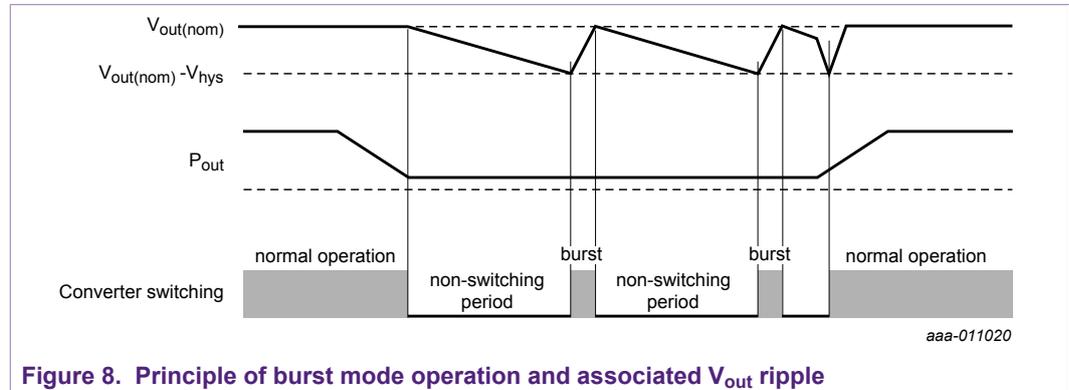
**Figure 8. Principle of burst mode operation and associated V_{out} ripple**

To maintain the spectral purity in burst mode, the switching frequency is kept the same as during normal operation. To limit the ripple in burst mode at the high fixed switching frequency (71 kHz), the burst period is set to a minimum of 150 µs (maximum 6.7 kHz).

To prevent audible nose, the peak current in burst mode is chosen as low as possible (145 mV).

Figure 9 shows the switching behavior during burst mode for different loads.

The minimum number of switching cycles within a burst is 1. At ultra-low load, the number of switching cycles is indeed 1. The repetition rate is regulated to well above 150 µs (see Figure 9).

The requested output power determines the number of pulses in each burst period. The digital circuit calculates the number of switching cycles so that the burst repetition timing does not exceed 150 µs. At higher output powers, the number of switching pulses increases. At low load, the number of pulses decreases (to a minimum of 1). Simultaneously, the switching frequency within the burst is 71 kHz. In this way, spectral purity is maintained.
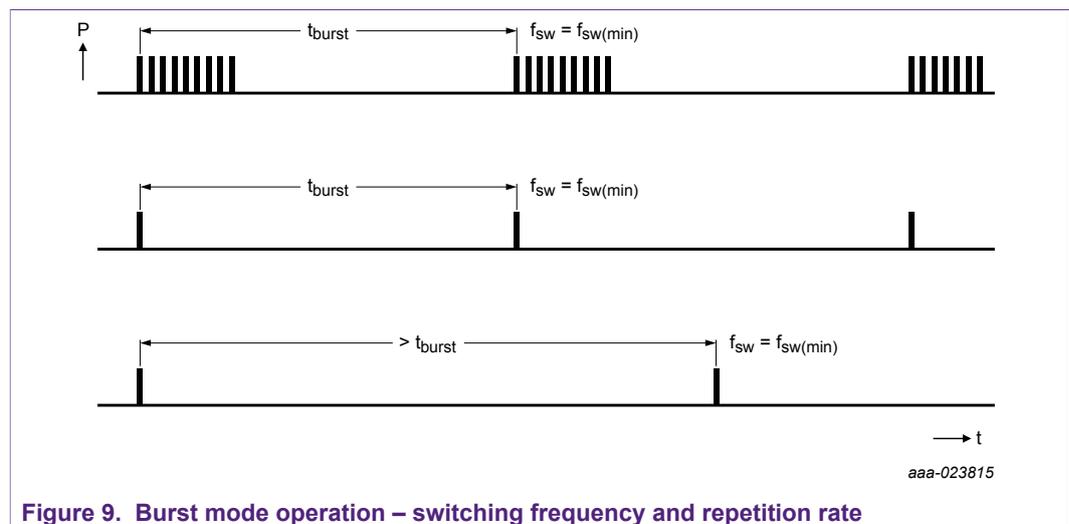
Figure 9. Burst mode operation – switching frequency and repetition rate

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In FF DCM mode, the internal offset, which keeps I_{CTRL} regulated at 80 μA, regulates the power. When the required output power is reduced in FF DCM mode at 71 kHz, the internal offset cannot be lowered further. The I_{pk} sense voltage is already at its lowest value (145 mV). In that case, I_{CTRL} increases to 100 μA and the IC enters burst mode.

The behavior of the CTRL pin in burst mode differs from its behavior in FF DCM mode. In burst mode, switching always starts when the current drawn from the CTRL pin drops to below 100 μA. Figure 10 shows the behavior of I_{CTRL} in burst mode at a very low load and in the middle and at the end of the burst.

Note: *The simplest way to measure I_{CTRL} is to add a 1 kΩ resistor from the emitter output of the optocoupler to ground. The sensitivity for oscilloscope measurement is 100 mV/100 μA.*

a. Very low load

b. Middle of burst

c. End of burst

Figure 10. Burst mode operation for different loads in burst related to I$_{CTRL}$
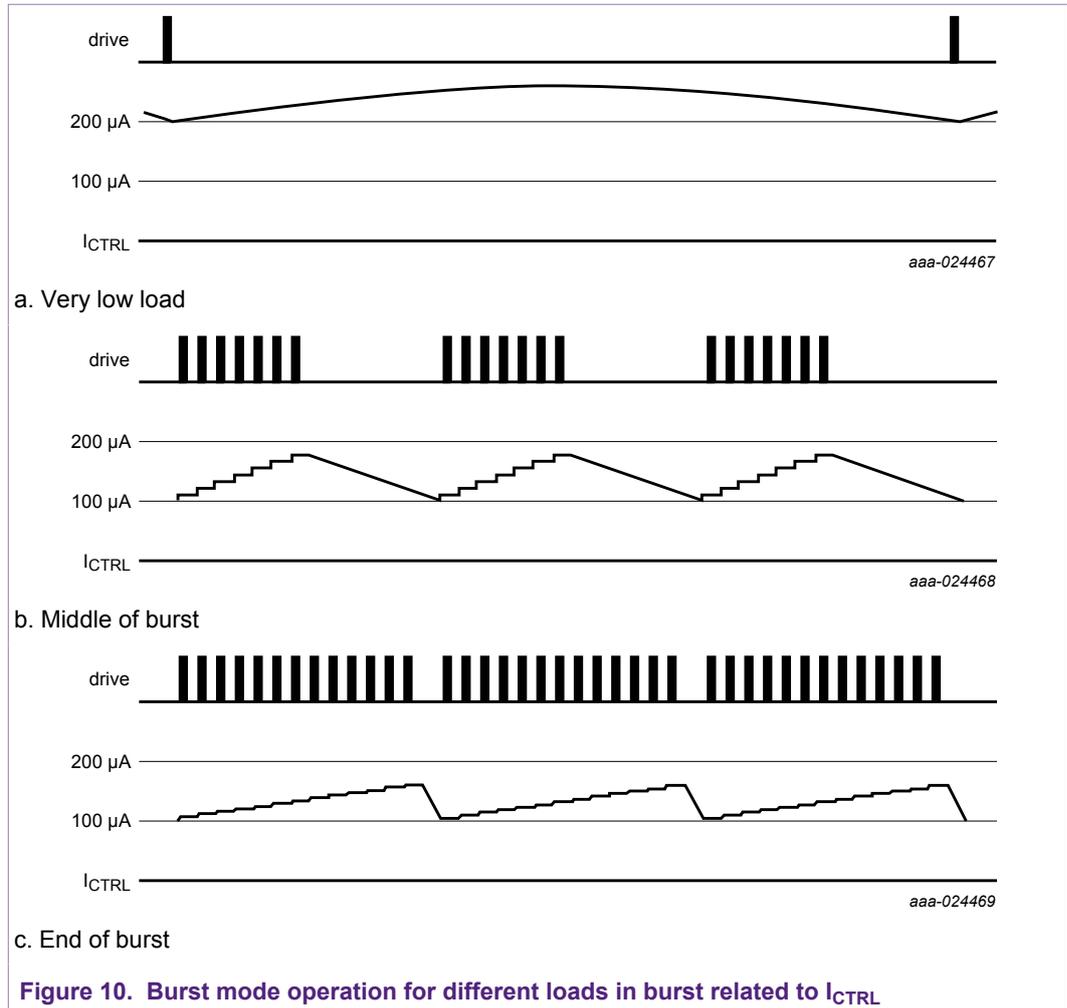
At very low loads, only one switching cycle is required to make I$_{CTRL}$ increase to exceed 100 μA. Only when the I$_{CTRL}$ drops again to below 100 μA, the next stroke is made. Depending on the winding ratio of the transformer and the output voltage, it is possible that two or three strokes are required to bring ICTRL above 100 μA. Except for the number of strokes per burst cycle, the behavior remains the same.

In the middle of the burst trajectory, the system is switching half the time and half the time it is off. With each stroke I$_{CTRL}$ increases. This condition generates the highest peak value for I$_{CTRL}$.

When the load increases further, the number of strokes per burst increases also until only one stroke per burst is missing. A minor load increase causes the IC to switch continuously to FF DCM at 71 kHz. When FF DCM is entered, I$_{CTRL}$ drops from 100 μA to 80 μA. The internal offset takes over the regulation.

(1) Lower limit
(2) Upper limit

**Figure 11. Burst mode frequency as a function of the number of strokes per burst**
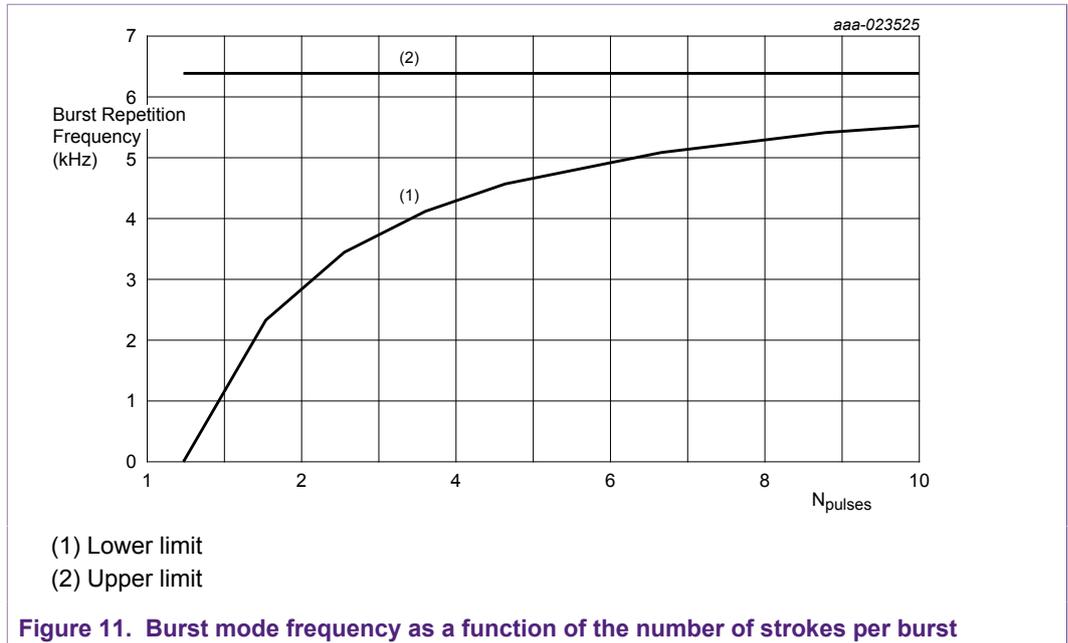
3.3.4 Loop gain and burst period

System control is programmed such that switching always stops when $I_{CTRL} > 200$ µA in burst mode and FF DCM. When the input voltage is at its maximum (264 Vac) and operation is at 50 % burst (in middle of the burst trajectory), the maximum I_{CTRL} peak level is reached. The loop gain determines the peak level. The gain of the optocoupler and the pull-up resistor on secondary side of the optocoupler diode influence the peak level.

When the switching stops earlier than the calculated burst-on time because of a high gain, the system remains working in burst mode. However, the burst period becomes shorter (burst frequency increases). The hysteresis of I_{CTRL} (between 100 µA and 200 µA) determines the switching behavior (see Figure 12).

a. Peak of I_{CTRL} remains below 200 µA

b. Peak of I_{CTRL} exceeds 200 µA and burst switching is stopped

Figure 12. Burst period when I_{CTRL} surpasses 200 µA
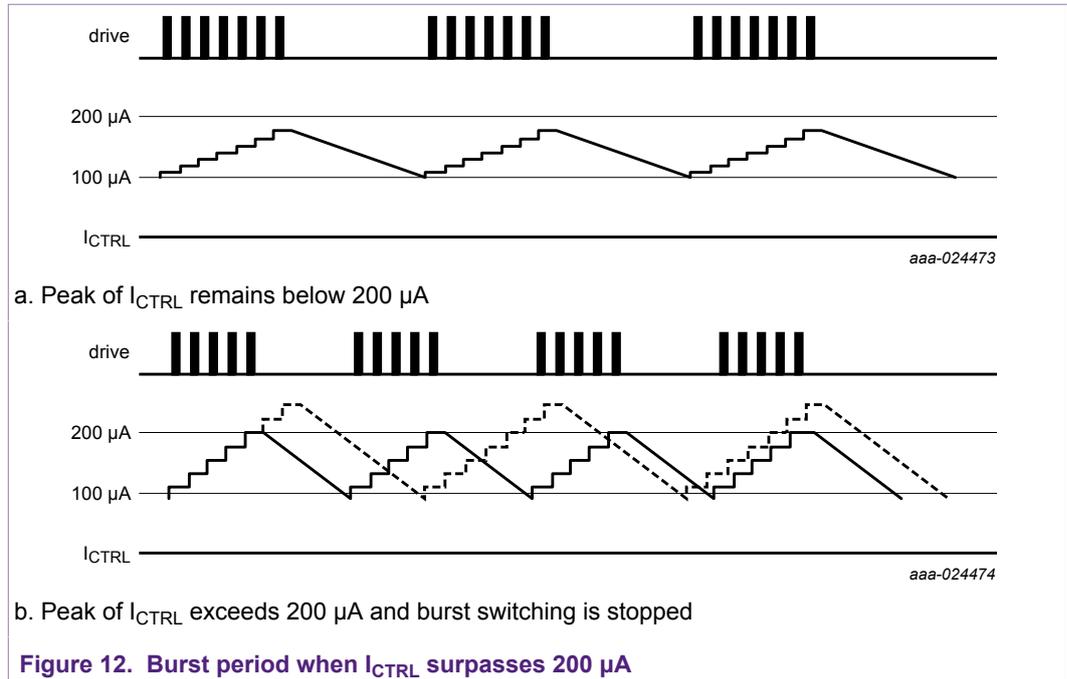
Figure 12(b) shows that the burst period reduces when I_{CTRL} exceeds the 200 µA level. The dashed I_{CTRL} line indicates the intended (precalculated) behavior.

The loop gain can be optimized to balance load step behavior and burst mode behavior. Select the value of the pull-up resistor of the optodiode on the secondary side such that the current, drawn from the CTRL pin (I_{CTRL}) is close to 200 µA at 50 % burst and at 264 V (AC).

3.4 TEA19362 start-up and supply

When the mains voltage is applied, the capacitors at the VCCH and VCCL pins are charged via the HV pin. When the voltage level at the VCCL pin reaches 14.9 V and all conditions are met (brownin, PROTECT pin), the IC starts switching. When the IC is switching, the auxiliary winding takes over the supply of the VCCH and VCCL pins.

3.4.1 Start-up with the HV current source

The HV pin provides two functions:

- High-voltage current source for charging the capacitors at the VCCH and VCCL pins before start-up
- Mains voltage sensing input for detecting brownin and brownout

The HV pin can be connected to the high voltage in two ways:

- With a diode/capacitor/resistor network before the mains rectifier bridge
- With a resistor network after the mains rectifier bridge

Figure 13 shows both configurations.

a. HV pin connected before the diode bridge   b. HV pin connected after the diode bridge

**Figure 13. Configurations for connecting the HV pin**
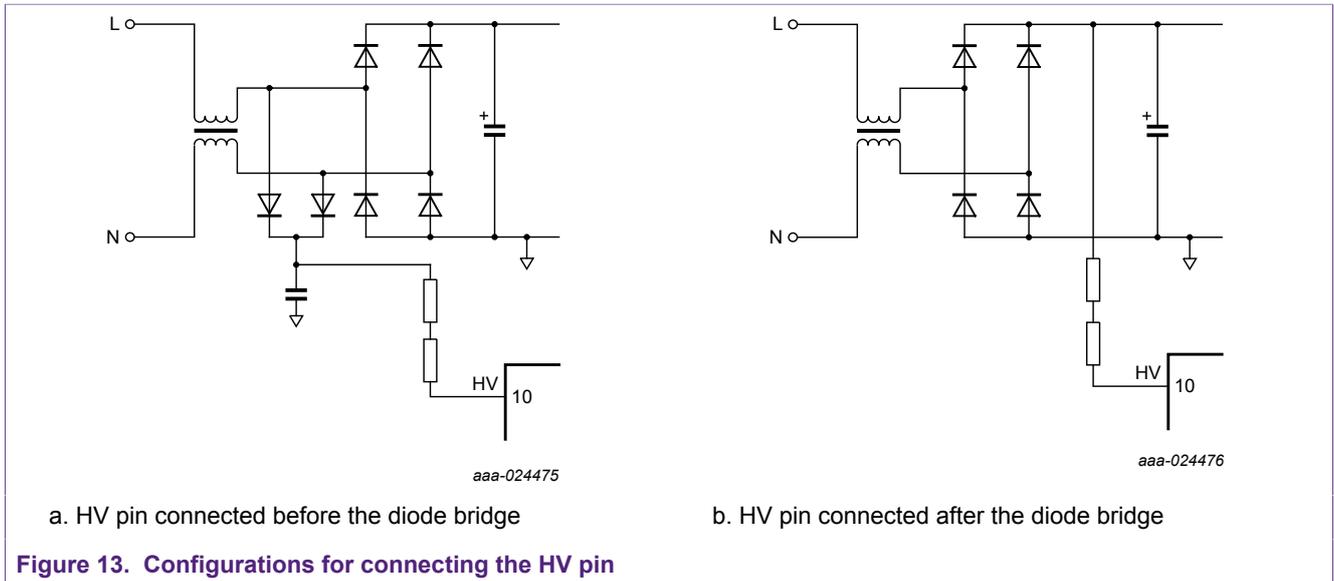
The start-up behavior of the two configurations is alike. However, the brownout behavior after the mains is unplugged is different.

Connecting before the diode bridge has the disadvantage that three additional components are required (two high-voltage diodes and a high-voltage capacitor). When the mains is unplugged, this configuration has the advantage that the voltage across the small capacitor drops quickly to below brownout level and halts switching operation. Only very limited power on the secondary side remains available after the mains is unplugged. To prevent EMI disturbance from the brownin/brownout measuring pulses of the HV pin, the capacitor located after the diodes in this configuration is a requirement.

Connecting the HV pin after the diode bridge saves components. However, when the mains is unplugged, the IC keeps switching. It delivers power to the secondary side until the voltage on the mains electrolytic capacitors drops to below the brownout level (approximately 70 V (DC)). For low load and high input voltages, it can take quite some time. During the time it takes, the output voltage remains regulated.

Figure 14 shows the supply configuration.

Figure 14. Supply configuration including start-up provision
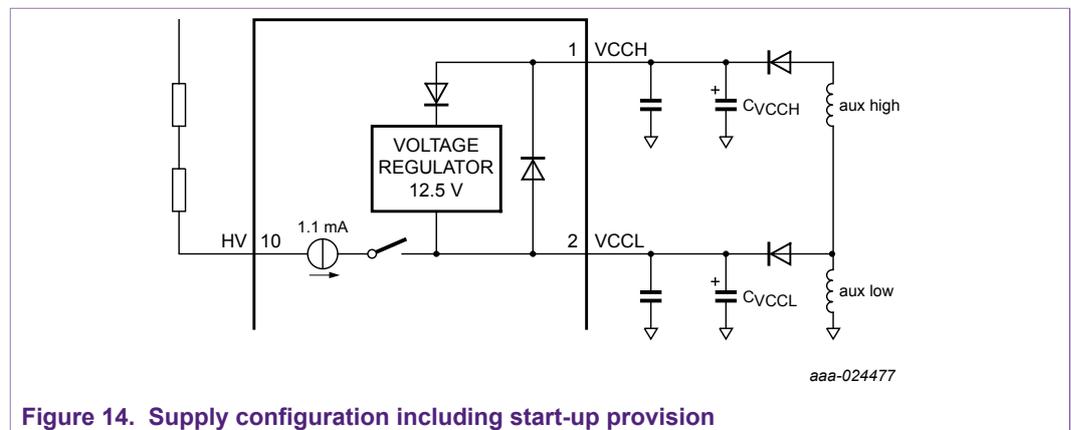
The main supply pin, which is directly connected to the internal IC supply is the VCCL pin. The VCCH pin is connected to the VCCL pin via an internal regulator. If the supply voltage via the AUX low is lower than 12.5 V, the internal regulator regulates the VCCL to 12.5 V. When the supply voltage via the AUX low pin exceeds 12.5 V, the regulator is turned off. The supply is taken from the VCCL pin. In this way, the lowest voltage that is high enough to supply the IC is always selected to save power. The IC consumes power from the supply as a current source. So, the supply dissipation increases almost linearly with the IC supply voltage.

To charge the capacitors on the VCCL pin and, via the diode, also the capacitors on the VCCH pin, an internal 1.1 mA current source is enabled at start-up. The internal current source is taken from the high-voltage mains connected to the HV pin. Charging these capacitors enables the use of the full capacitance available on both pins as an energy reservoir at start-up. If the capacitance value at the VCCH pin is high enough, it offers the possibility to use a lower capacitance value on the VCCL pin than is required for start-up. As long as VCCL is below system start-up level (14.9 V), the current consumption of the internal IC circuits is limited to 40 µA.

When the HV pin is connected before the bridge rectifier, the voltage on the pin may become close to 0 V. The current source is then temporarily unable to generate the 1.1 mA (typical) current required. A discontinuous increase of the VCC voltage can be observed. Depending on the applied input voltage, the series resistance between the HV pin and the mains voltage can also limit the current.

When VCCL reaches the start-up level (14.9 V) during charging, the internal circuits are activated. From this moment, the start-up sequence is activated. The IC current consumption increases (600 µA for the internal IC circuits, the current for the MOSFET drive, and the CTRL function). First, all protections are checked. Further start-up is halted until the brownin condition is met and the protect pin voltage exceeds 0.55 V. Then, switching is enabled. Switching commences with a soft start. During the soft start, the peak current increases to its maximum level in 15 steps. This current increase is achieved by increasing the voltage level for switch-off of the ISENSE pin from 0 mV to 510 mV. The current source of the HV pin remains active. However, it cannot provide all the energy required. So, the VCC voltage decreases until the auxiliary high or auxiliary low winding take over the supply. When the output voltage reaches the regulation level, the HV current source is switched off. The CTRL pin detects when the output voltage has reached the regulation level.

For a reliable implementation of a VCC supply at start-up and during burst operation under all conditions, use a 10 µF VCC capacitor. When space and/or cost are critical, it is possible to apply 10 µF on the VCCH pin and 1 µF on the VCCL pin. The only drawback to this configuration is that there is a slightly higher no-load power consumption. The higher power consumption occurs when a higher output voltage can be generated with the IC operating on the auxiliary low winding during normal (medium or high power level) operation. However, it must switch to auxiliary high during long non-switching periods (e.g. low power or no load).

The value of the capacitor chosen for the VCCH pin must be equal or higher than the value of the capacitor on the VCCL pin. The reason is that during burst the VCC capacitors are only charged at a very low repetition rate during a very short time. The peak charging current can easily surpass 1 A. When the auxiliary high provides the supply under this condition, the series impedance of the series regulator is too high to allow proper charging of a high-value capacitor on the VCCL pin.

3.4.2 Supply protection

Under varying load conditions, it can happen that the switching is stopped for longer periods. An example is when the load changes suddenly from full load to no load. When this sudden change occurs, switching on the primary side does not stop immediately. So, the output voltage increases slightly and exceeds the regulation level. The CTRL pin is pulled low and the IC stops switching via the optocoupler. Because there is no load, the output voltage only drops slowly to its regulation level. When no switching occurs for a longer time, the IC supply can drop to below the UVLO level. The IC then performs a safe restart.

To prevent a restart, the IC starts switching at minimal I_{pk} when the VCCL voltage drops to below 11 V ($V_{restart}$). The IC keeps switching until the VCCL voltage has increased to at least 100 mV above 11 V. The switching frequency is 71 kHz. When the VCCL voltage drops to 11 V again, the sequence is repeated. The sequence is repeated until V_{out} has dropped to the regulation level and the loop is in regulation again. Figure 15 shows the various signals.
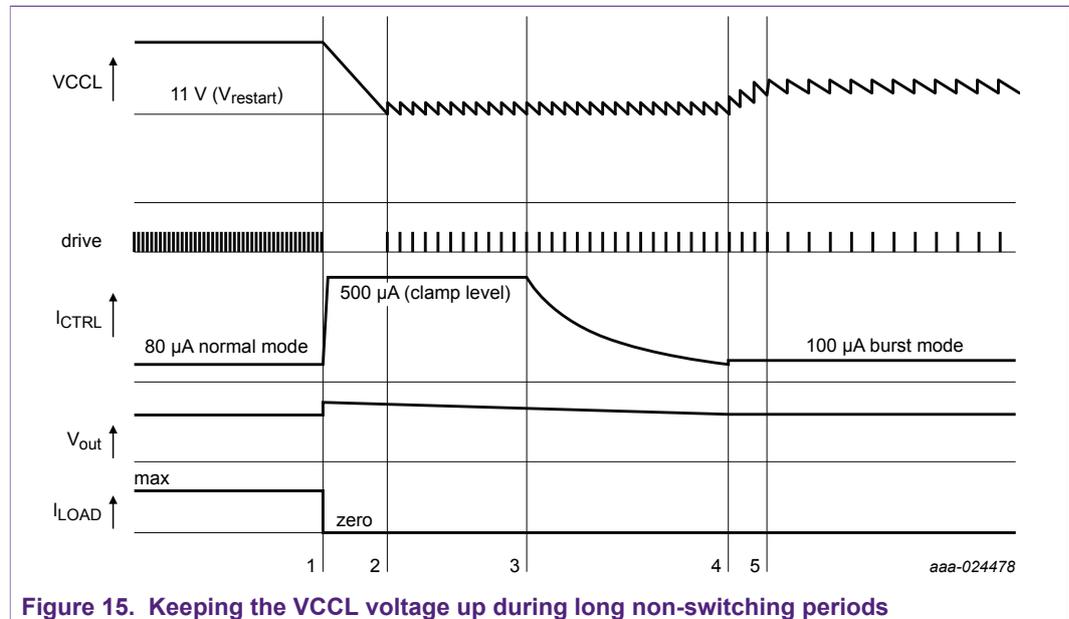
Figure 15. Keeping the VCCL voltage up during long non-switching periods

The sequence of events is explained using the numbers indicated next to the vertical dashed lines.

1. Load drops from maximum to zero
   Switching continues for a short while before stopping, causing V_{out} to exceed the regulation level. (For better understanding, the increase of V_{out} is exaggerated in Figure 15). Due to the V_{out} increase, I_{CTRL} also increases from the normal mode level (80 µA) to the clamp level (500 µA). The VCCL voltage starts to drop because switching stops.
2. The VCCL voltage has decreased to the $V_{restart}$ level (11 V)
   To keep the VCCL voltage above 11 V, strokes are inserted at minimal I_{pk}. When the VCCL voltage has increased by more than 100 mV, switching stops. The VCCL voltage drops again. When it reaches 11 V again, the sequence is repeated.

3. V$_{out}$ decreases slowly over time, causing I$_{CTRL}$ to decrease also.
When the optocurrent drops to below 500 µA on the primary side, I$_{CTRL}$ starts to drop
to below the saturation level. As long as V$_{out}$ keeps decreasing, I$_{CTRL}$ keeps dropping.
4. When I$_{CTRL}$ has dropped to 100 µA, normal burst switching is resumed.
The VCCL voltage increases to the normal level in burst mode.
5. The system is in normal burst mode again.
All voltages and currents are at the normal level.

Although this mechanism also works when the VCCL voltage becomes too low in burst
mode, design the supply such that the VCCL voltage is kept above 11 V during normal
burst mode. The drawback of the mechanism is that it regulates the VCCL voltage and
not V$_{out}$. It causes V$_{out}$ to exceed the regulation level. The increased V$_{out}$ increases the
optocurrent and I$_{CTRL}$ current. These additional currents increase the no-load power with
several mW.

3.5 Mains voltage detection

Mains voltage sensing is performed via sampling of the voltage on the HV pin. To
minimize power consumption due to current load on the mains, each measurement takes
only a short period (20 µs). The measurement interval is 1 ms. However, when a mains
voltage that exceeds the brownin level is detected, the measurement interval is increased
to 6.7 ms in normal mode and to 101 ms in burst mode. The reason for the increase is
saving power.

Measurements are taken during the sampling period. The HV pin is switched to the
ground level. The current that flows from the mains through the series resistor at the end
of the 20 µs period is measured. The internal circuit that connects the HV pin to ground
and measures the current introduces a voltage drop of approximately 2.9 V. So, during
the sampling period, a voltage of 2.9 V can be observed on the HV pin.

The two possible configurations for connecting the HV pin to the mains are already
discussed in Section 3.4.1. In both configurations, the sensing voltage is a DC with some
ripple.

Figure 16 shows the measuring setup of the mains sensing.
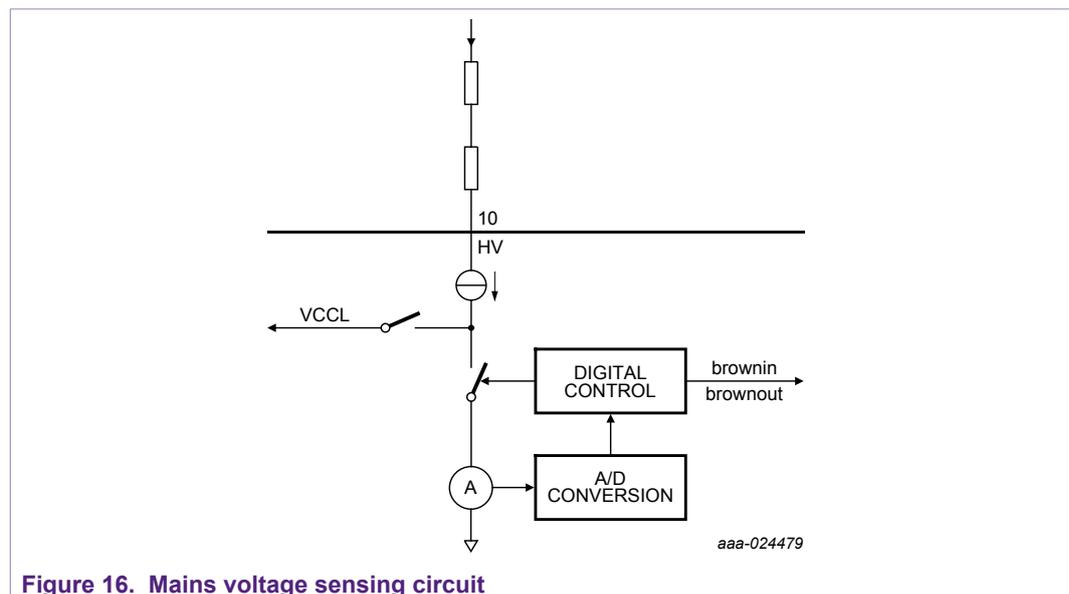
Figure 16. Mains voltage sensing circuit

When the mains sense switch closes, the current is measured. The value of the resistors between the HV pin and the rectified mains determine the current for lower input voltages. For higher input voltages, the current source in series limits the current to 1.1 mA.

3.5.1 Brownin

When the VCCL pin is charged to the start level, mains sensing is activated to generate one of the required conditions for starting the converter. The rectified mains voltage is sensed in the normal sequence of three pulses and a wait time of 6.7 ms. When one pulse shows a value that exceeds the brownin value (663 µA), converter start-up is enabled (as far as meeting the brownin requirements is concerned). Sensing continues after start-up.

The brownin level can be calculated with Equation 2:

$$R_{HV} = \frac{\sqrt{2} \times V_{mains(RMS)} - V_{meas(HV)}}{I_{bi(HV)}}$$

(2)

Example:

- $I_{bi(HV)}$ = 663 µA
- $V_{meas(HV)}$ = 2.9 V
- $V_{mains(RMS)}$ = 86.0 V; The required brownin level

$$R_{HV} = \frac{\sqrt{2} \times 86.0 - 2.9}{663 \times 10^{-6}} \approx 180 \ k\Omega$$

If the brownin level is not met when the VCCL voltage has reached V_{start}, the HV current source regulates the VCCL voltage on 14.9 V. In this way, when the brownin level is reached, the IC can start immediately.

3.5.2 Brownout

If the mains voltage remains below the brownout level for at least 30 ms, a brownout is detected. The system stops switching. This delay period is built in to ensure that the system does not stop switching during a short mains interruption.

The brownout level can be calculated with Equation 3:

$$R_{HV} = \frac{\sqrt{2} \times V_{mains(HV)} - V_{meas(HV)}}{I_{bo(HV)}}$$

(3)

Example:

- $I_{bo(HV)}$ = 587 µA
- $V_{meas(HV)}$ = 2.9 V
- $V_{mains(RMS)}$ = 76.5 V; The required brownout level

$$R_{HV} = \frac{\sqrt{2} \times 76.5 - 2.9}{587 \times 10^{-6}} \approx 180 \ k\Omega$$

The selection of a value for the HV pin series resistance determines the brownin and the brownout value.

(1) Brownin
(2) Brownout

Figure 17. Brownin and brownout levels as a function of the HV series resistor value
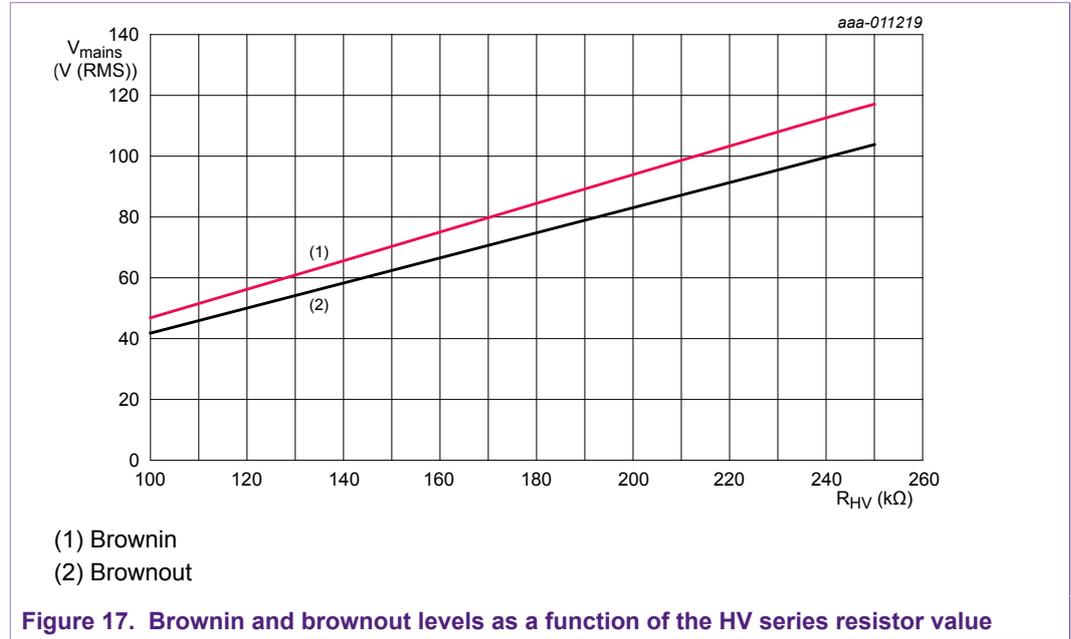
3.6 TEA1936T MOSFET driver

The TEA19362T has a powerful output stage. It directly drives the external power MOSFET. The maximum output voltage is limited to 10.5 V which is the voltage of the internal source supplying the driver stage.

Figure 18. Simplified model of the MOSFET driver
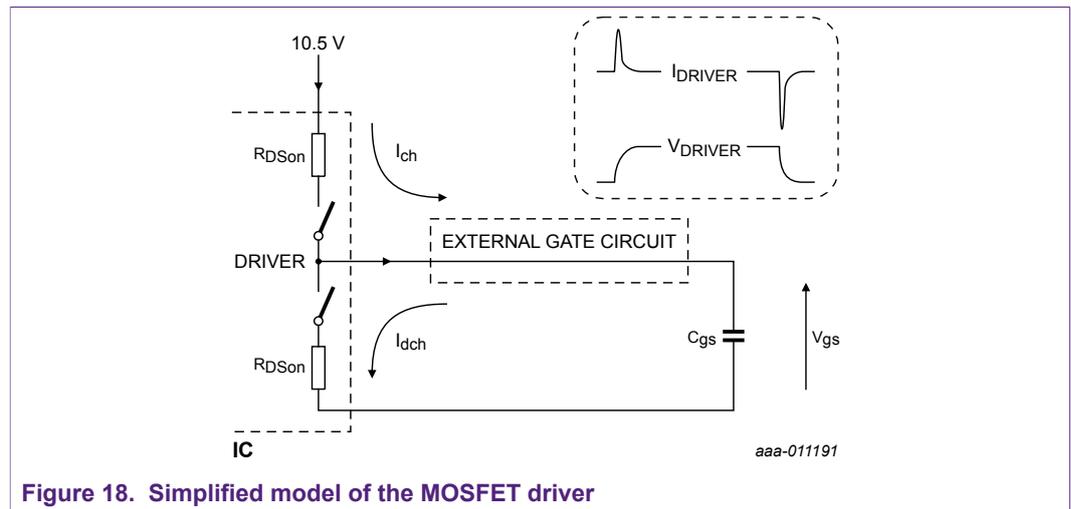
The model in Figure 18 shows that current is taken from the internal 10.5 V source when the external MOSFET is switched on by charging the gate to a high voltage.

The shape of the current flowing in and out of the DRIVER pin is related to:

- The supply voltage for the internal driver (10.5 V) at switch-on
- The characteristics of the internal driver MOSFETs (R_{DSon})
- The value of the gate capacitance of the external MOSFET
- The switch-on/switch-off gate threshold voltage of the external MOSFET

The TEA1936x data sheets provide the characteristics of the internal drivers.

Table 3. MOSFET driver characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{source(DRIVER)}$	source current on pin DRIVER	V_{DRIVER} = 2 V	-	−0.3	-	A
$I_{sink(DRIVER)}$	sink current on pin DRIVER	V_{DRIVER} = 2 V	-	0.3	-	A
		V_{DRIVER} = 10 V	-	0.75	-	A
$V_{O(DRIVER)max}$	maximum output voltage on pin DRIVER		9	10.5	12	V

3.7 Auxiliary windings

In the basic application, one or more auxiliary windings on the flyback transformer are used for two main functions:

- Supply voltage for the TEA19362T on the VCCL and the VCCH pins
- Sensing signal on the AUX pin
  In a transformer with separate auxiliary windings for the VCCL and VCCH pins, one of the two windings must be used to feed a signal to the AUX pin. In practice, it is the easiest to use the VCCL auxiliary winding because its voltage is lower and it saves some dissipation.

The signal from the auxiliary winding is used to sense several variables that are used for control and protection:

- Demagnetization detection
- Input voltage sensing for maximum output power compensations
- Output voltage sensing for indirect OVP

The voltage from an auxiliary winding of the flyback transformer is connected to the AUX pin using a resistive divider.

Figure 19 shows the circuit.
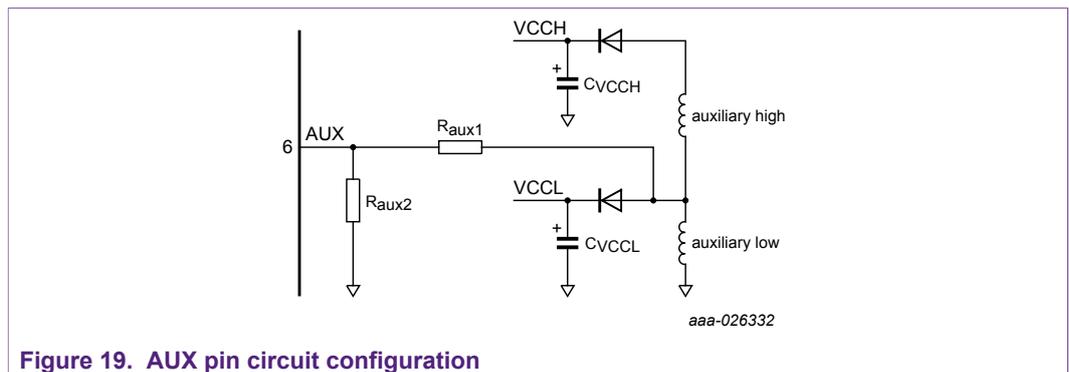
Figure 19. AUX pin circuit configuration

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As indicated, the resistive divider can also be connected to the auxiliary high winding, provided the values of the resistors are adapted for the higher voltages.

Each detection function has its own time slot in the repetitive AUX signal.
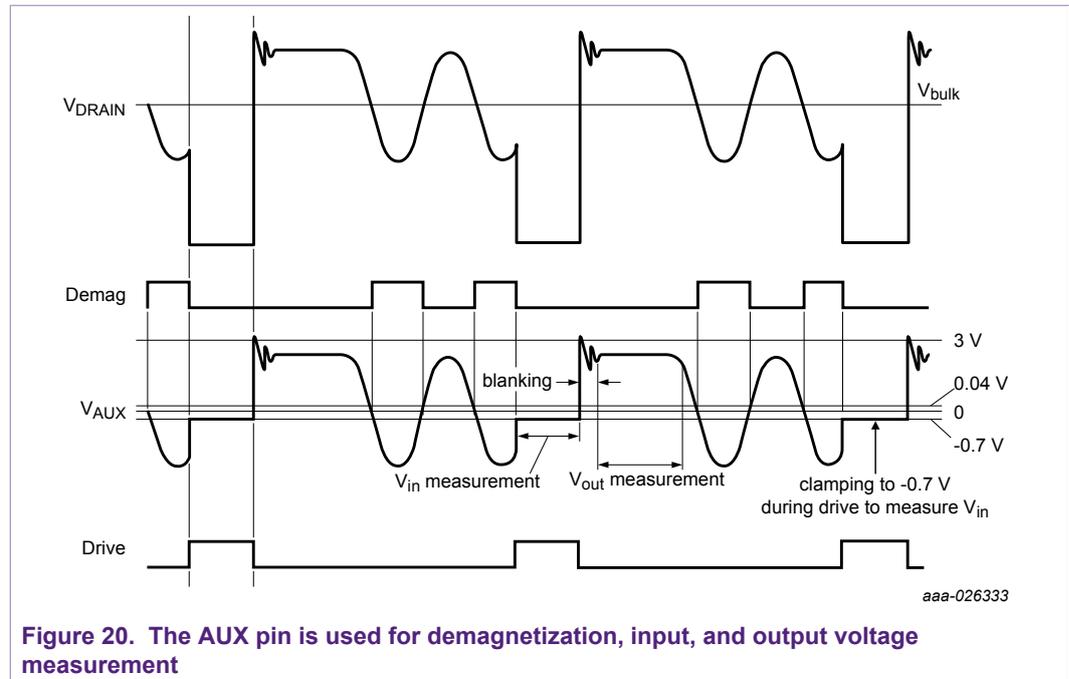
Figure 20. The AUX pin is used for demagnetization, input, and output voltage measurement

3.7.1 Demagnetization detection

When the signal on the AUX pin drops to below 40 mV, demagnetization is detected. This detection is essential for the DCM switching system. It shows that the transformer is demagnetized because the energy is transferred to the output and the current from the transformer to the output has become zero.

Demagnetization is also used to allow switch-on of the driver, so switching on in the top of the ringing is prevented. Switching on in the top of the ringing increases the switch-on losses.

3.7.2 Input voltage sensing for compensation

When the external MOSFET is switched on, the voltage at the auxiliary winding reflects the input voltage. During this period, an internal circuit clamps the voltage on the AUX pin to −0.7 V. The current from the auxiliary pin to the auxiliary winding via a series resistor is measured. This information is used to compensate for the overpower functions on the ISENSE pin.

The value of the resistor between the auxiliary winding and the AUX pin (R_{aux1}) and the winding voltage value during the primary stroke determine the current that flows. To achieve the required input voltage compensation level, the R_{aux1} value must match the voltage on the auxiliary winding. Figure 21 shows the relationship between the ISENSE switch-off voltage compensation and the current, measured through R_{aux1} during primary stroke.

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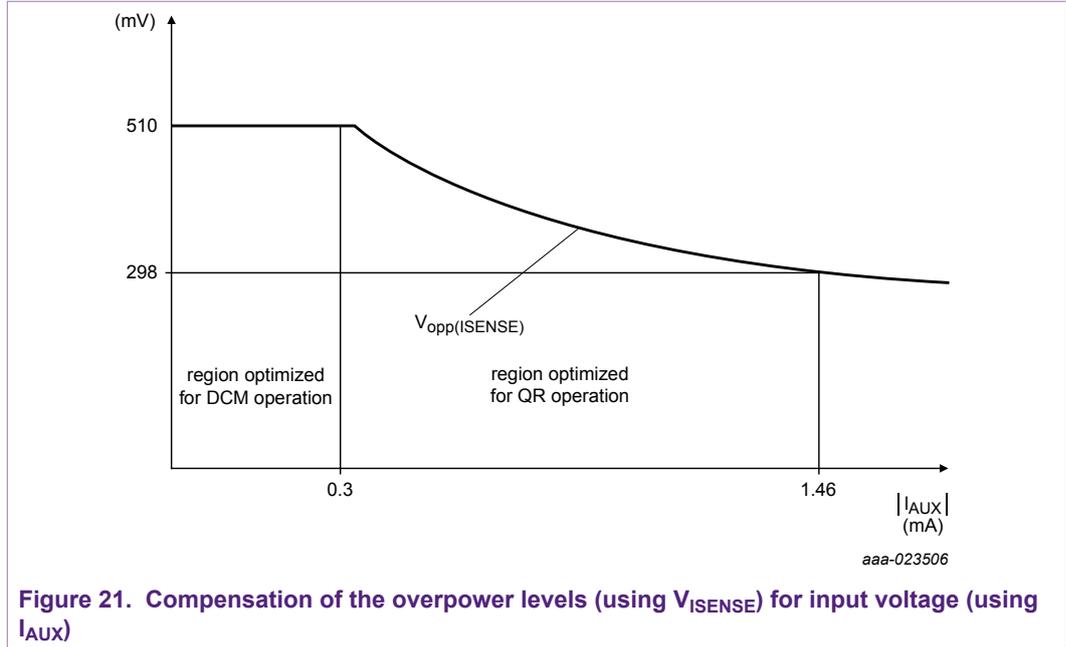
Figure 21. Compensation of the overpower levels (using V_{ISENSE}) for input voltage (using I_{AUX})

The compensation is optimized for use in QR mode. Though the IC can operate in QR mode, for spectral purity the TEA19362T must operate in DCM for all powers.

In DCM mode, the output power can be written as:

$$\tfrac{1}{2} \times L_p \times I_{pk}{}^2 \times f_{sw} \times \eta \tag{4}$$

Where:

- L_p is the primary inductance
- I_{pk} is the peak current value
- f_{sw} is the switching frequency
- η is the converter efficiency

In DCM mode, the maximum output power is only dependent on the maximum I_{pk} level. The maximum switch-off voltage level on the ISENSE pin, which triggers the OPP counter, determines the maximum I_{pk} level. This level is 510 mV. In practice, however, some I_{pk} overshoot exists for high input voltages, which is caused by the propagation delay time of the ISENSE comparator. This overshoot can be compensated by increasing the measured current on the AUX pin to slightly above 0.3 mA for high input voltages (e.g. exceeding 200 V (AC)). In this way, the maximum voltage level on the ISENSE pin can be reduced from 510 mV to e.g. 450 mV.

The main relationship between the input voltage for the flyback converter and the current measured at the AUX pin can be calculated with Equation 5:

$$I_{AUX} = \frac{V_{auxiliary\_winding} - V_{AUX}}{R_{aux1}} = \frac{V_{in} \times \frac{N_{aux}}{N_{prim}} - 0.7}{R_{aux1}} \tag{5}$$

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Because the AUX input combines the input voltage compensation with the OVP protection, a resistor R_{aux2} to GND is also connected. An additional small current flows to GND through the R_{aux2} resistor. At low mains voltage, a significant amount of current is added to the total current from the AUX pin (depending on the circuit values; e.g. 10 %).

$$I_{AUX(Raux2)} = \frac{0.7}{R_{aux2}} \tag{6}$$

$$I_{AUX(tot)} = \frac{V_{in} \times \frac{N_{aux}}{N_{prim}} - 0.7}{R_{aux1}} + \frac{0.7}{R_{aux2}} \tag{7}$$

The overpower functions use the compensation from the measured AUX current (see Section 3.8.1).

3.7.3 Output voltage sensing for OverVoltage Protection (OVP)

During the secondary stroke, the voltage on the AUX pin is proportional to the output voltage, which is used for an OVP protection for the secondary voltage.

To avoid a wrong level detection due to voltage ringing effects, output voltage sensing is enabled 2.4 µs after the primary MOSFET is switched off (see Figure 19 and Figure 20).

Together with the resistor for input voltage sensing (R_{aux1}), a voltage divider can be made using a resistor from the AUX pin to ground (R_{aux2}). The value of this resistor provides a conditioned signal at which an OVP can be detected. The preset internal level for OVP is 3 V. For a reliable protection function, the voltage on the AUX pin must reflect the output voltage accurately.

The basic relationship (neglecting the output voltage drop via the output rectifier and output cable) between the auxiliary voltage and the output voltage is the transformer turns ratio:

$$\frac{V_{auxiliary\_winding}}{V_O} = \frac{N_{aux}}{N_O} \tag{8}$$

The value of R_{aux1} must be determined for the overpower function. The value for R_{aux2} can be chosen to provide the correct protection level for the OVP.

$$V_{auxiliary\_winding} = \frac{N_{aux}}{N_O} \times V_O \tag{9}$$

$$V_{AUX} = \frac{R_{aux2}}{R_{aux1} + R_{aux2}} \times V_{auxiliary\_winding} = \frac{R_{aux2}}{R_{aux1} + R_{aux2}} \times \frac{N_{aux}}{N_O} \times V_O \tag{10}$$

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Example:

- $N_{aux} = N_O$
- $R_{aux1} = 47$ kΩ
- $V_{O(ovp)} = 25$ V
- $V_{AUX(ovp)} = 3$ V

Solving the equation above for R_{aux2}:

$$R_{aux2} = \frac{V_{AUX} \times R_{aux1}}{\frac{N_{aux}}{N_O} \times V_O - V_{AUX}} = \frac{3 \times 47 \times 10^3}{(1 \times 25) - 3} \approx 6.4\ k\Omega$$

3.8 Primary current sensing

The voltage across series resistor R_{sense} measures the primary current through the MOSFET switch. The ISENSE pin senses this voltage. In general, the peak level measured provides information about the power level.

The information about the input voltage (sensed by the AUX pin) and the current (sensed by the ISENSE pin) determines the maximum power level.

The converter power levels are set using the R_{sense} resistor value. During start-up and operation, the voltage on the ISENSE pin is used to decide when to switch off the MOSFET. It is also used to detect the various states of conversion.

3.8.1 Soft start

During soft start, the switch-off level on the ISENSE pin increases from zero to 510 mV (in 15 steps) in 3.6 sec. This increase minimizes stress and audible noise during supply turn-on.

Figure 22 shows an example of the I_{pk} behavior during start-up.
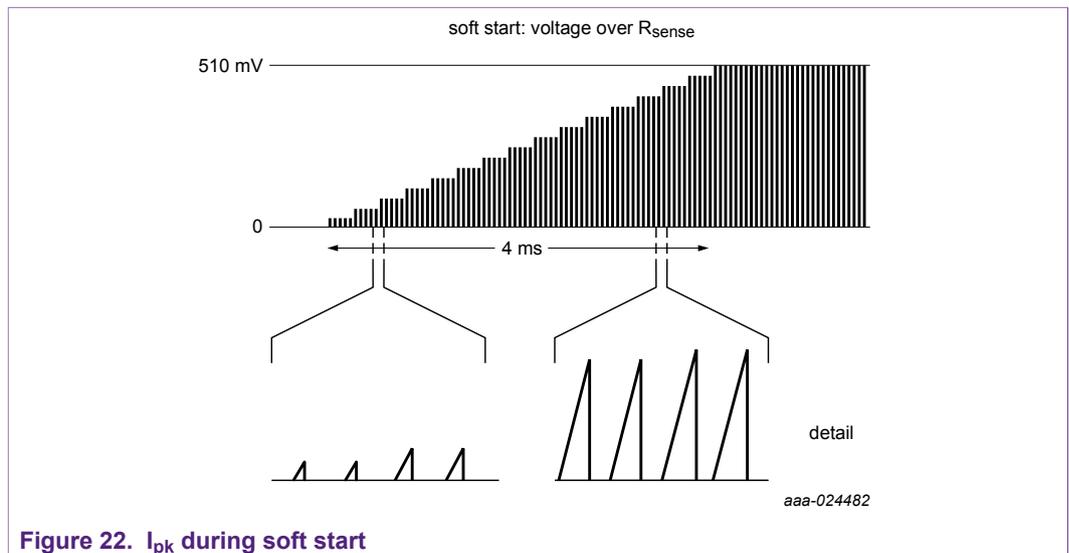
Figure 22. I_{pk} during soft start

The signal on the input of ISENSE is shown. It reflects the current, flowing through the R_{sense} resistor. It clearly shows the step-wise increase of I_{pk} until it reaches the maximum level.

3.8.2 OverPower Protection (OPP) counter

When the voltage on the ISENSE pin exceeds the overpower protection level (510 mV), the overpower counter is started. Depending on the input voltage compensation set on the AUX pin (see Section 3.7.2), the protection level can be lower for higher voltages. When the counter has finished, a safe restart is performed after 1000 ms. The counter delay time is 40 ms during start-up and 200 ms during operation. The shorter OPP counter timing during start-up reduces the input power during the output short circuit and repetitive restarts.

When V_{ISENSE} is lower than the protection level during one cycle, the overpower counter is reset.

When the reference voltage on the ISENSE pin is close to the protection level, the generated continuous average output power can be higher than the expected power. Due to variations of the ISENSE voltage over time, the counter can sometimes be reset.

3.8.3 OPP and UnderVoltage LockOut (UVLO) on the VCC pin

When the load increases to exceed the OPP level, the output voltage decreases. As a result, the voltage on the VCC pin drops as well. The UVLO protection can be triggered before the OPP counter has reached 200 ms (or 40 ms during start-up). To obtain the same behavior in an overpower situation (whether UVLO is triggered or not), the system enters the safe restart mode when overpower and UVLO is detected. The OPP counter value is ignored.

3.8.4 ISENSE pin accuracy

To ensure good quality information measured on the ISENSE pin, a leading-edge blanking is included. Parasitic capacitance can cause spikes, which trigger the peak current comparator prematurely. The ISENSE input is internally blanked the first 325 ns of each switch-on cycle.

A time delay exists between when the voltage level on the ISENSE pin reaches the MOSFET switch-off value and when the MOSFET is switched off ($t_{PD(sense)}$ = 120 ns). During that time, the primary current increases. The primary current increase during the delay period depends on the di/dt slope. The di/dt slope depends on the mains voltage. So, the resulting peak current in the converter partly depends on the mains voltage as well.
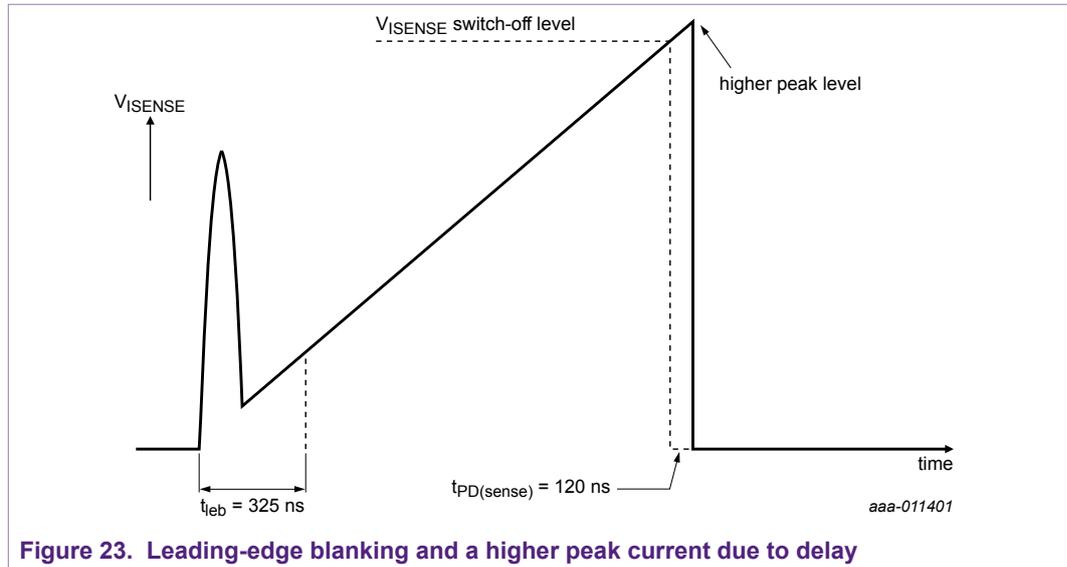
Figure 23. Leading-edge blanking and a higher peak current due to delay

Under extreme conditions, di/dt can also rapidly increase because the transformer starts to saturate. The di/dt slope depends on the transformer and converter design. These saturation conditions must be avoided because the converter operation is unpredictable.

3.8.5 ISENSE pin reference levels modulated by input voltage

During high output power conditions, the voltage ripple on the input voltage of the flyback converter has an impact on the compensation function of the AUX and ISENSE pins. Because the rectified mains voltage generates the input voltage, the bulk capacitor shows a ripple voltage when the output power is high. The result is that the average overpower levels are slightly lower at the lowest mains voltage or when a smaller value of the bulk capacitor is used.

3.9 Protections

If a protection is triggered, the controller stops switching. To ensure maximum up-time of the circuit when errors occur, every protection triggers a safe restart sequence.

To avoid false triggering, some protections have a built-in delay.

When the system stops switching, the VCCH and VCCL pins are not supplied via the auxiliary windings anymore. To perform a safe restart in a controlled way, the internal current source on the HV pin keeps the VCCL level above the critical level.

Table 4. Protections overview

Protection	Delay	Action	V_{CC} regulated
AUX open	no	wait until the AUX pin is connected	no
brownout	30 ms	wait until $V_{mains} > V_{brownin}$	yes
maximum on-time	no	safe restart 1000 ms	yes
OTP internal	no	safe restart 1000 ms	yes
OTP via PROTECT pin	2 ms to 4 ms	safe restart 1000 ms	yes

Protection	Delay	Action	V_{CC} regulated
OVP VCCL pin	4 cycles	safe restart 1000 ms	yes
OVP via AUX pin	4 cycles	safe restart 1000 ms	yes
overpower compensation	no	via AUX pin; cycle-by-cycle	-
overpower timeout	40 ms (start-up)	safe restart 1000 ms	yes
	200 ms (normal)		
overpower and UVLO	no	safe restart 1000 ms	yes
OCP	blanking time	cycle-by-cycle	no
UVLO	no	Wait until VCCL voltage > $V_{startup}$	yes

3.9.1 Safe restart sequence

If a protection is triggered and the system enters the safe restart mode, the system stops switching and restarts after an internally fixed period of 1000 ms. When the converter is not switching, the HV current source supplies the VCCL pin to 14.9 V. At restart, the system continues as in the normal start-up sequence.

3.9.2 Brownout

Brownout is discussed in <u>Section 3.5.2</u>.

3.9.3 Maximum on-time

To prevent extreme power under fault conditions, the controller limits the driver on-time for the external MOSFET to 55 μs. When the on-time exceeds 55 μs, the IC stops switching and enters a safe restart cycle. Normally, the on-time is never reached unless there is a fault condition.

3.9.4 OverTemperature Protection (OTP)

3.9.4.1 Internal OTP

When the internal temperature of the IC exceeds 140 °C, a safe restart is initiated. The temperature has to drop at least 10 °C before a restart is allowed.

3.9.4.2 OTP via the PROTECT pin

To provide overtemperature protection, an external temperature sensor can be connected to the PROTECT pin. Normally, an NTC resistor with a large value is used for good accuracy. During normal operation, the PROTECT pin delivers a current of 74 μA flowing out of the pin. When the voltage on the pin drops below 0.50 V, the protection is triggered. It forces a safe restart. To allow a restart, the voltage level on the PROTECT pin must exceed 0.55 V.

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When the voltage on the PROTECT pin exceeds 1.45 V, the internal current source is pinched off. When not used, connecting a capacitor on the PROTECT pin ensures that the capacitor is charged to 1.45 V. It is kept on that voltage, which disables the protection. A value of 10 nF works fine for this purpose.

3.9.5 OverVoltage Protection (OVP)

3.9.5.1 OVP on the VCCL pin

The VCCL pin can withstand a continuous 45 V. When the voltage on the VCCL pin exceeds 48 V, switching is stopped to protect the pin. To prevent erroneous triggering of the protection, the overvoltage must be present for 4 switching cycles.

3.9.5.2 OVP via the AUX pin

The OVP via the AUX pin is described in .

3.9.6 OverPower Protection (OPP)

OPP is described in and . The OPP input voltage compensation is described in .

4   Circuit design aspects

The circuit design is discussed using the schematic of a fast charge demo board. The board is designed to deliver output voltages of 5 V (DC), 9 V (DC), and 12 V (DC). The maximum output current is 2.1 A for all output voltages. Figure 24 shows the schematic.

Figure 24. Primary part direct charge demo board

4.1 Input section

A fuse (F1) prevents fire hazards that can be associated with unintended failure of components on the primary side of the application. A simple common-mode choke (L1) provides elementary filtering of unwanted EMI. The common-mode choke is preferably constructed in such a way that it includes some (controlled) leakage inductance. The leakage inductance can serve as a differential mode filter component without adding extra ohmic losses to the filtering circuit. Using the layout and the component placement, make sure that L1 does not pick up too much magnetic stray field of the transformer. The filter can be extended with a small X-capacitor (≤ 100 nF) between pins 2 and 3 of the common-mode choke. An additional differential mode filter (PI-filter) is found after the rectifier bridge. It consists of capacitors C1, C2, C3, C16, inductor L3, resistor R39, and ferrite bead FB2. FB2 is a small ferrite bead that plays a role in high-frequency noise suppression. Capacitors C1, C2, and C3 also operate as the buffer capacitors for the bus voltage (V_{bus}).

The HV pin of the TEA19362T IC is supplied from the rectified DC voltage after the diode bridge. Two resistors, R36 and R38, set the brownin and brownout levels. Two resistors in series are used to withstand the maximum DC voltage (375 V). For these resistors, 1206 SMD types with a voltage rating of 200 V can be used.

4.2 VCC supply voltage

Two auxiliary windings on the transformer provide the supply voltage for the internal operation of the TEA19362T. For optimal efficiency and lowest standby power, design the VCCH auxiliary winding voltage to keep VCCL above 12.5 V in a no-load condition at V_{out} = 5 V (default start-up condition for USB-PD). Check this requirement for all AC input voltages. It is important to keep the voltage on the VCCL pin well above $V_{restart}$ (11 V) in a no-load condition. When the voltage on the VCCL pin drops to below $V_{restart}$, additional strokes are made to increase it to 11 V. These additional strokes increase the output voltage. The increasing output voltage increases the optocurrent on the secondary side and the control current on primary side. The increasing optocurrent and control current increases the input power during no load with several mW.

When lower output voltages (e.g. 3 V) are also permitted for charging in current mode, check that VCCH is high enough to keep VCCL above 12.5 V under all required operating conditions at that output voltage.

Simply calculating the number of turns from the auxiliary windings cannot determine the voltage levels of the VCCH and VCCL pins (see Figure 25).

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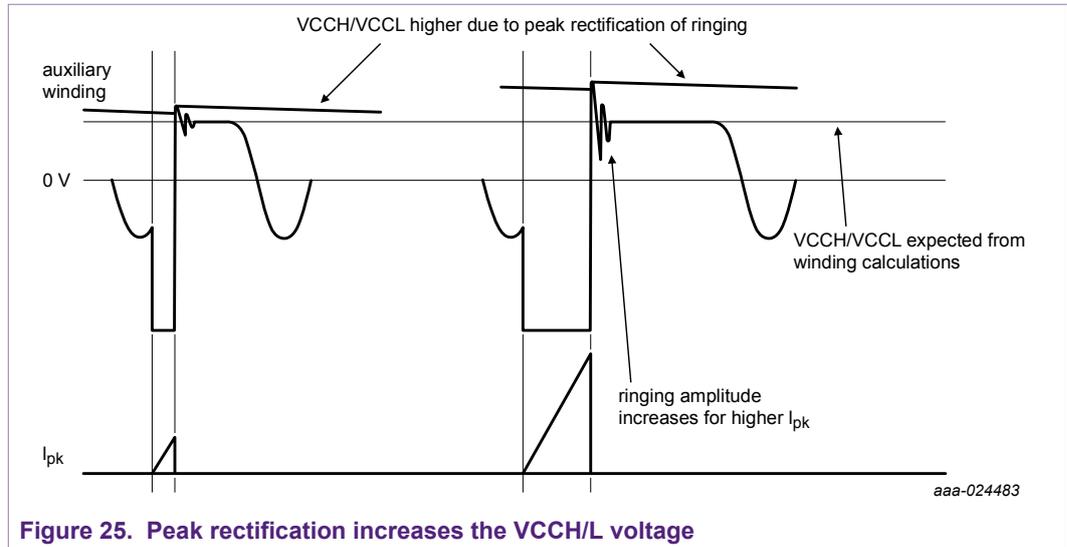
Figure 25. Peak rectification increases the VCCH/L voltage

Due to the ringing and peak rectification of the diode from the auxiliary winding to the VCCH/VCCL pins, the supply voltage can be much higher than expected from calculating the number of turns. The higher I_{pk}, the greater the ringing amplitude and the increase of the VCCH/VCCL voltage. A ratio of a factor 2 of the VCCH/VCCL voltage between burst mode (no load) and full load is not uncommon.

With faster rectifier diodes, the ratio between the supply voltages at burst no load and full load increases, because the peak rectification operation of these fast diodes is very good.

However, when covering a wide V_{out} range (e.g. 5 V to 20 V) and the voltage rating becomes tight, it is possible to use a slow diode for rectification. Because the slow diode conducts longer in reversed operation, the VCCH/VCCL capacitor damps the ringing. The damping reduces the VCCH/VCCL voltage increase for higher loads. The use of a slow diode for rectification causes some marginal efficiency loss. Standard mains diodes are suited for this purpose.

Finally, to tune the peak rectification more accurately, a fast diode with a small capacitor in parallel can be used.

When a limited output voltage range is required, only the VCCL pin can be used. In that case, use a 10 µF capacitor on the VCCL pin and connect the VCCH pin to the VCCL pin. Only one auxiliary winding is required for the supply.

When the VCCH pin and the VCCL pin are used, the capacitor on the VCCH pin must be 10 µF. The capacitor on the VCCL pin may range from 1 µF to 10 µF. A higher capacitance on the VCCL pin can achieve a slightly better no-load performance.

Place the VCCH/VCCL capacitors close to the pins. If that is not possible, put a 100 nF decoupling capacitor close to the pins.

4.3 I_{pk} current sensing

The peak current in the primary switch and in the primary inductance of the transformer is measured as the voltage across the parallel circuit of resistors R26 and R32. Putting two resistors in parallel eases tuning of the correct value and makes using smaller size SMDs possible. To minimize pickup of unwanted noise, place the filter, consisting of R21 and C19, as close to the ISENSE pin as possible.

4.4 MOSFET driver

The driver must be optimized for the used MOSFET. Driving the MOSFET too hard or too softly causes efficiency loss. For a flyback in DCM, switch-on must not be too fast. However, switch-off must be fast. Switch-on behavior is tuned using resistors R28 and R29. Their series resistance and the gate capacitance determine the speed of switch-on. The value of resistor R29 is chosen to balance efficiency and EMI. Resistor R28 mainly determines the switch-off speed, which is optimized for efficiency. Do not connect the driver directly to the MOSFET gate.

4.5 AUX pin

A resistive divider is connected to the AUX pin. The top of the resistive divider must be connected to one of the auxiliary windings, which provide the IC supply. In Figure 24, the signal that feeds to the AUX pin comes from the VCCH auxiliary winding. In that case, resistor R37 must be redimensioned accordingly. This resistor determines the mains compensation for the OPP level. The resistive divider and resistor R35 set the level for OVP (see Section 3.7 for details).

4.6 Feedback section

Avoid any noise and disturbance to the signal connected to the CTRL pin. The signal route from the optocoupler to the CTRL and GND pin must consist of two PCB tracks that are as short as possible. They must be routed next to each other, perfectly in parallel and without branches, other components, or current paths. Place capacitor C20 close to the CTRL pin and preferably across the two tracks coming from the optocoupler. Capacitor C20 and the internal resistance of the CTRL pin (1.5 kΩ) create an additional pole, which improves the loop stability.

4.7 PROTECT pin

The PROTECT pin is mostly used to provide a system OTP. When the voltage on the pin is lower than 1.45 V, a current of 74 µA flows out of the pin. The circuit is designed to use a 100 kΩ NTC (RT1). The exact temperature at which the PROTECT pin is triggered, can be tuned with the series resistor R27. When the voltage drops to below 0.50 V, the protection is triggered. When the voltage increases to exceed 0.55 V, the protection is cleared. To avoid any pickup of noise or disturbance, place capacitor C18 and resistor R27 close to the PROTECT pin.

The PROTECT pin can also be used for any other external protection. When the PROTECT pin is pulled down, switching stops. When the PROTECT pin is not pulled low any more, a safe restart initiates normal operation again.

When the PROTECT pin is not used, only connect a 1 nF to 10 nF capacitor close to the pin. The internal current source charges the capacitor to 1.45 V at start-up. The internal current source is then pinched off, which minimizes power consumption.

4.8 HV pin

Ensure that resistors R36 and R38 can withstand the maximum voltage at the highest mains input. The maximum DC voltage at capacitor C1 is 375 V, so resistors R36 and R38 must have a rating of at least 200 V. For the layout, the track from the HV pin with the resistors must not cross or come close to tracks leading to the PROTECT pin, the CTRL pin, or the AUX pin. When the HV pin track crosses or is routed near these tracks, crosstalk that originates from the very steep edges of the measuring pulses of the HV pin can cause a regulation disturbance.

4.9 Snubber section

To limit the overshoot of the ringing as a result of the primary to secondary stroke commutation, capacitor C15, resistors R21 and R22, and diode D4 constitute a clamp circuit. For proper working of the clamp, Diode D4 must be a slow type. Mains rectifier diodes are suited for this purpose. If necessary, the damping of the ringing can be controlled using resistor R22. Resistor R22 can be omitted in the circuit (use a short instead). Capacitor C15 and resistors R21 and R22 must have proper voltage ratings. When the leakage inductance (L_{lk}) of the transformer T1 is known, the voltage rating of these components can be calculated with Equation 11:

$$\frac{1}{2} \times L_{lk} \times I_{pk}^2 = \frac{1}{2} \times C15 \times V_{snub}^2 \tag{11}$$

which essentially results in:

$$V_{snub} = \sqrt{\frac{L_{lk}}{C15}} \times I_{pk} \tag{12}$$

Where:

- V_{snub} is the voltage that the snubber components capacitor C15 and resistors R21 and R22 must support
- L_{lk} is the maximum leakage inductance of the transformer
- I_{pk} is the highest peak current that can occur in the primary winding of the transformer This value is the maximum level on the ISENSE pin (510 mV) divided by the value of the sense resistor:

$$\frac{0.51}{R26 // R32} = \frac{0.51 \times (R26 + R32)}{R26 \times R32}$$

5 PCB layout aspects

Some PCB layout recommendations are given in this section. As an example, the layout of the 25 W USB-PD board of Section 4 is shown. Focus is on the left-hand side of the board where the primary side of the SMPS application resides. On the right-hand side of the PCB, the secondary side of the SMPS is implemented. In this case, the secondary side uses synchronous rectification driven with a TEA1993 SR controller. A TEA1905 USB-PD type C controller handles the interface the USB type C connector and the feedback to the primary side via the optocoupler.
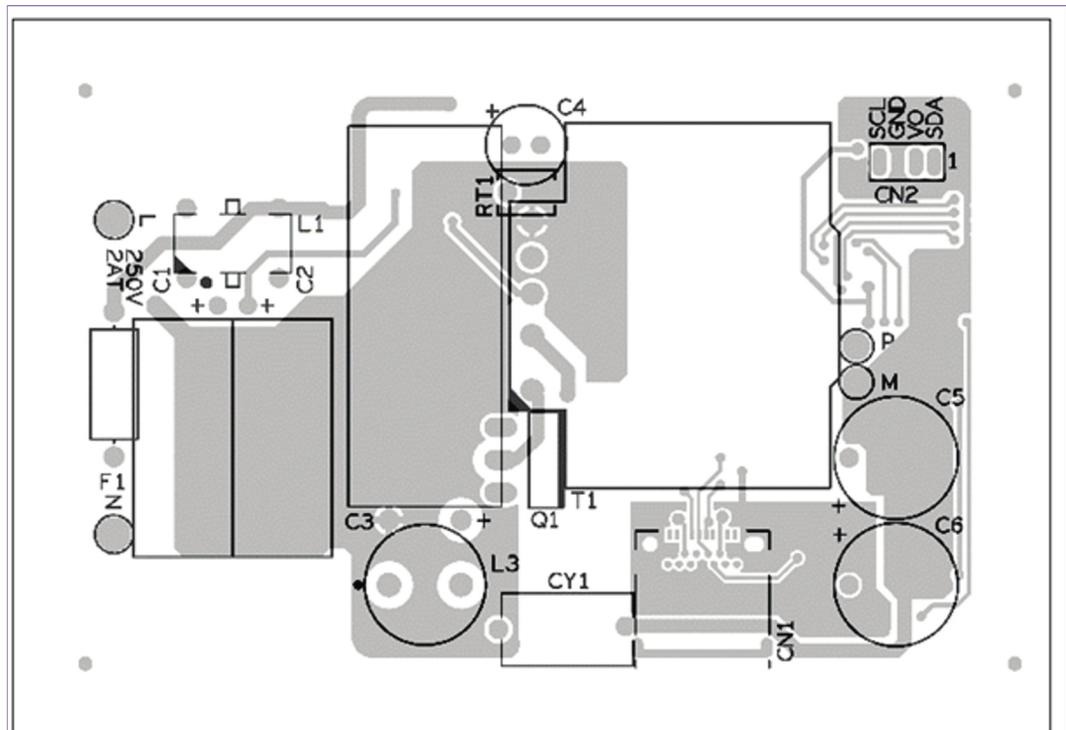
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Figure 26. Top copper and top silk screen
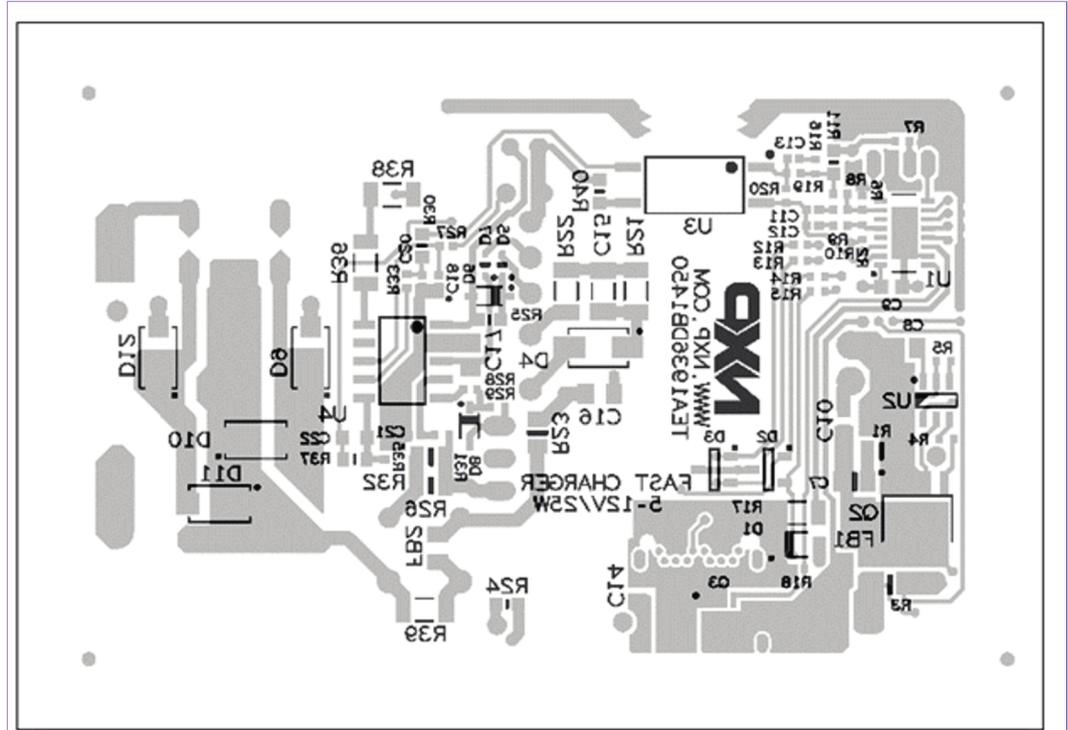
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Figure 27. Bottom copper and top silk screen (mirrored)

5.1 High current, high-frequency current loops

It is very important that the high-current and the high-frequency current loops are small. The enclosed area of the current loop, must be minimal. PCB traces must be as short as possible. Failing to meet this guideline may have adverse consequences for EMI emissions. They may also result in a higher than necessary susceptibility to induced EMI.

On the primary side, the main high-current/high-frequency current loop is the primary stroke loop. That loop follows the path C16 → T1 → Q1 → R26//R32 → C16. The negative electrode of capacitor C16 is the GND star point (see Section 5.6) on the primary side.

The main secondary stroke current loop is on the secondary side of this application. However, the snubber loop, which is also active during the secondary stroke does also carry a relatively high-current/high-frequency signal. Keep the loop T1 → D4 → R15// R21 → R22 → T1 small as well.

5.2 Lower current, high-frequency loops

The lower-current/high-frequency loops are less important. Keeping these loops small and the tracks short as well is beneficial for the application.

The most important of the lower-current/high-frequency loops is the MOSFET gate drive loop. That loop follows the path C17 → U4 → R28 → R29//D8 → Q1 → R26//R32 → C17.

Two additional lower-current/high-frequency loops are the VCCL loop and the VCCH loop:

- VCCL loop: T1 → D7 → C17 → T1
- VCCH loop: T1 → D25 → D6//R25 → C4 → T1
  A short often replaces D6//R25, reducing the loop to T1 → D25 → C4 → T1.

5.3 Sensitive signals

The signals that are connected to the ISENSE pin, the AUX pin, the CTRL pin, and the PROTECT pin are relatively low-amplitude signals. High-amplitude signals that have their origin in other nodes of the SMPS application can easily influence them. For that reason, take some measures that prevent the influence on these sensitive signals.

- The ISENSE pin has a relatively low-impedance connection (via R31) to an even lower impedance node (the R26//R32 sense resistors). So, the ISENSE pin is already immune to induced noise. Nevertheless, mount capacitor C21 very close to the TEA19362T ISENSE pin and the GND pin. Resistor R31 must have a very short connection to the ISENSE pin. If the trace leading to the R26//R32 sense resistors is slightly longer, that is fine.
- Place resistors R35 and R37 very close to the TEA19362T AUX pin. If capacitor C22 is mounted, place it also very close to the AUX pin. In addition, resistor R35 must have a short connection to the TEA19362T GND pin. The PCB traces between resistor R37 and transformer T1 and between the TEA19362T GND pin and T1 are probably slightly longer, which is not a problem. However, these two traces must run in parallel and the enclosed area within the traces must be minimal. The latter causes the signal fed to the AUX pin to be less susceptible to magnetically induced disturbances.
- The TEA19362T CTRL pin is a current controlled input. Nevertheless, resistor R33 and capacitor C20 must be mounted close to the CTRL pin and the GND pin. The traces fed to the emitter and collector pins of the U3 optocoupler must run in parallel. The enclosed area within the traces must be minimal. The GND connection of the optocoupler must not be combined with any other signal. The optocoupler must have its own connection to the TEA19362T GND pin.
- Capacitor C18 must be mounted close to the TEA19362T PROTECT pin and GND pin. Mount resistor R27 close to the PROTECT pin also. It minimizes the amount of copper connected to the PROTECT pin and reduces the potential amount of capacitive (dV/dt) crosstalk to that pin. Thermistor RT1 is potentially mounted remotely. The PCB track from resistor R27 and the GND track leading to RT1 must run in parallel. The enclosed area within the traces must be minimal.

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5.4 Noisy signals

The TEA19362T application produces noise in several locations in the circuit. That noise can either be voltage (dV/dt) noise or current (dI/dt) noise. Taking placement and layout precautions can prevent that the noise influences the operation of other parts of the TEA19362T circuit and other appliances through the emission of EMI.

Voltage (dV/dt) noise is coupled to other nodes in the circuit capacitively. The main high dV/dt nodes are:

- The drain node of MOSFET Q1 (the 'hot' side of the primary winding of transformer T1)
- The anode node of diode D5 (the 'hot' side of T1 VCCH auxiliary winding)
- The anode node of diode D7 (the 'hot' side of T1 VCCL auxiliary winding)
- The TEA19362T DRIVER pin
- The TEA19362T HV pin

Ensure that copper areas and traces associated with these nodes cannot cause crosstalk to sensitive nodes. Commonly used approaches would be:

- To keep these nodes away from sensitive nodes
- To minimize the copper area attached to these nodes
- To shield the nodes through a low-impedance (for example GND or a 'hard' fixed voltage) copper plane or trace

In this respect:

- Place MOSFET Q1 close to transformer T1
- Place diodes D5 and D7 close to transformer T1
- Try to keep the path from transformer T1 to R37//C22 short; R37//C22 must also be close to the TEA19362T AUX pin because of the sensitivity of the AUX pin node
- Place resistors R18 and R29 and diode D8 close to the TEA19362T DRIVER pin
  Try to keep the total length of the path from the DRIVER pin to the MOSFET Q1 gate short
- Place resistors R36 and R38 close to the TEA19362T HV pin
  It is not a problem when the path from the rectified mains voltage to resistor R38 is slightly longer. The reason is that the voltage at that node is a relatively 'fixed' (or low dV/dt) voltage

Current (dI/dt) noise is inductively coupled to other nodes in the circuit. The high dI/dt current loops are described in Section 5.1 and Section 5.2. To limit inductive coupling:

- Keep all high dI/dt loops small
  Preferably the traces are kept short. More importantly, the enclosed area within the loop must be minimized (keep feeding and return traces in parallel). Sometimes, it is possible to lay out a current loop as an 8-pattern. In that case, the magnetic field caused by the upper half of the 8 and the magnetic field caused by the lower half of the 8 partially cancel each other out at a slightly greater distance. In this way, magnetic stray field is reduced. Keep the track from the HV pin away from tracks to the CTRL pin, AUX pin, and PROTECT pin.
- Place the inductive filtering components L1 and L3 such that the magnetic stray field from transformer T1 does not couple to L1 and L3
  Using shielded magnetic components reduces susceptibility. However, placing the typical magnetic field patterns of the T1, L1, and L3 components perpendicularly, leads to minimized coupling. Taking the right precautions helps to achieve the EMI requirements of the application.

- Ensure that a high dI/dt trace or current path does not run close to and in parallel with a sensitive current path
Especially applicable to the sensitive current path that connects the optocoupler to the TEA19362T CTRL and GND pins. When two PCB traces (or current paths) are perpendicular, there is no inductive coupling in theory. In practice, the inductive coupling is minimized.

5.5 GND shield

Most connections between components are made on the bottom side of the PCB. Usually, most SMD components are mounted on the bottom side of the PCB. When a double-sided PCB is used, a major part of the copper that is available on the top side of the PCB can be used as a GND shield. The GND shield 'absorbs' high dV/dt noise. It limits the propagation of self-induced and externally induced noise to sensitive nodes.

A copper plane also helps to spread the heat that is dissipated in various components (mainly Q1, T1 and in some respects diodes D9, D10, D11, and D12). In that sense, the GND shield is also a relevant aspect in thermal management.

Important aspects of the GND shield are:

- The GND copper plane must not conduct current; especially, high-frequency high-amplitude currents must not flow in the GND shield
- The GND shield must have a single ground connection to the GND star point; ground loops through the GND shield must be avoided
- The GND shield must not be taken as a reference plane for a sensitive signal like the ISENSE signal, the AUX signal, the CTRL signal, or the PROTECT signal

5.6 GND star point

The GND star point is at the negative electrode of capacitor C16.
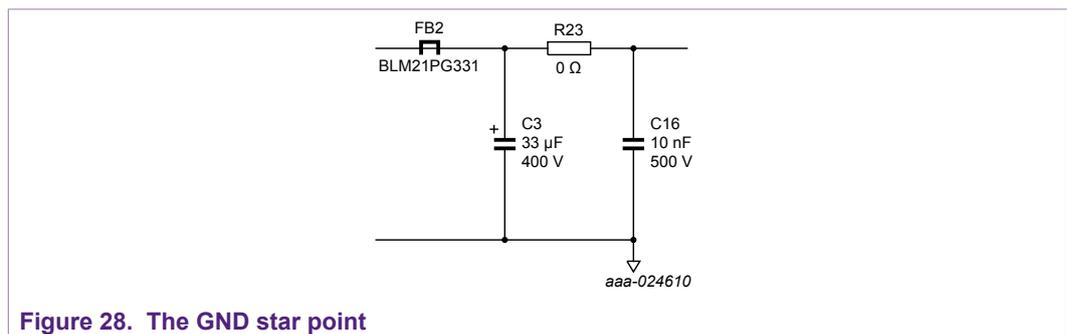
Figure 28. The GND star point

The following components must have their own (not combined) short connection to the GND star point:

- The parallel circuit of sense resistors R26//R32
- The TEA19362T GND pin

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Longer connections to the GND star point are allowed for:

- The negative electrode of capacitor C3
  The negative electrodes of capacitors C1 and C2, as well as the anodes of diodes D9 and D12 (rectifier bridge) must be connected to the negative electrode of capacitor C3. Do not connect them directly to the GND star point.
- The connection to the Y-capacitor CY1 (via resistor R24)
- The GND shield (see [Section 5.5](#))

The following components must have their (individual) connections to the TEA19362T GND pin. Do not connect them directly to the star point. Although, when the TEA19362T GND pin is very close to the star point, there may be little difference:

- Noise suppression capacitor C21
- Resistor R35
- Capacitor C18
  Thermistor RT1 is preferably connected to the negative terminal of capacitor C18 and not directly to the TEA19362T GND pin
- Capacitor C20
  The emitter of the U3 optocoupler is preferably connected to the negative terminal of capacitor C20 (via resistor R40) and not directly to the TEA19362T GND pin
- The 'cold' terminal of the T1 auxiliary windings
- Bulk capacitors C4 and C17
  Generally, connecting the T1 'cold' terminal and the C4 and C17 bulk capacitors to the star point is not a problem. When the connection between the TEA19362T GND pin and the star point is very short, the two points are the same. So, discriminating between the star point and the TEA19362T GND pin. is not necessary.

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6 Secondary side implementations - various options

Various secondary side implementations can cooperate with the TEA19362T primary side switcher.

Some examples:

- Single fixed voltage SMPS
  For example, a single 19.5 V output voltage (for notebooks).
- Multiple fixed voltage SMPS
  For example, simultaneous 12 V and 5 V output voltages.
- Single variable voltage SMPS
  For example, switchable (5 V, 9 V, 12 V, 19.5 V) or autoswitchable output voltage (for USB PD) that typically uses a TEA1903 or TEA1905 secondary controller.

Some implementation examples are described in the sections below. However, no extensive explanations are given. See the data sheets and application notes of the respective products that are used on the secondary side of that specific SMPS application for more information.

6.1 Single fixed output voltage

Figure 29. Typical single fixed output voltage SMPS

Figure 29 shows the single fixed output SMPS. To rectify the output voltage from the transformer, it uses a TEA1993T based synchronous rectifier circuit. Instead of a

synchronous rectifier circuit, a Schottky diode can be used to rectify the voltage from the transformer. For higher output voltages, using a Schottky diode instead of a synchronous rectifier is a solution that comes with a limited efficiency penalty. For low output voltages, the efficiency loss is significant.

The rectified voltage passes through a simple filter. It is then fed to the output terminals. The output voltage is also fed to a TL431-based regulator circuit. This circuit feeds an appropriate control signal to the optocoupler. That signal 'instructs' the TEA19362T to produce the desired amount of power.

6.2 Multiple fixed output voltages

The multiple fixed output voltage SMPS is a straightforward extension of the single fixed output voltage SMPS. The secondary winding on the transformer is duplicated and dimensioned to generate a different output voltage. The same is true for the rectification part.

Regulation is done using a TL431-based circuit. The dimensioning of resistors R6, R8, and R8A determines the output voltages of the two pairs of output voltage terminals. It also determines the weight that each output voltage has on the regulation mechanism.
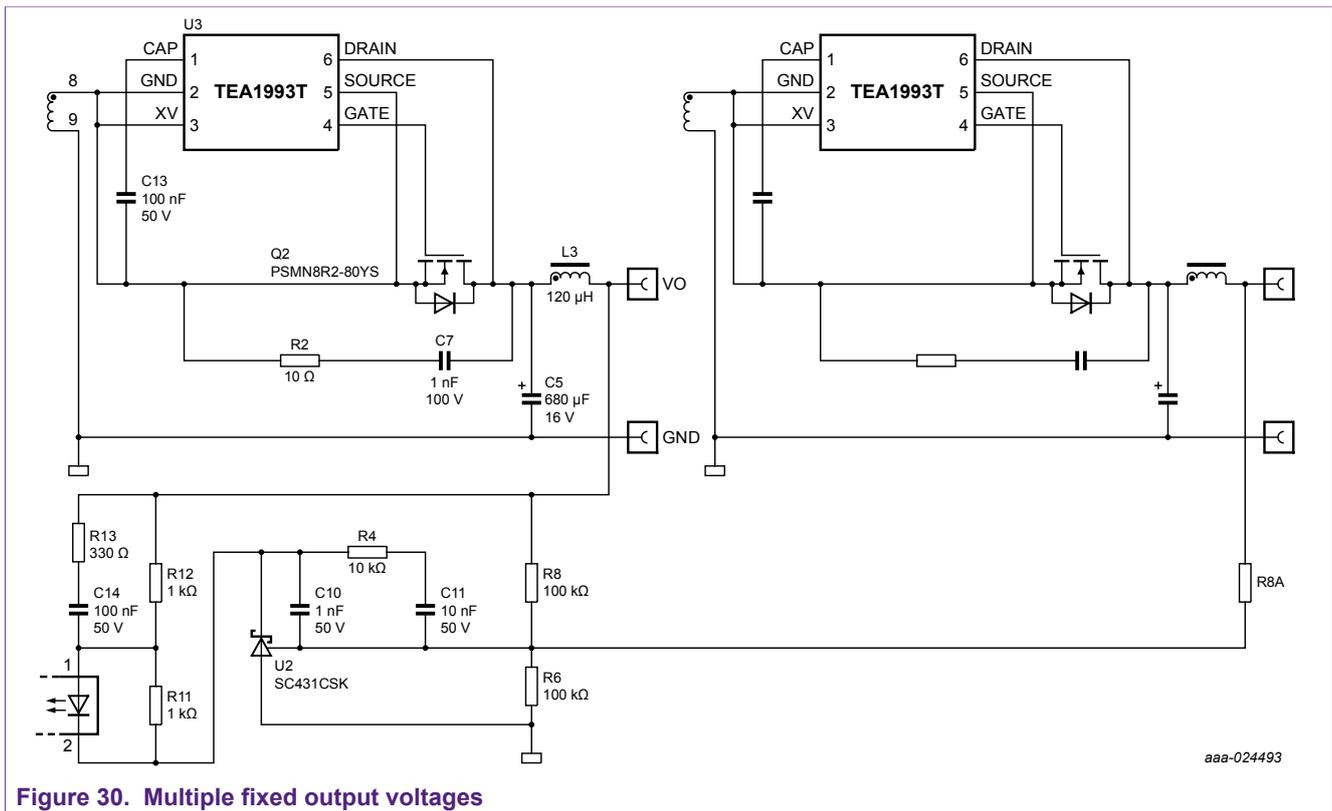
Figure 30. Multiple fixed output voltages

As in the single fixed output voltage SMPS, Schottky diodes can replace the synchronous rectifier circuits diodes. However, the consequence is efficiency loss (see Section 6.1).

6.3　Single variable output voltage

Figure 31 shows the USB PD SMPS. A TEA1993T-based synchronous rectifier rectifies the output voltage from the transformer. A TEA1905 USB PD controller negotiates the output voltage with the load. It switches the output voltage when required. It feeds the proper control signal to the optocoupler. In this way, the TEA19362T controller is 'instructed' to produce the right amount of power.

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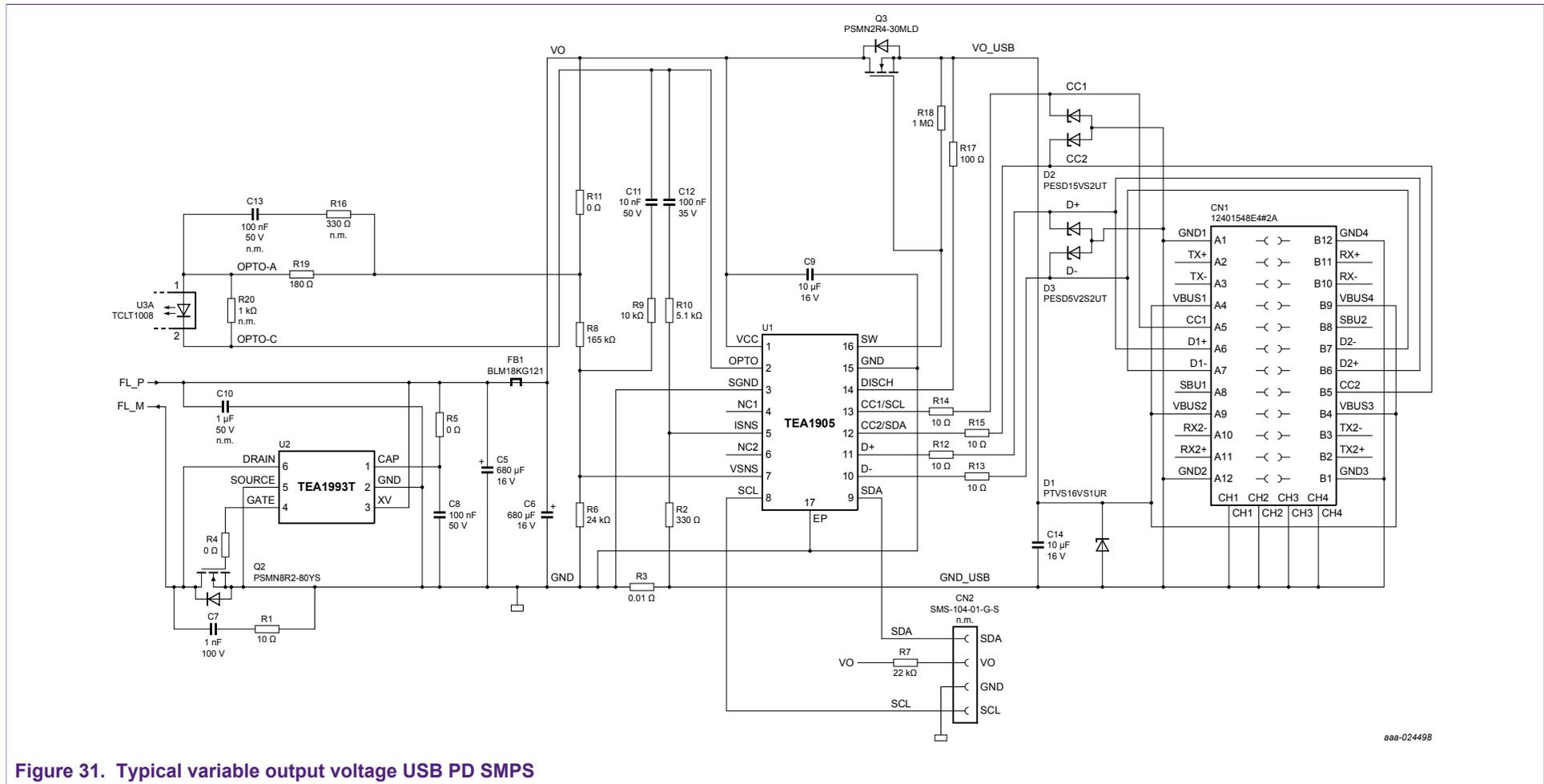
Figure 31.　Typical variable output voltage USB PD SMPS

7 Abbreviations

Table 5. Abbreviations

Acronym	Description
BCM	Boundary Conduction Mode
CC	Constant Current
CMN	Common-Mode Noise
CV	Constant Voltage
DCM	Discontinuous Conduction Mode
EMI	ElectroMagnetic Interference
FFM	Fixed-Frequency Mode
FRM	Frequency Reduction Mode
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
OPP	OverPower Protection
OTP	OverTemperature Protection
OVP	OverVoltage Protection
QRM	Quasi-Resonant Mode
SR	Synchronous Rectification
SMPS	Switched Mode Power Supply
UVLO	UnderVoltage LockOut

8 References

1 **TEA19362T data sheet** GreenChip SMPS primary side control IC with fixed frequency operation; 2016, NXP Semiconductors.

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