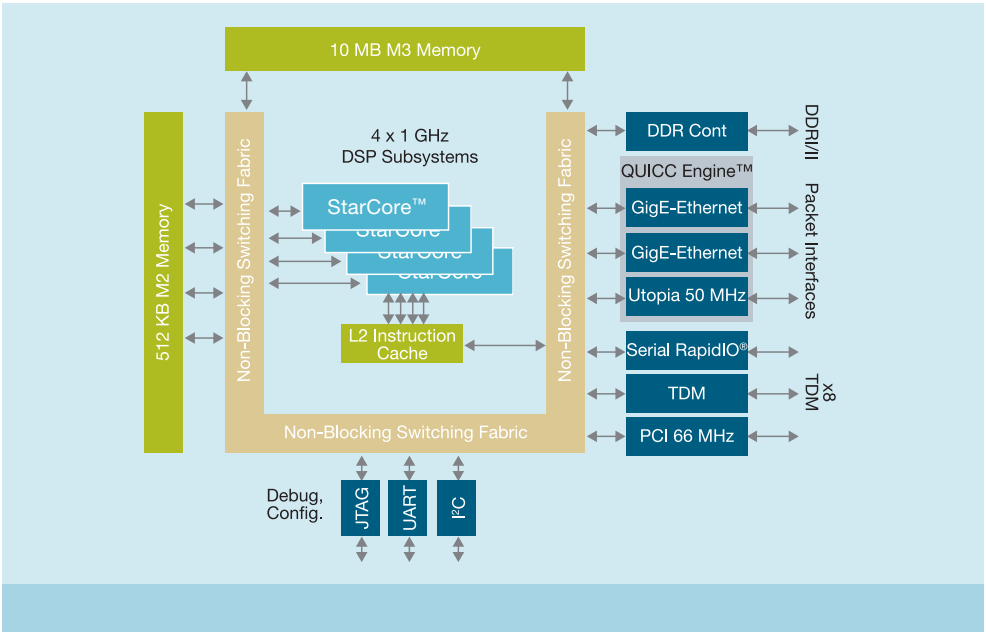
MSC8144

Freescale's MSC8144 third-generation multi-core Digital Signal Processor (DSP), targeting wireless and wireline infrastructure equipment, is Freescale's highest performing multi-core programmable DSP based on StarCore™ technology designed for optimal triple-play (voice, video and data) services. With four embedded cores running at up to 1 GHz each, the MSC8144 delivers 4 GHz-equivalent performance along with extensive scalability, programmability and network interfaces.

Freescale has a proven pedigree for developing processors that meet customers' current and future needs, and understanding market demands for a processing-intensive solution that supports legacy, transition and next-generation system interface requirements.

The MSC8144 meets those demands with the industry's largest on-chip memory and highest I/O bandwidth. Wireline and wireless applications ranging from carrier class/enterprise VoIP media gateway equipment and video conferencing equipment to WCDMA and WiMAX base stations are among the many that can benefit from this optimized solution. Achieving high voice and video channel densities with a focus on low power per channel and low cost per channel, the MSC8144 provides a robust and reliable DSP platform for telecom and enterprise infrastructure equipment makers.

MSC8144 Block diagram



Target Applications in Telecom and Enterprise Infrastructure Equipment

- Wireless IMS/transcoding gateway
- Carrier-class and trunking VoIP media gateway
- Video conferencing and H.324M media gateway
- 3G/3.9G/Super3G/WiMAX base stations
- Radio Network Controllers

One Programmable DSP Platform, Supporting Multiple Standards via Software

VoIP/Data Standards

- Wireless Codecs
  - AMR-NB and WB
  - EVRC
  - QCELP
  - EFR
- Wireline/Fax Codecs
  - G.729AB
  - G.723.1
  - G.726, G.726A
  - G.728
  - G.711 (App 1 and 2)
  - G.165/168
  - T.38, V90, V42, V34
  - iLBC

Videoconferencing Standards

- Video Codecs
  - MPEG-4
  - H.264/AVC
  - H.263
  - H.261
  - MPEG-2
  - 3G-H.324M

Wireless Standards

- 3GPP
- WiMAX
- GSM
- OFDM
- SDR
- TD-SCDMA
- CDMA-2000

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Key Advantages

- Convergence
  - Addresses voice, video and data processing
  - Supports extensive next-generation and legacy peripherals
  - Supports multiprotocol migration for triple-play and IMS networks
- Cost effectiveness
  - Achieves a new level of performance density for high-capacity infrastructure applications
  - Offers industry's largest embedded memory to help increase channel densities and reduce total system cost, board space and power dissipation
  - Highest performance at lowest power per channel
- Compatibility
  - Maintains binary compatibility for easy upgrade from today's SC140-based software
  - Offers user-friendly, high-level C code, control and DSP code

Features

- Four fully-programmable StarCore SC3400 DSP cores, each running at up to 1 GHz for 4 GHz-equivalent performance
- Each subsystem includes:
  - SC3400 DSP core
  - 16 KB instruction cache, 32 KB data cache
  - Memory Management Unit (MMU) for memory protection and address translation
  - Debug and profiling unit
  - Interrupt controller and timers
- 10.5 MB embedded memory—the industry's largest—in a single package.
- Architecture highly optimized for voice, fax, video and data compression processing with industry-leading channel densities
- QUICC Engine™ communications technology—dual internal RISC-based packet-processing engine supporting multiple networking protocols for reliable data transport over packet networks, while off-loading the processing from the DSP cores
- 128 KB shared L2-cache
- Supports next-generation and legacy interfaces
  - 1x/4x Serial RapidIO®
  - Packet
    - Dual Ethernet controllers supporting RGMII, SGMII, MII, RMII, SMII
    - UTOPIA L2 50 MHz 8-/18-bit slave, supporting AAL1, AAL2, AAL5 ATM adaptation layers in firmware
  - TDM
    - 2048 DS-0 channels in eight independent ports
  - Host/master
    - PCI—PCI 2.2 controller, master/agent, 32-bit at 66 MHz
- External memory interface
  - 16-/32-bit DDRI/DDRII at 400 MHz data rate, 32 channels DMA
- Debug, boot, configuration
  - I^2C, UART, EonCE/JTAG
- Package/voltage/process
  - 29 mm x 29 mm FCPBGA, 1 mm pitch
  - Core nominal voltage—1V
  - M3 memory voltage—1.2V
  - I/O voltage—1.8V/2.5V/3.3V
  - 90 nm SOI

Development Tools

Freescale CodeWarrior® Tools

- Integrated development environment
- ANSI 'C', 'C++' optimizing compilers
- Source level debugger
- SmartDSP-OS—multi-core, royalty-free operating system
- Multi-core, royalty-free operating system
- Integrated device drivers
- Integrated cycle and functional accurate simulators

Enea® OSEck RTOS

- OSEck real-time kernel
- Preemptive multi-tasking
- Multi-core DSP support
- OSEck soft kernel environment
- OSEck link handler
- OSEck illuminator
- Board support package

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

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