Fact Sheet

MPC7400

HOST MICROPROCESSORS

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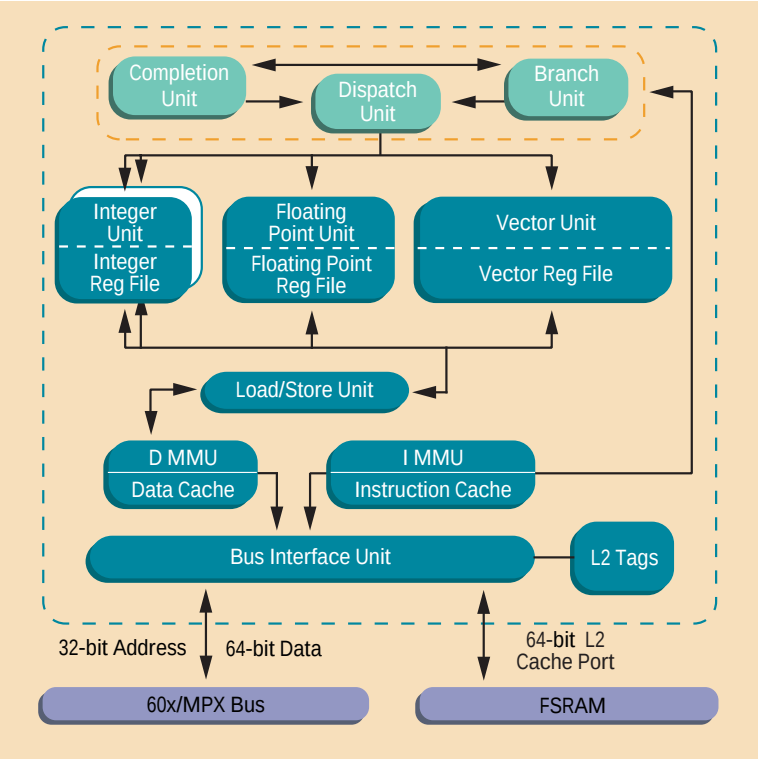
The MPC7400 host microprocessor is a high-performance, low-power, 32-bit implementation of the PowerPC Reduced Instruction Set Computer (RISC) architecture combined with a full 128-bit implementation of Motorola's AltiVec™ technology instruction set, creating a high-performance RISC microprocessor ideal for leading-edge computing, control, and signal processing functions. The MPC7400 supports the high-bandwidth MPX bus with minimized signal setup times and reduced idle cycles to increase maximum operating frequency to over 100 MHz, increased address bus bandwidth, increased data bus bandwidth, and more enhancements. To maintain backward compatibility for existing applications, the MPC7400 also supports the 60x bus protocol. MPC7400 microprocessors offer single-cycle double-precision floating-point performance, provide full symmetric multiprocessing (SMP) capabilities, and support up to 2 MB of backside L2 cache. While the MPC7400 is software-compatible with existing applications for MPC6xx and MPC7xx microprocessors, to utilize the full potential of this AltiVec technology-enabled device, some instruction changes in existing source code are required to interface with the vector execution unit.



SUPERSCALAR MICROPROCESSOR

MPC7400 microprocessors feature a high-frequency superscalar PowerPC architecture core, capable of issuing three instructions per clock cycle (two instructions + branch) into seven independent execution units:

- Two integer units
- Double-precision floating-point unit
- Vector unit
- Load/store unit
- System unit
- Branch processing unit

ALTIVEC TECHNOLOGY

AltiVec technology expands the capabilities of Motorola's G4 microprocessors by providing leading-edge, general-purpose processing performance while concurrently addressing high-bandwidth data processing and algorithmic-intensive computations in a single-chip solution. AltiVec technology:

- Meets the computational demands of networking infrastructure such as multichannel modems, echo cancellation equipment, and basestation processing.
- Enables faster, more secure encryption methods optimized for the SIMD processing model.

MPC7400 Host Processor	
CPU Speeds – Internal	350, 400, 450, and 500 MHz
CPU Bus Dividers	x3, x3.5, x4, x4.5, x5, x5.5, x6, x6.5, x7, x7.5, x8, x9
Bus Interface	64-bit
Bus Protocol	MPX/60x
Instructions per Clock	3 (2 + Branch)
L1 Cache	32 KB instruction 32 KB data
L2 Cache	512 KB, 1 MB or 2 MB
Core-to-L2 Frequency	1:1, 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1
Typical/Maximum Power Dissipation	5.0W/11.5W @ 400 MHz
Die Size	83 mm^2
Package	360 CBGA
Process	0.18µ 5LM CMOS
Voltage	1.8V internal, 1.8/2.5/3.3V I/O
SPECint95 (estimated)	21.4 @ 450 MHz
SPECfp95 (estimated)	20.4 @ 450 MHz
Other Performance	825 MIPS @ 450 MHz
Execution Units	Integer(2), Floating-Point, Vector, Branch, Load/Store, System

- Provides compelling performance for multimedia-oriented desktop computers, desktop publishing, and digital video processing.
- Enables real-time processing of the most demanding data streams (MPEG-2 encode, continuous speech recognition, real-time high-resolution 3-D graphics, etc.).

POWER MANAGEMENT

MPC7400 microprocessors feature a low-power 1.8V design with three power-saving user-programmable modes—nap, doze (with bus snoop), and sleep—which progressively reduce the power drawn by the processor. The MPC7400 also provides a thermal assist unit and instruction cache throttling for software-controllable thermal management.

CACHE AND MMU SUPPORT

The MPC7400 microprocessor has separate 32 KB, physically addressed instruction and data caches. Both caches feature cache locking and are eight-way set-associative. The MPC7400 microprocessor's dedicated L2 cache interface with on-chip L2 tags features a very fast (up to core speed, 1:1) interface to memory, instruction-only or data-only modes, and parity checking on both L2 address and data.

MPC7400 microprocessors contain separate memory management units (MMUs) for instructions and data, supporting 4 petabytes (2^{52}) of virtual memory and 4 GB (2^{32}) of physical memory. They also offer four instruction block address translation (iBAT) and four data block address translation (dBAT) registers.

MPX BUS INTERFACE

MPC7400 microprocessors support the MPX bus architecture with a 64-bit data bus and a 32-bit address bus. Support is included for burst, split, and pipelined transactions; data streaming; out-of-order transactions; and data intervention (in SMP systems). The interface provides snooping for data cache coherency. The MPC7400 implements MERSI coherency protocol for multiprocessing in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

EXAMPLE APPLICATIONS

- Networking and telecommunications infrastructure
- High-performance computing (scientific, medical, etc.)
- Desktop and portable computing

CONTACT INFORMATION

Motorola offers user's manuals, application notes, sample code, and full local support for all of its processors. For more information, visit:
http://motorola.com/smartnetworks

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at:
1-800-521-6274 or http://motorola.com/semiconductors

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