Fact Sheet

MPC603R

MICROPROCESSOR

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The Motorola MPC603r microprocessor is a low-power implementation of the PowerPC Reduced Instruction Set Computer (RISC) architecture. The MPC603r microprocessor offers workstation-level performance packed into a low-power, low-cost design ideal for desktop computers, notebooks, and battery-powered systems, as well as printer and imaging equipment, telecommunications systems, networking and communications infrastructure, industrial controls, and home entertainment and educational devices. Industrial-grade, extended-temperature MPC603r microprocessors are available for harsh operating environments. The MPC603r microprocessor is software- and bus-compatible with the MPC7xx and MPC74xx microprocessor families.

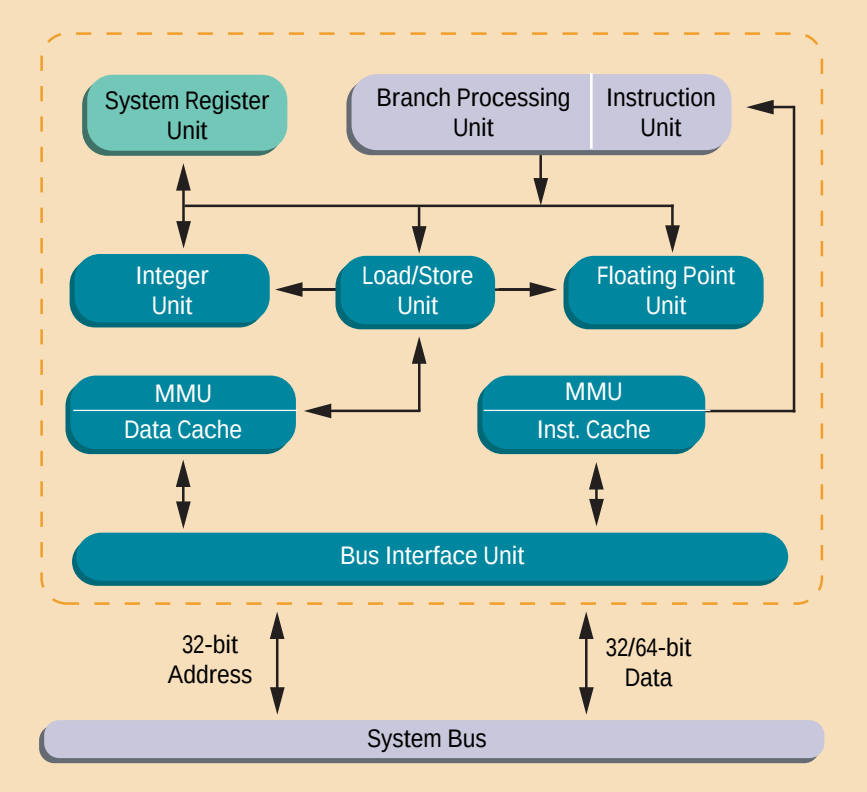
SUPERSCALAR MICROPROCESSOR

The MPC603r microprocessor is a superscalar design capable of issuing three instructions per clock cycle into five independent execution units, including:

- Integer unit
- Load/store unit
- Floating-point unit
- System register unit
- Branch processing unit

The ability to execute multiple instructions in parallel, the ability to pipeline instructions, and the use of simple instructions with rapid execution times yields maximum efficiency and throughput.

MOTOROLA MPC603R BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

The MPC603r microprocessor features a low-power 2.5V or 3.3V design with three power-saving modes—doze, nap, and sleep. These user-programmable modes progressively reduce the power drawn by the processor. The microprocessor also uses dynamic power management to selectively activate functional units as they are needed by the executing instructions. Unused functional units enter a low-power state automatically without affecting performance, software execution, or external hardware.

CACHE AND MMU SUPPORT

The MPC603r microprocessor has separate 16 KB, physically addressed instruction and data caches. Both caches are four-way set-associative. The microprocessor also contains separate memory management units (MMUs) for instructions and data. The MMUs support 4 petabytes (2^{52}) of virtual memory and 4 GB (2^{32}) of physical memory. Access privileges and memory protection are controlled on block or page granularities. Large, 64-entry translation lookaside buffers (TLBs) provide efficient physical address translation and support for demand virtual-memory management on both page- and variable-sized blocks.

FLEXIBLE BUS INTERFACE

The MPC603r microprocessor has a selectable 32- or 64-bit data bus and a 32-bit address bus. Support is included for burst, split, and pipelined transactions. The interface provides snooping for data cache coherency. The microprocessor maintains MEI coherency protocol in hardware, allowing access to system memory for additional caching bus masters, such as DMA devices.

CONTACT INFORMATION

Motorola offers user's manuals, application notes, and sample code for all of its processors. Local support for these products is also provided. This information can be found at: http://motorola.com/smartnetworks

For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at 800-521-6274 or http://motorola.com/semiconductors

	MPC603r 100-133 MHz	MPC603r 200-300 MHz
CPU Speeds – Internal	100 and 133 MHz	200*, 266 and 300 MHz
CPU Bus Dividers	x1.5, x2, x2.5, x3, x3.5, x4	x2, x2.5, x3, x3.5, x4, x4.5, x5, x5.5, x6
Bus Interface	64- and 32-bit modes	64- and 32-bit modes
Instructions per Clock	3 (2 + Branch)	3 (2 + Branch)
L1 Cache	16 KB instruction 16 KB data	16 KB instruction 16 KB data
Typical/Maximum Power Dissipation	4.2W/5.3W @ 133 MHz	4.0W/6.0W @ 300 MHz
Die Size	98 mm^2	42 mm^2
Package	240 CQFP, 255 CBGA	255 CBGA - all: 255 PBGA @200
Process	0.5µ 4LM CMOS	0.29µ 5LM CMOS
Transistors	2.6 million	2.6 million
Voltage	3.3V	3.3V I/O, 2.5V internal
SPECint95 (estimated)	3.9 @ 133 MHz	7.4 @ 300 MHz
SPECfp95 (estimated)	3.1 @133 MHz	6.1 @ 300 MHz
Other Performance	188 MIPS @ 133 MHz	423 MIPS @ 300 MHz
Execution Units	Integer, Floating-Point, Branch, Load/Store, System Register	Integer, Floating-Point, Branch, Load/Store, System Register

*see hardware specifications for operation at lower frequencies

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