MOTOROLA MPC106
PCI BRIDGE/MEMORY CONTROLLER

The MPC106 PCI Bridge/Memory Controller provides a PowerPC architecture compliant bridge between MPC6xx and MPC7xx microprocessors and the Peripheral Component Interconnect (PCI) bus. PCI support allows system designers to design systems quickly using peripherals already designed for PCI and the other standard interfaces available in the personal computer hardware environment. The MPC106 integrates secondary cache control and a high-performance memory controller that supports DRAM, SDRAM, EDO DRAM, ROM and Flash ROM. The MPC106 uses an advanced, 3.3-volt CMOS process technology and is fully compatible with TTL devices.

Multiprocessor and L2 Cache Support

The MPC106 supports a programmable interface to microprocessors operating at bus frequencies up to 83.3 MHz. The MPC106 processor interface allows for a variety of system configurations by providing support for either a second processor or a secondary (L2) cache. The L2 cache control unit generates the arbitration and support signals necessary to maintain a write-through or write-back lookaside cache.

PCI Bus Support

The MPC106 PCI interface is designed to connect the processor and memory buses to the PCI local bus without the need for "glue" logic. The MPC106 acts as both a master and slave device on the PCI bus.

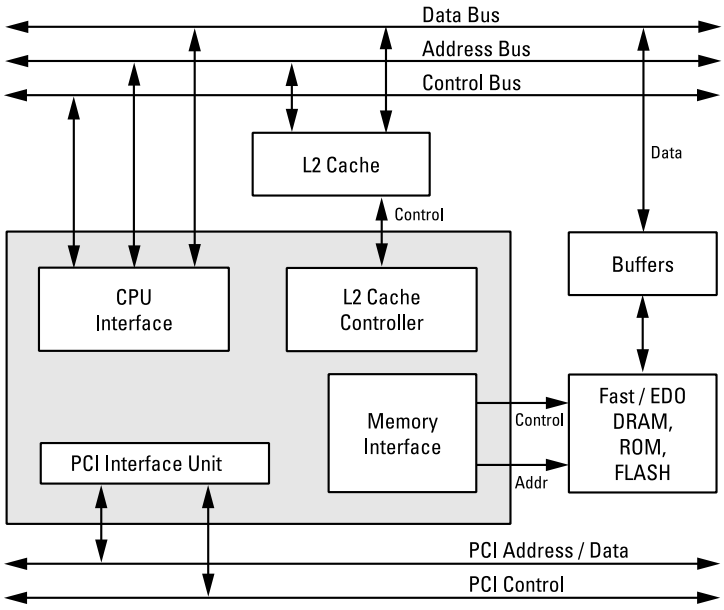
Integrated Memory Controller

The memory interface controls processor and PCI interactions to main memory. It supports a variety of DRAM, SDRAM or EDO DRAM, and ROM or Flash ROM configurations.

Power Management

The MPC106 provides hardware support for four levels of power reduction–nap, doze, sleep, and suspend. The MPC106 design is fully static, allowing internal logic states to be preserved during all power saving modes.

Motorola MPC106 Block Diagram



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MPC106 Major Features

Processor Interface

- Processor frequency up to 350 MHz and processor bus frequency up to 83.3 MHz
- 64-bit data bus and 32-bit address bus
- Provides support for either an external L2 cache or a secondary processor
- Full memory coherency supported

Secondary cache control

- 256-Kbyte, 512-Kbyte, 1-Mbyte sizes
- Direct-mapped
- Provides support for either asynchronous SRAM, burst SRAM, or pipelined burst SRAM
- Supports external lookaside L2 cache controller

PCI Interface

- Compliant with PCI specification, revision 2.1
- Interface operates up to 33 MHz
- 3.3-volt/5.0-volt compatible
- Read and write buffers to improve PCI performance
- Concurrent transactions on processor and PCI busses supported

Memory Interface

- Supports page mode DRAM, SDRAM, or EDO DRAM
- High-bandwidth (64-bit) data bus
- Supports 1 to 8 banks built of x1, x4, x8, x9, x16 or x18 DRAM chips
- 1 Gbyte of RAM space, 16 Mbytes of ROM space
- Supports writing to Flash EPROMs
- Supports parity or error-correcting code (ECC)

IEEE 1149.1-compliant, JTAG boundary-scan interface

304-pin ball grid array (BGA) package

Contact Information

- For more information on Motorola processors, point your web browser to:
  http://motorola.com/smartnetworks
- For all other inquiries about Motorola products, please contact the Motorola Customer Response Center at:
  Phone: 800-521-6274 or
  http://www.motorola.com/semiconductors