Freescale Semiconductor, Inc.

The Effect of Solder-Joint Temperature Rise on Ceramic-Ball-Grid Array to Board Interconnection Reliability: The Motorola PowerPC 603™ and PowerPC 604™ Microprocessors and MPC105 Bridge/Memory Controller

R. David Gerke

Gary B. Kromann

Ⓜ MOTOROLA

Advanced Packaging Technology
6501 William Cannon Dr., OE55
Semiconductor Products Sector,
Austin, Texas 78735

ABSTRACT

To predict solder joint reliability of surface-mount technology, a key parameter is: the temperature rise above ambient at the solder joint, ΔT. In-situ field temperature measurements were taken for a range of computer platforms in an office environment, at the central-processing units. Printed-circuit boards (PCB) were not uniform, therefore only maximum temperature regions of the board were measured. These maximum temperatures revealed the mean to be less than 20°C above ambient (i.e., $\Delta T < 20$°C) regardless of the power of the device. The largest ΔT measured in any system was less than 30°C above ambient. These temperature measurements of actual computer systems are in close agreement with IPC-SM-785. By utilizing the measured PCB temperature rise, solder joint fatigue life was calculated for the 21mm ceramic ball-grid-array (CBGA), the package for the PowerPC 603™ and PowerPC 604™ RISC microprocessors. For the MPC105 PCI Bridge/Memory Controller package, data from both the 21mm and 25mm CBGA, were used for the estimate . At an average on-off ΔT of 20°C, the 21mm CBGA and the 21 x 25mm CBGA have an estimated fatigue life of over 25 years and over 20 years; respectively.

NOMENCLATURE

Main Variables

AF	=	acceleration factor
T_{max}	=	highest T_{on} temperature (K)
ΔT	=	T_{on} - T_{off}
f	=	thermal cycling frequency; # of cycles must be at least 6 per day

### Subscripts

l	=	lab conditions
f	=	field conditions

INTRODUCTION

PowerPC 603 and PowerPC 604 Microprocessors and MPC 105 Bridge/Memory Controller

The scaleable PowerPC™ microprocessor family, jointly developed by Apple, IBM, and Motorola, is being designed into high-performance cost-effective computers (including notebooks, desktops, workstations, and servers). The PowerPC 603 microprocessor is a low-power implementation of the PowerPC Reduced Instruction Set Computer architecture. The PowerPC 604 microprocessor is a 32-bit implementation of the PowerPC architecture, and is software and bus compatible with the PowerPC 601™ and PowerPC 603 microprocessors. Both devices may be offered in a 21mm controlled-collapsed-chip-connection/ceramic-ball-grid array (C4/CBGA) (Figure 1).

The MPC105 PCI Bridge/Memory Controller provides a PowerPC Reference Platform (PReP) compliant bridge between PowerPC 603 or PowerPC 604 RISC micro-processors and the Peripheral Component Interconnect (PCI) bus. The MPC105 integrates secondary control and a high-performance memory controller that supports DRAM, SDRAM, ROM, and Flash ROM. The MPC105 uses an advanced, 3.3 volt CMOS process technology and is packaged in a 21 by 25 mm (16 x 19 ball matrix) C4/CBGA.
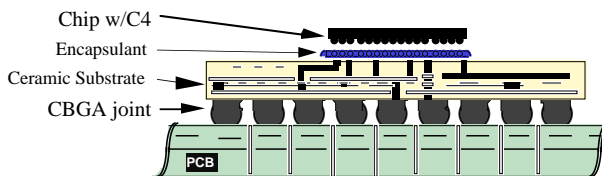
Figure 1.   C4 Ceramic-Ball-Grid Array: Cross-sectional View (not to scale)

Objective

To predict solder joint reliability of surface-mount interconnect technologies, such as the CBGA, a key parameter is the: temperature rise above ambient of the solder joint. This data is often not available in the open literature and/or the system "worst-case" temperatures are often used. Therefore, field-temperature measurements at or near the central-processing unit (CPU) were taken for a variety of computer platforms under typical office use. In addition, as printed-circuit boards (PCBs) are not uniform, the objective was to identify, the **maximum** board temperature.

The results of the maximum field-temperature measurements, were used to predict package-to-board reliability solder-fatigue lifetime for initial C4/CGBA offerings of the PowerPC microprocessor product family; the PowerPC 603 and PowerPC 604 microprocessors and the MPC105. The solder fatigue lifetime will be presented for failure rates of 100ppm and 1000ppm (per package) for field conditions of 365 days usage per year with up to 6 on/off cycles per day.

C4-Ceramic-Ball-Grid Array Module

Computer system performance has dramatically improved over the past three decades. Much of this improvement is a result of increased integration of components at the semiconductor level, made possible by reduced feature sizes. These reduced feature sizes have resulted in several semiconductor integrated-circuit (IC) trends, all of which are increasing: gate count, chip inputs/outputs, chip size, operating frequency, and power consumption. In summary, these trends have placed an increased emphasis on microelectronics packaging design.

To satisfy customer requirements for surface mountable packages with reduced size, the C4/CBGA format was chosen. The C4 technology has a long history of producing reliable product at International Business Machines Corporation. Work has been performed at Motorola that supports the International Business Machines Corporation data; therefore, the C4 joint reliability is not discussed in this report. Motorola has supplied customers with ceramic ball-grid-array packages for many years, primarily in the Land Mobile Products Sector (LMPS). In contrast to the PowerPC microprocessor family packages, these packages are small in size and lead count (100 I/O and below). The packages chosen for the PowerPC microprocessor family are larger in size and lead count (21mm, 255 I/O's, minimum).

This paper presents the solder fatigue life projections for the first three CBGA PowerPC microprocessor products that will be introduced by Motorola; that is, the PowerPC 603 and PowerPC 604 microprocessors in 21mm CBGA and the MPC105 in a 21mmx25mm CBGA. This interconnect technology has been previously described by Kromann, et al. (1994), Kromann (1994), Gerke (1994) and Motorola C4 Packaging Manuals (1993 & 1994).
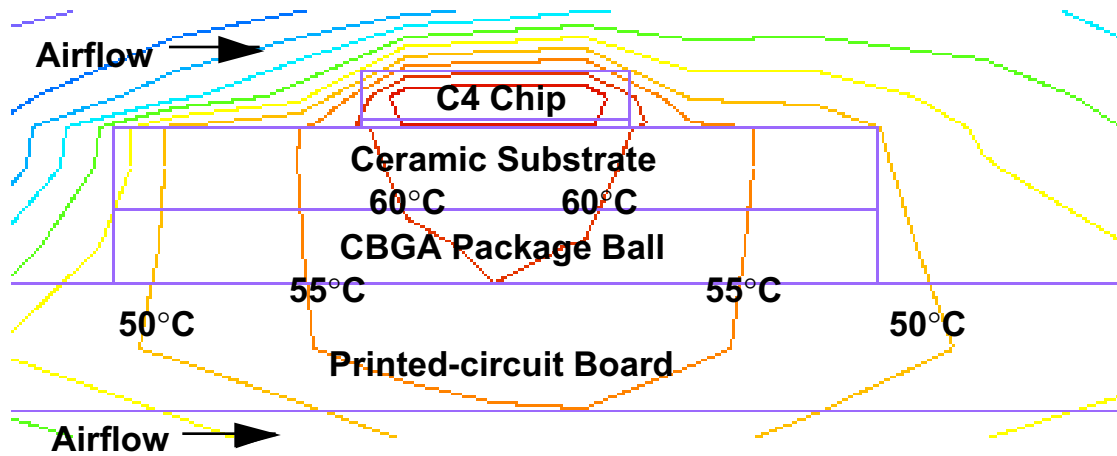
Printed-circuit Board Temperatures of Computer Systems

In-situ field-temperature measurements at or near the central-processing unit (CPU) were taken for a variety of operating computer platforms under typical office use. We wished to identify maximum printed-circuit board (PCB) temperatures for the following computer systems:

- Notebooks/Laptops
- Personal Computers
- Workstations
- Servers

Temperature Measurement Procedure. Temperature probing an operating computer system is an arduous task. One must use caution to avoid: electro-static discharge, electrical shorting, and contact with component/system air-mover blades. To avoid electrical shorting, probing the solder joint was not possible; therefore, PCB regions at or near the CPU were measured. The typical measurement procedure was as follows:

- The computer cabinets were opened and maximum temperatures were identified, while the machine was operating.

- The computer cabinets were replaced and the machines dynamically stressed.

- The CPUs were active and the usual monitoring took more than three hours.

- Temperatures were measured with a very fine-gauge thermocouple taped and thermally grounded by at least 3 cm along the point of interest.

- Multiple readings were recorded and only the maximum temperature is reported.

- For dual-processor systems, data for the highest temperature CPU is reported.

- In some cases the maximum board temperature was not at the CPU. This data is also presented.

- Data is estimated to be within 5% error.

Figure 2. CBGA and Printed-circuit Board Contour Temperatures for Typical Computer Systems.

RESULTS
Printed-Circuit Temperatures

For the results presented in this paper, modeling and experimental measurements have shown differences between the solder joint and the PCB temperature. Figure 2. shows a temperature contour of a CBGA package under computer-system operational conditions (e.g. air velocity is 1 m/s) showing the temperature difference is less than 5°C, between the measured field data of the PCB and the maximum solder-joint temperature. Again, the key objective was to identify maximum printed-circuit boards (PCBs) temperatures while the computer systems were in typical use. Printed-circuit boards (PCB) were not uniform; therefore, only maximum temperature regions of the board were measured.

For uniprocessor computer systems, the maximum board temperatures, were at or near the central-processing unit (CPU). The data reported here is considered to be the maximum board temperatures, one might expect in typical office use, under stressed operational system loading conditions. The maximum board temperature rise measured was 28°C (Figure 3), and the mean for this limited data set was 17°C (Figure 4). A frequency histogram of this data is shown in Figure 4. These findings concur with IPC-SM-785.

In most cases, the maximum temperature was at the CPU. However, in several computer systems, the board in the CPU region was actually at a lower temperature, than ancillary components. In addition the following results are noted:

- Printed-circuit boards of operational computer systems showed large temperaure variations.

That is, it is not too difficult to find regions that were only slightly above ambient temperatures.

- For the data reported here, there was a wide range in CPU power dissipations (1 to 30 watts); however, this had little effect on the board temperatures. That is, the high-power CPUs typically used enhanced thermal management schemes (larger heat sinks and/or active heat sinks, e.g. fan sinks) to remove heat off the component "case". Thus, the board temperature at or near the CPUs did not exhibit a significantly larger temperature rise, than other systems.

- Two systems used active muffin fans, attached to a pin-fin heat sink.

- For one tower workstation, the secondary cache memory was operating at a higher temperature than the CPU.

- All CPU had active or passive heatsinks.

- For one desktop workstation system, the region of the CPU and the region of the graphics card (PGA without heat sink), experienced temperature rises of 11°C and 23°C; respectively. Note, the board on the graphics controller card, was 12°C higher than the CPU region.

- For one network server, the memory-management unit (assumed) adjacent to the CPU (with a fan-heatsink) was running 2°C higher. Therefore, both data points are plotted.
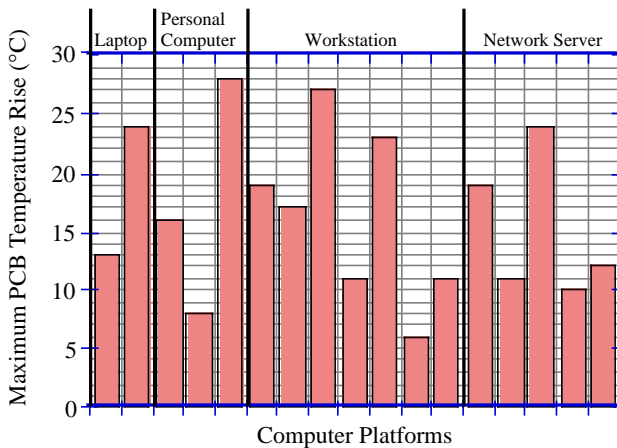
Figure 3. Printed-circuit Board Temperature Rise Above Ambient for Various Computer Systems

Figure 4. Distribution of Temperature Rise Data.

- Excluding, the laptop computer, all other computer systems had forced-convection cooling systems, which resulted in linear air velocities of 0.5 to 2 m/s.

Reliability Test Vehicle.

Substrates (21mm and 25mm) used to study CBGA solder joint reliability were designed to mate to a PCB so that each interconnection element between the substrate and PCB could be monitored electrically. Each connection to the PCB was monitored continuously during thermal cycle testing. The daisy-chain pattern on the substrate has connections made without using a C4 chip; therefore, a co-fired conductor layer is used to provide the interconnections. This technique is preferred for independent testing of the CBGA joints over others because it isolates the board interconnections (and not the other connections internal to the package). PCBs were coated with both hot air solder leveling (HASL) and organic (benzotriazole) coating process. The PCBs used were 4-layer epoxy-glass, 1.57 mm (62 mils) thick and characterized to have a glass-transition temperature (Tg) of 118°C minimum and a thermal-expansion coefficient of 21 ppm/°C in the array site (18 ppm/°C in the base material) Gerke (1994). Figure 5 illustrates the localized TCE effect that the metallization (i.e. plated through holes) in the PCB can have relative to making calculations for solder fatigue.

Accelerated air-to-air temperature cycle testing for CBGA joints were cycled over a range of 20°C to 80°C (at 3 cycles per hour) on a sample of 40 packages for the 25mm packages and 0°C to 100°C (at 1.5 cycles per hour) for the 21mm packages. Details for both tests have been documented Banks et al. (1994) and Gerke (1994). For illustrative purposes, the fatigue-life results of the 20°C to 80°C testing is presented in Figure 6. The CBGA wear-out
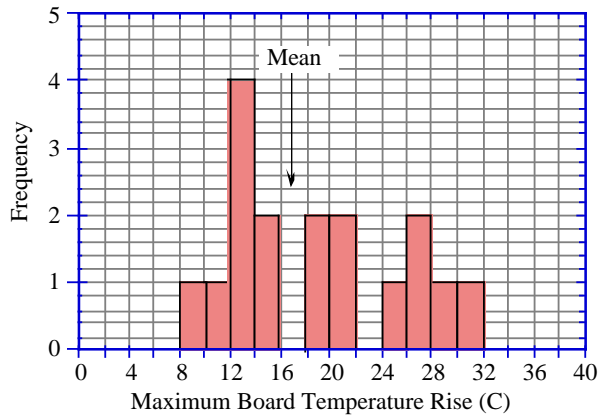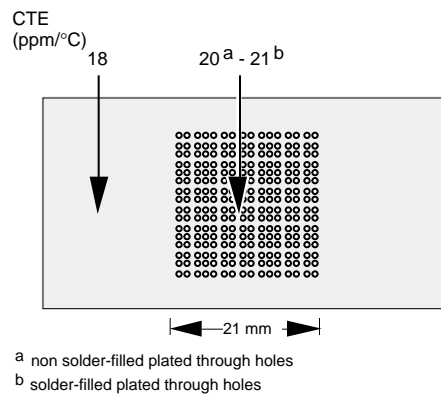
80°C testing is presented in Figure 6. The CBGA wear-out mechanism follows a log-normal distribution. Final separation is characterized as a primary crack propagating through the eutectic solder at the PWB side of the high-lead ball as verified by cross-sectioning.

Module-To-Board Reliability

In consideration of the system-level thermal design options presented, the ΔT's presented in this section are considered to be typical and upper bounds that may be expected during product use, 25 - 45°C and 25 - 55°C; respectively. Thermal excursions occur through on-off cycles. The greatest reliability concern in the C4/CBGA packaging technology is solder fatigue in the CBGA joints during these thermal excursions. Small ΔT's associated with the interconnect joint equate to longer life when compared to large ΔT's. Therefore, thermal management design can influence the solder joint temperature rise (ΔT's).

CTE (ppm/°C)

18   20 [a] - 21 [b]

|←— 21 mm —→|

[a] non solder-filled plated through holes
[b] solder-filled plated through holes

Figure 5. In-plane TCE distributions of a 4 layer printed wiring board determined by thermal mechanical analysis (TMA) (Gerke 1994).
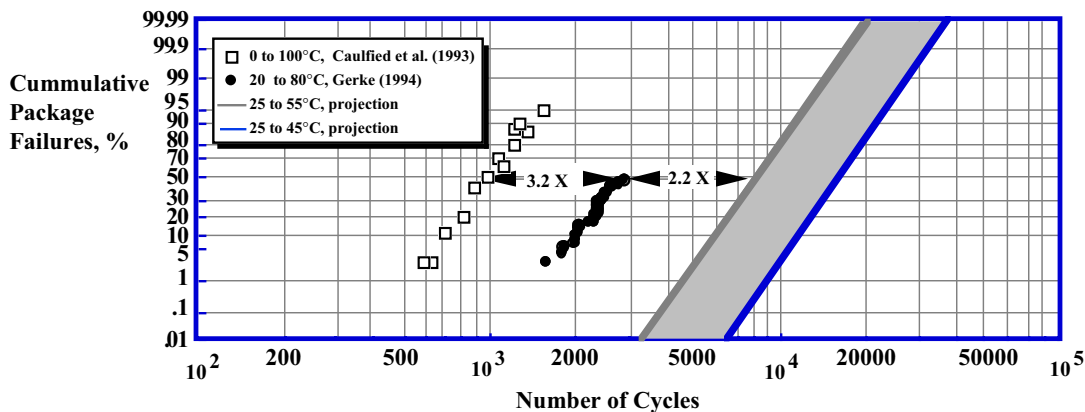
Figure 6. CBGA fatigue life distribution (log-normal) for a 25mm substrate air-to-air temperature cycled from 20°C-80°C and compared to predictions made for two temperature cycle conditions using Equation 1.

The purpose of accelerated-temperature-cycle testing is to compare the mechanical and the electrical robustness of the assembly when subjected to a thermal cyclical environment. Correlation to the accelerated temperature cycle testing and actual field use can be made by use of daisy-chain test vehicles and the application of a modified Coffin-Manson relationship. Acceleration factors can be calculated to predict field-life cycles from the accelerated-stress test.

The version of the Coffin-Manson equation typically used for CBGA's has been detailed previously by Caulfield, et al. (1993). For solder interconnections of a fixed geometry, the strain term can be reduced to a delta temperature term, ΔT, which comprises each thermal cycle as illustrated in Equation 1.

$$AF = [\Delta T_l / \Delta T_f]^{1.9} (f_f / f_l)^{1/3} \exp[1414(1/T_{max_f} - 1/T_{max_l})] \quad (1)$$

The acceleration factor (AF) is simply a multiplier applied to a known set of data to predict the failure rate of the condition. In the case of 25°C-55°C and 20°C-80°C, the AF (or multiplier) is 2.2X (assumptions for this calculation will be presented in a later sub-section). In other words, the fatigue life of the smaller ΔT is 2.2X times longer than the 20°C-80°C case. Typically, the 50% fail value is applied to the AF factor to translate between failure distributions (Figure 6).
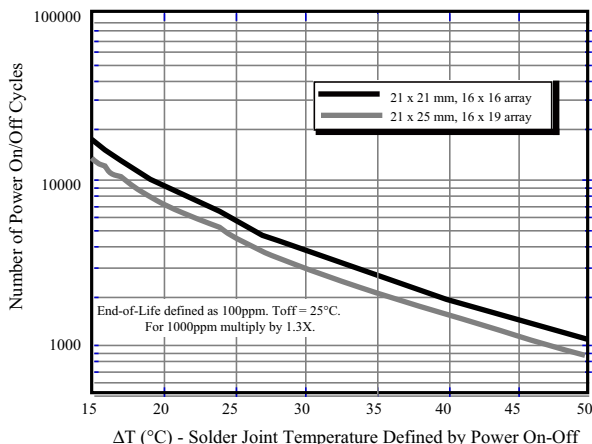
CBGA Solder Fatigue Life Projections. Predictions for typical computer applications were projected by using accelerated test data and the method described as follows: a) failure distributions, such as those from Figure 6 were extrapolated down to the 0.01% (100ppm) and 0.1% (1000ppm) levels, b) the number of cycles to failure at those levels were noted, c) the number of cycles was then multiplied by an acceleration factor (Equation 1) for the temperature range of interest.

The fatigue life estimates described above are generally thought to be very conservative for the solder joints studied. The assumptions are: 1) on the average, the system would be turned on and off up to 6 times per day [Coffin-Manson 24 hour period] and 2) the system would be cycled over the full thermal excursion each and every time the system was turned on.

The maximum solder fatigue damage frequency that can be applied for most desktop office environment operating temperatures is 1 on-off cycle every 4 hours (i.e., 6 per 24 hours). This is due to the solder requiring time to stress relax at both temperature extremes (full on and full off) generated in the office environment. During the course of an average work day, which is generally considered to be 8 to 10 hours long it is probable then to accumulate maximum fatigue damage by having 2 evenly spaced on-off cycles. Cycles occurring more frequently do not accumulate as much damage per cycle as the above described situation. More frequent cycling, while higher in total number of cycles, do not necessarily accumulate more solder fatigue damage than a low number of long cycles. Therefore, laptop machines and mini-power cycles are not generally considered to be as harmful to the solder joints when being compared to a low number of slow on-off cycles.

The above method was utilized to make predictions for the PowerPC microprocessor product CBGA packages 21mm and 25mm (used to estimate the 21x25mm CBGA solder fatigue life) for the PowerPC 603 and PowerPC 604 microprocessors and the MPC105; respectively. These predictions are shown in Figure 7. The assumptions used for Figure 7 were calculated to be consistent with IPC-SM-785. Failure rates of 100ppm are plotted and failure rates of 1000ppm can be easily be calculated by multiplying the 100ppm number of cycles by 1.3.

Freescale Semiconductor, Inc.

Figure 7. CBGA Solder Fatigue Field Life Projections. Each cycle is assumed to represent the full temperature excursion.

Figure 7 shows the solder joint fatigue life for the 21mm ceramic ball-grid-array (CBGA), the package for the PowerPC 603 and PowerPC 604 microprocessors to be over 9200 cycles and the 21x25mm CBGA, the package for the MPC 105, to be over 7300 cycles for an average full on/off cycle ΔT of 20°C. For a desktop computer application turned on and off on the average of one time per day, the equivalent fatigue life would be over 25 years for the 21mm and over 20 years for the 21 x 25mm CBGA; respectively. A 'worst' case desktop situation, as described above would, with 2 on-off cycles per work day would yield over 10 years of life for both packages.

SUMMARY

To predict solder joint reliability of surface-mount technology, a key parameter is: the temperature rise above ambient at the solder joint, ΔT. However, little data exists in the open literature for printed-circuits boards or components leads. Therefore, in-situ field temperature measurements were taken for a range of computer platforms at the central-processing units.

Printed-circuit boards (PCB) were not uniform; therefore, only maximum temperature regions of the board were measured. These maximum temperatures revealed the mean to be less than 20°C above ambient (i.e., $\Delta T < 20$°C) regardless of the power of the device. The largest ΔT measured in any system was less than 30°C above ambient. High power microprocessors generally had more efficient heat sinking than lower power microprocessors resulting in consistent temperature rises at the PCB. These temperature measurements of actual computer systems are in close agreement with IPC-SM-785.

By utilizing the measured PCB temperature rise, solder joint fatigue life was calculated for the 21mm ceramic ball-grid-array (CBGA), the package for the PowerPC 603 and PowerPC 604 microprocessors and the 21mm x 25mm CBGA, the package for the MPC105 package. It was estimated that the solder fatigue life of a 21mm CBGA at an average on-off ΔT of 20°C to be over 25 years and for the 21 x 25mm CBGA to be over 20 years. Small ΔT's associated with the interconnect joint equate to longer life when compared to large ΔT's. Therefore, thermal management design can influence the solder joint temperature rise (ΔT's). Due to efficient designs, high power devices were found to have relatively cool board temperatures.

ACKNOWLEDGMENTS

REFERENCES

Banks, D. R., Burnette, T. E., Gerke, R. D., Mammo, E. and Mattay, S., 1994 "Reliability Comparison of Two Metallurgies for Ceramic Ball Grid Array," *Proceedings of the International Conference on Multichip Modules*, Denver, CO, April 13 - 15, 1994, pp. 529 - 534.

Caulfield, T., Benenati, J. A. and Acocella, J. 1993, "Surface Mount Array Interconnections for High I/O MCM-C to Card Assemblies," *Proceedings of the International Conference on Multichip Modules*, Denver, CO, April 1993, pp. 320-25.

DeHaven, K. and Dietz, J., 1994, "Controlled Collapse Chip Connection (C4) - An Enabling Technology", *Proceedings of the 44th Electronic Components & Technology Conference*, Washington, D.C., May 1 -4, 1994, pp. 1 - 6.

Gerke, R. D., 1994, "Ceramic Solder-Grid-Array Interconnection Reliability Over a Wide Temperature Range," *Proceedings of NEPCON/West '94,* Anaheim, CA, February 27 - March 4, 1994, pp 1087 - 1094.

Kromann, G.B., 1994, "Thermal Modeling and Experimental Characterization of the C4/Surface-Mount-Array Interconnect Technologies", *Proceedings of the 44th Electronic Components & Technology Conference,* Washington, D.C., May 1 -4, 1994, pp. 395 - 402.

Kromann, G. Gerke, D. and Huang, W. 1994, "A Hi-Density C4/CBGA Interconnect Technology for a CMOS Microprocessor," *Proceedings of the 44th Electronic Components & Technology Conference,* Washington, D.C., May 1 -4, 1994, pp. 22 - 27.

IPC- SM-785, "Guidelines for Accelerated Reliability Testing of Surface Mount Technology," *Institute for Interconnection and Packaging Electronic Circuits,* Lincolnwood, IL.

Motorola Customer Version of "C4 Product Design Manual-Volume I: Chip and Wafer Design," Motorola C4 Product Design Center, Austin, TX, 1993.

Motorola Customer Version of "C4 Product Design Manual-Volume 2: Packaging Design" Motorola C4 Product Design Center, Austin, TX, 1994.

Norris, K. C. and Landzberg, 1969, A. H. "Reliability of Controlled Collapse Interconnections," *IBM Journal of Research and Development*, May, 1969, pp. 266-71.