Quad Transceivers

MC92602

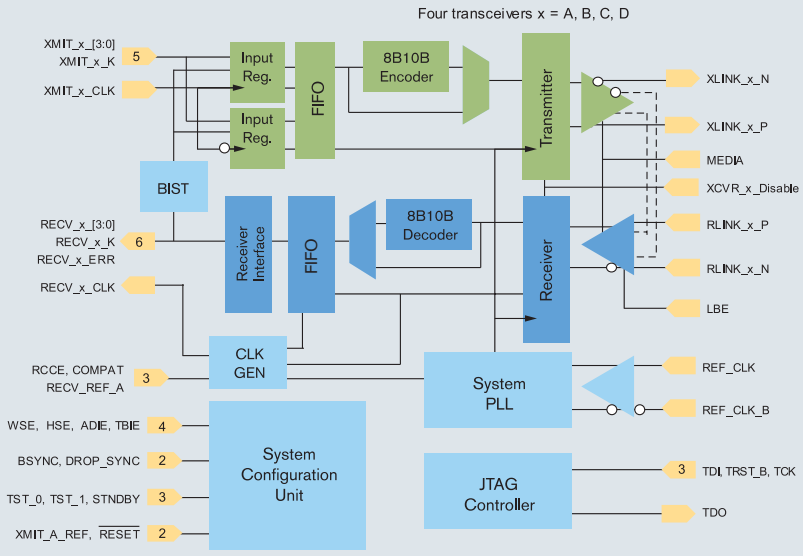
Overview

Freescale Semiconductor's MC92602 quad transceiver is a high-speed, full-duplex, serializer/deserializer (SerDes) data interface. With four transceivers, the MC92602 transceiver transmits and receives coded data at a rate of 1.0 gigabit per second (Gbps) through each 1.25 gigabaud link. Building on the successful transceiver technology of Freescale's MC92600 quad transceiver, the MC92602 transceiver is designed with reduced width interfacing and is ideal for high-density board applications requiring a low number of interface signals.

Signal input/output (I/O) count is reduced relative to the MC92600 transceiver by operating the parallel interfaces at 125 MHz double data rate (DDR2) 4-bits wide per channel, per direction. The I/O interface is high-speed transceiver logic (HSTL) Class I, source terminated, which is an accepted signaling method for 125 MHz DDR2 data for FR-4 board traces up to eight inches. This aggressive signaling scheme offers excellent board density without making unreasonable signal integrity demands on the interfacing device's system logic.

Like its predecessors, the MC92602 is specifically designed for low power consumption—even with all links operating at full speed, its high-performance design is engineered to consume less than 1.2W. To provide excellent board density in applications with a large number of channels, the MC92602 transceiver is offered in a JEDEC Solid State Technology Association standard, 196-pin, 15 mm body size package.

MC92602 QUAD SERDES BLOCK DIAGRAM



Typical Applications

> High-density board applications for chip-to-chip intrasystem communications using Ethernet protocol

> Blade applications with a high number of 1-gigabit Ethernet (GbE) ports

> High-speed data transfer applications in high-bandwidth backplane and chassis-to-chassis networking

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Product Highlights

> Four full-duplex differential data links

> Selectable speed range: 1.25 Gbaud or 0.625 Gbaud

> Rate adaptation for Ethernet packet streams

- Context-sensitive rate adaptation during receipt of idle and data code groups
- Supports jumbo frame lengths of up to 16 KB
- Supports frame bursting

> Low power: 1200 mW, under typical conditions, while operating all transceivers at full speed

> Unused transceiver channels may be individually disabled to reduce power consumption

> JTAG support and full-speed built-in self-test (BIST) functions

Data Interface

> Internal Fibre Channel 8B/10B encoder/decoder that may be bypassed when in 10-bit interface mode

> DDR2, source synchronous, 4-bit/5-bit data interfaces

> Transmit data clock is selectable between per-channel transmit clock or channel “A” transmit clock

> Link-to-link synchronization supports aligned, multichannel, word transfers

> Synchronization mechanism tolerates to 40-bit times of link-to-link media delay

> Selectable idle character alignment mode enables transfers with automatic realignment or unaligned data transfers (when in 10-bit mode)

> Received data may be clocked at the recovered clock or the reference clock frequencies

Link Interface

> Links drive 50-ohm or 75-ohm media (100-ohm or 150-ohm differential), backplane or cable

> Link inputs have on-chip receiver link termination and are hot-swap compatible

Parametrics

> Power supply

- Core power supply: 1.8V ± 0.15 Vdc
- HSTL I/O power supply: 1.5V ± 0.1 Vdc or 1.8V ± 0.15 Vdc
- Link I/O power supply: 1.8V ± 0.15 Vdc

> Power dissipation

- Typical operation: <300 mW per channel at maximum speed

Package

> 196-pin MAPBGA (15 mm x 15 mm body size, 1.0 mm ball pitch)

Technical Specifications

> All channels have:

- 8B/10B encoder/decoder that can be enabled or bypassed
- Clock generation/recovery
- Independent, HSTL, 4-bit/5-bit, DDR2 interface with parallel-to-serial, serial-to-parallel conversion
- Idle/control character generation/detection

> Transceiver links operate over 50-ohm or 75-ohm media (100-ohm or 150-ohm differential) for lengths of up to 1.5 meters of FR-4 board/backplane, or 10 meters of coaxial cable

> No external loop filter or termination components required

> System BIST test modes with error counters

> Loop-back BIST isolated from link inputs and outputs

> IEEE® 1149.1 standard JTAG boundary scan support

> Differential reference clock input with single-ended reference clock input option (125 MHz maximum)

> Frequency offset tolerance between transmitter and receiver in excess of ± 250 part per million (ppm)

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

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