Signal Controllers

56F8157

Target Applications

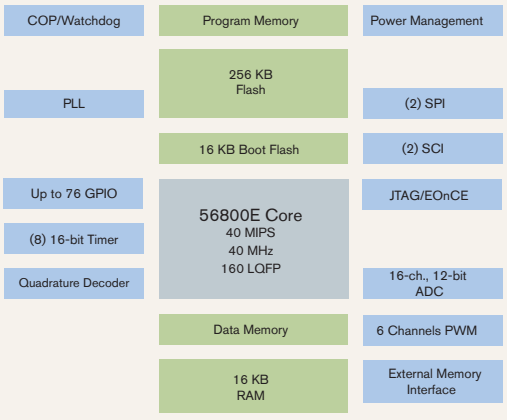
- > Polyphase metering
- > UPS
- > Electric vehicles
- > Currency validation
- > Industrial control/ connectivity
- > Home appliances
- > Smart relays
- > Fire and security systems
- > Medical monitoring

Overview

Having met the memory needs of your application, do you long for more general-purpose input/output (GPIO) pins? Wishing for a handful of additional GPIO without having to pay for additional memory you don't need? Your wishes have been granted. The 56F8157 offers identical memory and peripheral capabilities as the 56F8156, but the 56F8157 has 14 additional GPIO pins.

If the challenge you face is not one of functionality but one of memory, the 56F8157 has you covered. The 56F8157 comes in the same packages and package pin-outs as the 56F8147. You keep the same functionality while doubling your program memory. How's that for a migration strategy?

The 56F8157 is further proof that the 56F8100 Family is the right choice to overcome all of your design challenges.



56800E Core Features	Benefits
> Up to 40 MIPS at a guaranteed 40 MHz core frequency	> Hybrid architecture facilitates implementation of both control and signal processing functions in a single device
> JTAG/enhanced on-chip emulation (EOnCE™) for unobtrusive, real-time debugging	> High-performance, secured Flash memory eliminates the need for external storage devices
> Four 36-bit accumulators	> Extended temperature range up to +105°C allows for operation of nonvolatile memory in harsh environments
> 16- and 32-bit bidirectional barrel shifter	> Flash memory emulation of EEPROM eliminates the need for external nonvolatile memory
> Parallel instruction set with unique addressing modes	> 32-bit performance with 16-bit code density
> Hardware DO and REP loops available	> On-chip voltage regulator and power management reduce overall system cost
> Three internal address buses	> Off-chip memory expansion capabilities allow for glueless interfacing with the additional memory of external devices without sacrificing performance
> Four internal data buses	> This device boots directly from Flash, providing additional application flexibility
> Architectural support for 8-, 16- and 32-bit single-cycle data fetches	> High-performance pulse-width modulation (PWM) with programmable fault capability simplifies design and promotes compliance with safety regulations
> MCU-style software stack support	> PWM and analog-to-digital converter (ADC) modules are tightly coupled to reduce processing overhead
> Controller-style addressing modes and instructions	> Low-voltage interrupts (LVIs) protect the system from brownout or power failure
> Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)	> GPIO pins support application-specific needs
> Proven to deliver more control functionality with a smaller memory footprint than competing architectures	> Simple in-application Flash memory programming via EOnCE or serial communication

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Memory Features

> Architecture permits as many as three simultaneous accesses to program and data memory

> On-chip memory includes high-speed volatile and nonvolatile components

- 256 KB of Program Flash
- 16 KB of Data Flash
- 16 KB of Boot Flash

> All memories operate at 40 MHz (zero wait states) over temperature range (-40°C to +105°C), with no software tricks or hardware accelerators required

> Flash security feature prevents unauthorized accesses to its content

> Off-chip memory expansion capabilities provide a simple method for interfacing additional external memory and/or peripheral devices

- Access up to 4 MB of external program memory or 32 MB of external data memory

> External accesses supported at up to 40 MHz (zero wait states)

56F8157 Peripheral Circuit Features

> PWM module with six outputs and four programmable fault inputs

> Two serial peripheral interfaces (SPIs)

> Two serial communications interfaces (SCIs)

> Eight 16-bit timers with input and output compare capability

> Four-input quadrature decoder

> On-chip 3.3V to 2.6V voltage regulator

> Software-programmable Phase-Lock Loop (PLL)

> 12-bit ADCs with 16 inputs, self-calibration and current injection capability

> Up to 76 GPIO pins

> External reset input pin for hardware reset

> Computer operating properly (COP)

> Integrated power-on reset and LVI module

> I^2C communications master mode (emulated)

Award-Winning Development Environment

> Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.

> The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, CodeWarrior tools and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

Product Documentation

56F8300 Peripherals Manual	Detailed peripheral description of the 56F8300 family of devices ***Order Number:*** MC56F8300UM
56F8357/ 56F8157 Technical Data Sheet	Electrical and timing specifications, device-specific peripheral information and package and pin descriptions ***Order Number:*** MC56F8357
56F8157 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces ***Order Number:*** MC56F8157PB
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit core processor and the instruction set ***Order Number:*** DSP56800ERM

Ordering Information

Part	MC56F8157
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	160
Temperature Range	-40°C to +105°C
Order Number	MC56F8157VPY

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

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