56F8146

Target Applications

> Polyphase metering
> UPS
> Electric vehicles
> Currency validation
> Industrial control/networking
> Home appliances
> Smart relays
> Fire and security systems
> Medical monitoring

Overview

If you find yourself needing a little more memory or simply need to interface to other devices in your system in a parallel fashion, then the 56F8146 is the device for you. Moving to this 144-pin LQFP package allows you to take advantage of its included external memory interface for these additional tasks.

You will still enjoy 136 KB of on-chip Flash memory, pulse-width modulation (PWM) outputs, analog-to-digital converter (ADC) inputs and timer channels, along with the capability of interfacing with other devices in your system.

Whether you are adding performance to your control application, or control capabilities to your signal processing system, you can benefit from the flexibility and compatibility provided by the 56F8145 and 56F8146.

COP/Watchdog	Program Memory	Power Management
PLL	128 KB Flash	(2) SPI
	8 KB Boot Flash	(2) SCI
Up to 62 GPIO	56800E Core 40 MIPS 40 MHz 144 LQFP	JTAG/EOnCE
(8) 16-bit Timer		
Quadrature Decoder		16-ch., 12-bit ADC
	Data Memory	6 Channels PWM
(2) FlexCAN	8 KB RAM	External Memory Interface

56800E Core Features

> Up to 40 MIPS at a guaranteed 40 MHz core frequency

> DSP and microcontroller (MCU) functionality in a unified, C-efficient architecture

> JTAG/enhanced on-chip emulation (EOnCE™) for unobtrusive, real-time debugging

> Four 36-bit accumulators

> 16- and 32-bit bidirectional barrel shifter

> Parallel instruction set with unique addressing modes

> Hardware DO and REP loops available

> Three internal address buses

> Four internal data buses

> Architectural support for 8-, 16- and 32-bit single-cycle data fetches

> MCU-style software stack support

> Controller-style addressing modes and instructions

> Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)

> Proven to deliver more control functionality with a smaller memory footprint than competing architectures

Benefits

> Hybrid architecture facilitates implementation of both control and signal processing functions in a single device

> High-performance, secured Flash memory eliminates the need for external storage devices

> Extended temperature range up to +105ºC allows for operation of nonvolatile memory in industrial applications

> Flash memory emulation of EEPROM eliminates the need for external nonvolatile memory

> 32-bit performance with 16-bit code density

> On-chip voltage regulator and power management reduce overall system cost

> Off-chip memory expansion capabilities allow for glueless interfacing with the additional memory of external devices without sacrificing performance

> This device boots directly from Flash, providing additional application flexibility

> High-performance PWM with programmable fault capability simplifies design and promotes compliance with safety regulations

> PWM and ADC modules are tightly coupled to reduce processing overhead

> Low-voltage interrupts (LVIs) protect the system from brownout or power failure

> Simple in-application Flash memory programming via EOnCE or serial communication

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Memory Features

> Architecture permits as many as three simultaneous accesses to program and data memory

> On-chip memory includes high-speed volatile and nonvolatile components

  ▪ 128 KB of Program Flash

  ▪ 8 KB of Data RAM

  ▪ 8 KB of Boot Flash

> All memories operate at 40 MHz (zero wait states) over temperature range (-40°C to +105°C), with no software tricks or hardware accelerators required

> Flash security feature prevents unauthorized accesses to its content

> Off-chip memory expansion capabilities provide a simple method for interfacing additional external memory and/or peripheral devices

  ▪ Access up to 1 MB of external program memory or 1 MB of external data memory

  ▪ External accesses supported at up to 40 MHz (zero wait states)

56F8146 Peripheral Circuit Features

> PWM module with six outputs and four programmable fault inputs

> Two serial peripheral interfaces (SPIs)

> Two serial communications interfaces (SCIs)

> Eight 16-bit timers with input and output compare capability

> On-chip 3.3V to 2.6V voltage regulator

> Software-programmable Phase-Lock Loop (PLL)

> 12-bit ADCs with 16 inputs, self-calibration and current injection capability

> Up to 49 general-purpose input/output (GPIO) pins

> External reset input pin for hardware reset

> Computer operating properly (COP)

> Integrated power-on reset and LVI module

> I²C communications master mode (emulated)

Product Documentation

56F8300 Peripherals Manual	Detailed peripheral description of the 56F8300 family of devices **Order Number:** MC56F8300UM
56F8346/ 56F8146 Technical Data Sheet	Electrical and timing specifications, device-specific peripheral information and package and pin descriptions **Order Number:** MC56F8346
56F8146 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces **Order Number:** MC56F8146PB
DSP56800E Reference Manual	Detailed description of the DSP56800E architecture, 16-bit core processor and the instruction set **Order Number:** DSP56800ERM

Ordering Information

Part	MC56F8146
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	144
Temperature Range	-40°C to +105°C
Order Number	MC56F8146VPY

Award-Winning Development Environment

> Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.

> The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A complete set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, CodeWarrior tools and EVMs create a complete, scalable tools solution for easy, fast and efficient development.

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