# Late Write Architecture

## Fast SRAMs for High-End RISC and Telecommunications Markets

Late Write FSRAMs are primarily designed to provide RISC CPUs with high performance L2 cache. By offering a variety of speed grades and I/Os; Motorola Late Write SRAMs can be used as L2 cache by MIPS, PA-RISC, Alpha, UltraSPARC, and Power RISC CPUs. Late Writes also provide a high bandwidth cache solution for embedded processors and ASICs in switching applications.

The major advantage of the Late Write architecture is that write data is supplied to the memory one clock cycle after address. Back-to-back read-to-write access is possible with the register/latch devices.

These parts are JEDEC standard pinout and are pin-for-pin compatible with our competitors Late Write devices.

### Product Description

The 4-megabit and 8-megabit Late Write FSRAMs are high speed synchronous SRAMs designed to provide high performance in secondary cache and ATM switch, Telecom, and other high speed memory applications. The current 4-megabit devices are organized as 256K words by 18 bits and 128K words by 36 bits and are fabricated in Motorola's state-of-the-art MOS-11 facility. The 8-megabit devices, and a new 4-megabit device, are fabricated in Motorola's MOS-13 facility using a high performance CMOS process, with copper interconnect. The 8-megabit devices are organized as 512K words by 18 bits and 256K words by 36 bits.

For single clock devices, the differential CK clock inputs control the timing of read/write operations of the RAM. At the rising edge of the CK clock all addresses, write enables, and synchronous selects are registered. An internal buffer and special logic enable the memory to accept write data on the rising edge of the CK clock, a cycle after address and control signals. For register/register devices, read data is available after the next rising CK clock edge. For register/latch devices, read data is available at the falling edge of the CK clock. The synchronous write and byte enables, allow writing to individual bytes or the entire word.

### Features

- Byte Write Control
- 1.8 V, 2.5 V, 3.3 V Operation
- Boundary Scan (JTAG) IEEE 1149.1 Compatible
- Differential Clock Inputs
- Optional x18 or x36 Organization
- 119-Bump, 50 mil (1.27 mm) Pitch, 14 mm x 22 mm Plastic Ball Grid Array (PBGA) and Flip Chip PBGA Packages Available

### HSTL, Register/Register (Pipelined) Single Clock Features

- Extended HSTL — I/O (JEDEC Standard JESD8-6 Class I Compatible)
- HSTL — User Selectable Input Trip-Point
- Programmable Impedance Output Drivers
- Register/Register Synchronous Operation
- 3/3.3/3.7/4/4.4/5/6/7/8 ns Cycle (4-megabit)
- 3.0/3.3/3.7/4.0/4.4/5.0 ns Cycle (8-megabit)

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### LVTTL, Register/Register (Pipelined) Single Clock Features

- LVTTL 3.3 V I/O ($V_{DDQ}$)
- Register/Register Synchronous Operation
- 5/6/7/8 ns Cycle (4-megabit)

### 2.5 V I/O, Register/Register (Pipelined) Single Clock Features

- 2.5 V I/O ($V_{DDQ}$)
- Register/Register Synchronous Operation
- 4/5/6/7/8 ns Cycle (4-megabit)

### HSTL, Register/Latch Single Clock Features

- HSTL — I/O (JEDEC Standard JESD8-6 Class I Compatible)
- HSTL — User Selectable Input Trip-Point
- HSTL — Compatible Programmable Impedance Output Drivers
- Register/Latch Synchronous Operation
- 5.5/6.5/7.5/8.5/9/9.5 ns Latency (4-megabit)
- 4.0/4.2/4.4 ns Latency (8-megabit)

### LVTTL, Register/Latch Single Clock Features

- LVTTL 3.3 V I/O ($V_{DDQ}$)
- Register/Latch Synchronous Operation
- 8.5/9/9.5 ns Latency (4-megabit)

### 2.5 V I/O, Register/Latch Single Clock Features

- 2.5 V I/O ($V_{DDQ}$)
- Register/Latch Synchronous Operation
- 5.5/6.5/7.5/8.5/9/9.5 ns Latency (4-megabit)

### Contact Information

- Motorola offers data sheets, application notes and models for Fast Static RAM products. In addition, more information is provided for these products at:

  **http://motorola.com/fastsrams**

- For all other inquiries about Motorola products, please contact the Motorola Customer Response Center:

  **Phone: 800–521–6274**
  **Email: crc@crc.email.sps.mot.com**