Fact Sheet

Automotive-grade Bluetooth® LE 6.0 MCU with channel sounding

KW47: Bluetooth channel sounding MCU with on-chip localization compute engine

The KW47 MCU family empowers next-generation automotive systems with Bluetooth LE (BLE) 6.0 channel sounding, enabling precise, secure and low-power distance measurement and localization. By leveraging phase-based ranging (PBR) and round-trip time (RTT) techniques, KW47 delivers centimeter-level accuracy far beyond traditional RSSI methods. Its integrated localization compute engine (LCE) accelerates complex positioning algorithms by up to 45%, enabling real-time responsiveness for automotive applications. Beyond BLE 6.0, KW47 anticipates future standards validated at Bluetooth Special Interest Group (BT SIG), ensuring unmatched security, interoperability and user experience.

The KW47 is NXP's first automotive-qualified Bluetooth low energy 6.0 MCU, with channel sounding and an integrated LCE. With integrated support for CAN FD, LIN and EdgeLock® secure enclave, the KW47 meets rigorous automotive standards—including AEC-Q100 grade 2, AUTOSAR, ASPICE, MISRA—and is CCC-certified, making it a secure and future-ready solution for next-generation vehicles. KW47 also features NXP's proprietary BLE handover capability, enabling seamless BLE connection transfer via CAN with enhanced security and continuity. KW47's unique multi-core architecture with dedicated core for application, radio, accelerator and security enables seamless operation of BLE, CAN and others without any interruption.

Anticipating future requirements, KW47 aligns with future BLE enhancements validated at BT SIG, including advanced attack resilience and China Compulsory Certification (CCC)-certified channel sounding security.

Moreover, NXP's KW47 has additional advanced features successfully validated at NXP and pending NXP's next qualifications at BT SIG, such as BLE 6.0 TxSNR, AM attack resilience, BLE 6.0 LE test mode enhancement and inline phase return (IPR).

Key features

- Application core
  - Up to 96 MHz Arm® Cortex®-M33 core
  - Localization compute engine
- Memory
  - Up to 96 Hz Arm Cortex-M33 core with 2 MB program flash and 264 Kb SRAM
- Future-proof features
  - BLE anticipated feature-ready
  - BT SIG validation and interoperability leadership
  - Early access program for partners
- Radio subsystem with dedicated core, flash and RAM
  - Secure 512 kB flash supporting upgradable software radio
  - 171 KB SRAM optimized for link layer support
  - 2.4 GHz BLE core version 6.0 upgradeable radio supporting up to 24 simultaneous hardware connections in any central/ peripheral combination
- Security
  - Edgelock secure enclave core profile with Edgelock 2GO support
  - Phase-based normalized attack detector metric (NADM)
  - AM attack resilience
  - CCC-certified channel sounding security
- Optional CAN FD interface
- -40 to 125 °C operating temperature

Target applications

- Smart car access
- Phone as a key
- Keyfob
- Two-wheeler access
- Telematics

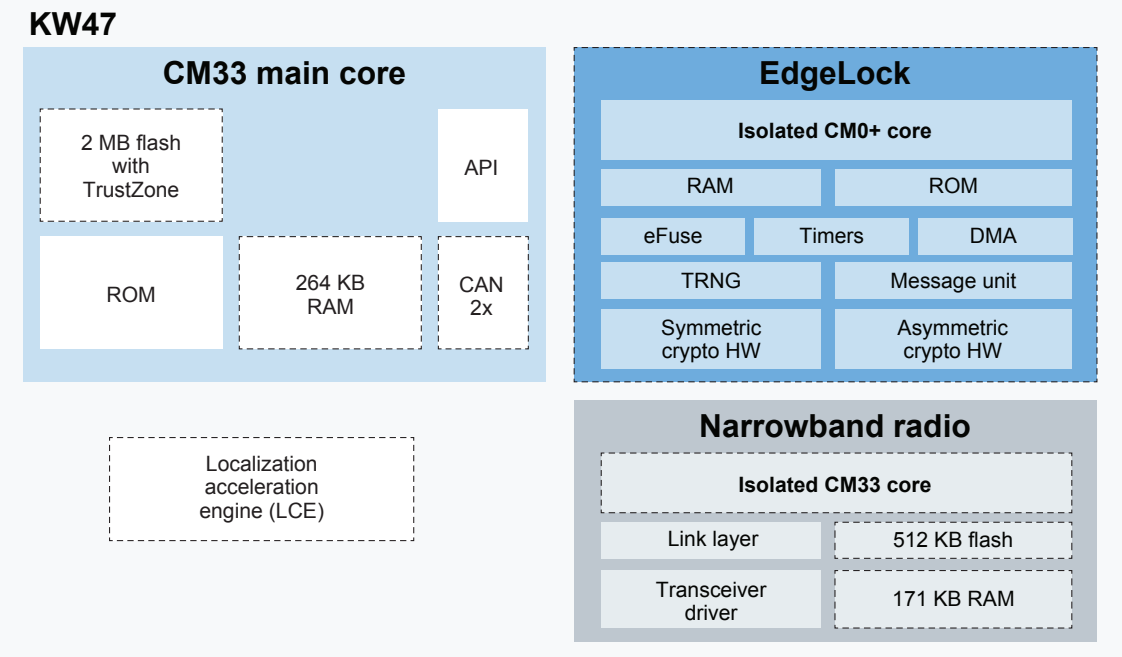
Enablement tools

- Development hardware
  - KW47-LOC localization board
  - KW47 evaluation kit consisting of KW-MCXW-EVK-MB mother board and KW47-001-M10 daughter card
- Runtime software
  - MCUXpresso SDK
- Compiler
  - MCUXpresso IDE
  - IAR embedded workbench
  - GCC Arm embedded toolchain
- Debugger
  - MCU-Link (on-board debug probe with KW47 EVK boards)
  - SEGGER J-Link
  - CMSIS-DAP

Orderable samples

Part number	Flash	SRAM	Operating frequency	Radio	LCE	CAN FD	Qualification	Package
KW47B42ZB7AFTBT	2 MB + 512 kB	256 kB + 171 kB	96 MHz	Y	Y	Y	AEC-Q100	48 HQFN “wettable”
KW47B42Z97AFTBT	1 MB + 512 kB	256 kB + 171 kB	96 MHz	Y	Y	Y	AEC-Q100	48 HQFN “wettable”
KW47B42Z83AFTBT	1 MB + 512 kB	128 kB + 171 kB	96 MHz	Y	N	N	AEC-Q100	48 HQFN “wettable”

Architecture block diagram



Indicates modification/addition compared to KW45

Product specifications

Flash	2 MB program flash with ECC	SRAM	264 kB with ECC and parity
Timer/PWM	• Two 6-channel 32-bit timers (TPM) with PWM capability • Two 32-bit low-power timers (LPTMR) or pulse counters • 4-channel 32-bit low-power periodic interrupt timer • One 56-bit timestamp timer • 32-bit seconds real time counter (RTC) with 32-bit alarm and independent power supply	Analog	• 16-bit single ended SAR Analog-to-digital converter (ADC) up to 2 Msps • Two high-speed analog comparators (CMP) with 8-bit digital-to-analog converter (DAC)
Application core	• Arm Cortex-M33 core up to 96 MHz	Security	• EdgeLock secure enclave with symmetric and asymmetric key encryption
Radio core	• Dedicated CM33 core running at up to 64 MHz with 512 kB flash and 171 kB SRAM	Radio sensitivity	• 106 dBm 125 kbps long range receive sensitivity • 102 dBm 500 kbps long range receive sensitivity • 97.5 dBm 1 Mbps receive sensitivity • 95 dBm 2 Mbps receiver sensitivity
Package	• 7 x 7 mm 48HVQFN with “wettable” flanks	Temp	• -40 to 125 °C

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