Signal Controllers

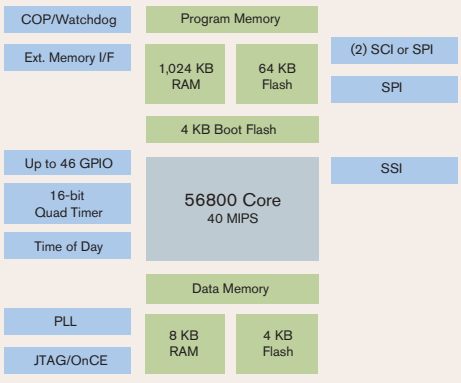
56F826

Target Applications

> Noise suppression
> ID tag readers
> Sonic/subsonic detectors
> Security access devices
> Remote metering
> Sonic alarms
> General-purpose devices

Overview

The 56F826 is a member of the 56800 core-based family of digital signal controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller (MCU) with a flexible set of peripherals to create an extremely cost-effective solution for general-purpose applications. Because of its low cost, configuration flexibility and compact program code, the 56F826 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for compilers to enable rapid development of optimized control applications.



56800E Core Features	Benefits
> Efficient 16-bit 56800 family digital signal controller engine with dual Harvard architecture	> Low-power applications supported by multiple operating modes
> As many as 40 MIPS at 80 MHz core frequency	> Flash memory is engineered to provide reliable, nonvolatile memory storage, eliminating the need for external storage devices
> Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)	> Easy to program with flexible application development tools
> Two 36-bit accumulators, including extension bits	> Optimized for C compiler efficiency
> 16-bit bidirectional shifter	> Simple updating of Flash memory through serial peripheral interface (SPI), serial communications interface (SCI) OnCE, using on-chip boot loader
> Parallel instruction set with unique addressing modes	> Simple interface with other asynchronous serial communication devices and off-chip EE memory
> Hardware DO and REP loops	> Sophisticated debugging using OnCE to view core, peripheral and memory contents
> Three internal address buses and one external address bus	
> Four internal data buses and one external data bus	
> Instruction set supports both DSP and controller functions	
> Controller-style addressing modes and instructions for compact code	
> Efficient C compiler and local variable support	
> Software subroutine and interrupt stack with depth limited only by memory	
> JTAG/on-chip emulation (OnCE™) debug programming interface	

Energy Information

> Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
> Dual power supply, 3.3V and 2.5V
> Wait and multiple stop modes available

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56F826 16-bit Digital Signal Controller

> Up to 40 MIPS at 80 MHz core frequency
> DSP and MCU functionality in a unified, C-efficient architecture
> Hardware DO and REP loops
> MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
> 72 KB On-chip Flash
  - 64 KB Program Flash
  - 4 KB Data Flash
  - 4 KB Boot Flash
> 1,024 KB Program RAM
> 8 KB Data RAM
> Up to 128 KB each of external memory expansion for program and data memory
> One SPI
> One additional SPI or two SCIs
> One synchronous serial interface (SSI)
> One general-purpose quad timer
> JTAG/OnCE for debugging
> 100-pin LQFP package
> 16 dedicated and 30 shared general-purpose input/outputs (GPIOs) pins
> One time of day module

56F826 Memory Features

> Harvard architecture permits as many as three simultaneous accesses to program and data memory
> On-chip memory including a low-cost, high-volume Flash solution
  - 72 KB On-chip Flash
    - 64 KB Program Flash
    - 4 KB Data Flash
    - 4 KB Boot Flash
    - 1,024 Program RAM
  - 8 KB Data RAM
> Off-chip memory expansion capabilities
  - As much as 128 KB data memory
  - As much as 128 KB program memory

56F826 Peripheral Circuit Features

> General-purpose quad timer
> One SPI
> A second SPI or two SCIs
> SSI
> 16 dedicated GPIO pins
> 30 shared GPIO pins
> Computer operating properly (COP)/ watchdog timer
> Two external interrupt pins
> External reset pin for hardware reset
> JTAG/OnCE for unobtrusive, processor speed-independent debugging
> Software-programmable, Phase-Lock Loop (PLL)-based frequency synthesizer
> One time-of-day (TOD) module

Award-Winning Development Environment

> Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.
> The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Product Documentation

DSP56800 Family Manual	Detailed description of the 56800 family architecture and 16-bit DSP core processor and the instruction set ***Order Number:*** DSP56800FM
DSP56F826/827 User's Manual	Detailed description of memory, peripherals and interfaces of the 56F826/827 ***Order Number:*** DSP56F826-827UM
DSP56F826 Technical Data Sheet	Electrical and timing specifications, pin descriptions and package descriptions ***Order Number:*** DSP56F826
DSP56F826 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces ***Order Number:*** DSP56F826PB

Ordering Information

Part	DSP56F826
Supply Voltage	3.0V–3.6V, 2.25V–2.75V
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	100
Frequency (MHz)	80
Order Number	DSP56F826BU80

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

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