

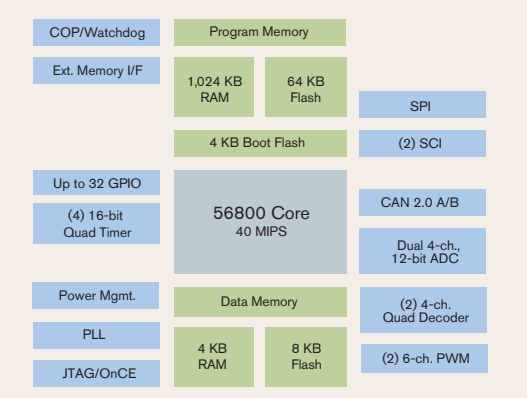
56F805

Target Applications

- > Regenerative drives
- > ID tag readers
- > Winders/pullers
- > Glass breakage detection
- > Critical reliability drives
- > Cable test equipment
- > HVAC
- > Remote monitoring
- > Automotive control
- > General-purpose devices
- > Switched-mode power supplies

Overview

The 56F805 is a member of the 56800 core-based family of digital signal controllers. It combines, on a single chip, the processing power of a DSP and the functionality of a microcontroller (MCU) with a flexible set of peripherals to create an extremely cost-effective solution. Because of its low cost, configuration flexibility and compact program code, the 56F805 is well-suited for many applications. The 56800 core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and MCU applications. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.



56800E Core Features

- > Efficient 16-bit 56800 family digital signal controller engine with dual Harvard architecture
- > As many as 40 MIPS at 80 MHz core frequency
- > Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)
- > Two 36-bit accumulators, including extension bits
- > 16-bit bidirectional barrel shifter
- > Parallel instruction set with unique addressing modes
- > Hardware DO and REP loops
- > Three internal address buses and one external address bus
- > Four internal data buses and one external data bus
- > Instruction set supports both DSP and controller functions
- > Controller-style addressing modes and instructions for compact code
- > Efficient C compiler and local variable support
- > Software subroutine and interrupt stack with depth limited only by memory
- > JTAG/on-chip emulation (OnCE™) debug programming interface

Benefits

- > Onboard voltage regulator and power management is designed to reduce overall system cost by allowing for a single supply voltage
- > Flash memory is engineered to provide reliable, nonvolatile memory storage, eliminating the need for external storage devices
- > Easy to program with flexible application development tools
- > Simple updating of Flash memory through serial peripheral interface (SPI), serial communications interface (SCI) or OnCE, using on-chip boot loader
- > Program can boot directly from Flash
- > Supports multiple processor connections
- > Patented distortion correction in pulse-width modulation (PWM) for reducing design risk and better performance control
- > PWM and analog-to-digital converter (ADC) modules are tightly coupled to reduce processing overhead
- > Low-voltage interrupts (LVIs) protect the system during brownout or power failure
- > Simple interface with other asynchronous serial communication devices and off-chip EE memory

Energy Information

- > Fabricated in high-density CMOS with 5V-tolerant, TTL-compatible digital inputs
- > Uses a single 3.3V power supply
- > On-chip regulators for digital and analog circuitry to lower cost and reduce noise
- > Wait and stop modes available

56F805 16-bit Digital Signal Controller

- > Up to 40 MIPS at 80 MHz core frequency
- > DSP and MCU functionality in a unified, C-efficient architecture
- > Hardware DO and REP loops
- > MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- > 76 KB On-chip Flash
 - 64 KB Program Flash
 - 8 KB Data Flash
 - 4 KB Boot Flash
- > 1,024 KB Program RAM
- > 4 KB Data RAM
- > Up to 128 KB each of external program and data memory
- > Two 6-channel PWM modules
- > Two 4-channel, 12-bit ADCs
- > Two quadrature decoders
- > CAN 2.0 A/B module
- > Two SCIs
- > SPI
- > Four general-purpose quad timers
- > JTAG/OnCE port for debugging
- > 14 dedicated and 18 shared general-purpose input/output (GPIO) lines
- > 144-pin LQFP package

56F805 Memory Features

- > Harvard architecture permits as many as three simultaneous accesses to program and data memory
- > On-chip memory including a low-cost, high-volume Flash solution
 - 76 KB On-chip Flash
 - › 64 KB Program Flash
 - › 8 KB Data Flash
 - › 4 KB Boot Flash
 - 1,024 KB Program RAM
 - 4 KB Data RAM
- > Off-chip memory expansion capabilities
 - As much as 128 KB data memory
 - As much as 128 KB program memory

56F805 Peripheral Circuit Features

- > Two PWM modules each with six PWM outputs, three current sense inputs and four fault inputs; fault-tolerant design with dead-time insertion; supports both center- and edge- aligned modes
- > Two 12-bit ADCs, which support two simultaneous conversions; ADC and PWM modules can be synchronized
- > Two quadrature decoders
- > Four general-purpose quad timers
- > Two SCIs
- > CAN 2.0 A/B module
- > SPI
- > 14 dedicated GPIO pins, 18 multiplexed GPIO pins
- > Computer operating properly (COP)/watchdog timer
- > Two dedicated external interrupt pins
- > External reset input pin for hardware reset
- > External reset output pin for system reset
- > JTAG/OnCE module for unobtrusive, processor speed-independent debugging
- > Software-programmable, Phase-Lock Loop (PLL)-based frequency synthesizer

Award-Winning Development Environment

- > Processor Expert™ (PE) technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.
- > The CodeWarrior™ Integrated Development Environment (IDE) is a sophisticated tool for code navigation, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, PE technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Learn More: For more information about Freescale products, please visit www.freescale.com.

Product Documentation

DSP56800 Family Manual	Detailed description of the 56800 family architecture and 16-bit DSP core processor and the instruction set Order Number: DSP56800FM
DSP56F80x User's Manual	Detailed description of memory, peripherals and interfaces of the 56F801, 56F802, 56F803, 56F805 and 56F807 Order Number: DSP56F801-7UM
DSP56F805 Technical Data Sheet	Electrical and timing specifications, pin descriptions and package descriptions Order Number: DSP56F805
DSP56F805 Product Brief	Summary description and block diagram of the core, memory, peripherals and interfaces Order Number: DSP56F805PB

Ordering Information

Part	DSP56F805
Supply Voltage	3.0V–3.6V
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	144
Frequency (MHz)	80
Order Number	DSP56F805FV80