Digital Signal Controllers

DSP56855

General-purpose solution for systems requiring a DSP with greater on-chip memory in a smaller package

The 56800E core is based on a Harvard-style architecture consisting of three execution units operating in parallel, allowing as many as six operations per instruction cycle. The microprocessor-style programming model and optimized instruction set allow straightforward generation of efficient, compact code for both DSP and microcontroller (MCU) applications. The instruction set is also highly efficient for C compilers, enabling rapid development of optimized control applications.

Target Applications

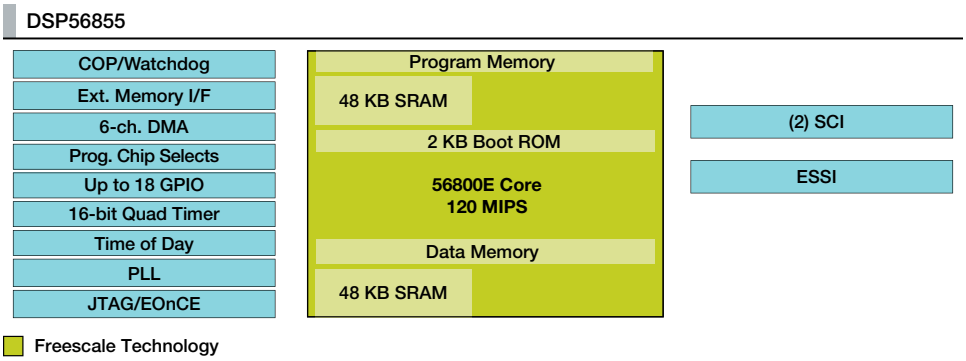
- Internet audio decoding
- Digital telephone answering devices
- Voice recognition and command
- Embedded modem/data pump
- Voice processing
- General-purpose devices
- Hands-free automotive devices

Overview

The 56855 core offers 48 KB of on-chip program SRAM and 48 KB data SRAM in a 100-pin LQFP package. The serial peripheral interface (SPI) and the 8-bit host interface have been removed to provide flexibility with fewer features to meet customer price/performance expectations. This device is ideal for systems that require a DSP with greater on-chip memory in a smaller package, but do not require an extensive peripheral set. The 56855 includes a quad timer module with a signal external output.

56800E Core Features

- Efficient 16-bit digital signal controller engine with dual Harvard architecture
- 120 MIPS at 120 MHz core frequency
- Single-cycle 16 x 16-bit parallel multiplier-accumulator (MAC)
- Four 36-bit accumulators, including extension bits
- 16-bit bidirectional shifter
- Parallel instruction set with unique addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Four hardware interrupt levels
- Five software interrupt levels
- Controller-style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/enhanced on-chip emulation (EOnCE) debug programming interface



Benefits

- Easy to program with flexible application development tools
- Supports multiple processor connections
- 16-bit quad timer module (with one external pin) that allows capture/compare functionality and can be cascaded
- Quad timer module can also be used for simple digital-to-analog conversion functionality
- Enhanced synchronous serial interface (ESSI) with enhanced network and audio modes
- Time of day (TOD) module for applications requiring clock display
- Flexible 6-channel direct memory access (DMA) allows both internal and external memory transfers with almost no CPU interruption
- External memory expansion up to 4 MB words program memory or up to 16 MB words data memory increases capabilities of device for larger algorithms

Energy Information

- Fabricated in high-density CMOS with 3.3V, TTL-compatible digital inputs
- Wait and stop modes available

56855 16-bit Digital Signal Processors

- 120 MIPS at 120 MHz
- 48 KB program SRAM
- 48 KB data SRAM
- 2 KB boot ROM
- Access up to 4 MB of program or 16 MB data memory
- Chip select logic for glueless interface to ROM and SRAM
- Six independent channels of DMA
- ESSI
- Two serial communications interfaces (SCIs)
- General-purpose 16-bit quad timer
- JTAG/EOnCE for unobtrusive, real-time debugging
- Computer operating properly (COP)/ watchdog timer
- TOD
- 100-pin LQFP package
- Up to 18 general-purpose input/output (GPIO) pins

56855 Memory Features

- Harvard architecture permits up to three simultaneous accesses to program and data memory
- On-chip memory
  - 48 KB program SRAM
  - 48 KB data SRAM
  - 2 KB boot ROM
- Off-chip memory expansion
  - Access up to 4 MB of program memory or up to 16 MB of data memory (using chip selects)
  - Chip select logic for glueless interface to ROM and SRAM

56855 Peripheral Circuit Features

- General-purpose 16-bit quad timer with four external pins*
- Two SCIs*
- ESSI module*
- Computer operating properly (COP)/ watchdog timer
- JTAG/EOnCE for unobtrusive, real-time debugging
- Six independent channels of DMA
- TOD
- Up to 18 GPIO pins

*Each peripheral I/O can be used alternately as a GPIO.

Award-Winning Development Environment

- Processor Expert technology provides a rapid application design (RAD) tool that combines easy-to-use, component-based software application creation with an expert knowledge system.
- The CodeWarrior Integrated Development Environment is a sophisticated tool for code navigating, compiling and debugging. A comprehensive set of evaluation modules (EVMs) and development system cards will support concurrent engineering. Together, Processor Expert technology, the CodeWarrior tool suite and EVMs create a comprehensive, scalable tools solution for easy, fast and efficient development.

Product Documentation

Product	Order Number	Description
DSP56800E Reference Manual	**DSP56800ERM**	Detailed description of the 56800E architecture, 16-bit DSP core processor and the instruction set
DSP5685x User's Manual	**DSP5685xUM**	Detailed description of memory, peripherals and interfaces of the 56853, 56854, 56855, 56857 and 56858
DSP56855 Technical Data Sheet	**DSP56855**	Electrical and timing specifications, pin descriptions and package descriptions
DSP56855 Product Brief	**DSP56855PB**	Summary description and block diagram of the core, memory, peripherals and interfaces

Ordering Information

Part	DSP56855
Supply Voltage	1.8V, 3.3V
Package Type	Low-Profile Quad Flat Pack (LQFP)
Pin Count	100
Frequency (MHz)	120
Order Number	DSP56855BU120

For more information, visit freescale.com

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