MOTOROLA

Communications and Advanced
Consumer Technologies Group

MC68328

Device Errata
MC68328

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Mask Set 3G58E

This document lists the Errata for the 3G58E mask set of the MC68328 DragonBall microprocessor. This document and other information on this product is maintained on the World Wide Web at:

http://www.mot.com/pps

CPU Errata

1. PC5_DTACKB cannot be used as an I/O.

While PC5_DTACKB is programmed as an I/O pin, the internal DTACKB signal is permanently asserted. This causes all access to become zero wait-state regardless of the settings in the chip select registers. The workaround is the PC5_DTACKB pin must be programmed for the DTACK function (default).

2. First clock pulse after wakeup is sometimes a “runt”.

Depending on the phase of CLK32 when the wakeup signal occurs, the first CLKO pulse is shorter than normal. In some instances, the runt will cause the processor to not respond to wakeup events. The workaround is to set SYSCLKSEL bits in PLL Control Register ($fff202) to divide by 4 (001) before entering sleep. Immediately after wakeup, restore SYSCLKSEL to divide by 1 (100).

3. IRQEN bit in PWM Control Register does not function.

Bit 14 in the PWM Control Register ($fff500) does not function. The PWM interrupt is always enabled. The workaround is to disable PWM interrupts by setting Bit 7 in the Interrupt Mask Register ($fff306). Disable PWM wakeup events by clearing Bit 7 in the Interrupt Wakeup Enable Register ($fff30a).

4. Real Time Clock continues to keep time while the RTC Enable bit (bit 7) ($fffboc) is clear.

The Real Time Clock always keeps time while the RTC enable is clear and this is correct operation. However, the RTC Enable Bit must be set to allow interrupts, RTC wakeup events, or the StopWatch function. NOTE: The Real Time Clock is not cleared on reset. Upon initial power up, the value in the Hours, Minutes and Seconds register will be random.

5. Clear control bits for edge mode interrupts are reversed.

In edge triggered interrupt mode, the Interrupt Status Register ($fff30c) clear function nibble is bit-reversed. The workaround is to clear interrupts (only while configured as edge interrupts) as follows:

IRQ6 ($fff30c bit 19) write 1 to bit 16 (IRQ1 in the data manual) to clear.
IRQ3 ($fff30c bit 18) write 1 to bit 17 (IRQ2 in the manual) to clear.
IRQ2 ($fff30c bit 17) write 1 to bit 18 (IRQ3 in the manual) to clear.
IRQ1 ($fff30c bit 16) write 1 to bit 19 (IRQ6 in the manual) to clear.

6. SPI-Slave does not receive data reliably.

The SPIS module indicates that it has data ready for reading before an 8-bit transfer is complete. Disabling the module does not clear the error and resynchronize the shift register.The workaround is to emulate The SPIS module in software for data rates slower than 20 kbps.

7. Timer capture edge feature does not operate reliably.

The capture-on-edge of the two general purpose timers will not reliably generate an interrupt or latch a counter value in the capture register. This feature will be fixed in revision 0H58B.

8. Reading the TXPOL bit returns the value of the RXPOL bit.

The TXPOL bit in the UART miscellaneous register (Base + $908, bit 2) does not return the value written to the bit, rather the value of the adjacent bit, RXPOL (bit 3). The workaround is the actual value of the TXPOL bit is the value written to the TXPOL bit. The value read is the value of the RXPOL bit. The function of TXPOL is not affected. Also, the RXPOL bit or it's function is not affected.