Mask Set Errata for Mask 0N89D

Introduction

This report applies to mask 0N89D for these products:

- PXS20

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e3866: ADC Self Test algorithm S0 result can be incorrect at low temperature

Errata type: Errata

Description: The ADC Self Test algorithm S step 0 (S0) measures ADC Vbandgap / VDD_HV_ADR. In the case where the S0 step occurs after the ADC has sampled and converted a value close to VDD_HV_ADR at low temperature (for example -40C) in some process corners the sampling time (specified by INPSAMP_S) of 80h is not long enough to allow the correct ADC sampling capacitor settling. This may lead to an incorrect converted value.

The Band Gap in the above specified condition is slow in discharging the sampling capacitor when the previous sampled voltage is much larger than the Band Gap output voltage (nominally 1.2V). The larger the voltage sampled before S0, the slower is the settling.

This issue can also affect S1 algorithm results since S1 = VDD_HV_ADV / Vbandgap.

Workaround: To eliminate the problem it is mandatory to:

(a) increase the sampling time for S supply self test (INSAMP_S) from 80h to FFh and

(b) insert a sacrificial ADC conversion immediately before the S supply self test.

The user software must insert a single-shot S algorithm Step 0 conversion (also called sacrificial S0 conversion) before the normal S supply self test to achieve accurate sample capacitor settling. The user software must prohibit any other conversions between the sacrificial S0 conversion and normal S0 conversion of the S supply self test.

e4168: ADC: "Abort switch" aborts the ongoing injected channel as well as the upcoming normal channel

Errata type: Errata

Description: If an Injected chain (jch1,jch2,jch3) is injected over a Normal chain (nch1,ch2,ch3,ch4) the Abort switch doesn't behave as expected.

Expected behavior:

Correct Case (without SW Abort on jch3): Nch1-> Nch2(aborted)->Jch1 -> Jch2> Jch3 ->Nch2(restored)-> Nch3->Nch4

Correct Case(with SW Abort on jch3): Nch1-> Nch2(aborted)->Jch1 -> Jch2> Jch3(aborted) ->Nch2(restored)-> Nch3->Nch4

Observed unexpected behavior:

Fault1 (without SW abort on jch3): Nch1-> Nch2(aborted)->Jch1 -> Jch2> Jch3 -> Nch3->Nch4 (Nch2 not restorted)

Fault2 (with SW abort on jch3): Nch1-> Nch2->Jch1 -> Jch2> Jch3(aborted) ->Nch4 (Nch2 not restored & Nch3 conversion skipped)

Workaround: It's possible to detect the unexpected behavior by using the CEOCFR0 register. The CEOCFR0.EOC_CHx field will not be set for a not restored or skipped channel, which indcates this issue has occurred. The CEOCFR0.EOC_CHx fields need to be checked before the next Normal chain execution (in scan mode). The CEOCFR0.EOC_CHx fields should be read by every ECH interrupt at the end of every chain execution.

e4016: ADC: Presampling on channels 9, 10, 15 leads to incorrect results

Errata type: Errata

Description: On ADC channels 9 (for factory test only) , 10 (VREG_1.2V), 15 (TSENS) when performing presampling using VSS_HV_ADR (PREVAL0=01) and bypassing the sampling (PRECONV=1) results in an incorrect converted presampled value.

Workaround: ADC Conversion Timing Register 1 (CTR1) and Presampling Control Register (PSCR), field PREVAL1(bits 27:28) can be programmed to select the conversion durations and reference voltages for ADC channels 9, 10, 15.

e4186: ADC: triggering an ABORT or ABORTCHAIN before the conversion starts

Errata type: Errata

Description: When ABORTCHAIN is programmed and an injected chain conversion is programmed afterwards, the injected chain is aborted, but neither JECH is set, nor ABORTCHAIN is reset.

When ABORT is programmed and normal/injected chain conversion comes afterwards, the ABORT bit is reset and chain conversion runs without a channel abort.

If ABORT, or ABORTCHAIN, feature is programmed after the start of the chain conversion, it works properly.

Workaround: Do not program ABORT/ABORTCHAIN before starting the execution of the chain conversion.

e4166: CTU: FIFO full and concurrent push and pop operations

Errata type: Errata

Description: With a full FIFO, if concurrent FIFO read and write operations occur, then the order of the FIFO is not correct.

For example, FIFO is full and contains data A,B,C,D. Then there are POP and a PUSH requests in the same clock cycle. After the PUSH and POP operations instead of correct data B,C,D,E, the FIFO contains the data B,C,E,D. Data A is pushed out correctly, but data E and D are swapped.

Application software can detect the swap between E and D by reading the CTU.FLx.ADC and CTU.FLx.N_CH fields, unless E and D refer to the same ADC and same channel.

Workaround: To reduce the risk of this issue 2 suggestions are given:

1) lower the FIFO threshold to less than the size of the FIFO (probability is reduced, but can't be fully excluded).

2) forbid 2 consecutive conversions from the same ADC and channel source to allow swap detection by reading the CTU.FLx.ADC and CTU.FLx.N_CH fields.

e3659: FLASH: Resuming after a suspend during an Erase may prevent the erase from completing.

Errata type: Errata

Description: If an erase suspend (including the flash put into sleep or disabled mode) is done on any block in the low Address Space (LAS) or the Mid-Address Space (MAS) except the 16KB blocks, or if a suspend is done with multiple non-adjacent blocks (including the High Address Space [HAS]), the flash state machine may not set the FLASH_MCR[DONE] bit in the flash Module Control Register. This condition only occurs if the suspend occurs during certain internal flash erase operations. The likelihood of an issue occurring is reduced by limiting the frequency of suspending the erase operation.

Workaround: If the suspend feature (including disable and sleep modes) of the flash is used, then software should ensure that if the maximum time allowed for an erase operation occurs without a valid completion flag from the flash (FLASH_MCR[DONE] = 1), the software should abort the erase operation (by first clearing the Enable High Voltage (FLASH_MCR[EHV]) bit, then clearing the Erase read/Write bit (FLASH_MCR[ERS] bit) and the erase operation should be restarted.

Note: The cycle count of the sector is increased by this abort and restart operation.

e4272: Flash: May fail to exit Power On Reset (POR) properly

Errata type: Errata

Description: There is a low probability (approximately once per 200,000 POR events) that the Flash may fail to respond. This may cause the device to hang in the reset state. The watchdog resets will not recover the flash from the failure state.

Workaround: Internal resets are not effective to recover from this condition. A power down/up cycle is required.

e4215: Flash: May fail to wake up after reset from STOP mode

Errata type: Errata

Description: If the device is in STOP mode with the flash in power-down mode or in low-power mode (configured by mode configuration registers ME_<mode>_MC - FLAON flash power-down control bits : "01" flash is in power-down mode, "10'" flash is in low-power mode) and a 'functional' reset (non-'destructive' reset) occurs, the device may fail to wake up correctly. Instead, the device remains in the static mode (in a wait loop in SAFE mode), and the application will not resume execution.

Workaround: Never configure the flash to be in power-down or low-power mode, but rather always configure the flash to be in normal mode (configured by mode configuration registers ME_<mode>_MC - FLAON flash power-down control bits : "11" flash is in normal mode) for all device modes.

e3320: Flash: single bit correction status is not available in the Error Correction Status Module (ECSM) and in the Fault Collection and Control Unit (FCCU).

Errata type: n/a

Description: A single bit error correction by the Flash is not passed to the Error Correction Status Module (ECSM) and to the Fault Collection and Control Unit (FCCU). The single bit error correction is only flagged by the SBC bit of the Flash Module Configuration Register (MCR).

Workaround: Poll the SBC bit (Single Bit Correction Status) of the Flash Module Configuration Register (MCR) to detect a single bit error correction event.

e4340: LINFlexD: Buffer overrun can not be detected in UART Rx FIFO mode

Errata type: Errata

Description: When the LINFlexD is configured in UART Receive (Rx) FIFO mode, the Buffer Overrun Flag (BOF) bit of the UART Mode Status Register (UARTSR) register is cleared in the subsequent clock cycle after being asserted.

User software can not poll the BOF to detect an overflow.

The LINFlexD Error Combined Interrupt can still be triggered by the buffer overrun. This interrupt is enabled by setting the Buffer Overrun Error Interrupt Enable (BOIE) bit in the LIN Interrupt enable register (LINIER). But the BOF bit will be cleared when the interrupt routine is entered, preventing the user to identify the source of error.

Workaround: Buffer overrun errors in UART FIFO mode can be detected by enabling only this source in the LIN Error Combined interrupt.

e3950: MC_ME: Possibility of Machine Check on Low-Power Mode Exit

Errata type: Errata

Description: When executing from the flash and entering a Low-Power Mode (LPM) where the flash is in low-power or power-down mode, 2-4 clock cycles exist at the beginning of the RUNx to LPM transition during which a wakeup or interrupt will generate a machine check due to the flash not being available on RUNx mode re-entry. This will cause a machine check interrupt.

Workaround: For an application to avoid an issue with machine check, two workarounds are suggested:

1) Configure the application to avoid the machine check interrupt by executing the transition into low power modes from RAM.

2) Configure the application with the machine check interrupt handler located in RAM.

e4334: MC_RGM: Device stays in reset state on external reset assertion.

Errata type: Errata

Description: On an external reset that is configured to be 'long' the device may remain in reset if the system clock is configured to be sourced by a clock source other than the 16 MHz Internal RC Oscillator (IRCOSC). Recovery from the reset in this case can only be achieved via a power-down and power-up cycle.

The failure condition can only be seen with the following Reset Generation Module (MC_RGM) settings for Functional Event Short Sequence register, External Reset field (RGM_FESS[SS_EXR]) and Functional Bidirectional Reset Enable register, External Reset field (RGM_FBRE[BE_EXR]):

- RGM_FESS[SS_EXR] = 0b0 (long external reset)

- RGM_FBRE[BE_EXR] = 0b0 (asserted on external reset event)

Note 1: This condition can only occur if the cause of the device reset was the external reset assertion. It does not occur if, for example, the device reset was due to a power-on.

Note 2: RGM_FESS[SS_EXR] = 0b0 and RGM_FBRE[BE_EXR] = 0b0 are the default settings out of power-on reset (POR).

Workaround: There are two possible workarounds. In both, the workaround takes effect only after software has reconfigured the MC_RGM. Therefore, in order to ensure that the issue cannot occur after POR exit and before the software has executed the workaround, the system clock must not be re-configured in the Mode Entry module (MC_ME) to be sourced by a clock source other than the IRCOSC until after the workaround has been executed.

Workaround #1:

Always configure the external reset event to prevent the external reset output to be driven by the MC_RGM by writing 0b1 to RGM_FBRE[BE_EXR].

If the external reset has been configured to be long (RGM_FESS[SS_EXR] = 0b0) and self testing has been enabled via the flash option, the external reset pin will still be asserted from the time of external assertion until reset sequence exit after start-up self test execution.

If the external reset has been configured to be long (RGM_FESS[SS_EXR] = 0b0) and self testing has been disabled via the flash option, the external reset pin will still be asserted from the time of external assertion until the chip configuration is loaded from the flash during reset PHASE3.

If the external reset has been configured to be short (RGM_FESS[SS_EXR] = 0b1), the external reset pin will still be released as soon as it is no longer asserted from off-chip.

Workaround #2:

Always configure the external reset as 'short' by writing 0b1 to RGM_FESS[SS_EXR]. In addition, use software to trigger a long 'functional' or 'destructive' reset via the Mode Entry module (MC_ME) if flash initialization or start-up self test is required.

The impact of this workaround is the additional time that the device is in reset (due to the short reset sequence triggered by the external reset) and the overhead required for software to check the reset status and request a software reset.

e3697: e200z: Exceptions generated on speculative prefetch

Errata type: Errata

Description: The e200z4 core can prefetch up to 2 cache lines (64 bytes total) beyond the current instruction execution point. If a bus error occurs when reading any of these prefetch locations, the machine check exception will be taken. For example, executing code within the last 64 bytes of a memory region such as internal SRAM, may cause a bus error when the core prefetches past the end of memory. An ECC exception can occur if the core prefetches locations that are valid, but not yet initialized for ECC.

Workaround: Do not place code to be executed within the last 64 bytes of a memory region. When executing code from internal ECC SRAM, initialize memory beyond the end of the code until the next 32-byte aligned address and then an additional 64 bytes to ensure that prefetches cannot land in uninitialized SRAM.

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